UNIVERSITÉ DE NEUCHÂTEL
INSTITUT DE MICROTECHNIQUE

LOW-POWER ARCHITECTURES FOR SINGLE-CHIP DIGITAL IMAGE SENSORS

Steve Tanner

THÈSE

PRÉSENTÉE À LA FACULTÉ DES SCIENCES
POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

Novembre 2000

…Cherchez les choses d’en haut…

Epître aux Colossiens, Ch. 3 v. 1

A la mémoire de Fabrice

IMPRIMATUR POUR LA THESE

Low-Power Architectures for Single-Chip Digital Image Sensors

de M. Steve Tanner

UNIVERSITE DE NEUCHATEL

FACULTE DES SCIENCES

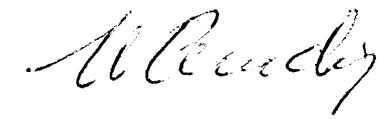
La Faculté des sciences de l'Université de Neuchâtel sur le rapport des membres du jury,

MM. F. Pellandini (directeur de thèse), M. Ansorge, P. Seitz, R. Siegwart (EPFL) et J. Grupp (Asulab)

autorise l'impression de la présente thèse.

Neuchâtel, le 21 septembre 2000

Le doyen:



J.-P. Derendinger

Abstract

This research work is part of an academic and industrial collaboration whose main theme is the development of low-power, small-size micro-systems for the acquisition and processing of images. Such micro-systems are made with sub-blocks of different nature: image acquisition (with its optics and solid-state sensor), image processing (correction, filtering, compression), data storage, restitution and transmission, etc.

This thesis, realised at the Institute of Microtechnology (University of Neuchâtel, Switzerland), deals with the image acquisition block and focuses on the development of low-power architectures allowing the realisation of single-chip digital image sensors.

Until recently, applications in portable electronic imaging were limited by the excessive power consumption of the image sensor and related electronic equipment. However, due to the tremendous growth of multimedia and battery-powered electronic devices, the need to dispose with such low-power image acquisition systems has become very great.

Traditionally realised in CCD (Charge Coupled Device) technology, solid-state image sensors are today more and more fabricated with CMOS technologies. An important gain in power consumption and manufacturing costs is achieved, and part of the image processing related hardware can be integrated on the same chip than the sensor itself, particularly the analog to digital conversion of the signal.

The main objective of this thesis is to minimise power consumption of such a circuit at different levels: A/D conversion, sensor general architecture and circuit system integration.

In the first part of the work, low-power Analog-to-Digital Converters (ADCs) adapted for video applications were developed, integrated and tested. Their parallel architecture allows a lower working frequency (with a favourable impact on power consumption) and a better compatibility with the inherently parallel output data structure of the sensor.

Next, the work was focused on digital sensor architectures at different levels: sensor-ADC interface, sensor addressing modes for minimising power consumption, circuit control through dedicated on-chip circuitry.
Finally, the developed approaches were validated through the realisation, in collaboration with the "Centre Suisse d'électronique et de Microtechnique" (CSEM), of two single-chip digital image sensors.
Compared to other realisations relying on relatively similar approaches, the two realisations have been shown to approach the lowest limit in terms of power consumption, while maintaining acceptable image quality and die area.
In order to reduce further power consumption, new approaches need to be investigated, based on drastic voltage supply reduction and increased on-chip signal processing features for reducing the amount of data needing to be transferred outside the chip.

Résumé

Ce travail de recherche s'inscrit dans une collaboration académique et industrielle dont le cadre général est le développement de micro-systèmes à faible consommation et faible encombrement pour l'acquisition et le traitement d'images. De tels micro-systèmes sont constitués de différents sous-blocs de nature relativement différentes: acquisition de l'image (comprenant une optique classique et un senseur photo-électrique), traitement de l'image (correction, filtrage, compression, etc.), stockage, restitution ou transmission de l'information, contrôle, etc.
La présente thèse réalisée à l'Institut de Microtechnique (Université de Neuchâtel, Suisse) concerne la partie acquisition de l'image et se focalise sur le développement d'architectures à faible consommation permettant la réalisation de senseurs d'image mono-composants entièrement numériques.
Encore récemment, les applications portables dans le domaine de l'imagerie électronique étaient limitées par la consommation excessive du capteur d'images et de l'électronique associée. Or, à cause de l'explosion du multimédia et des appareils électroniques portables, le besoin de disposer de tels systèmes à faible consommation est très fort.
Les senseurs d'image, longtemps réalisés en technologie CCD (Charge Coupled Device), sont de plus en plus fabriqués avec les technologies CMOS, qui ont énormément évolué. Les avantages en coût de fabrication et en consommation électrique sont importants, et une partie du traitement du signal venant du senseur d'image peut être intégré sur la même puce que ce dernier, en particulier sa conversion analogique / numérique (A/N).
Les buts de ce travail de thèse sont de minimiser autant que possible la consommation électrique d'un tel circuit en travaillant sur le convertisseur analogique / numérique (CAN), sur l'architecture générale du senseur et sur l'intégration système du circuit.
Dans une première partie du travail, des CAN à faible consommation adaptés pour les applications vidéo ont été développés et testés. Leur architecture

parallèle permet d'une part une plus faible fréquence de travail (ce qui a un impact favorable sur la consommation) et d'autre part une meilleure compatibilité avec le senseur, dont la structure est intrinsèquement parallèle.
Ensuite, le travail s'est focalisé sur les architectures de senseurs numériques à différents niveaux: interface senseur-CAN, modes d'adressage du senseur pour en minimiser la consommation, contrôle du circuit par une logique dédiée.
Enfin, les principes architecturaux ont été validés par la réalisation, en collaboration avec le Centre Suisse d'électronique et de Microtechnique (CSEM), de deux senseurs d'images mono-composants entièrement numériques.
Comparées à d'autres travaux utilisant des approches similaires, les deux réalisations se sont révélées être proches de la limite de performance maximale en termes de consommation électrique, tout en gardant une qualité d'image et une surface en silicium acceptables.
Pour réduire encore la consommation électrique, de nouvelles approches doivent être envisagées, basées sur une réduction drastique de la tension d'alimentation et sur une intégration accrue, sur le même circuit, d'unités de traitement du signal, afin de réduire la quantité d'information à transmettre à l'extérieur.

Abbreviations and notations

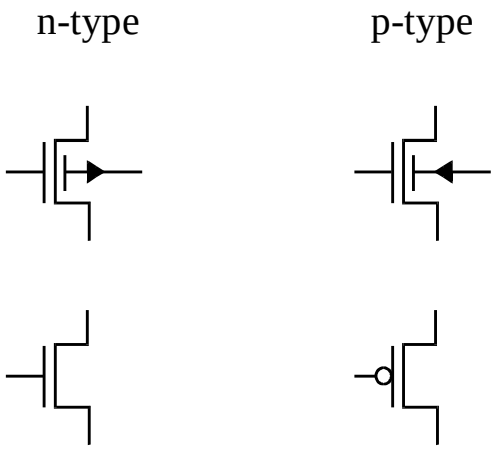
Abbreviations

ADC	Analog-to-Digital converter (Chapter 3)
APS	Active Pixel Sensor (Chapter 2)
CMOS	Complementary Metal-Oxide Semiconductor
DNL	Differential Non Linearity (Chapter 3)
ENB	Effective Number of Bit (Chapter 3)
FPN	Fixed Pattern Noise
INL	Integral Non Linearity (Chapter 3)
LSB	Least Significant Bit (Chapter 3)
MOS-FET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
MTF	Modulation Transfer Function (Chapter 2)
OTA	Operational Transconductance Amplifier
RGB	Colour space representation with red, green and blue components
rms	root mean square value
SNDR	Signal to Noise and Distortion ratio (Chapter 3)
SNR	Signal to Noise Ratio
Y-Cb-Cr	Colour space representation with luminance and chrominance components

Notations

MOS-Transistor notation

The following figure give the convention used in this report about transistor types:



If not specified, the transistor bulk is connected to Vss for n-type MOS-FET transistors, ant to Vdd for p-types, respectively.

Table of Contents

Chapter 1
Introduction

The research presented in this Ph. D. report addresses the development of miniaturised integrated circuits able to perform digital image acquisition, with emphasis on low-power operation, and realised in standard CMOS technology.

Today, electronic imaging is steadily gaining in importance. With devices like digital still cameras, DVD players, portable video recorders (camcorders), multimedia personal computers, etc., the electronic image is everywhere.

A key component of this vast domain is the image sensor. This "electronic eye", used with a traditional optical system, transforms the viewed scene into electrical information that can be stored, processed or transmitted by subsequent electronic units.

The last decade (1990-1999) was characterised with the explosion of portable electronic devices like GSM mobile phones, laptops and palm-sized computers. However, the use of electronic imaging in such devices is still limited. This is mainly due to the high power consumption of the sensor itself, the resulting system complexity, the high processing requirements for still or video-rate image applications and the size of the overall system.

The need for low-power image sensors is thus becoming very great. And, since the targeted markets are consumer products, cost-effective solutions are important, and are very often solved at the system level.

Therefore, the main objective of this research work is to develop miniature image sensors with the three main characteristics: low-power operation, low system complexity and low cost.

1.1 Today's image sensors

1.1.1 A page of history

The adventure of solid-state image sensors began in the 1960's with early realisations of passive photodiode arrays that were addressed like random access memories through MOS-FET devices. In the early 1980's, however, they were replaced with the superior CCD (charge coupled device) image sensors. The CCD was originally invented as an alternative analog memory device for digital computers, but thanks to its unusual properties of almost perfect charge storage and transport, it became quickly the most widely used image sensor technology.

For more than 15 years, CCDs entirely dominated the market of solid-state image sensors. Nowadays, they show a high level of technological maturity, and offer excellent image quality and high resolution. Applications extend from low cost PC video cameras to high performance megapixel scientific imagers. The CCD technology, however, suffers from several basic limitations:

- High power consumption due to the required operation voltage.
- Low fabrication yield, implying higher fabrication costs.
- Non-standard technology process.
- Incompatibility with other technologies (CMOS), meaning limited on-chip signal processing electronics.
- Specific image quality potential problems (blooming, smear).
- No pixel random access allowed.

In order to overcome those limitations, several research teams tried in the late 1980's to explore other ways, like the bipolar [Tana90] and charge modulation device (CMD) image sensors [Ogata91]. The CCD supremacy was finally contested when it became obvious that, thanks to the ever shrinking technology design rules, it would be possible to realise very small pixels using the almost-forgotten MOS-FET principle. Moreover, the CMOS technology would allow the realisation of complete mono-chip video cameras [Foss93] with standard analog and digital on-chip signal processing electronics. The early realisations, based on passive CMOS pixels, showed very promising results [Rens90]. Buffering inside the pixel was added [Yadid91], and optimised to give the well-known concept of Active Pixel Sensor (APS) [Foss93]. Since then, CMOS image sensors became a very active research topic all around the world. First commercial products based on CMOS image sensors appeared on the market in 1996-97.

1.1.2 APS versus CCD

The principal differences between CCD and CMOS APS image sensors are summarised below [Dier97].

Technical performances

The main technical advantages of the CMOS APS approach are a more flexible pixel operation (logarithmic mode, random access, etc.) and reduced power consumption. CCDs are however less noisy and they show a higher sensitivity (see Table 1-1).

Criterion	CCD	CMOS APS
Spectral response	400-1000 nm	400-1000 nm
Peak quantum efficiency	>50%	>50%
Dynamic range	1e4 linear	1x 10^3 linear or 1x 10^6 logarithmic
Dark limit	0.1 lux typical	1 lux typical
Noise photons	10	100
Integration time	40 ms typical	40 ms typical
Max. frame rate	10 kHz	>> 10 kHz
Pixel number	800K typical	800K typical
Pixel pitch	5-10 µm	5-10 µm
Power dissipation (*)	500 mW typical	50 mW typical
Focal plane processing	none	possible
Access method	serial only	serial, random.

* This value includes external clock generators.

Table 1-1: Technical performance comparison between CCD and CMOS APS

Image quality

CCDs show in general a better image cosmetic quality (low noise, high uniformity, low fixed pattern noise), but are more sensitive to an excess of generated charges (smear, blooming).

Fabrication and costs

One of the key advantages of the CMOS APS is to use the standard CMOS technology and hence to add the benefits of a low cost process, an access to many foundries and the use of standard tools and technological libraries

(standard cells, simulation models, etc.). The development of image sensors is no longer restricted to a few companies and foundries, as it is with the CCD technology.

1.1.3 The camera-on-a-chip paradigm

But certainly the most decisive advantage of the CMOS APS approach is the possibility to integrate, on the same chip as the image sensor, electronics for analog and digital signal processing [Wang90], [Foss93]. These electronics can be designed using standard tools and CMOS libraries, and may include:

- Analog signal processors.
- Analog to digital (A/D) converters.
- Digital Signal Processors (DSP).
- Microprocessors.
- Memories (RAM, FLASH).
- Transmission units (RF, serial, etc.).

It is then possible to design complete on-chip systems called "cameras-on-a-chip". Those systems represent a second-generation of solid-state image sensor technology [Foss95]. Their advantages are:

- Reduced number of components, implying in turn a reduction in system complexity and costs.
- Reduced power consumption.
- Ease of system design and interfacing.

1.1.4 CMOS digital image sensors: the situation today

CMOS image sensors are, at the beginning of the year 2000, well established in the market of video sensors for consumer products (PC-camera, still digital photography). The digital imager especially, with on-chip ADC, is becoming a standard product. Table 1-2 shows the performances of the main CMOS digital image sensors already or soon available on the market. For the moment, intensive on-chip digital processing, although feasible, is limited.

Company	Model	Resolution	Pixel [µm]	Dynamic range [dB]	ADC resolution	Frame rate	Power consumption
Agilent	HDCS-2000	640 x 480	9.0	63	10 bit	15	150 mW @ 3.3V
Conexant	CN1024	1024 x 768	7.0	60	10 bit	25	150 mW @ 3.3V
OmniVision	OV7610	644 x 484	8.4	48	8 bit	30	200 mW @ 5.0V
PixelCam	PCS2210	1032 x 776	7.5	66	10 bit	20	180 mW @ 3.3V
IMS	HDRC-2	640 x 480	12	120	10 bit	30	450 mW @ 3.3V
IMEC	Ibis4	1280 x 1024	7.0	66	10 bit	8	300 mW @ 5.0V
Motorola	SCM2001	640 x 480	7.8	50	10 bit	30	400 mW @ 3.3V
PVS	PVS 800	800 x 600	7.5	56	10 bit	?	150 mW @ 5.0V
Photobit	PB300	640 x 480	7.9	60	8 bit	30	300 mW @ 5.0V
Photobit	PB720	1280 x 720	7.9	60	10 bit	60	250 mW @ 5.0V
Toshiba	TCM5033T	640 x 480	5.6	57	10 bit	30	60 mW @ 2.8V
VVL Vision	VV5500	648 x 484	7.5	57	10 bit	?	80 mW @ 3.3V

Table 1-2: A selection of CMOS APS image sensors already or soon available on the market.

1.2 Future trends in CMOS image sensors

1.2.1 Future applications

The CMOS image sensor technology will gain in maturity and performance in the coming years, and will undoubtedly soon replace the CCD sensors in many "traditional" applications such as digital still cameras and video camcorders.

But the advantages of CMOS image sensors in terms of costs and power consumption will allow the emergence of a totally new range of applications. Coupled with the impressive processing capabilities of the new deep sub-micron technologies and their low-power consumption, such products may soon appear:

- Integration of image sensors on battery-powered electronic devices: portable digital assistants (PDA), laptops, and mobile phones.
- Ultra-miniature camera systems (credit card-sized camcorders, camera watches, etc.).
- Wireless videophones with MPEG image coding and UMTS wireless transmission.
- Battery-powered artificial vision and image recognition devices for access verification, security, robotics, vehicle guidance, etc.

1.2.2 Market perspectives

Digital image applications are expected to increase dramatically in the near future. As an example, the revenues for the worldwide digital camera market (CCD and CMOS) are estimated to reach $4 billions in 2002. Today, the typical annual increase is 35% [Phot99].

Considering CMOS sensors only, the total global market is estimated to be worth about $500 millions in the next three years [Gray99]. The CMOS image sensor market has experienced tremendous growth in the past few years. The forecast for worldwide revenues leads to a compound annual growth rate of almost 60% for the period 1997-2004 [Frost99].

1.2.3 Present limitations

However, the use of CMOS image sensors as a replacement solution for CCDs suffers from the inertial strength of the well-established world of CCD imaging and the lack of courage to leave this technology [Gray99]. For the new applications promised by the advantages of CMOS imaging, the difficulty is very often the amount of data that has to be processed, and the actual limited architecture for battery-powered image processing systems. A true

democratisation of digital imaging involves then not only the image sensor itself, but also the whole system (optics, processing and storage/transmission).

In spite of the numerous advantages brought by the CMOS sensors, the CCD devices are not going to disappear; their superior image quality and excellent noise performances will remain decisive advantages in many applications.

1.3 Presentation of the thesis

1.3.1 Frame of collaboration, partnership

This Ph. D. work has been led under several research and development projects:

- MICROCAM: a basic research project of the Swiss Priority Program Minast, whose topic was the development of "Miniaturised low-power camera system for integration in consumer micro-systems and intelligent surveillance networks". Academic partner: CSEM SA (Swiss Center for Electronic and Microtechnology), Zürich. Industrial partners: Asulab SA, Siemens Building Technologies AG (Cerberus division), EM-Microelectronics Marin SA.
- The MicroSwiss project TR-IT 005 for the development of new low-power Analog-to-Digital Converters.
- Industrial projects.

1.3.2 Scope of the research

This work focuses on the digital design of a CMOS camera-on-a-chip. The following topics are covered:

- Design of low power, video-rate Analog to Digital Converters.
- Study, at the architectural level, of low-power all-digital image sensors.
- Design of logic blocks for on-chip control (exposure time, sensor control, clock generators).

The image sensor design itself (pixel design and signal amplification) is not treated in this work and was not a research topic of the author. The sensor blocks of the two digital cameras, presented in Chapter 6, were designed by the CSEM facilities of Zürich.

1.3.3 Organisation of the report

Chapter 2 consists of a general presentation of the CMOS APS sensor principles and main implementations.

The main principles and techniques for the design of low-power video Analog to Digital Converters are exposed in Chapter 3. The design, realisation and characterisation results of three different video converters are described.

The fourth chapter develops several concepts about digital image sensor architectures, with issues like parallelism optimisation, sensor addressing logic strategies, sensor-ADC interface.

Chapter 5 presents the main logic building blocks that were designed for the on-chip control: exposure time control, inter-channel offset calibration and chip interfaces.

The practical realisations designed during this thesis are exposed in Chapter 6, with two CMOS digital image sensors:

- APS256D, a versatile sensor with 256 x 256 pixels of resolution.
- VGACAM, an imager designed for low-power digital photography.

Finally, the conclusions on this work are presented in Chapter 7.

1.3.4 Main contributions

The contributions of this thesis to the field of the CMOS digital image sensors can be estimated to be:

- Study and realisation of low-power ADCs for video applications, and their efficient implementation on an image sensor chip.
- Study and implementation of the control of original pixel operation modes and sensor addressing architectures.
- Power consumption optimisation of a digital image acquisition system.

1.3.5 Publications

Part of the work described in this report has already been the subject of some publications. The low-power ADCs realisations of Chapter 3 were presented at two international conferences. The first was the International Conference on Electronics, Circuits and System (ICECS) in Lisbon, in September 1998 [Tann98], and the second was the International Symposium on Integrated Circuits (ISIC) in Singapore, in September 1999 [Tann99].

The first digital camera chip (APS256D) was presented at an international workshop of the COST254 European program [Blanc99]. The second one (VGACAM) will be presented at the Electronic Imaging Conference that will take place in the beginning of 2001 [Tann01]. This circuit was also the subject of a patent (European Patent number 0340-00-00200597.3), deposed by Asulab SA.

References

[Blanc99]: N. Blanc, S. Lauxtermann, P. Seitz, S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, E. Doering, "Digital Low-Power Camera on a Chip", *Proc. of Int'l. COST254 Workshop on Intelligent Communication Technologies and Applications with Emphasis on Mobile Communications*, May 5-7, 1999, Neuchâtel, Switzerland, pp. 80-83.

[Dier97]: B. Dierickx, IMEC, presented at the *IEEE Workshop on CCD & Advanced Image Sensors*, June 4-7, 1997, Bruges, Belgium. See also: http://www.imec.be/bo/ccd/evs.html.

[Foss93]: E. R. Fossum, "Active Pixel Sensors - are CCDs dinosaurs?", in *CCDs and Optical Sensors III*, *Proc. SPIE*, vol. 1900, pp. 2-14, 1993.

[Foss95]: E. R. Fossum, "Low Power Camera-on-a-Chip Using CMOS Active Pixel Sensor Technology", *Proc. SLPE'95*, pp. 74-77, October 1995.

[Frost99]: Frost and Sullivan, World Image Sensor Markets, 1999, report #5159-32.

[Gray99]: O. Graydon, "CCD producers see a future in CMOS", in *OLE*, pp. 58-60, May 1999.

[Ogata91]: M. Ogata, T. Nakamura & al, "A small pixel CMD image sensor", *IEEE Trans. Electron Devices*, vol. 38, pp. 1005-1010, 1991.

[Phot99]: Photonics Spectra, p. 92-96, August 1999.

[Rens90]: D. Renshaw, P. B. Denyer, G. Wang, M. Lu, "ASIC Image Sensors", *IEEE ISCS'90*, tech. papers, pp. 3038-3041, 1990.

[Tana90]: N. Tanaka, S. Hashimoto, M. Shinohara, & al, "A 310 k-pixel bipolar imager (BASIS)", *IEEE Trans. Electron Devices*, vol. 37, pp. 964-971, 1990.

[Tann98]: S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, “An 8-bit Low-Power ADC Array for CMOS Image Sensors”, *Proc. ICECS98*, September 7-10, 1998, Lisbon, Vol. 1, pp. 147-150.

[Tann99]: S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, “A 10-bit Low-Power Dual-Channel ADC with Active Element Sharing”, Proc. ISIC99, September 8-10, 1999, Singapore, pp. 529-532.

[Tann01]: S. Tanner, S. Lauxtermann, M. Waeny, M. Willemin, "Low-Power Digital Image Sensor for Still Picture Image Acquisition", submitted at *Symp. on Electronic Imaging 2001*, San Jose, USA, January 21-26, 2001.

[Yadid91]: O. Yadid-Pecht, R. Ginosar, Y. Shacham Diamand, "A random access photodiode array for intelligent image capture", *IEEE Trans. Electron Devices*, vol. 38, pp. 1772-1780, 1991.

[Wang90]: G. Wang, D. Renshaw, P.B. Denyer and M. Lu, "CMOS video Cameras", *Proc. EURO ASIC'91*, 1991, pp. 100-103.

Chapter 2
CMOS Image Sensors

This chapter is an overview of CMOS image sensors, from their physical operating principle to their implementation. Its objective is to present key points for a successful integration of the sensor into a more complex system.

First, the electro-optical properties of the photodiode are presented. Then, the in-pixel amplification principle is described, as well as the main pixel implementations and operating modes. Pixel arrays are further introduces, as well as their related addressing and analog signal conditioning electronics. Finally, some common parameters used for sensor characterisation are presented.

2.1 Photo-detection in CMOS technology

2.1.1 Interaction of light with silicon - carrier photo-generation

Silicon (Si) is the semiconductor used in standard CMOS process. Incident light (photons) interacts with the semiconductor's electrons by transferring to them their energy, allowing the electrons to move to the conduction band. An electron-hole pair is then photo-generated. Since the bandgap of Si is 1.12 eV, only photons with sufficient energy will interact with electrons. The absorption coefficient α [Sze81, p. 750] thus depends strongly on the wavelength of the incident light; for energies below the bandgap, the material is essentially transparent. The higher the energy (the lower the wavelength), the better the material absorption, and the smaller the penetration depth. For too short wavelengths, however, the corresponding absorption coefficient α is very large and the radiation is absorbed very near the surface, where the recombination time of electron-hole pair is short.

2.1.2 The p-n junction for carrier collection

If the photo-generated electron-hole pairs are not separated and collected, they recombine in the material and no photo-detection is possible. A high electric field region must then be used in order to separate photo-generated electron-hole pairs. This is performed with the use of a p-n junction, formed at the contact of two different doped semiconductor regions, like the source and drain diffusions of a MOS-FET transistor.

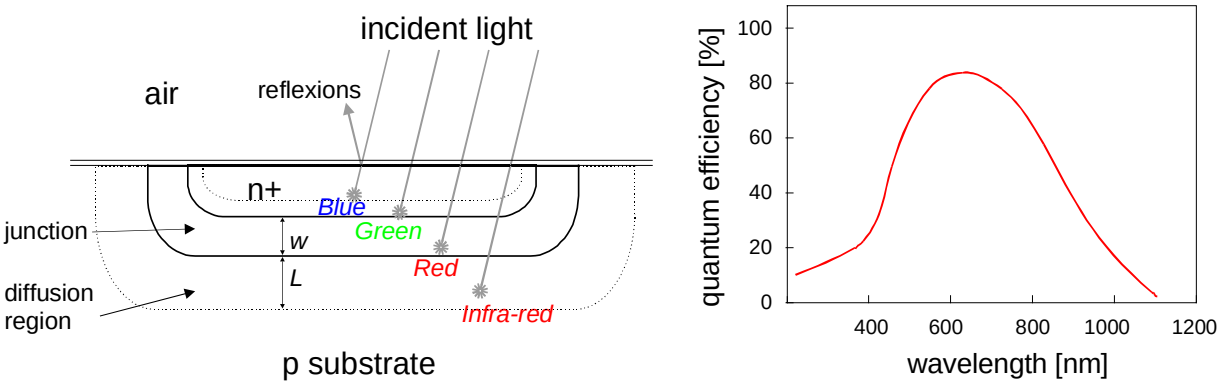


Figure 2-1: a) p - n+ junction with diffusion region and b) typical Silicon light quantum efficiency.

Figure 2-1 a) shows a profile of a p - n+ junction with incident light of various wavelengths. Electron-hole pairs generated inside the depletion region are collected, as well as those generated inside the diffusion regions on each side of the junction. Figure 2-1 b) shows a typical quantum efficiency chart for Silicon in function of the wavelength. The quantum efficiency η is the number of photo-generated charge pairs over the number of incident photons.

The diffusion region contributes mainly to the collection of carriers generated by infra-red light, and its width L can be important (more than 10 microns). In a pixel array, this can cause a reduction in contrast due to horizontal diffusion to adjacent pixels [Foss95]. This is why an infra-red filter is very often used to improve image quality.

The width w of the depletion region is given by [Sze81, p. 77]:

$$w = \sqrt{\frac{2 \cdot \varepsilon \cdot \varepsilon_o}{q \cdot N_{lower}} \cdot \Phi_T} \quad \text{with} \quad \Phi_T = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \qquad \text{Equ. 2-1, Equ. 2-2.}$$

where ε = 11.7 (dielectric constant of Si), ε_o = 8.86 x 10^{-12} [F/m] (permittivity of free space), N_{lower} is the lowest impurity concentration between n+ and p, Φ_T is the built-in voltage, N_A and N_D are the concentrations of acceptors and donors respectively. q = 1.602 x 10^{-19} [C] (elementary charge).

The depletion region features a junction capacitance C, given by:

$$C = \varepsilon_o \cdot \varepsilon \cdot \frac{A}{w} \qquad \text{Equ. 2-3.}$$

where A is the equivalent junction area. For more accurate calculations of the junction capacitance, the side-wall capacitors of the junction should be taken into account. Usually, for CMOS APS pixels, C ≅ 0.5 fF/μm^2.

2.1.3 Current in an illuminated reverse-biased p-n junction

Without illumination, the current in a p-n junction (diode) at temperature T is given by the general expression [Sze81, p. 92]:

$$I = I_o \cdot (e^{\frac{qV}{mkT}} - 1) \quad \text{with} \quad I_o = qD\frac{n_i^2}{N \cdot L}A \qquad \text{Equ. 2-4.}$$

where V is the bias voltage applied across the junction and I_o denotes the diffusion current. D is the diffusion coefficient, L is the diffusion length (see Figure 2-1) and N is the minority carrier concentration. In reverse-biased mode, however, another current, called generation current I_{gen}, is added. This current slightly varies with the bias voltage V and is dominant for CMOS technology at room temperature. k = 1.38 x 10^{-23} [J·K^{-1}], n_i (Si) = 10^{10} [cm^{-3}] (300 K).

Both generation and diffusion current are caused by thermally generated charge carrier pairs. They form the temperature dependant dark current I_s . In silicon, I_s doubles for each increase in temperature of about 8-9 K. At room temperature, the dark current is about a few nA per square centimetre.

Under illumination with the incident (monochromatic) optical power density P the reversed-bias diode shows the following current:

$$I = -I_s - P\frac{q\lambda}{hc}\eta \qquad \text{Equ. 2-5.}$$

h = 6.62 x 10^{-34} [J·s]
c = 2.998 x 10^8 [m·s^{-1}]

for the quantum efficiency η at the wavelength λ.

2.1.4 Photodiode modes in APS sensors

The reverse-biased voltage mode is very well suited to image sensors due, among other reasons, to its low current consumption. The small signal equivalent circuit of the reverse-biased photodiode is given in Figure 2-2, where I_{ph} denotes the photo-generated current, I_s the dark current and C the photodiode capacitance:

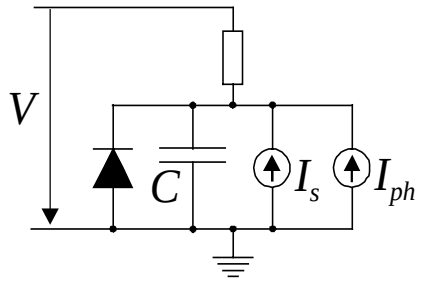


Figure 2-2: Small-signal equivalent circuit of a reverse-bias photodiode.

The reverse-biased photodiode can be operated in several modes:

Integration mode

This mode is the most commonly used in APS image sensors. The photodiode capacitor is periodically charged through a transistor to a specific reverse bias voltage. Illumination causes the photodiode capacitor to discharge in proportion to the light intensity. The (almost) resulting linear response mode can be seen as a photo-generated charge integration mode. Linearity is limited mainly by the capacitor dependence of the reverse-bias voltage.

Current mode

In this mode, the photodiode is not used as a capacitor, but as a current source. Since the linear relationship between photo-current and incident light power is valid for at least 10 decades, very high dynamic range sensors can be designed using this mode, especially sensors with logarithmic response.

2.2 Active pixel

2.2.1 Passive MOS-FET pixel

Early image sensors were realised using the passive MOS-FET pixel consisting of one photodiode and one selection transistor. In this type of sensor, pixels are

arranged into a line by line addressable array (Figure 2-3). When addressed, the pixel photodiode is connected to the column line, which is in turn connected to an output amplifier. Between two consecutive readout cycles, the photodiode capacitor, initially reverse-biased to a reference voltage, discharges in function of light intensity. During readout, the output amplifier charges the photodiode again to the reference voltage, while measuring how much charge is necessary to do so. This measure corresponds to the generated photo-charge, and the column output amplifier produces a proportional output voltage level.

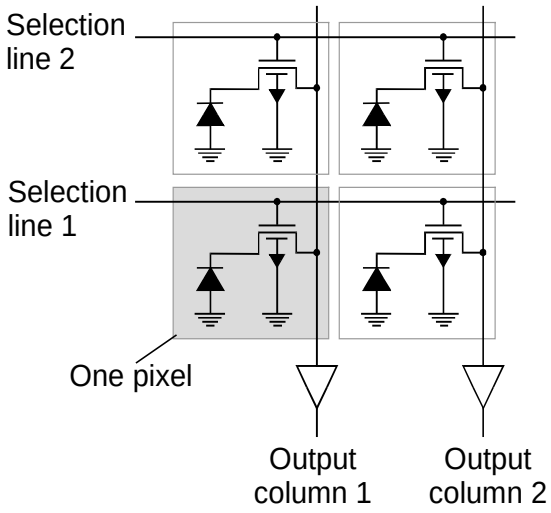


Figure 2-3: Array of passive MOS-FET pixels.

The basic limitation of this approach is the large capacitance at the column amplifier input, caused by the long column line parasitic capacitance. In [Klaa67], it is shown that the Johnson noise in the channel of a single MOS-FET can be referred back to its input and translated into an effective (but hypothetical) gate charge noise, being proportional to the input capacitance. Therefore, the important input parasitic capacitance degrades the performance of the column output amplifier.

This capacitance problem can be alleviated using the so-called Active Pixel Sensor.

2.2.2 Active Pixel Sensor (APS) structure

The idea behind the APS is to move the first MOS-FET device of the column amplifier directly inside the pixel. In this way, the input capacitance of this transistor is minimised, and the corresponding noise figure of the amplification path is improved. A minimum number of three MOS-FET transistors is then required for an APS pixel (Figure 2-4): a source-follower transistor

(amplification), a reset transistor (reset of the gate and photodiode capacitor to the reference voltage) and a selection transistor. The output signal is fed to the column line.

The pixel operation includes three different phases:

- Reset phase: the source follower gate and photodiode capacitor are reset to a constant voltage (usually Vdd) through the reset transistor.
- Integration phase: during this phase, the internal node discharges with light.
- Read phase: the pixel is selected with the selection transistor.

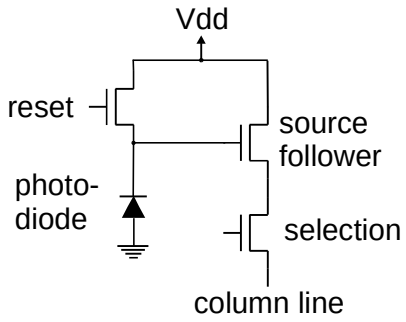


Figure 2-4: Basic APS pixel structure with three n-type transistors.

Based on this first simple configuration, other electronics can be incorporated into the pixel, like photo-gate pixel [Mend94], programmable current source for offset pixel operation [Viet96], electronic shutter with on-pixel memory [Aw96], local feedback loop for high frequency bandwidth [Hupp97], etc.

2.2.3 APS pixel limitations [Seitz96]

Fill factor

The fill factor is the ratio of the light sensitive area of the pixel over its total area. For a given pixel size, the more on-pixel electronics there are, the less the pixel will be sensitive to light. A compromise between pixel size, pixel complexity and fill factor has then to be found. Usually, in APS image sensors, the fill factor is chosen to be 30-40%. Of course, if a higher sensitivity is required, bigger pixels can be designed.

Photon shot noise

The photo-generation of carriers in the photodiode is a statistical process following a Poisson distribution. The maximum quantum-noise limited signal to noise ratio of the photodiode will then depend on the maximum number of

electrons the photodiode capacitance can accept (full-well charge). For example, if the photodiode capacitance is 15 fF, the charge-to-voltage conversion ratio will be 10 μV per electron. A voltage swing of 1 V will corresponds to 100'000 electrons, showing a Poisson noise of 316 electrons. The maximum signal-to-noise ratio will then be 20 x $\log_{10}$ (100'000/316) = 50 dB [Seitz96].

Fixed Pattern Noise (FPN)

Due to process variations and device mismatches, each transistor has slightly different parameters (threshold voltage, etc.). As a consequence, each APS pixel will have a slightly different reset level. This non-uniformity can be considered as a fixed noise, this is why it is called "Fixed Pattern Noise". Its value is usually equal to a few mV rms. Since the FPN is constant, processing the difference between two output values — with and without illumination — can easily compensate it (double sampling operation).

Reset noise

When the reset transistor closes, it induces a kTC noise in the pixel node, caused by the RC-filtered Johnson noise of the reset transistor channel resistor. The charge variance corresponding to this noise is given by:

$$q^2 = kTC \qquad (k = 1.38 \times 10^{-23}\ [\mathrm{J \cdot K^{-1}}],\ q = 1.602 \times 10^{-19}\ [\mathrm{C}]) \qquad \text{Equ. 2-6.}$$

For instance, the rms number of noise electrons in a photodiode with a capacitance of C = 100 fF, introduced by the reset operation at room temperature, is calculated to be 127 electrons [Seitz96].

This kTC noise is difficult to suppress because, unlike the FPN, it is different for each reset operation. A double sampling can also be used, but the same kTC noise must be read for both operations (Correlated Double Sampling), which is difficult with APS sensors because the two sampling operations are separated in time by the exposition itself.

MOS-FET noise

The source follower transistor of the pixel is affected by two different noise sources:

- *"1/f"* noise (or flicker noise). This noise is caused by the charge carrier density fluctuation in the channel, and due to its 1/f power spectrum, it is dominant at low frequencies. Its influence can be neglected at the usual operating row readout frequency of image sensors (a few KHz) by using non-minimum-sized transistors.

- Johnson (resistor) noise in the channel with a white noise power spectrum (thermodynamic origin).

The Johnson noise in the channel can be referred back to the MOS-FET gate input and translated into an effective (but hypothetical) gate charge noise ΔQ. Its rms value is, for a MOS-FET in saturation:

$$\Delta Q = C_{GS}\sqrt{\frac{8 \cdot k \cdot T \cdot B}{3 \cdot g_m}} \qquad \text{Equ. 2-7.}$$

where C_{GS} is the equivalent gate capacitance (including the photodiode capacitance), B is the measurement bandwidth and g_m is the trans-conductance of the MOS-FET. For instance, if C_{GS} = 160 fF, B = 10 MHz, T = 300 K, g_m = 10^{-3} [C·V^{-1}·s^{-1}], the resulting charge noise corresponds to 11 electrons (corresponding, for C_{GS} = 160 fF, to a rms voltage of 11 μV).

Shot noise or current noise

The shot noise is a purely statistical phenomenon, and describes the fact that a current is always associated with a statistical uncertainty of its exact value, due to the quantified nature of charge carriers. The shot noise variance of a current I is given by:

$$i^2 = 2 \cdot q \cdot I \cdot B \qquad (q = 1.602 \text{ x } 10^{-19} \text{ [C]}) \qquad \text{Equ. 2-8.}$$

where B is the measurement bandwidth. For instance, a current of 1 nA will show a current noise of 0.018 nA at a measurement bandwidth of 1 MHz.

Dark current

The dark current of the photodiode is another fundamental limitation of the pixel accuracy. It can be related to a noise expressed in electrons per second because it is proportional to the photodiode integration time.

Numerical example on pixel noise

In order to illustrate the contribution of each noise source and the overall pixel noise performance, let us choose a pixel with the following parameters:

- Photodiode and source follower gate capacitance C_{eff}: 50 fF
- Output voltage swing: 1.5 V
- Bandwidth B of the source follower: 1 MHz.

- Trans-conductance g_m of the source follower: 10^{-3} A·V^{-1}.
- Bias current of the source follower: 2 µA.
- Capacitive load of the output node: 1 pF.

From C_{eff}, and the output voltage swing, the following parameters are determined: sensitivity = 3.2 µV/e, full well charge = 470'000 electrons. The different noise sources can then be calculated:

- Photon shot noise = $0.0032 \cdot \sqrt{NGE}$ mV rms (*NGE* = number of generated electrons).
- Reset noise = 0.28 mV rms.
- MOS-FET noise = 3.3 µV rms.
- Current shot noise = 0.8 nA.

These noise contributions are plotted in Figure 2-5 in function of the number of photo-generated electrons. The electronic noise (photon-independent) is dominant for low light levels. For higher intensities the photon shot noise becomes dominant, but since this noise is proportional to the square root of the number of electrons, the overall SNR increases and is maximum when the light intensity reaches its saturation value (full well).

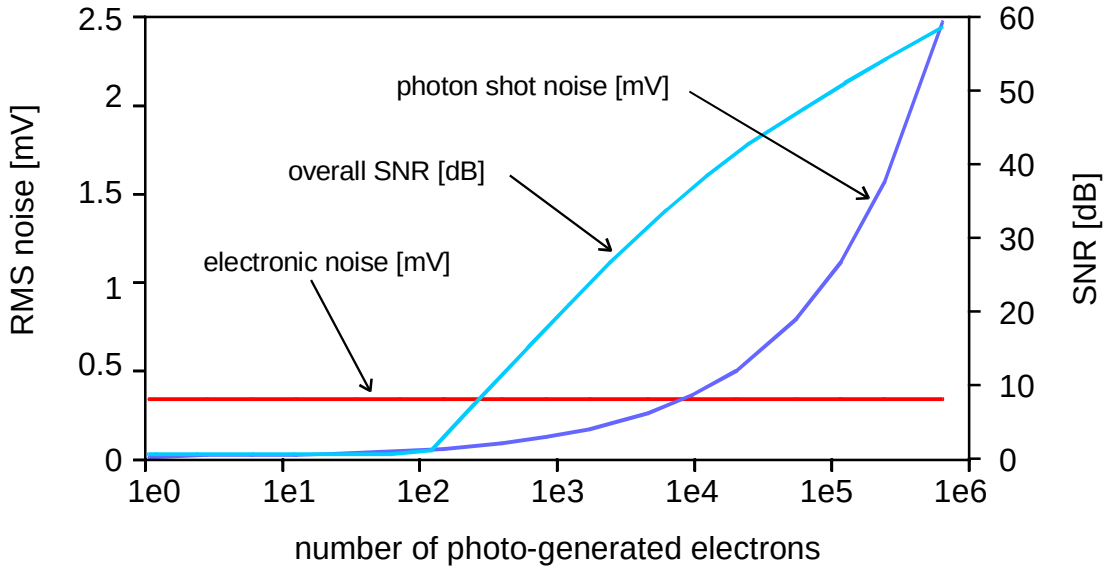


Figure 2-5: Overall noise and corresponding SNR in function of light intensity.

2.3 Pixel array

2.3.1 General structure

An Active Pixel Sensor includes the pixel array, a row addressing logic block, a column addressing block, an analog column processing block and an output buffer block (Figure 2-6).

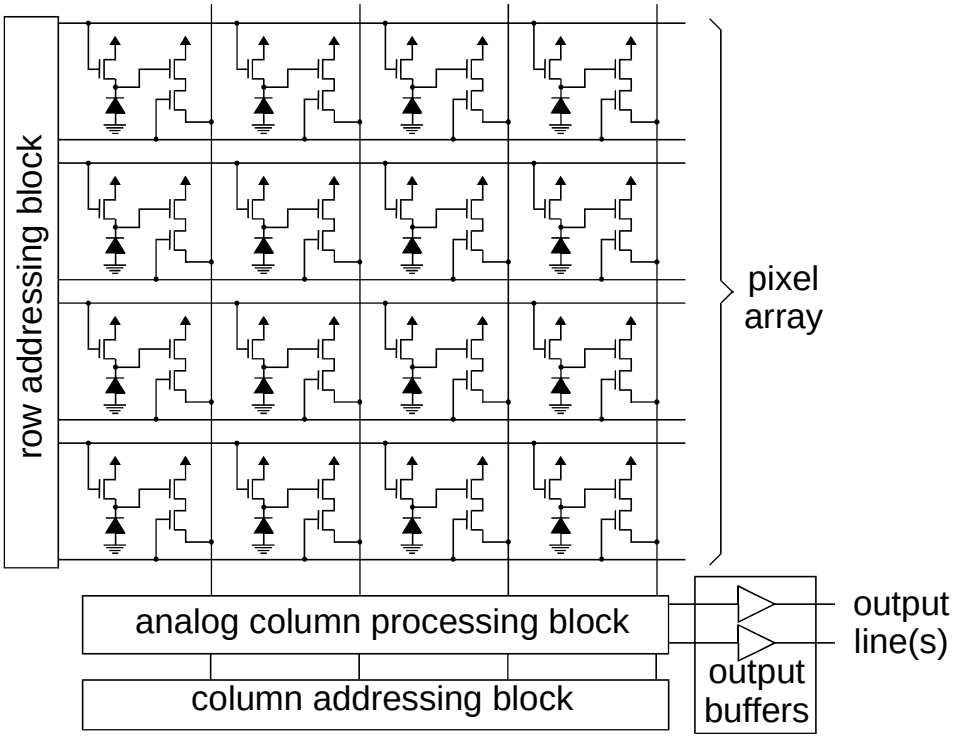


Figure 2-6: General architecture of an APS sensor.

The pixels are usually controlled through horizontal lines. The vertical direction is generally used for routing the output column lines and global signals to all the pixels (power supply, etc.). While the row addressing logic directly accesses the pixels, the column addressing logic acts on the analog column processing block. Depending on the parallelism in the readout architecture, one or several columns may be amplified at the same time through the output buffer block.

2.3.2 Modes of operation

Depending on the pixel structure and on the addressing logic, several operation modes are possible for the pixel array. The next paragraph presents several of the most used modes. They can in some cases be combined.

Line (or snap-rolling) shutter mode

In this operation mode, the pixel photodiode is operating in the charge integration mode (see sub-section 2.1.4). Therefore, all the pixels are first reset row by row by a scanning reset operation performed by the row addressing logic (Figure 2-7). Then, an integration phase occurs where photo-charges generated by light are collected by the photodiode. Finally, the row addressing logic performs a scanning read operation where each row is selected one by one and read out. Of course, the reset and readout scanning frequencies must be the same in order to ensure an equal exposure time for each pixel.

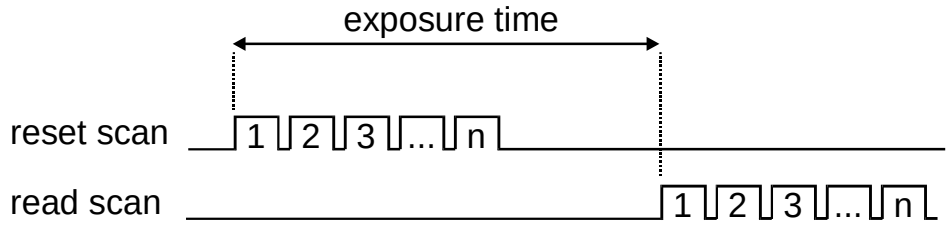


Figure 2-7: Timing diagram of the line shutter mode (sensor with n rows).

The line shutter mode is used with the basic APS pixel presented in Figure 2-4. It can also be used with more complex pixels. This shutter mode is unfortunately limited in speed by the scanning readout frequency, and is in general not suited to the acquisition with short exposure times, like the acquisition of moving objects.

Global (electronic) shutter mode

In this mode, the integration phase of all the pixels begins and ends at the same time, as it is the case with a mechanical shutter encountered in traditional film-based photo cameras. First, the pixels are all reset at the same time through a global reset signal. Then, the integration phase occurs. The scanning readout, in this case, cannot be performed directly afterwards, because each pixel row would have a slightly different exposure time, the last read out rows being longer exposed than the first ones. So a modified pixel must be used in which a local memory node, protected from light, can store at the end of the integration phase the pixel output value. An example of such a pixel is shown in Figure 2-8 [Aw96], using only n-type MOS devices. A shutter transistor is added, enabling to separate the photodiode node from the source follower gate node, this latter becoming the analog memory node.

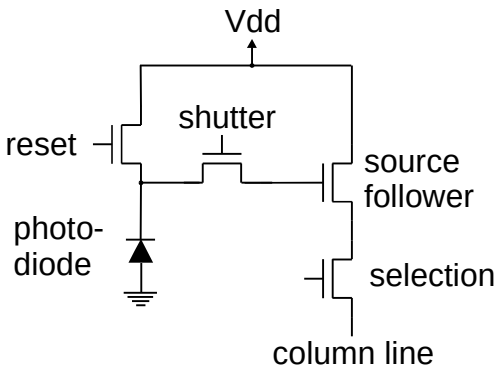


Figure 2-8: Schematic diagram of a pixel with shutter function.

A possible timing diagram of the global (electronic) shutter mode is represented in Figure 2-9. The exposure time starts once the reset pulse is low (inactive), and stops when the shutter transistor closes. This latter stays open during the integration phase, allowing the source follower gate capacitance to be used for integration.

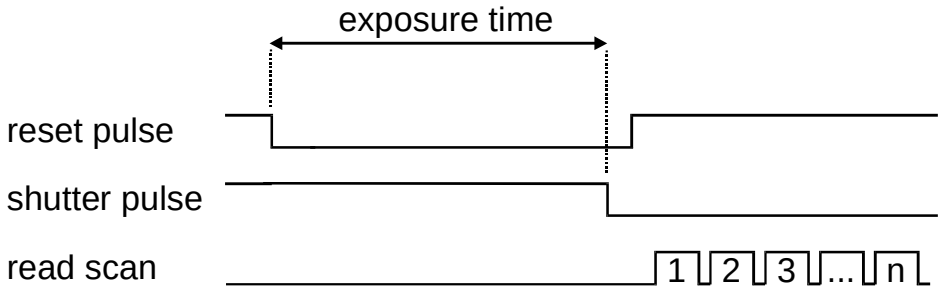


Figure 2-9: Timing diagram of the global shutter mode (sensor with n rows).

The global shutter mode allows having a very short, homogeneous exposure time for all pixels. It also relaxes the readout speed requirement, since this latter no longer degrade the image quality.

The main limitations of the global shutter mode is the pixel memory, difficult to design and subject to several degradations (charge injection of the shutter transistor, leakage current strongly temperature dependent, photo-charge collection, etc.).

Current-mode (logarithmic) operation

The two previously presented modes concerned sensors with pixels in integration mode, corresponding to a linear behaviour of the output voltage in

function of light intensity. However, any APS pixel can be operated in current mode (see sub-section 2.1.4) by using the reset transistor as a resistor like in Figure 2-10, where M1 is continuously biased by a constant voltage V_G.

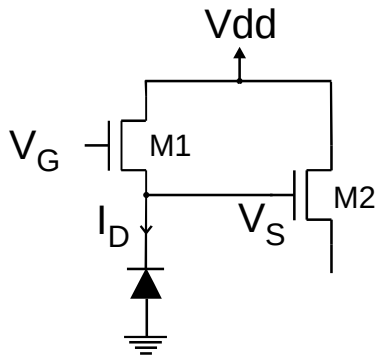


Figure 2-10: Pixel operating in logarithmic mode.

The reset voltage V_G must be chosen so that the reset transistor is working in weak inversion ($V_{GS} < V_T$). In weak inversion, the drain current increases exponentially with the gate voltage and is, in a first approximation, independent of the drain voltage:

$$I_D \cong I_{Do} \cdot \exp\frac{q \cdot V_{GS}}{nKT} \qquad \text{Equ. 2-9.}$$

Expressed in a logarithmic scale, this equation becomes:

$$\ln(I_D) = \ln(I_{Do}) + \frac{q \cdot V_{GS}}{nKT} \qquad \text{Equ. 2-10.}$$

If the gate voltage of transistor T1 is constant, the source voltage will decrease following a logarithmic law with the photo-generated current I_D. The pixel response is logarithmic. Since, for MOS-FET devices, $n \approx 1.5$, the voltage swing on the pixel node is about 40 mV per decade of light. The corresponding dynamic of such a pixel is very high compared to the linear response, as it is shown in Figure 2-11, where the output swing of a pixel is represented in function of the number of incoming photons for both linear and logarithmic modes.

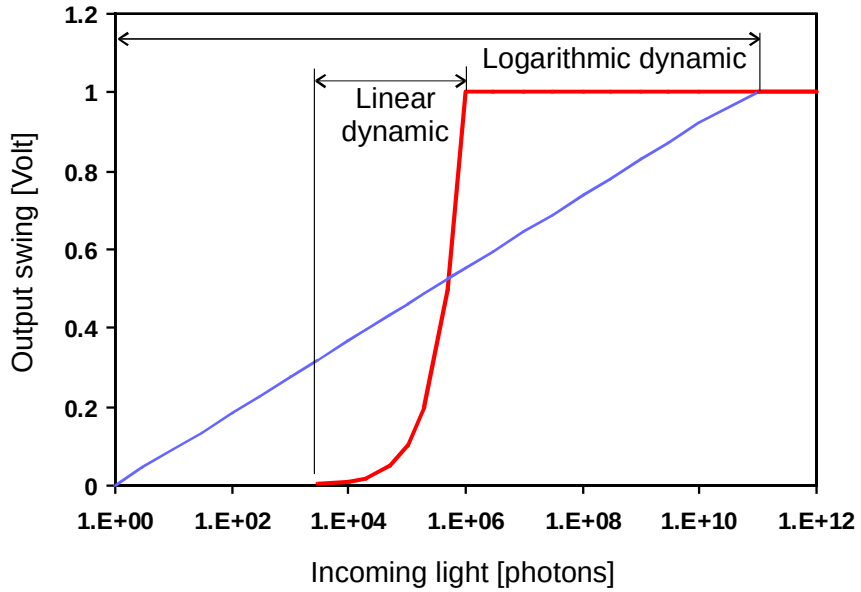


Figure 2-11: Linear and logarithmic dynamic of a pixel.

With the logarithmic response, the integration phase is not necessary, since only the instantaneous current flowing through the pixel is of interest. Thus, an image acquisition consists only of a scanning readout.

2.3.3 Row and column addressing

Shift register addressing logic

For applications requiring a complete image readout, a sequential addressing logic can be chosen. It consists usually of a shift register with as much registers as the number of rows/columns (Figure 2-12 a). A pulse is introduced into the shift register, and propagates along, selecting a different row/column at each clock cycle.

Decoder addressing logic

Another implementation for the row/column addressing logic relies on a decoder with as many output lines as there are rows/columns (Figure 2-12 b). For instance, an 8-bit input decoder can address at maximum a $2^8 = 256$ rows/columns sensor. The decoder can be controlled with a counter, a state machine or other logic. This implementation allows windowing, random access or sub-sampling acquisition of the pixel array.

Sub-sampled images

Image sub-sampling occurs when only one pixel over *n* is read out either horizontally, or vertically, or in both directions, *n* being usually a power of two. An image with the same angle of view but with reduced resolution can then be obtained. An elegant solution for a sub-sampling addressing logic consists of mixing a shift register with a decoder, as represented in Figure 2-12 c).

Like any sub-sampling operation, image sub-sampling is likely to cause aliasing artifacts, which may severely degrade the image quality.

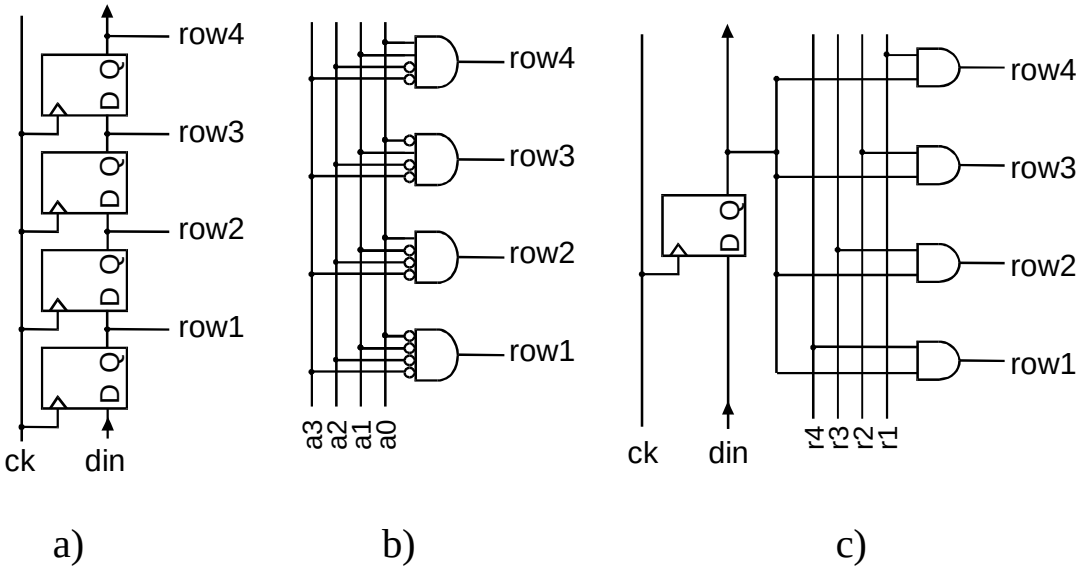


Figure 2-12: a) Shift register, b) Decoder and c) Mixed addressing logic.

Global and row addressing combinations

As previously seen in sub-section 2.3.2, a global shutter mode requires the use of global signals selecting all the pixels at the same time. A "row-wise" selection of the pixels may nevertheless also be required, so that a mixed logic which is able to handle both modes must be implemented. Figure 2-13 shows an example of such logic, able to globally address the reset and shutter lines (through signals "global-rs" and "global-sh"). The reset signals can also be addressed row by row.

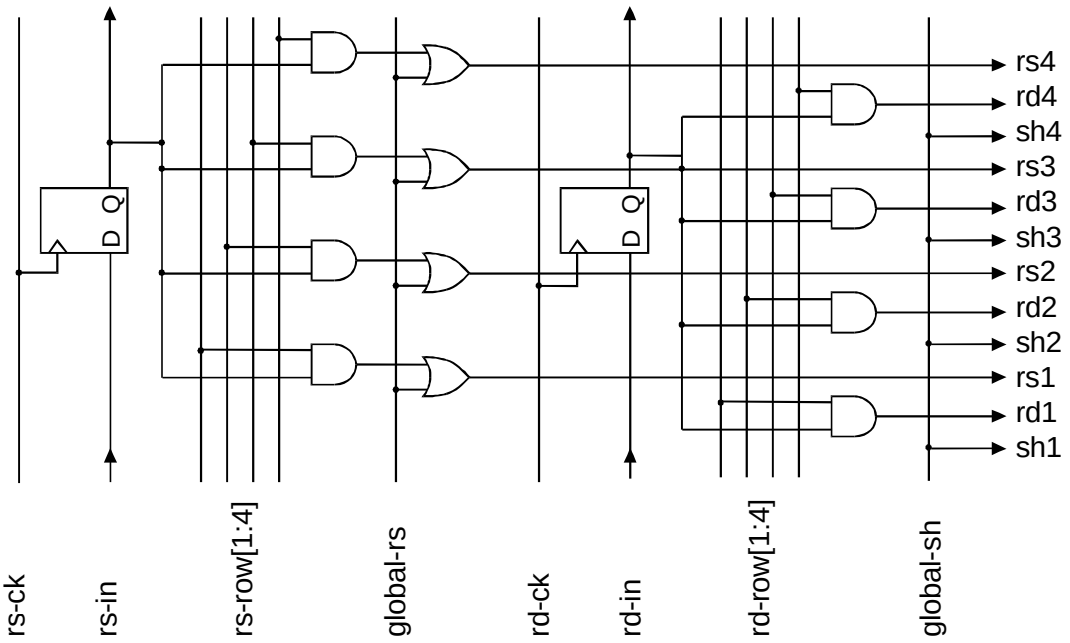


Figure 2-13: Global and row addressing logic for a pixel with global shutter.

Level shifters

A close look at the pixel of Figure 2-4 shows that, with a unique supply voltage Vdd, the maximum reset voltage of the pixel will be Vdd - V_T, where V_T is the threshold voltage of the reset transistor. This "loss" in the reset voltage reduces the pixel output dynamic by the same amount V_T. While this reduction may not be critical for voltage supplies around 5 V, it becomes serious at 3 V.

This reduction in signal swing can be alleviated by using a reset gate voltage increased by a value of V_T above Vdd. By this way, the photodiode is reset at its maximum voltage of Vdd, and the maximum of dynamic is obtained at the output. A higher voltage than Vdd can be generated either on-chip by DC-DC up-converters, or off-chip. Level shifters are used in order to convert the reset signals into a higher voltage.

The same technique can also be used for the other transistors of the pixel.

2.4 Analog signal conditioning

2.4.1 On-pixel amplifier and column readout line

The first element of the signal amplification path is the source follower of the pixel itself. This amplification element must be polarised with a current. A single transistor (M3 in Figure 2-14) is most commonly used as current source. This transistor is common for all the pixels of a column.

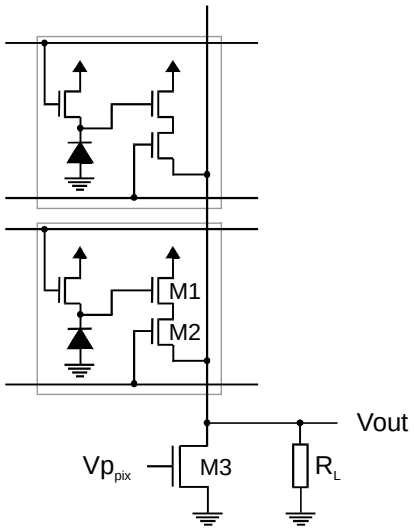


Figure 2-14: Column line and pixel current source.

This first stage source follower amplifier has a limited voltage gain of 1, and is merely devoted to converting the photo-charge into a voltage with maximum sensitivity, while providing a lower impedance to the subsequent amplification stages [Seitz96]. The dimensioning of M1, M2 and M3 is critical for the sensor performance in terms of noise (especially MOS-FET noise and current noise, see sub-section 2.2.3) and output dynamic.

2.4.2 Analog column processing stage (column amplifier)

Once the source follower stage has converted the photo-charge into a voltage, the signal of each column readout line is fed into an analog column processing stage, where several operations can be performed: noise suppression through a (correlated) double sampling stage, signal amplification, etc. Figure 2-15 shows three examples of column analog processing stages.

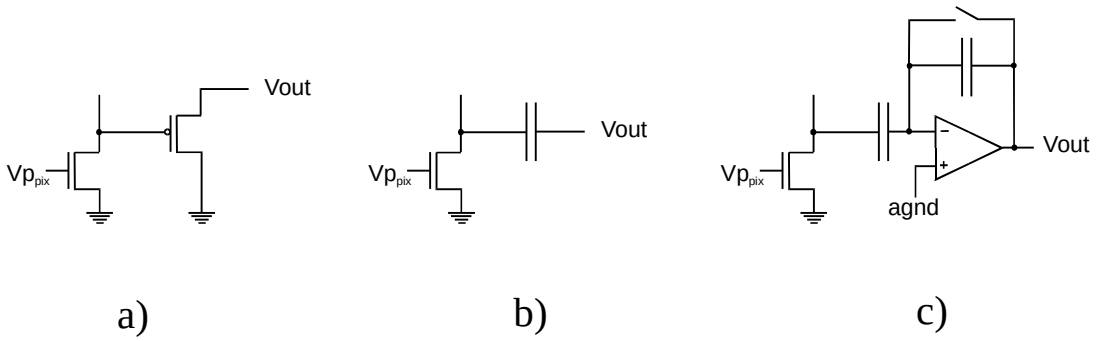


Figure 2-15: Three examples of analog column processing stages with a) source follower, b) double sampling capacitor and c) complete double sampling stage with OTA amplification.

2.4.3 Output bus and output buffer

The signals coming out from the analog column processing stages are usually multiplexed into one (or several) output readout bus(ses) in order to form the sensor output signal. The selection of each column stage output is performed through a switch by the column addressing logic.

Finally, the signal is processed through the output buffer block that may perform different operations depending on the application, for instance:

- Buffering for driving other units or pads.
- Second stage of a double sampling unit.
- Current source for a second source follower stage.
- Programmable gain amplification.
- Non-linear (gamma correction) [Wang91] or linear (RGB to Y-Cb-Cr) transformation.

The next figure shows two examples of output buffers with their corresponding analog column processing stage, column addressing logic and output bus.

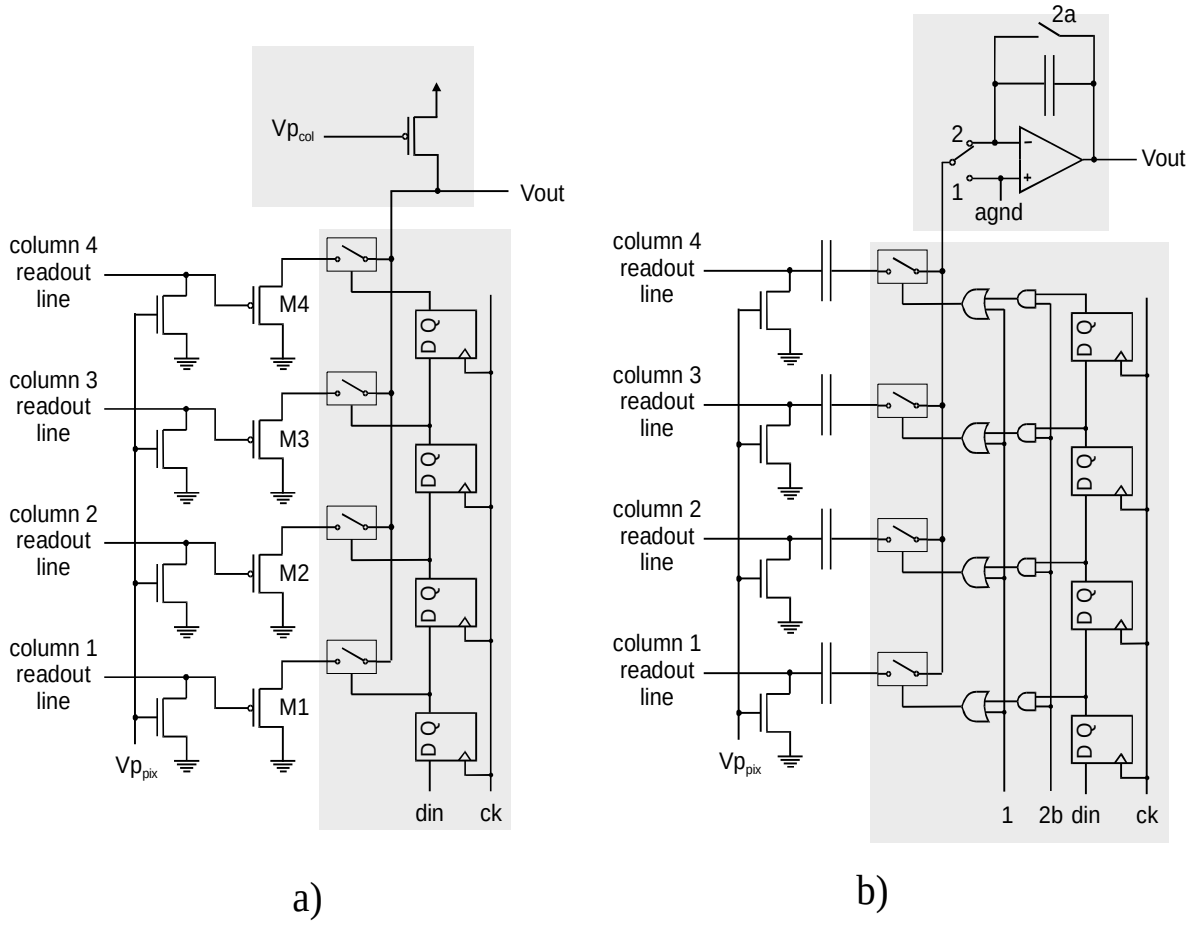


Figure 2-16: Two examples of column readout circuitry and output buffers.

Figure 2-16 a) shows an output buffer made only of a current source transistor biased with the voltage Vp_{col}. This is the current source of the column source follower transistors M1 to M4. Figure 2-16 b) represents a more complex output buffer with a switched integration capacitor and an amplifier. This second configuration is able to perform, in association with the column capacitors, a FPN suppression operation. In those two examples, the column addressing logic is made of a shift register addressing successively each column (four columns are represented).

2.4.4 Fixed Pattern Noise suppression

The pixel-to-pixel reset voltage fluctuation in a CMOS sensor introduces an equivalent noise of a few mV rms called fixed pattern noise (see sub-section 2.2.3). This source noise is usually dominant. Assuming that it is constant over time, it can easily be suppressed.

A first, straightforward noise suppression method consists of storing, preferably in the digital domain, a complete black image, containing no signal but only FPN. Then, when a normal image is acquired, the difference between the two images is calculated to produce a corrected final image. This method may not be efficient in practice because it requires the calibration of each sensor by taking a black image from it and storing it into a permanent memory. Then, each time an image is taken, the difference must be computed.

The usual method for FPN suppression is called "Double Sampling". It is performed row by row in the column readout circuitry of an APS sensor. For each row, the following steps are carried out:

1. Selection of the pixel row. The output pixel values are available on the column readout lines.
2. First sampling of the column readout lines: the illuminated pixel values of the whole row are stored.
3. Reset of the pixel row. The reset pixel values are available on the column readout lines.
4. Second sampling of the column readout lines: the reset pixel values of the whole row are stored.
5. The difference between the two samples is amplified, resulting in a FPN-free signal.

An implementation of a FPN suppression stage is partially shown in Figure 2-16 b), while the corresponding timing is shown in Figure 2-17. In a first phase (signal 1), output pixel values are stored into the column capacitors, their right plate being grounded. Then, during a second phase, the right capacitor plate is

left floating and the pixel is reset. The charge inside each capacitor therefore corresponds to the difference between output and reset pixel voltages. This charge is read out by the switched capacitor output buffer, column after column (signals 2a and 2b, four columns are shown).

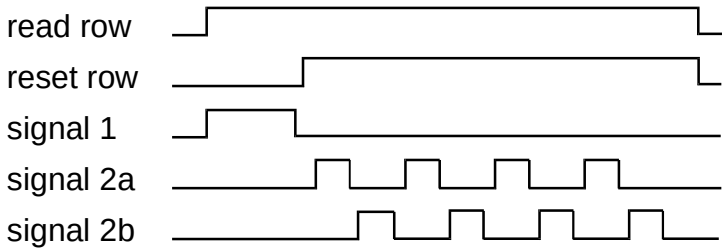


Figure 2-17: Timing of the FPN stage shown in Figure 2-16 b).

2.5 CMOS sensors characterisation

This last section enumerates the main parameters used to characterise a CMOS image sensor - or to establish its specifications.

2.5.1 Sensitivity parameters

The sensitivity of an image sensor is its ability to be sensitive to light. This faculty can be expressed in several different ways.

Spectral response (SR), quantum efficiency

The spectral response is the ratio between photo current and incoming light power for a given wavelength. It is expressed in Ampere per Watt [A/W].

The quantum efficiency η is the ratio between the number of generated electrons and the number of incoming photons for a given wavelength. η and *SR* are linked by the following relation:

$$\eta = SR \cdot \frac{hc}{q\lambda}$$

$h = 6.62 \times 10^{-34}$ [J·s] = Planck constant
$c = 3 \times 10^{8}$ [m·s^{-1}] = speed of light

Equ. 2-11.

Sensitivity

The sensitivity is the ratio between the output signal and the input signal for a given wavelength. Usually, the output signal is expressed in [Volt·s^{-1}] and the input signal in [W·m^{-2}]. If the human eye sensitivity characteristics must be taken into account, the input signal is expressed in [lux].

Sensitivity in lux, ASA/ISO

The sensitivity may also be simply expressed in lux, without any reference to the output signal. In this case, it is a measure of the minimum light conditions required for a "good" sensor operation. For visible light, 1 W/m^2 is about 70 lux. The sensitivity is sometimes also given in ASA/ISO units, which is an empirical procedure to obtain equivalent photo-chemical film speed.

2.5.2 Noise parameters

Noise

The noise measurement of a sensor is usually performed in the darkness, with short integration times (in order to avoid the effect of leakage currents), and consists of the acquisition of many images. The rms deviation of the output voltage for one pixel is then calculated and gives, in millivolt, the "purely electronic" sensor noise, also called "noise floor" because it is measured with the best conditions.

The noise can be converted into an rms number of electrons through the charge conversion factor C_{eff}, which is the ratio between photo charge at the pixels and output voltage. C_{eff} corresponds to the effective capacitance of the pixel, and is expressed in Farad.

Signal to noise ratio (SNR)

The signal to noise ratio is given by the output signal voltage range divided by the output signal rms noise. Its value strongly depends on the measurement conditions (light intensity, integration time). For strong intensities, the SNR is usually limited by the Poisson photon distribution, and for weak signals it is usually limited by the sensor electronic performances.

Dynamic range

The Dynamic range is the ratio of the light saturation intensity with the light noise equivalent intensity. Usually, the best noise figure is chosen (noise in the darkness with small integration time = noise floor). In a linear system, this is the same as SNR (if the best noise figure for SNR measurement has also been chosen).

2.5.3 Spatial response parameters

Modulation transfer function (MTF)

The modulation transfer function is a measurement of the sensor spatial frequency response. Both horizontal and vertical directions may be characterised. The measurement consists of projecting on the sensor a pattern with a spatially modulated amplitude (spatial frequency) (Figure 2-18 a).

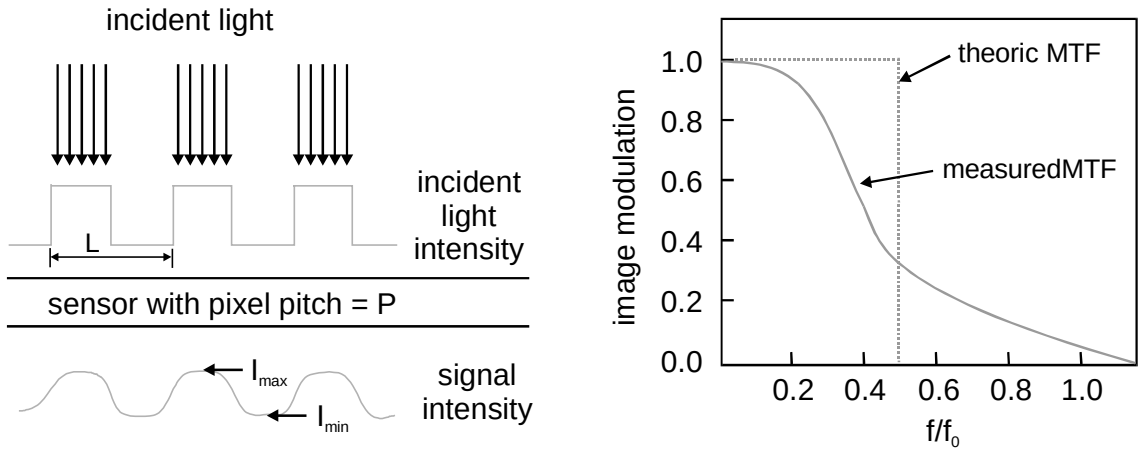


Figure 2-18: a) Incident light and b) Transfer function for a MTF test.

Ideally, the sensor should be able to detect the spatial frequency of the incident light as long as its frequency is not higher than the sensor spatial frequency resolution. If we define the signal modulation with its maximum and minimum intensity [Duto93]:

$$M_{signal} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \qquad \text{Equ. 2-12.}$$

the modulation transfer function is then the ratio of the signal modulation with the light modulation:

$$MTF = {M_{signal}}/{M_{light}} = M_{signal} \qquad \text{Equ. 2-13.}$$

The MTF depends on the incident light spatial frequency $f = 1 / L$, whose range is usually chosen to extend from 0 to the spatial frequency resolution $f_o = 1 / P$

of the sensor, where P is the sensor pixel pitch and L the modulation spatial period of the incident light. Figure 2-18 b) shows an ideal MTF, whose value is equal to one for spatial frequencies below the "Nyquist" frequency $f = 0.5 \cdot f_0$. For $f > 0.5 \cdot f_0$, the MTF is zero because no spatial modulation can be detected any more. An example of a measured MTF is also represented in Figure 2-18 b).

2.5.4 Other parameters

Blooming

When the sensor is over-illuminated in certain areas, the excess of generated carriers may not be collected and may diffuse in adjacent pixels that are not illuminated. This effect is named blooming, and may cause an increase in size of the saturated objects of the image.

Defective pixels

Defective pixels are unavoidable due to the process yield, and are of different types:

- The pixel appears always black (= reset), or always white (= empty).
- The pixel has an excessive dark current and appears black, grey or white depending on the integration time.
- The pixel sensitivity is too different compared to the overall sensitivity.

Defective pixels are invariant and, like FPN, their effect on the image can easily be corrected as long as their number is not too high or they are not grouped in clusters.

2.6 Conclusion

The working principles of the CMOS active pixel were presented, as well as its main limitations. The general architecture of a pixel array was explained, from the addressing logic to the readout analog amplifiers. Finally, some of the most common parameters used for the characterisation of CMOS image sensors were given.

References

[Aw96]: C. H. Aw and B. A. Wooley, "A 128 x 128 Pixel Standard CMOS Image Sensor with Electronic Shutter", *IEEE JSSC*, Vol. 31, No. 12, pp. 1922-1930, December 1996.

[Duto93]: Michel Dutoit, "Technologies Microélectroniques", notes de cours, EPFL, pp. IV-28 to IV-30, 1993.

[Foss95]: E. R. Fossum, "Low Power Camera-on-a-Chip using CMOS Active Pixel Sensor Technology", *Proc. SLPE'95*, October 1995.

[Klaa67]: F. M. Klaassen, J. Prins, "Thermal noise of MOS transistors", *Philips Research Reports*, Vol. 22, pp. 505-514, 1967.

[Mend94]: S. Mendis, S. E. Kemeny, E. R. Fossum, "CMOS Active Pixel Image Sensor", *IEEE Trans. on Electron Devices*, Vol. 41, No. 3, pp. 452-453, March 1994.

[Seitz96]: P. Seitz, "Semiconductor Photosensors", *Lecture course at the University of Neuchâtel*, 1996.

[Sze81]: S. M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, New-York, 1981.

[Viet96]: O. Vietze and P. Seitz, "Image sensing with programmable offset pixels for increased dynamic range of more than 150 dB", *Proc. SPIE*, Vol. 2654, 1996.

[Wang91]: G. Wang, D. Renshaw, P. B. Denyer and M. Lu, "CMOS video cameras", *Proc. IEEE EURO ASIC'91 Conference*, pp. 100-103, 1991.

Chapter 3
Low Power Video ADCs

Analog to Digital (A/D) Conversion for video applications has gained importance with the emergence of numeric algorithms and standards for video and television (HDTV, MPEG, etc.). Digital techniques are also applied to image acquisition devices, and are gently establishing themselves in the electronics consumer market with products such as DV (Digital Video) camcorders and digital still cameras.

The introduction of CMOS imagers allows the integration on the same chip of both AD converter and image sensor, and has two indirect consequences: the first is to give more importance to a low-power A to D implementation. Indeed, with the CMOS sensor being a very low power device, any other on-chip block must feature the same characteristics in order to keep the overall power consumption low. This is less the case with CCD imagers whose power consumption is dominant. The second consequence is to give more consideration to small size ADCs in order to minimise the overall chip area encompassing both image sensor and A/D converter.

This chapter presents several low-power video ADCs developed during this thesis. The key issue is low-power operation, but other important considerations are also taken into account when justifying the choice of the A/D conversion principle, over all the possible approaches.

Sections 3.1 to 3.4 form a general introduction about low-power video ADCs, and comment the main technical choices that were made. Sections 3.5 and 3.6 present a first converter (8-bit), relying on a parallel-serial approach. Sections 3.7 and 3.8 present a second and third realisation with 10 bit of resolution, both developed around a parallel-pipelined architecture. Finally, section 3.9 summarises the performances of the three realisations.

3.1 Analog to Digital conversion

An analog to digital conversion consists of transforming an infinite (continuous) precision physical value into a finite (quantized) precision number. In the electronic domain, an analog to digital converter transforms usually (but not only) a voltage value into a digital binary representation.

An ADC is characterised by its transfer function and by general, static and dynamic parameters, described in the following sub-sections. A more complete description can be found in [Hoes94] and [Shei86].

3.1.1 ADC transfer function and general parameters

The transfer function of an ADC is a uniform staircase characteristic, representing the relation between all analog inputs within the specified input range and a limited number of digital output codes. The transfer function is static and is not a frequency response. An example is shown in Figure 3-1, representing both ideal (without errors) and practical (with errors) transfer functions of a 4-bit ADC with binary encoding (other codes are possible [Shein86]).

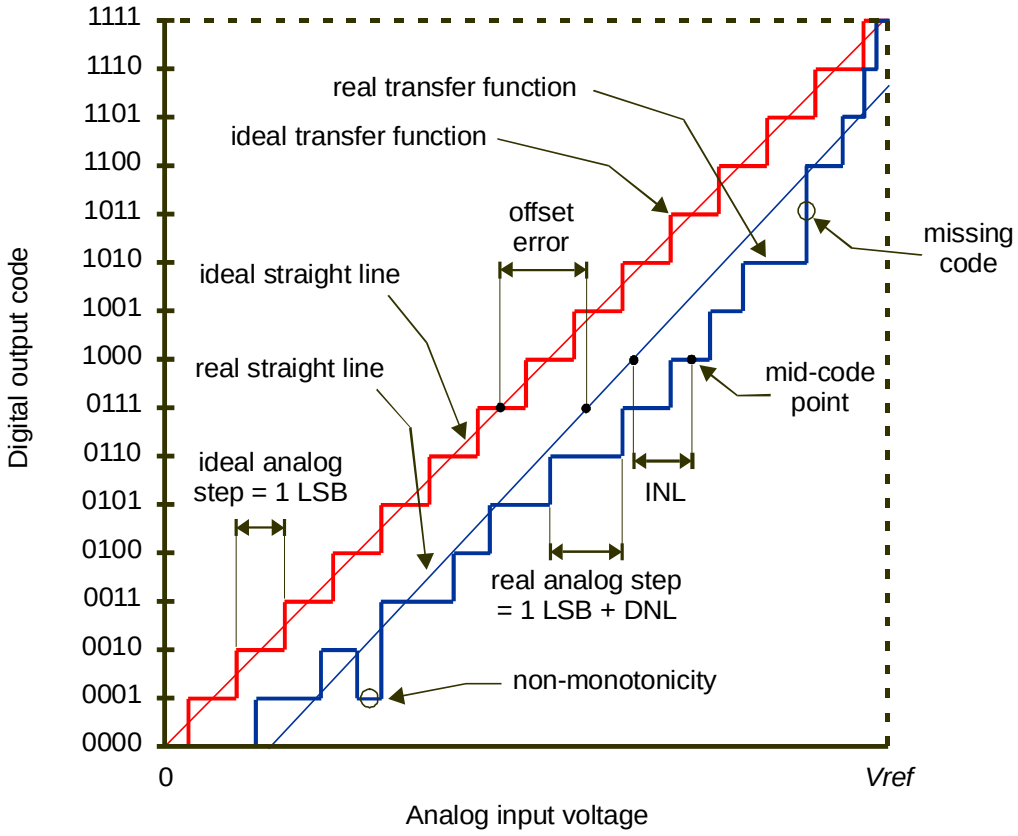


Figure 3-1: Ideal and real transfer functions for a 4-bit ADC.

The ideal straight line of an ADC is crossing all the mid-code points of the ideal transfer function. The real straight line can be obtained from the real transfer function by either: 1/ Connecting the mid-code points of its extreme codes, 2/ Performing a linear regression on its mid-code points or 3/ Performing a linear regression, but without the extreme portions. The third method is usually used, and will be considered in the following, with the valid interval specified.

Resolution

The resolution *n* defines the number of quantification levels 2^n of an ADC; it represents also the number of bit of the digital code. It can be a non-integer value. For bipolar converters (signed result), *n* includes the sign bit.

Reference voltage

The reference voltage V_{ref} defines the input range of the converter and the value V_{LSB}, which is the input voltage corresponding to an LSB (Least Significant Bit). Those values change if the converter is unipolar or bipolar (Table 3-1).

Converter type	Input range	V_{LSB}
Unipolar	$0 \le V_{in} \le V_{ref}$	$V_{ref} / 2^n$
Bipolar	$- V_{ref} \le V_{in} \le V_{ref}$	$V_{ref} / 2^{n-1}$

Table 3-1: Input range and LSB voltage value in function of V_{ref} .

Quantization error

The quantization error is the natural error that occurs when a signal is digitised. It is comprised between –0.5 and +0.5 LSB. The quantization error can be displayed in function of the input voltage, and gives the error function of an ADC:

$$\varepsilon_q = V_{in} - N * V_{LSB} \qquad \text{Equ. 3-1}$$

where *N* is the digital code corresponding to V_{in} .

3.1.2 ADC static parameters

Offset and gain error

The offset error of an A/D converter is the horizontal distance separating the ideal and the real straight line for the same output digital code. Usually, the

minimum code is chosen for computing the offset error [Ti95]. An offset error is expressed in input-referred LSB.

The gain error of an ADC is the difference in slope between the ideal and the real straight line, usually expressed in %. If expressed in LSB, it corresponds to the resulting input-referred absolute error over the whole dynamic.

Monotonicity and missing codes

The monotonicity of an ADC is respected when an increasing of the input voltage does not result in an decreasing of the digital output code (Figure 3-1).

An ADC is said to have no missing code when all the possible output digital codes can be generated (Figure 3-1).

Differential Non-Linearity error

The Differential Non-Linearity (DNL) error is a measure of the uniformity of the transfer function step sizes. It corresponds to the maximal difference between the analog input range corresponding to an output code and the ideal step V_{LSB} [Ti95]. Each digital output code has its associated DNL value, expressed in LSB. If the absolute value of the DNL error is less than 1 LSB, the converter has no missing codes. If it is strictly less than 0.5 LSB, the converter is monotonic. The DNL can never be smaller than –1.

Integral Non-Linearity error

The Integral Non-Linearity (INL) error is the deviation of code mid-points from their ideal location on the real straight line (see Figure 3-1). In this error, the gain, offset and quantification errors are not included. Each output digital code has its associated INL value, expressed in LSB. The INL can be obtained by integration (summation) of the DNL errors.

3.1.3 ADC dynamic parameters

Signal to Noise Ratio

The Signal to Noise Ratio (SNR) of an ADC is defined by [Robe89], [Ti95]:

$$SNR = \sigma_s^2 \Big/ \sigma_\varepsilon^2 \qquad \text{Equ. 3-2}$$

where σ_s^2 and σ_ε^2 represent the variance of the input signal and the variance of the quantification error, respectively. If the input signal is a sinusoid of amplitude *A*, its variance is:

$$\sigma_s^2 = A^2/2 \qquad \text{Equ. 3-3}$$

The estimation of the quantification error variance is made under the assumption that its error probability $p(\varepsilon)$ is uniform within a quantification interval of $(-V_{LSB}/2; V_{LSB}/2)$. In this interval: $p(\varepsilon) = 1/ V_{LSB}$. We get [Font83]:

$$\sigma_\varepsilon^2 = \int_{-\frac{V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} \varepsilon_q^2 \cdot p(\varepsilon) d\varepsilon = \frac{V_{LSB}^2}{12} \qquad \text{Equ. 3-4}$$

The Signal to Noise Ratio (SNR) is then:

$$SNR = \frac{6 \cdot A^2}{V_{LSB}^2} = \frac{3 \cdot A^2 \cdot 2^{2n}}{2 \cdot V_{ref}^2} \qquad \text{Equ. 3-5}$$

The SNR will be maximal for maximal amplitude input. Expressed in dB, it is:

$$SNR_{MAX} = \frac{3}{2} \cdot 2^{2n} = 1.76 + 6.02 \cdot n \quad \text{[dB]} \qquad \text{Equ. 3-6}$$

3.1.4 Special requirements for video applications

Resolution

In a video system, the ADC resolution defines the number of quantification levels for the image intensity (grey–levels). The relative dynamic of the human eye depends on the image content, but is usually in the range of 10^2. An 8-bit ADC (256 grey-levels) has then a sufficient resolution in most applications. However, if the image has a low contrast, or has regions with very small gradients in intensity, this value may not be sufficient. This is the case in medical imaging where images obtained by radiography often contain vital details of the same intensity as the background, and thus need ADCs with 10 or even 12 bit of resolution. However, most of the applications do not require more than 8 bit.

Sampling rate

The second main requirement for video ADCs is the sampling rate; depending on the targeted video application, its range extends from 1 to 65 MSample/s (Millions of Sample per second), and even more for high-speed video cameras, not described here. Table 3-2 gives an overview of the required sampling rates for usual image sizes. Frame rate is assumed to be 30 frame/s (frame per second).

Format	Horiz.	Vert.	Pixel number	Sampling rate
QCIF	176	144	25'344	760'320
CIF	352	288	101'376	3'041'280
VGA	640	480	307'200	9'216'000
SVGA	800	600	480'000	14'400'000
XGA	1'024	768	786'432	23'592'960
SXGA	1'280	1'024	1'310'720	39'321'600
HDTV	1'800	1'200	2'160'000	64'800'000

Table 3-2: required sampling rates for common video formats.

3.1.5 Characterisation of A to D converters

We basically distinguish between static ADC tests, aiming at characterising the transfer function of the ADC, and dynamic tests, whose goal is to have information on the ADC behaviour in the frequency domain [Hoes94].

Static testing: ramp test method

In the ramp test, a precision voltage source is used to generate a DC analog input signal that can be incremented in very small step sizes. At each step, the ADC samples the DC level a number of times. These data are collected and analysed by a computer, that defines, by code apparition probability, the location of transition points between output codes. The process is performed over the whole input range, with ascending and descending ramps. DNL, INL, gain and offset errors can thus be determined.

Dynamic testing: FFT method

Several methods exist for ADC dynamic testing (histogram analysis, FFT, pulse test) [Hoes94]. They are sometimes preferred to static test because they are faster and, for high frequency signals (referred to the sampling rate), they better

characterise the ADC behaviour in real application. Their drawback is that they can mask important ADC anomalies (monotonicity, transition-level noise, etc.).

The FFT method [Miel96] is the most commonly used, and gives important parameters like SNR, SINAD and THD, explained below. In this method, a pure sinusoidal input is sampled, and a Fast-Fourier Transform (FFT) is performed on the collected data. The SNR is then the ratio of the magnitude of the fundamental frequency to the root mean-square (RMS) value of all other frequency magnitudes, but without the DC and harmonics components. It can be calculated from the normalised-magnitude FFT graph, and, since the SNR is a positive decibel value, we have:

$$SNR_{MEASURED} = -20\log\left\{\sum\left[10^{(noise/20)}\right]^2\right\}^{1/2} \quad \text{[dB]} \qquad \text{Equ. 3-7}$$

The SINAD (Signal to Noise and Distortion Ratio), also called SNDR, is calculated the same way, but the harmonics are included in the noise. The effective number of bit (ENB, ENOB) is calculated from the SINAD by:

$$ENB = [(SINAD) - 1.76]/6.02 \quad \text{[bit]} \qquad \text{Equ. 3-8}$$

3.2 Issues for Low-Power ADC operation

The successful design of an ADC in terms of low power consumption involves classical methods used in low-power mixed-IC design, but mainly depends on an efficient optimisation made at the system and algorithmic levels, particularly the choice of the conversion principle.

The analog and digital parts of an ADC do not have always the same design constraints, especially concerning low-power implementation; for instance, decreasing the supply voltage is desired for the digital part, but degrades the SNR in the analog blocks. A compromise between analog and digital constraints is very often to be found.

3.2.1 Digital low-power design

The purely digital part of an ADC usually contributes to a small proportion of the total power consumption. This contribution tends nevertheless to increase with the resolution; high resolution ADCs need more control, decimation filters (for delta-sigma ADCs) or calibration logic in order to reach the required specifications.

There are two major sources of power dissipation in digital CMOS circuits [Chan92]:

$$P_{tot} = P_{dyn} + P_{stat} \rightarrow \begin{cases} P_{dyn} = \alpha_{0\rightarrow 1} \cdot (C_l \cdot V_{dd}^2 \cdot f_{clk} + I_{sc} \cdot V_{dd} \cdot f_{clk}) \\ P_{stat} = I_0 \cdot V_{dd} \end{cases}$$ Equ. 3-9, Equ. 3-10

The first term P_{dyn} is the switching component, present only with logic transitions, where C_l is the load capacitance, f_{clk} the working frequency and $\alpha_{0\rightarrow 1}$ the node transition activity. I_{sc} represents the short circuit current; it is generally negligible at low Vdd and less than 10% of P_{dyn} at high Vdd [Veen84]. The dynamic power consumption is very dominant in circuits with important logic activity.

The second term P_{stat} is due to leakage current I_0, composed of junction leakage current (technology-dependant, but usually negligible) and of sub-threshold MOS current, directly dependent on the technology threshold voltages.

While the static power consumption is technology dependent, the dynamic power consumption can be minimised on several levels:

Physical and layout level optimisation

A reduction of the supply voltage Vdd has a quadratic effect on the power consumption. Therefore, whenever possible, the logic will be supplied with the lowest voltage. An elegant solution is to supply the digital part of an ADC with a fraction of the voltage for the analog part, so that analog block performances are not degraded by a too low voltage supply (as an example, see [Gris97]).

At the layout level, connections have to be minimised, especially those with a high switching activity, in order to minimise the $C_l \cdot f_{clk}$ product. Transistor sizing should ensure that all delay paths are equalised, avoiding unnecessary fast signals or too slow transitions. In general, minimal size transistors should be used whenever possible.

Logic level optimisation

A given logic function should be implemented by using as few resources as possible. Since ADCs are designed to operate at a given frequency, dynamic logic is an interesting alternative, but care has to be taken that its state is correctly defined when the circuit is in standby mode.

Switching activity has to be reduced to its strict minimum by applying hierarchical gated clock techniques, and by avoiding glitch activities, whose contribution to power consumption may be important.

3.2.2 Analog low-power design

The analog part of an ADC is usually the most power-consuming part; for instance, in the case of the 8 – 12 bit range video SC-pipelined ADCs, the main part of the academic realisations show an analog power consumption comprised between 50 and 90 % of the overall ADC consumption. The main effort in the design of low-power ADCs must therefore be done in the analog domain.

Active element design

Most of the ADCs need active elements providing signal amplification, like op-amps or OTAs. The simplest amplifier structures (simple 2-stage, class A, like the Miller OTA) are the most commonly used in low-power design because of their good compromise between performance and power consumption [Lee94]. If a DC gain higher than 70-80 dB is required, other structures must be chosen, like the regulated folded-cascode amplifier [Cho95], the replica-amp gain enhancement amplifier [Yu93], the telescopic amplifier [Sack90], gain-boosted techniques [Bult90] and other approaches, at the expense of power consumption.

Comparator design

Dynamic comparators should be used whenever possible because they do not rely on power consuming active elements.

Voltage supply reduction

For analog design, it is shown that a voltage supply reduction does not always lead to a power consumption reduction [Vitt94], [Pelu98] for several reasons:

- Threshold of MOS transistors.
- Loss of maximal amplitudes (SNR degradation).
- Limits of conduction in analog switches.
- Low speed of MOS transistors.
- Limited stack of transistors.

This is particularly the case for S-C circuits, where practical realisations of 10-bit S-C 1.5 bit/stage pipelined ADCs show that the optimum in power consumption is between 2 and 3 Volt (Figure 3-2). Below this value, the power consumption increases again.

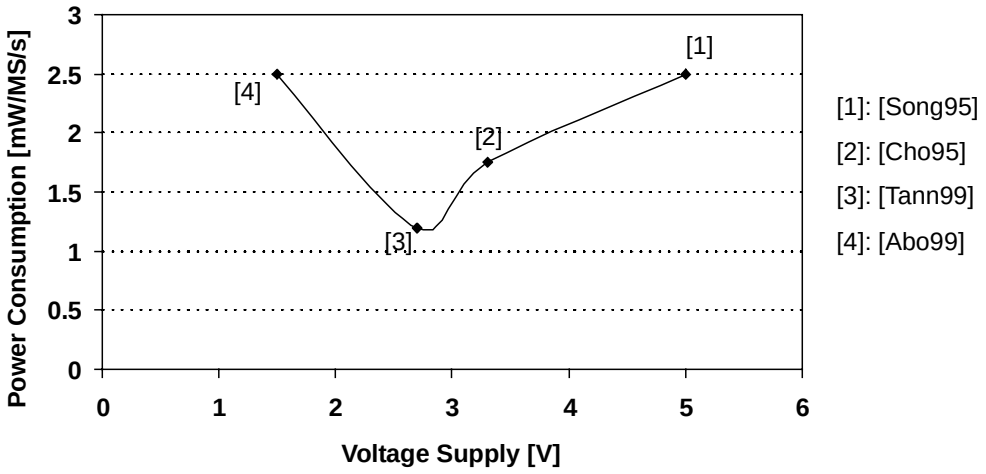


Figure 3-2: Power consumption of 10-bit S-C 1.5 bit/stage pipelined ADCs in function of the voltage supply.

3.2.3 Architectural and Algorithmic level optimisation

Usually, the most important gain in power consumption can be made at the architectural and algorithmic level [Chan92], [Raba94]. This is true for ADCs, both for analog and digital design.

Choice of the conversion principle

The determining parameter in a low-power ADC design is the conversion principle, involving both analog and digital parts. Among all the possible approaches, the designer must select the most appropriate solution in order to fulfil the specifications, such as:

- Supply voltage.
- Resolution.
- Sampling rate.
- Available area.
- Design complexity.
- Environment (Power supply or substrate noise, etc.).

Parallelism

In order to compensate the loss of speed due to reduced voltage, a certain level of parallelism (or pipelining) may be chosen, which can have an impact on the

conversion principle itself. The degree of parallelism is limited by economic reasons (die area), and, for analog blocks, by inter-channel matching problems (see Section 3.4 for more details).

Analog versus digital complexity

Depending on the conversion principle, the complexity of the A/D converter can be balanced between the analog and the digital part. For a low-power implementation, the analog complexity will usually tend to be minimised (reduced number of amplifiers, dynamic comparators, etc.) as far as the conversion principle allows it. Digital error compensation algorithms will usually be preferred to analog ones. Imperfections of analog components (mismatch, offset, etc.) must be solved at the system level. Nevertheless, in some cases (folding architectures for instance), an apparently complex analog processing block can dramatically reduce the overall power consumption [Vore97]. Therefore, analog solutions should not be discarded without a meticulous study of their impact on the whole ADC system.

Current-mode versus Voltage-mode

Switched-Capacitor (S-C) solutions are usually preferred to Switched-Current (S-C) because of their overall simplicity and efficiency [Vale93]. Yet, the current-mode approach is a viable alternative for low-power implementation, and can lead to remarkable results, if introduced and studied at the system level [Yots95], [Wang99].

3.3 Evaluation of different video ADC techniques

There are four main conversion principles used in video ADCs: full-flash, folding, two-step (subranging), and pipeline. Each of them has its advantages and drawbacks. This section presents an overview of those methods and highlights the most adapted for a low-power approach.

3.3.1 Full-flash A/D Converters

A simple way to make a high-speed A/D converter is to use a full-flash structure, consisting of a vector of 2^n -1 comparators with n being the number of bits (Figure 3-3 a). Each comparator is connected with one input to the input voltage and with the other input to a reference voltage, generally generated by a resistor ladder. The outputs of the comparators (thermometer code) are fed into encoding logic that generates the binary code. The advantage of the full-flash converter is its ease of design and its good high frequency behaviour. The

disadvantages are the required number of comparators, and for resolutions above 7 bit, the comparators and reference voltage accuracy.

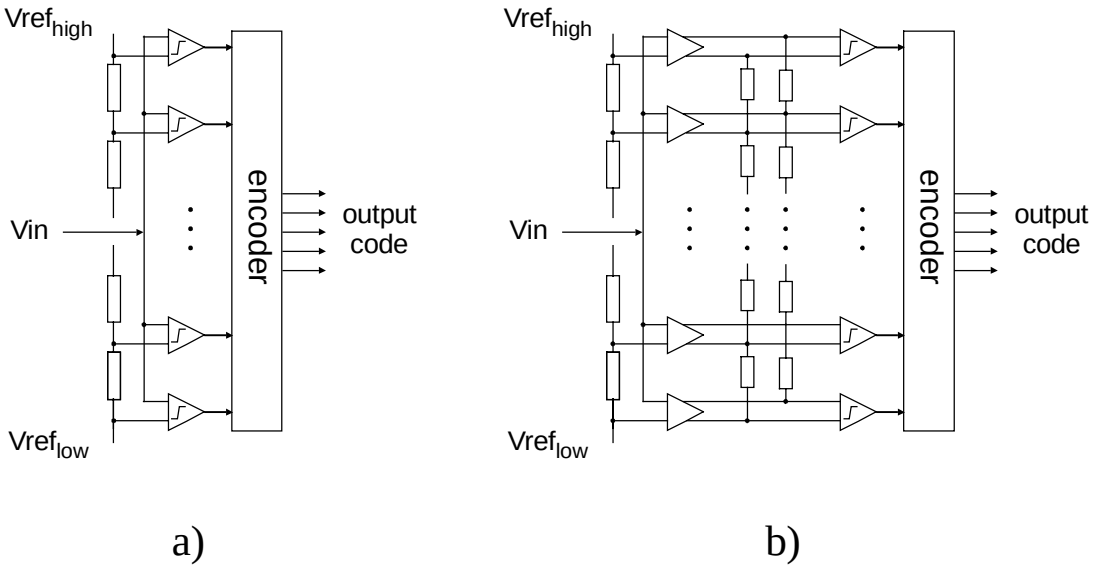


Figure 3-3: a) Full-flash ADC and b) Full-flash ADC with preamplifiers and averaging resistors.

For a given technology, speed and voltage supply, the consequence of an increased resolution by one bit on the power consumption can be approximated as follow: a decreased LSB value by a factor of two implies a doubled comparator gain in order to keep the same speed. Since the gain is proportional to g_m, which is proportional to i, the comparator power consumption is doubled. And, since the number of comparators is doubled, the overall power consumption is multiplied by four. This explains why, even at the eight bit level, full-flash ADCs have prohibitive area and power consumption [Pelg94], while at the six-bit level they are still attractive [Tsuk98], [Mehr99].

In order to relax comparator requirements (offset), special techniques have been developed, like distributed preamplifiers and averaging techniques [Katt91], [Bult97] (Figure 3-3 b).

3.3.2 Folding A/D Converters

The idea of the folding principle comes from the observation that, in full-flash ADCs, the comparators are used only in a small invariant input interval. The number of comparators could be reduced if they were each used more than once. An analog, non-linear block, called the folding circuit, is used to transform the continuous input range into a periodic signal with reduced amplitude, hence

reducing decision levels (Figure 3-4a). The same comparators can be then used for each period of the folded signal, leading to a reduced number of comparators [Naut95], by a factor equal to the number of folds - or periods. As it is not possible, after folding, to distinguish in which fold the signal is located, coarse comparators are necessary to form the MSBs of the digital code. For an 8-bit folding ADC, the required number of comparators is 8 (coarse) + 32 (fine) = 40 comparators.

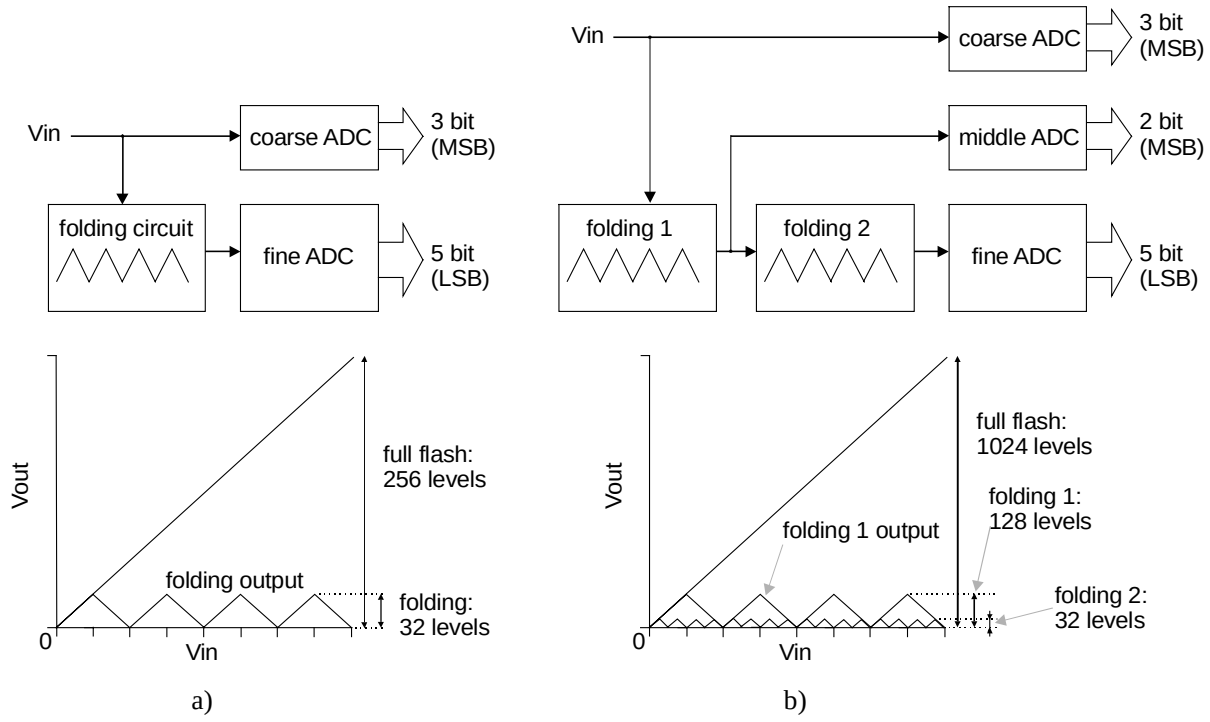


Figure 3-4: a) Single 8-bit folding and b) Cascaded 10-bit folding structures.

Disadvantages of the folding method are a difficult design of the folding block in terms of frequency response and linearity, and a fundamental limitation in resolution caused by the resistor ladder inaccuracy.

For resolutions higher than 8 bit, the simple folding approach is not sufficient for keeping comparator count low. A cascaded folding approach is then used, consisting of folding again each segment of the first folded signal (Figure 3-4b). Resolutions of 10-bit [Bult97] and even 12-bit [Vore97] have been reported while maintaining power consumption and comparator count low. For instance, [Vore97] reports a 12-bit cascaded folding ADC needing only 50 comparators, instead of 80 or 128 for a single folding approach, or 4096 for a full-flash implementation.

Unlike the full-flash approach, the folding ADC is a good candidate for low-power operation. However, the complex folding block design makes it difficult to implement.

3.3.3 Two-step A/D Converters

Another way to decrease the number of comparison levels of a full-flash ADC is to use the two-step architecture [Raza95]. In a first step, a coarse estimation (MSBs) of the analog input signal A is obtained (Figure 3-5a), and used to produce an analog signal B around the input level. Then, in a second step, the difference C between the previously produced signal B and the input signal A is used to determine the fine estimation (LSBs) of the input.

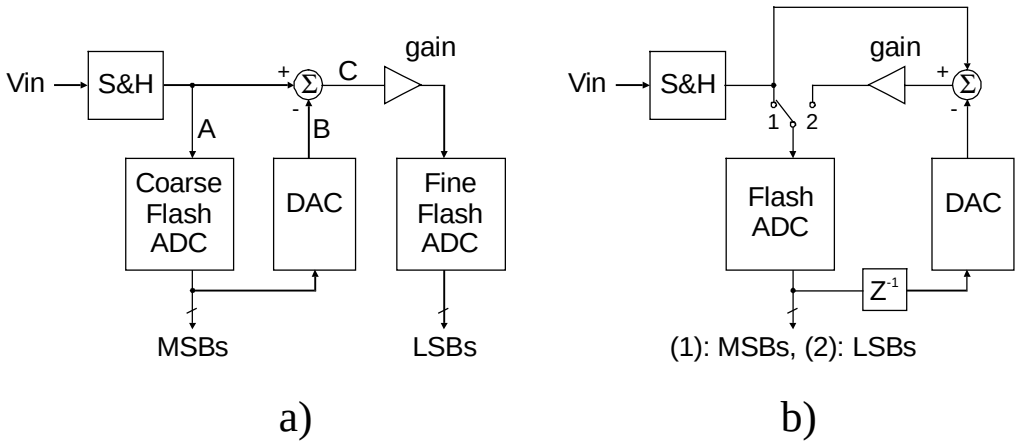


Figure 3-5: a) Two-step ADC and b) Two-step ADC in cyclic mode (two phases)

Usually, an amplification block is used to adapt the dynamic of signal C for the fine flash ADC, reducing the comparator resolution requirement [Raza92]. Thus, the signal C, after rescaling, can be passed again to the coarse flash ADC, so avoiding the use of a second flash bank, and leading to a cyclic mode two-step ADC [Song90] (Figure 3-5 b). Other techniques can also be used, like multi-step [Maye96], pipelining [Kusu93].

Another implementation, called the subranging ADC [Ding85], does not require an explicit subtraction. In this topology, the coarse stage identifies a reference voltage range around the input voltage. This reference range, made of two voltages, is passed to the fine stage and divided into a new set of references corresponding to the fine stage references. The drawbacks of this implementation are the required accuracy of the fine stage comparators of 1 LSB, and the slow interstage processing.

Some low-power implementations of the two-step approach show very good results, like the subranging capacitive interpolation [Kusu93], or the mixed-mode approach [Yots95], combining a voltage-mode coarse stage and a current-mode fine stage.

The resolution of the two-stage ADC is usually limited by matching problems (ladder resistor) to 10 bit, although careful design achieved higher resolution [Raza92]. Its potential for a low-power implementation is high.

3.3.4 Pipelined A/D Converters

The concept of pipelining, often used in digital circuits, can also be applied in the analog domain to achieve higher speed where several operations must be performed serially. This is the case in ADCs, where the conversion can be performed in a sequential manner from the most to the least significant bit. In a pipeline, all the stages are processing different samples concurrently, and the throughput rate depends only on the speed of each stage. Moreover, each stage can be optimised for its specific resolution (scaling), giving usually a better overall result than a cyclic implementation.

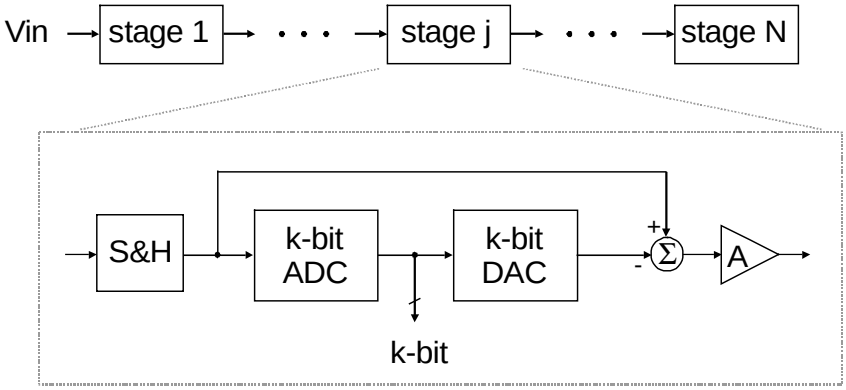


Figure 3-6: General pipelined ADC architecture

A pipelined N-stage ADC is represented in Figure 3-6. Each stage has its own sample and hold unit, and resolves a given number of bit - for instance, stage *j* resolves *k* bits. In a stage, the difference between the input voltage and its quantified value is amplified with a gain *A* to give the residue voltage, used in the following stages. Usually, $A = 2^k$. This allows the residue voltage to match the input dynamic of the following stage.

The number of bits resolved in each stage and hence the number of stages of a pipelined ADC depends on various considerations such as overall resolution and speed. Multi-bit per stage structures are usually more difficult to implement and slower than single-bit ones. This is why the 1-bit and 1.5 bit per stage structures are the most popular implementations [Cho95], [Song95], [Yu96].

Another important advantage of a pipelined architecture is that, in principle, area and power consumption grow linearly with the number of bits. In practice,

however, the first stages are more power-consuming due to their accuracy requirements.

Finally, pipelined ADCs are also usually limited to 10-bit of resolution, due to matching problems, but they are the easiest video ADCs to calibrate, this for two reasons: 1/ No supplementary hardware is required and 2/ The required number of correction coefficients is small. Resolutions of 12 bit [Oris98] and even 15 bit [Kwak97] ADCs operating at video-rates have been reported.

The pipelined ADCs, and particularly their switched-capacitor implementation, are simple to design, low-power and easy to upgrade to higher resolution. Their main limitation is speed, limited by the OTA performances.

3.3.5 Summary of the main video ADC techniques

A selection of the most power efficient ADC realisations found in the literature is displayed in the following figures. Two figures of merit are taken into account: the first, displayed on the x-axis, is the energy per sample, expressed in mW per MHz. The second is the speed per area ratio, expressed in MHz per square millimetre, and displayed on the y-axis. The comparison is made for the three resolutions of 8, 10 and 12 bit.

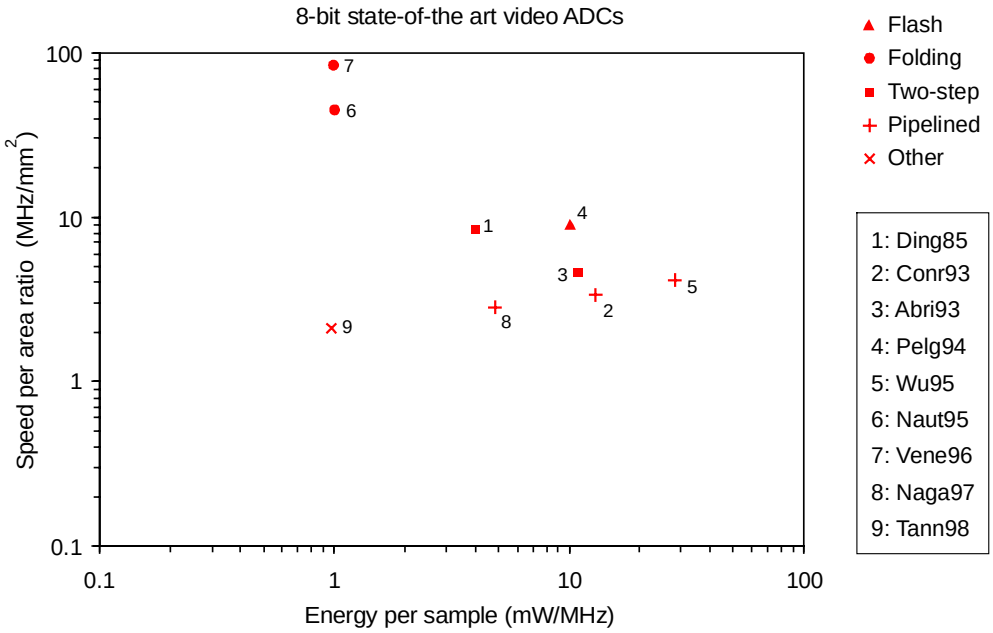


Figure 3-7: 8-bit state-of-the-art video ADCs.

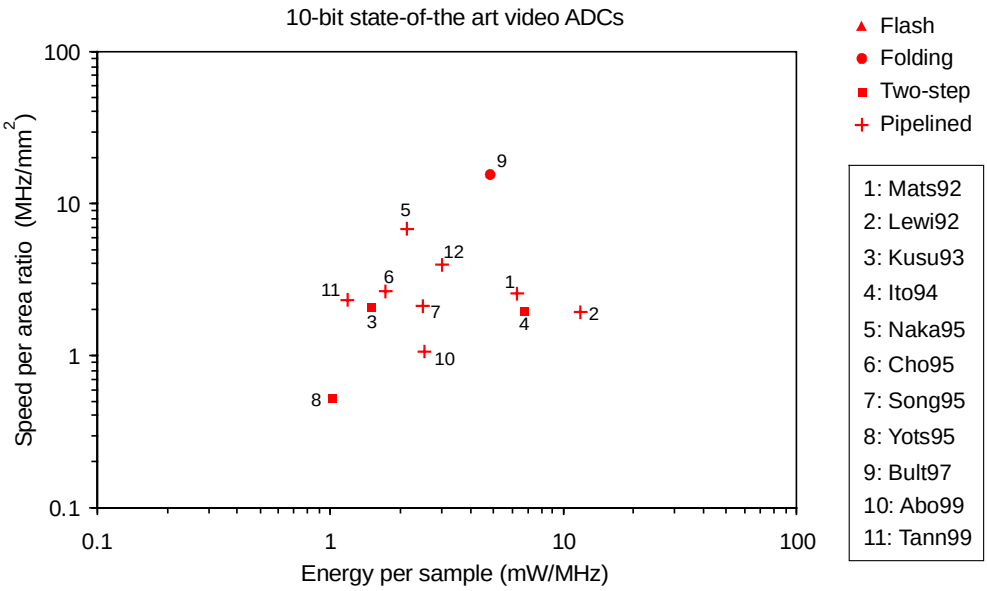


Figure 3-8: 10-bit state-of-the-art video ADCs.

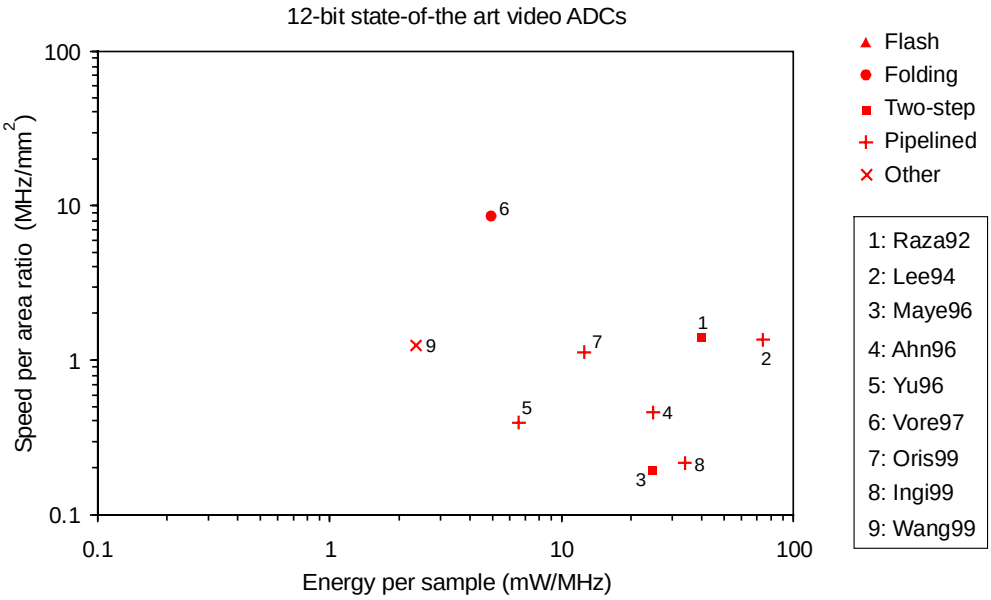


Figure 3-9: 12-bit state-of-the-art video ADCs.

From those experimental results, the following conclusions can be drawn:

- The most compact solution is the folding ADC.
- In terms of power consumption, the best implementations are optimised combinations of several approaches.
- The pipelined ADC is well represented in all the resolutions.

3.4 ADC parallel processing

3.4.1 Principle

Parallelism can be advantageously used in ADCs in order to increase the conversion rate [Con93], [Bla80]. The input signal is first distributed on each unit (time de-multiplexing), and then recombined at the output (time multiplexing) in order to reconstruct the digitised input signal.

In the field of AD conversion for image sensors, the output sensor signal is by nature multi-dimensional. A time-domain de-multiplexing function is then unnecessary, and one can take full advantage of the inherently parallel structure of image sensors by using an array of slower but power optimised ADCs, as represented in Figure 3-10 b).

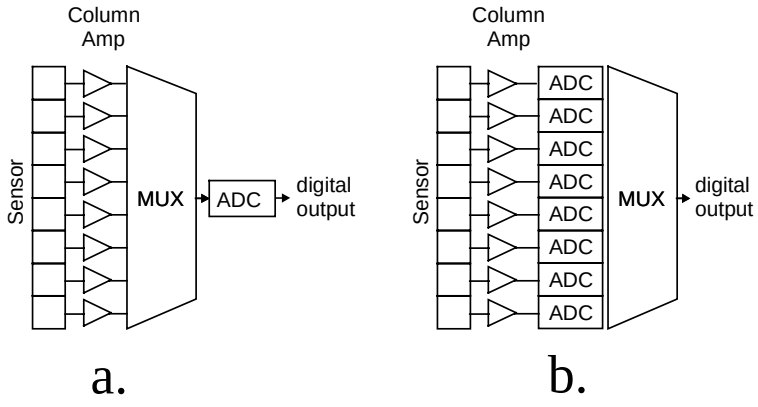


Figure 3-10: a) Single and b) Multiple ADC configuration for image sensors.

The advantages of this approach over the usual single ADC solution are:

- Using several devices working in parallel can alleviate the intrinsic speed limitation of a given ADC technique.
- Existing ADC principles designed for slower applications (audio, etc.) can be reused for fast acquisition.
- The AD conversion speed can be easily adjusted by changing the number of ADC cells used.
- A slower ADC clock rate may result in saving power, even with a high number of converters.

The way to implement an array of AD converters will strongly depend on the type of converter used. Limitations in area, resolution, conversion speed and power consumption will decide which architecture fits the best a given conversion.

3.4.2 Limitations in resolution

However, one is then faced with potential matching difficulties: any offset, gain, or timing mismatch *between* the multiple ADC channels results in fixed-pattern effects reducing the overall absolute resolution of the conversion. This topic has been widely discussed, and we can find numerous analyses of mismatch effects on ADC arrays [Bla80], [Jenq88], [Petr91]. The main characteristics of those studies are summarised below:

Cell resolution and array overall resolution

The ADC cell resolution is limited both by quantified error and limited linearity. The average error power between the best fit line $ax + b$ and the real transfer function of the ADC can be expressed as in [Bla80]:

$$E_p = \left\langle \delta^2 \right\rangle, \quad \text{with} \quad \delta(x) = \hat{x} - (ax + b) \qquad \text{Equ. 3-11}$$

in which $\hat{x}$ is the quantified level of x, and a and b are error minimisation terms corresponding to the best fit converter gain and offset. If several converters are used in an array, each ith converter will have its best-fit line with the corresponding a_i and b_i parameters. The ideal case would be that all the a_i and b_i parameters would be equal respectively. Let us assume that in reality they are Gaussian random variables and identically distributed with variances σ_a^2 and σ_b^2. The variance of parameters a_i is the gain error, and will degrade the overall resolution, as well as the variance of parameters b_i, giving the offset error.

Gain mismatch error

The gain mismatch error gives a noise source proportional to the amplitude of the input signal. According to [Bla80], the equivalent error power for a sinusoidal input is given by:

$$Ep_G = \frac{Vpp^2}{8} \cdot \sigma_a^2 \qquad \text{Equ. 3-12}$$

where *Vpp* is the peak-to-peak amplitude of the input signal. The corresponding SNR is given in [Petr91] (Equ. 3-13). It should be noted that since the SNR is

proportional to the power of the input signal, the resulting expression depends only on the gain variance σ_a^2.

$$SNR = -10\log_{10}\left(\sigma_a^2\right) \qquad \text{Equ. 3-13}$$

Offset mismatch error

The offset mismatch error gives a noise source that does not depend on the amplitude of the signal. Its equivalent sinusoid error power is given by:

$$Ep_O = \sigma_b^2 \qquad \text{Equ. 3-14}$$

The corresponding SNR contains this time the sinusoid amplitude *Vpp*:

$$SNR = -10\log_{10}\left(\frac{\sigma_b^2}{2 \cdot Vpp^2}\right) \qquad \text{Equ. 3-15}$$

Phase skew and jitter error

Any time mismatch between channels (= clock skew: propagation mismatches) or within a channel (= clock jitter: phase noise) will give an additional error. For instance, if the Sample & Hold phases of each ADC are slightly different, the analog sampled voltage will also be different, leading to a degradation of the overall inter-channel SNR. For a sinus input, the error power due to timing mismatches is given by:

$$Ep_T = \frac{Vpp^2}{8} \cdot \omega^2 \cdot \sigma_t^2 \qquad \text{Equ. 3-16}$$

where ω is the pulsation of the input sinusoid, and σ_t^2 is the time variance of the clock cycle. The corresponding SNR is given by:

$$SNR = -10\log_{10}\left(\omega^2 \cdot \sigma_t^2\right) \qquad \text{Equ. 3-17}$$

The error associated with time mismatch is in general dominant in ADC arrays, as long as the input signal is continuously changing during the sampling phase. For CMOS image sensors, however, the pixel itself acts as a Sample and Hold circuit and thus provides a stable signal during ADC sampling phase. The error due to phase skew and jitter can then generally be neglected in this case.

3.5 Parallel-serial ADC

3.5.1 The basic cell: RSD cyclic (serial) ADC

The first approach followed in the development of parallel ADCs is to select an ADC with the smallest die area and lowest power consumption possible. Among all the techniques used in AD conversion, the cyclic converter offers the advantage of a very small die size. Furthermore, the RSD cyclic ADC developed and patented by IMT [Heu96] features very low power consumption with a reasonable conversion speed. The experience acquired at IMT on the development of such ADCs [Gris95], [Heu96], [Gris97] has thus been a decisive reason to choose this type of converter for the parallel-serial ADC.

3.5.2 Principle of the RSD cyclic converter

The Redundant Signed Digit (RSD) converter, whose algorithm is given in Figure 3-11, was first published in [Gin88], and is nowadays commonly used.

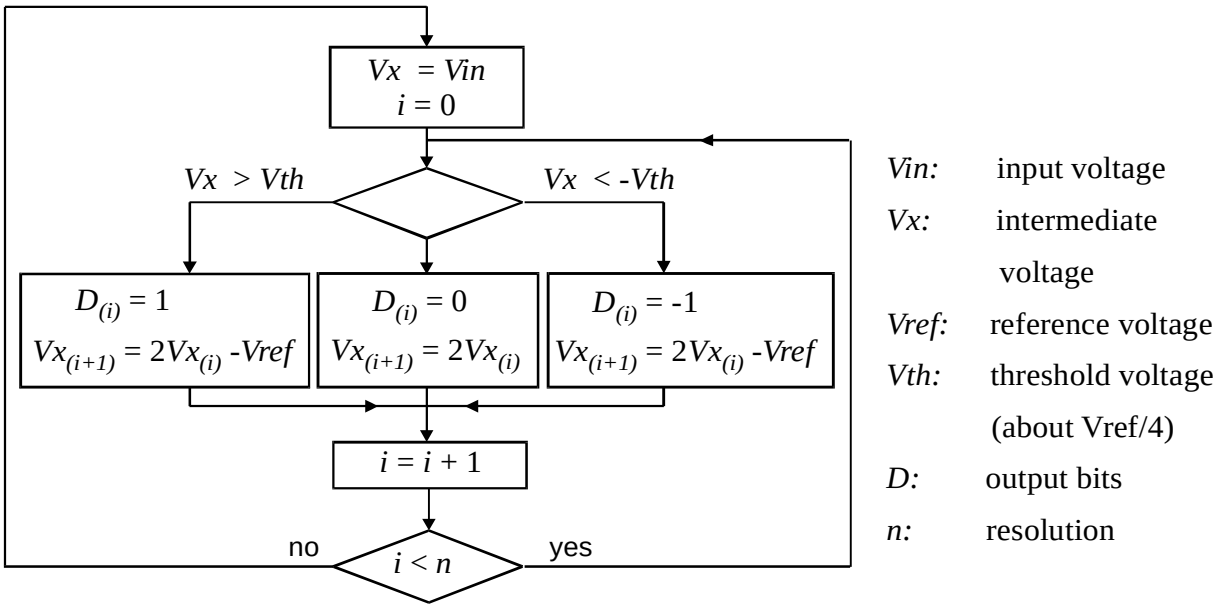


Figure 3-11: Cyclic RSD converter algorithm.

The advantages of the RSD algorithm over a conventional cyclic algorithm are fully described in [Gin88] and [Gin92] and are mainly:

- Tolerant to comparator offset (up to ± *Vref* /4).
- Tolerant to loop offset error: active element offset and switch charge injection gives only a digital offset and does not contribute to DNL or INL.

- A fully digital correction is possible due to guaranteed non-missing decision levels.
- Active element saturation causes digital saturation (no distortion for low-level input signals).

The accuracy limitations of the RSD conversion depend on the way it is implemented, but mainly they are due to:

- Mismatch of the elements for multiplication by 2 and subtraction of *Vref*.
- Op Amp finite gain and settling time.
- Noise.
- Charge injection.

3.5.3 Implementation

The operations of the algorithm are performed with three identical switched capacitors. The related schematic is shown in Figure 3-12. The converter can be implemented with a single OTA (Operational Transconductance Amplifier), and only one reference voltage is needed. The architecture is single-ended (non-differential) in order to minimise the number of components and logic.

In this scheme, *Cr* and switches 7 and 8 are involved in reference voltage addition or subtraction while *C1* and *C2* are used for the doubling. Four different phases (I to IV) can be distinguished:

- Phase I: Sample and reset. *C2* is connected to *Vin* while the other two capacitors are reset.
- Phase II: Initialisation. The load on *C2* is transferred to *C1* and $Vx = Vin$.
- Phase III: Copy. At the falling edge of signal 3, the comparison occur and gives the cycle result *D* (signals *pos* and *neg*). *Vx* is copied into *C2* through switch 2, and *Cr* is charged or not depending on the comparison result.
- Phase IV: Update. Switches 7 and 8 are inverted, and the load of *C2* is transferred on *C1*. The resulting voltage *Vx* on *C1* is thus $2 \cdot Vin$, $2 \cdot Vin + Vref$ or $2 \cdot Vin - Vref$ depending on the values of *pos* and *neg*.

Phases III and IV are repeated until the LSB is known. Including the acquisition phase, *n*-1 cycles are needed for an *n* bit result.

The result *D* of the comparison (signals *pos* and *neg*) can take three values:

- $D = 10$ ($pos = 1$, $neg = 0$) if $Vx > Vth$.
- $D = 00$ ($pos = 0$, $neg = 0$) if $Vth >= Vx >= -Vth$.
- $D = 01$ ($pos = 0$, $neg = 1$) if $Vx < -Vth$.

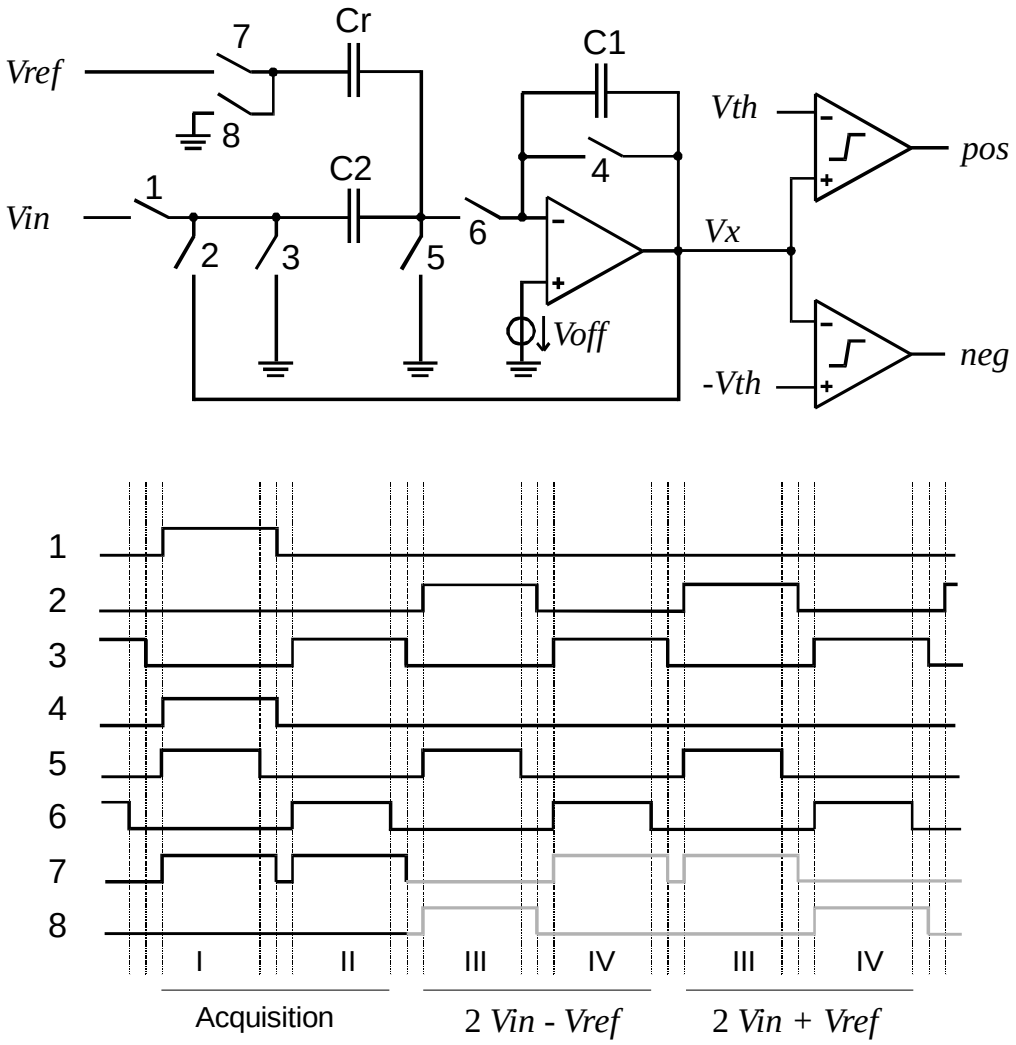


Figure 3-12: Schematic of the cyclic RSD ADC and switches timing diagram.

It is important to ensure that the charge injection generated by the switching activity does not depend on the input voltage (it must be a constant value to generate only offset). This is the case for the following reasons:

- Switches 5 and 6 always open before 2 and 3 respectively, which ensures that the charges injected by switches 2 and 3 will not add to the load of *C2* since it has a floating plate.
- The voltage of the node common to capacitors *C2* and *Cr* is always equal to ground, which means that the charge injected by switches 5 and 6 is constant, and independent of *Vin*. Furthermore, by choosing switches 5 and 6 of equal dimension, the charge injected by the opening of switch 5 can be compensated when switch 6 closes.

3.5.4 Limitations in resolution

As explained in [Gin92], the limitations in the conversion accuracy are mainly due to capacitor mismatch between *C1*, *C2* and *Cr*, and to the limited gain of the OTA. Those two elements act on the doubling factor and on the reference subtraction or addition.

Considering the schematic of Figure 3-12, and if:

- *a* = OTA gain
- *Voff* = OTA offset
- *Cp* = parasitic capacitance between ground and the common node of *C2* and *Cr*.
- *Qinj* = sum of all the charges injected during one cycle.

At the end of the first cycle (phases I and II), the output voltage *Vx* is (see appendix A for a detailed mathematical development):

$$Vx_1 = \left(\frac{a}{a+3+Cp/C1} \right) \cdot \left[Vin \cdot \left(\frac{C2}{C1} \right) + \left(\frac{Qinj}{C1} \right) \right] + 3 \cdot Voff \qquad \text{Equ. 3-18}$$

This first conversion cycle (i = 1) adds a gain and an offset error to the input voltage *Vin*. The corresponding charge in *C1* is:

$$Q1_1 = C1 \cdot \left[\left(\frac{1+a}{a} \cdot Vx_1 \right) - Voff \right] \qquad \text{Equ. 3-19}$$

The next conversion cycles (i > 1, with phases III and IV repeated) show the following transfer function:

$$Vx_i = \left(\frac{a}{a+3+Cp/C1} \right) \cdot \left[Vx_{i-1} \cdot \left(\frac{C2}{C1} + \frac{a+1}{a} \right) + D_{i-1} \cdot Vref \cdot \frac{Cr}{C1} \right] + \qquad \text{Equ. 3-20}$$

$$2 \cdot Voff + Vinj$$

Where *Vinj* is the constant voltage related to *Qinj*, and $D_{i\text{-}1}$ is the comparison result of the previous cycle (-1, 0, 1).

The ideal gain of 2 is degraded by a factor ε because of the finite OTA gain and of the mismatch between *C1* and *C2* :

$$2+\varepsilon = \left(\frac{a}{a+3+Cp/C1} \right) \cdot \left(\frac{C2}{C1} + \frac{a+1}{a} \right) \qquad \text{Equ. 3-21}$$

The ideal reference subtraction of factor 1 is degraded by a factor β because of the finite OTA gain and mismatch between *Cr* and *C1*:

$$1+\beta = \left(\frac{a}{a+3+Cp/C1} \right) \cdot \left(\frac{Cr}{C1} \right) \qquad \text{Equ. 3-22}$$

The two relations Equ. 3-18 and Equ. 3-20 can be written again as follow:

$$Vx_1 = (1+\delta) \cdot Vin + Voff1 \qquad i = 1 \qquad \text{Equ. 3-23}$$

$$Vx_i = (2+\varepsilon) \cdot Vx_{i-1} + D_{i-1} \cdot (1+\beta) \cdot Vref + Voff2 \qquad i > 1 \qquad \text{Equ. 3-24}$$

Where δ is the gain error of the acquisition cycle, ε is the doubling error, β is the reference subtraction error and *Voff1, Voff2* are the offset voltages of the first and following cycles respectively.

Differential non linearity (DNL)

The DNL (see sub-section 3.1.2) will be maximal for the maximum of changes between two consecutive digital codes. With the present RSD converter, the critical codes are [1,-1,0,0,....,0] and [0,1,0,0,...,-1]. Their corresponding residue values are, for the same input voltage Vx_1 [Gin92] and after *n* conversion cycles:

[1,-1,0,0,....,0]:

$$Vxa_n = (2+\varepsilon)^{n-1} \cdot Vx_1 - (2+\varepsilon)^{n-2} \cdot (1+\beta) \cdot Vref + (2+\varepsilon)^{n-3} \cdot (1+\beta) \cdot Vref \qquad \text{Equ. 3-25}$$

[0,1,0,0,...,-1:

$$Vxb_n = (2+\varepsilon)^{n-1} \cdot Vx_1 - (2+\varepsilon)^{n-3} \cdot (1+\beta) \cdot Vref + (1+\beta) \cdot Vref \qquad \text{Equ. 3-26}$$

The difference is:

$$Vxb_n - Vxa_n = (1+\beta)\cdot Vref \cdot \left(\varepsilon(2+\varepsilon)^{n-3}+1\right) \qquad \text{Equ. 3-27}$$

This residue has to be divided by $(2+\varepsilon)^{n-1}$ to be reported to the input voltage, and multiplied to 2^{n-1} to give a result in LSB units. The corresponding maximum DNL is then:

$$MaxDNL \cong \varepsilon \cdot 2^{n-3} \quad [\text{LSB}] \qquad \text{Equ. 3-28}$$

The worst case is for ε maximum. Standard CMOS processes have typically a maximum capacitor mismatch ratio of 0.4%, and a minimum gain for a two-stage OTA can be estimated to about 2000 (66 dB). The parasitic plate capacitor can be estimated to be 20% of the C1 value. This gives a maximum factor ε_{max} of:

$$\varepsilon_{\max} = \left(\frac{a}{a+3+Cp/C1}\right)\cdot\left(\frac{C2}{C1}+\frac{a+1}{a}\right)-2 \qquad \text{Equ. 3-29}$$

ε_{max} = *-6.6 e-3* $\rightarrow$ $MaxDNL \cong -0.21$

A MATLAB simulation shows in Figure 3-13 the DNL of such a converter, the target being 8 bit of resolution:

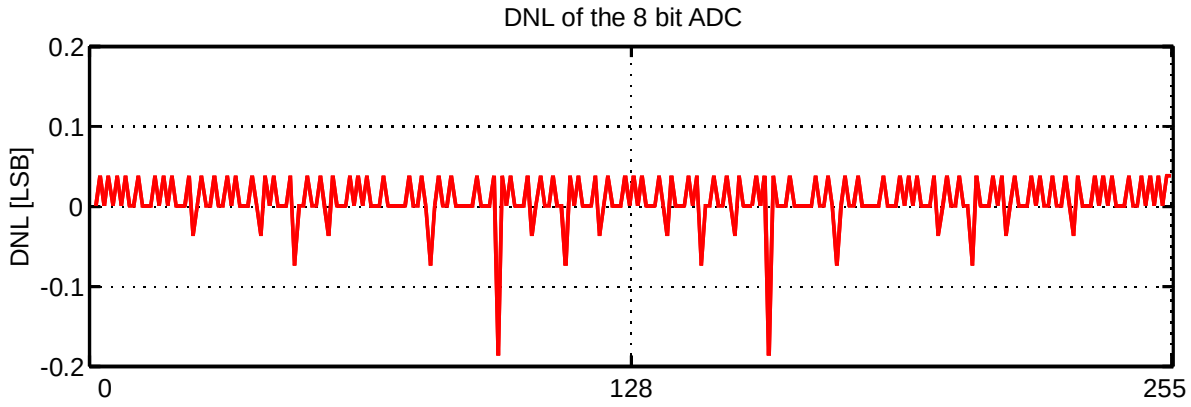


Figure 3-13: DNL of a RSD 8-bit cyclic converter with maximum gain error.

Integral non linearity (INL)

The INL obtained with our 8 bit RSD cyclic converter will be maximal if the mismatches and finite OTA gain have cumulating effects. Figure 3-14 shows an example of INL with the same conditions than in Figure 3-13:

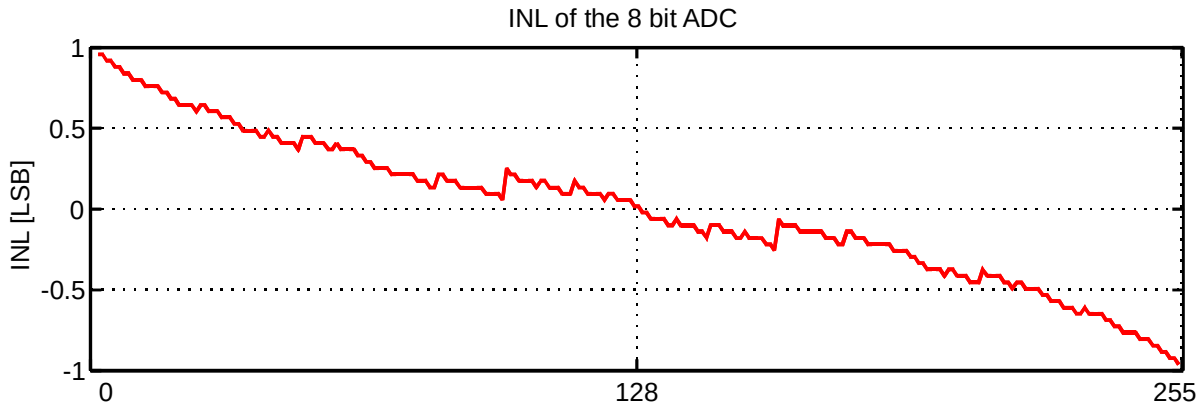


Figure 3-14: INL of a RSD 8-bit cyclic converter with maximum gain error.

The INL graph shows the gain error of the converter. This error is mainly due to the factor δ of the first cycle. It could be possible to suppress this first cycle by changing the scheme and timing of the converter.

Effect of OTA offset

The following simulation in Figure 3-15 shows the effect of an OTA offset of 3 mV on the error function. We see that this offset only contributes to a digital offset, and does not degrade the linearity.

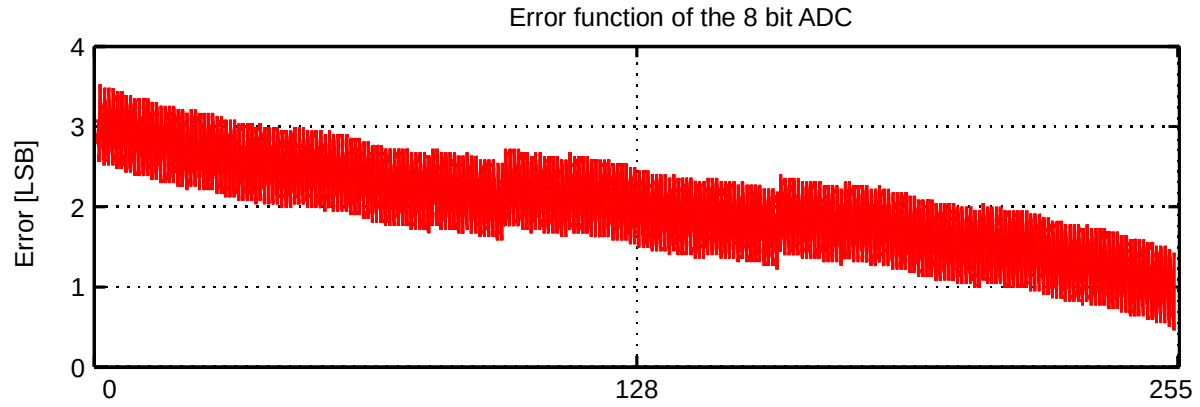


Figure 3-15: Effect of an OTA offset of 3 mV on the error function.

3.6 Parallel-serial realisation and performance

A parallel-serial ADC was designed by implementing an array of 32 RSD cyclic AD converters working in parallel. This section describes the realisation of the ADC cell, the array, and the test results.

3.6.1 Cyclic RSD ADC cell

The specifications for the ADC basic cell are listed in Table 3-3:

Resolution	8 bit
Sampling rate	> 100 kHz
Power consumption @ Vdd = 3 Volt	< 1 nJ/Sample
Operating voltage	2.6 – 3.2 Volt
Geometric pitch	4 sensor columns
Die area (technology: 1 μm)	< 0.1 mm2

Table 3-3: ADC basic cell specification.

Capacitor size

In order to minimise power consumption and area, C1, C2 and Cr (see Figure 3-12) have to be as small as possible. However, their size cannot be scaled down to the KTC noise limit (less than 0.1 pF) due to the matching: the bigger the capacitors are, the better the matching is. A compromise has been found with capacitors of 1 pF.

OTA design

The OTA chosen for that application is a classic 2 stage single ended Miller operational transconductance amplifier, well suited for low power and low voltage applications. The schematic of this amplifier is shown in Figure 3-16. The current ratio between stages 1 and 2 has been chosen to 1:2.5, to ensure a sufficient slew-rate for the second stage. M10 is used as a switch. When the signal “St” is high, the OTA is operating in its normal mode. When “St” is low, no current can flow through M5, and thus the Miller capacitor does not discharge. The ADC requirements given in Table 3-3, as well as simulation results given in Figure 3-13 and Figure 3-14 lead to the following OTA specifications:

- Settling time: < 450 ns for a residual oscillation of 4 mVpp, corresponding to half a LSB for an input dynamic of 2 Vpp.

- GBW: 3 MHz
- Phase margin: > 65 °
- DC gain: > 65 dB (to minimise DNL)

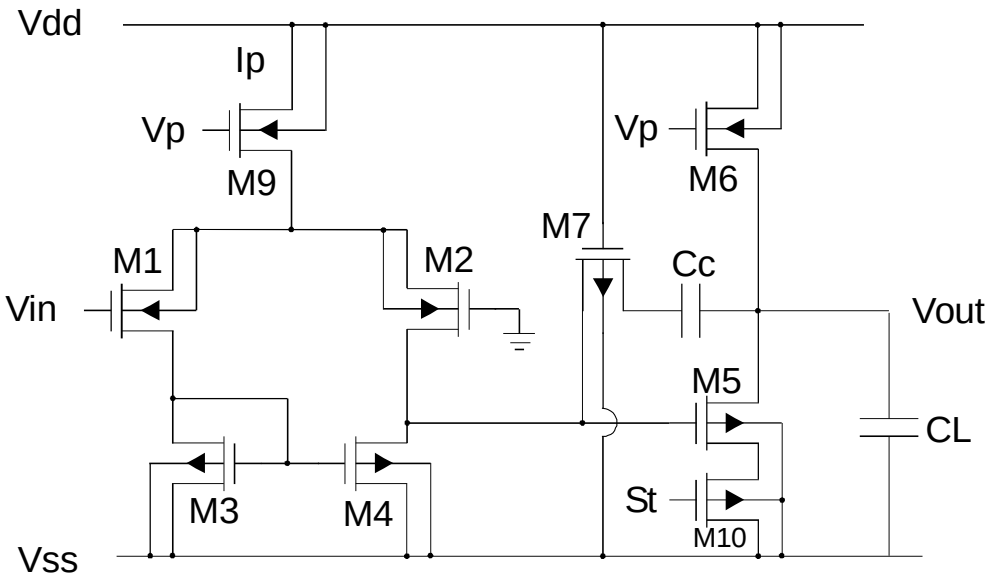


Figure 3-16: Miller OTA schematic diagram.

First SPICE simulations have shown that a current *Ip* of 9 µA is sufficient to reach the required specifications. The corresponding transistor dimensions are given in Table 3-4:

Transistor	Type	W [µm]	L [µm]	I [µA]	Operation
M1, M2	P	260	1	4.5	W. I.
M3, M4	N	5	5	4.5	S. I.
M5	N	10	2	22.5	S. I.
M6	P	9	2	22.5	S. I.
M7	N	3	8	-	S. I.
M9	P	9	5	9	S. I.
M10	N	10	1	22.5	S. I.
Cc = 0.34 pF	W. I. = weak inversion			S. I. = strong inversion	

Table 3-4: Transistor dimensions of the Miller OTA.

A fine level SPICE simulation of the OTA layout has given the following performances:

DC gain	82 dB
Gain Bandwidth	11 MHz
Phase margin	60°
Slew-rate pos	15 e6 V/s
Slew-rate neg	15 e6 V/s
Settling time (0.2%)	380 ns
Power dissipation (@ ± 1.5 V)	95 µW

Table 3-5: OTA performance (simulated).

The poor phase margin corresponds to peaking on the time domain, but residual oscillation remain under ½ LSB after the required settling time.

Comparators

Since the comparators do not have to be very accurate, they can be realised using simple strobed cross-coupled inverters, shown in Figure 3-17. Furthermore, in order to avoid the generation of the two reference voltages (*Vth* and -*Vth*), a capacitor Cth is added, producing the desired offset. This capacitor must be about ¼ of the load capacitors C1, in order to produce a threshold voltage of about *Vref* /4.

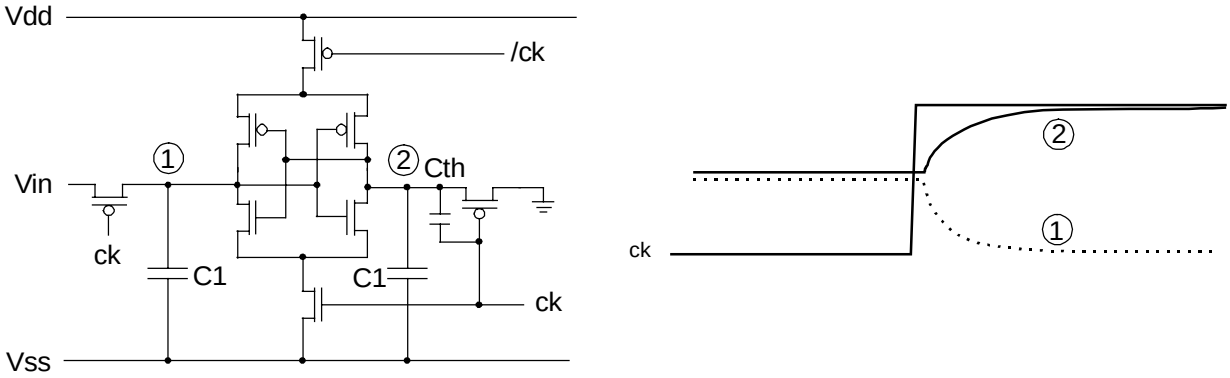


Figure 3-17: Left : comparator, schematic diagram. Right : evolution in function of time of the voltage of nodes 1 and 2 with a clock rising edge.

The outputs of the comparators (nodes 1 and 2) are sampled by a tri-state inverter in order to be dynamically memorised during a whole clock cycle.

RSD to 2's complement conversion

The raw serial output of the RSD converter is made of ternary signals coded on two bits (signals *pos* and *neg*, see Figure 3-12). This redundant format has to be converted into 2's complement format. This operation can be realised using an eighth bit shift register and half adders, as explained in [Gin92]. The shift register is realised with dynamic latches. Figure 3-18 shows the schematic of this circuitry, the output being a parallel signal *b* of *n* bits.

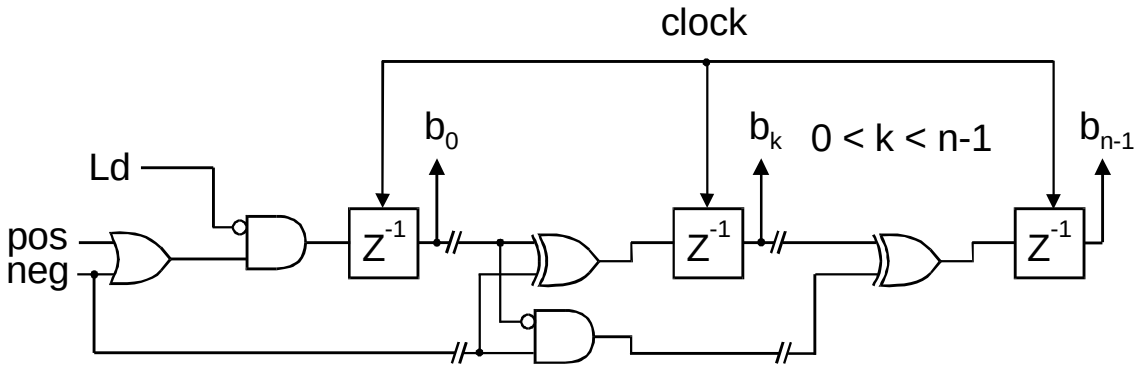


Figure 3-18: RSD to two's complement conversion logic.

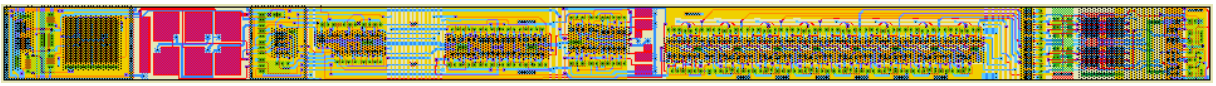
At the first cycle of the acquisition, signal Ld has to be set to one in order to initialise correctly the shift register.

Layout considerations

The basic cell must have a pitch as small as possible to enable it to be used in a matrix of converters, as explained in chapter 1. A width of 60 µm has been chosen for two reasons: 1) it is wide enough to offer sufficient space for two square centro- symmetrical capacitors of 1 pF each, and 2) the actual pixel pitch of CMOS image sensors for 1 µm technology, is about 15 µm: four pixel columns could be converted with one RSD AD converter.

Since this matrix converter is likely to be integrated on the same chip than CMOS image sensors, it will be directly exposed to light. The generated charges could then be collected by the converters, which would degrade the conversion accuracy. This is why special care has been taken to protect the ADC from light by using the metal2 layer as a light mask whenever possible.

The basic cell looks like a thin stick, with the analogue input at the left end and the digital output lines at the right end (Figure 3-19). The pitch is 60 µm, while the length is 908 µm. From left to right, we have: the OTA, the capacitors, the switches, the clock generation logic with control lines, the comparators with their capacitors, the RSD to 2's complement converter, the output buffers (3 state) with the eight output digital lines, and the logic of the output digital multiplexer, consisting of a shift register.



OTA	capacitors & switches	logic for clock generation	compa-rators	RSD to 2's compl. conversion logic	output buffer & shift reg

Figure 3-19: layout of the basic cell (top) and floor-plan (bottom).

3.6.2 Array architecture

Structural and operational organisation

The interconnection between the image sensor and the ADC array is supported by an *M* lines-wide analog bus, so as to take full advantage of the inherently parallel structure of image sensors, while disposing of a certain flexibility in the organisation of the ADC array. The pitch of the ADC cell can this way be fixed independently of the pixel pitch of the image sensor.

Clearly, during each operational clock period of the ADC array, *M* pixel signals are conveyed to a bank of *M* converters for simultaneous signal sampling. From the *n* clock periods needed by the RSD converters to perform an *n*-bit conversion, only the first one devoted to signal sampling requires a connection to the analog bus. The remaining *(n-1)* periods are then processed internally, so that the analog bus can be released to let other converter banks perform signal acquisitions. Globally, the ADC array is thus organised as a time-interleaved parallel ADC structure, composed of *n* banks of *M* converters each.

Figure 3-20 shows the architecture retained for the designed prototype circuit, with $n = 8$ and $M = 4$, resulting in a total of 32 converters. The *n* ADC banks are steered by selection lines controlling the sampling phase occurring at the beginning of the conversion cycles (cf Figure 3-20). The corresponding timing diagram is given in Figure 3-21. The ADC array is connected to an experimental 128 x 8 pixel CMOS image sensor implemented on the same chip.

The proposed architecture offers a high level of flexibility, the parameter *M* providing an easy way for adjusting the overall sampling rate. Moreover, the constituent ADCs operate at an *M* times lower clock rate, which is beneficial for low-power design.

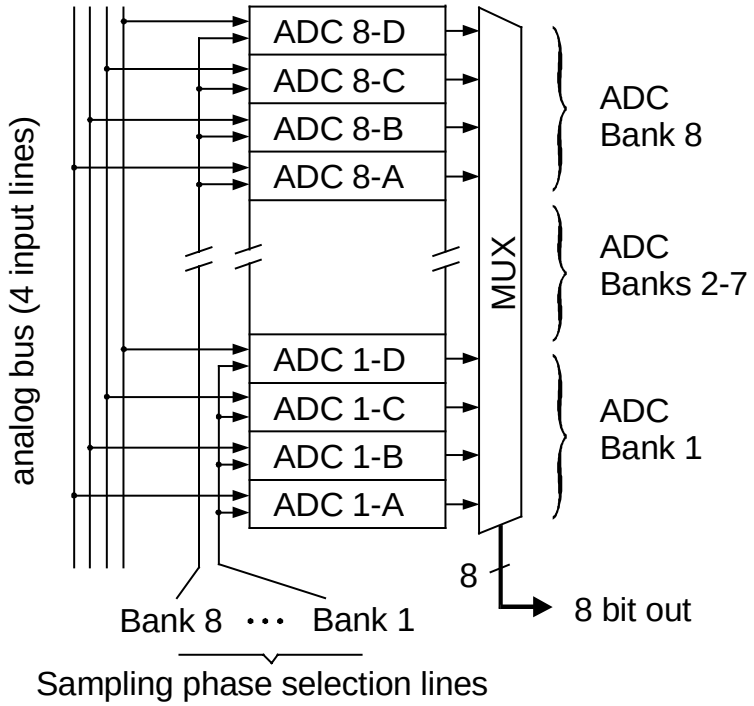


Figure 3-20: ADC array architecture.

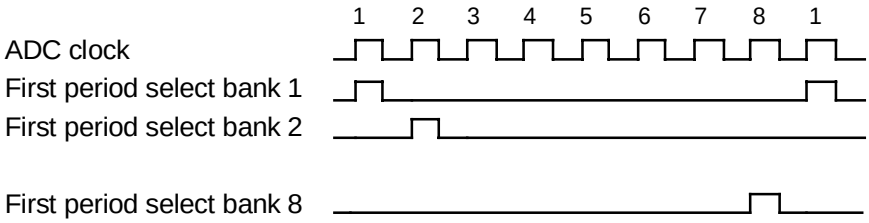


Figure 3-21: Timing diagram of the select lines.

Input and output data multiplexing scheme

As shown in Figure 3-22, the column lines of the sensor are grouped into sets of four signals, which are successively connected to the analog bus under the control of an input addressing shift register (SR). Similary, the 8-bit parallel output data produced by the ADCs are read out through a time-multiplexed digital bus, controlled by an output addressing SR. Whereas the input SR is

operating at the same rate than the ADC cells (cf *ADCclock* signal), the output SR is running four times faster (cf *OUTclock* signal) to keep track of the information flow. Figure 3-23 shows the timing diagram of the output multiplexing.

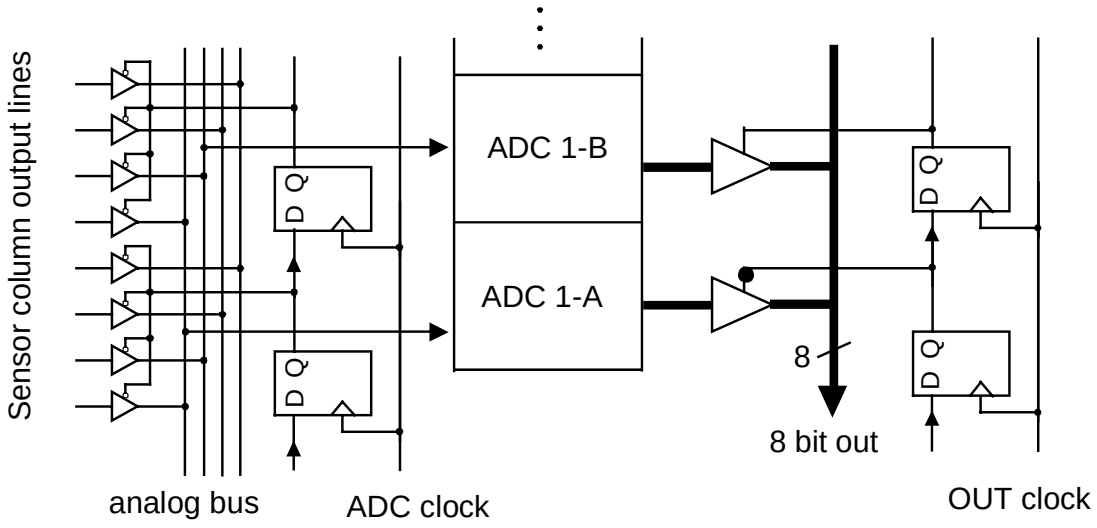


Figure 3-22: Input and output multiplexing.

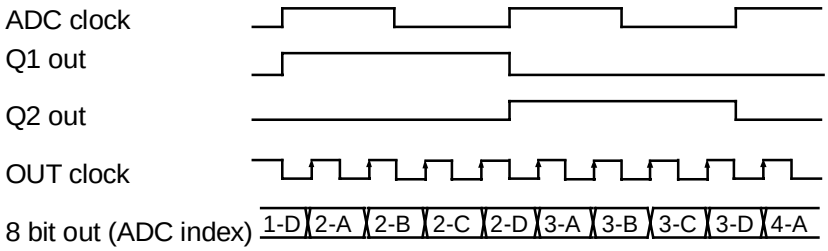


Figure 3-23: Input and output timing diagram.

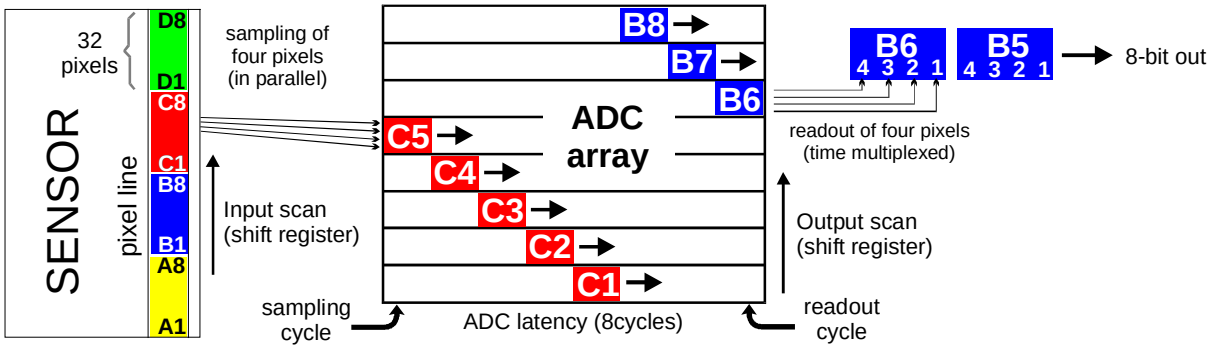


Figure 3-24: ADC array operation.

In order to illustrate the overall operation of the ADC array, Figure 3-24 shows the scanning of an image sensor line by the ADC array. The line is represented on the left of the figure, in the vertical direction, and consists of successive blocks of 32 pixels each, denoted A1..A8, B1..B8, etc. At each clock cycle of the "ADC clock" signal (see Figure 3-23), the ADC array is sampling four pixels in parallel out of those blocks of 32 pixels, and through the four analog bus lines represented in Figure 3-22. The AD conversion proceeds internally for the four samples, and eight latency cycles later the digital results are available at the ADC outputs and are successively read out. The pixel line is thus reconstructed, and is represented on the right side of the figure (blocks B5 and B6).

Speed requirements

The number of 32 converters for the array has been chosen to offer a sufficient speed for video operation on a medium resolution sensor. Table 3-6 gives some results in ADC sampling frequency for a wide range of image sensor, using the matrix approach described in this report, where the pitch of an ADC cell is four times the pitch of a pixel column. The sampling rate of each ADC cell is assumed to be 131’072 Sample/s in each case.

Sensor size	Number of ADCs	Total sampling rate	Max. frame rate
128 x 128	32	4.194 MHz	256 frame/s
256 x 256	64	8.388 MHz	128 frame/s
512 x 512	128	16.777 MHz	64 frame/s
1024 x 1024	256	33.554 MHz	32 frame/s

Table 3-6: ADC array size in function of sensor size.

The ADC array test circuit is targeted for a 256 x 256 pixel sensor working at a speed of at least 32 frame/s. A number of 32 ADC has been chosen, which gives a frame rate of 64 frame/s.

Chip floorplan and performances

Figure 3-25 shows the layout of the test circuit. It was integrated into the ALP1LV 1-µm double-metal double-poly CMOS technology from EM Microelectronic Marin SA, Switzerland. From left to right, we have a test structure (this is the basic ADC cell but with a resolution of 12 bit), a 128 x 8 pixel test sensor, also placed vertically, with the reset logic (on the top) and read logic (on the bottom). We then have the ADC array, occupying most part of the design. The bottom of the chip is made of standard cells (control logic part). Die

size is 3.07 x 2.16 mm = 6.63 mm2. The ADC array occupies 1.75 mm2, the logic 0.4 mm2, and the sensor 0.6 mm2.

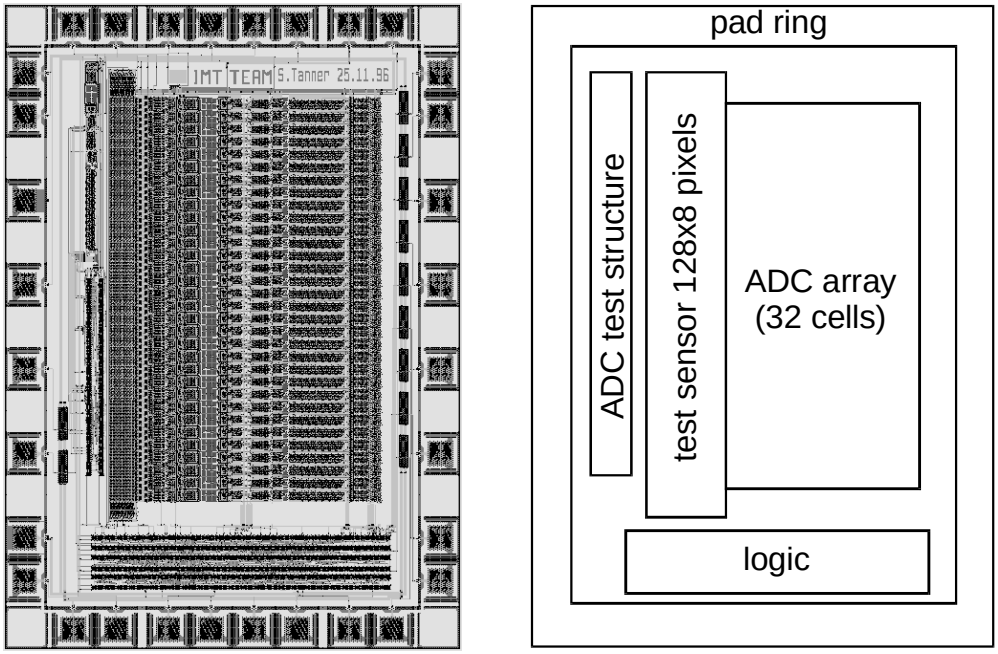


Figure 3-25: Layout of the ADC array test chip (left) and floor-plan (right).

3.6.3 Test results

Linearity and spectral tests were performed in order to characterise the basic cells, while power consumption and inter-channel errors measurements were made in order to characterise the whole array.

Linearity tests

Since the logic was made mainly in order to read the test sensor, it was not easy to perform the linearity tests of DNL and INL on the ADC basic cell of the array. The 12-bit converter was used instead (it is exactly the same design but four more conversion cycles are performed), and the output was rounded to 8 bit. For a rail-to-rail input ramp (from –1.3 V to + 1.3 V), the following linearity errors were obtained (Figure 3-26, Figure 3-27). We see that the DNL is -0.5 /+0.2 LSB, and INL ±0.4 LSB. Analogue saturation near the supply voltages corresponds to a digital saturation.

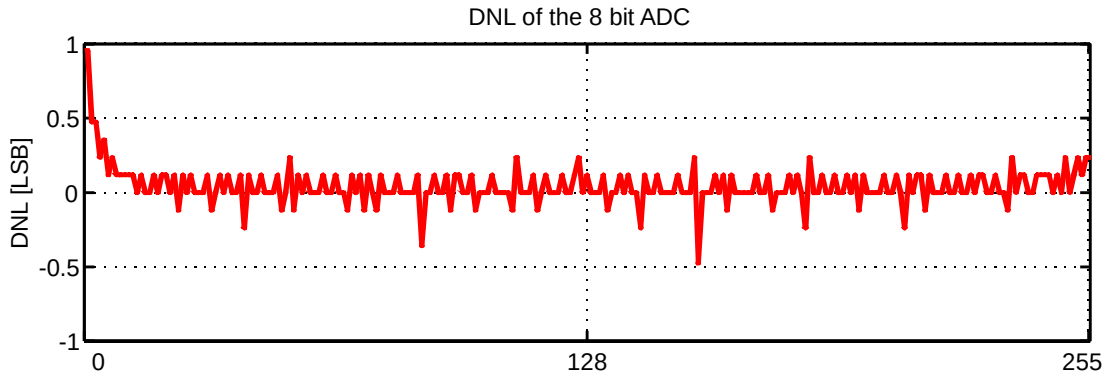


Figure 3-26: Measured Differential Non Linearity.

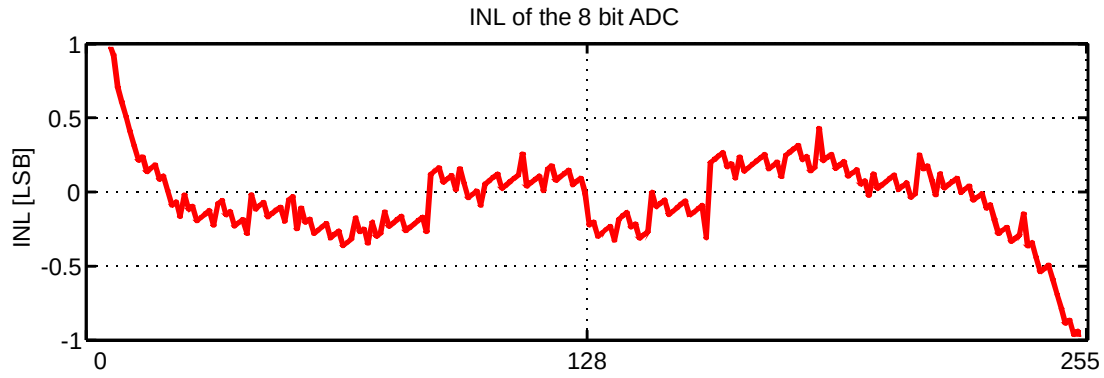


Figure 3-27: Measured Integral Non Linearity.

DNL and INL are higher than expected (compared to the simulations of section 3.5). This is certainly caused by an excessive capacitor mismatch of Cr due to a bad layout drawing, and could be easily improved.

A summary of the characteristics of the basic cell is reported in the next table:

(V_{DD} = ± 1.3 V IF NOT SPECIFIED, T = 25 °C)

Supply voltage:	± 1.2 - ± 1.7	Volt
Input signal range:	± (Vdd – Vsat)	Volt
Nominal sampling rate:	131’072	Hz
DNL:	- 0.5 / + 0.2	LSB
INL:	± 0.4	LSB
Input-referred noise:	< 0.5	LSB
Analogue power consumption	30	µA
Digital power consumption	~ 12	µA

Table 3-7: Experimental results of the ADC basic cell

Spectral Tests

The 12-bit ADC was also used to evaluate the SNR of the basic cell through spectral tests. The following parameters were applied to the circuit:

- Supply voltage: ± 1.3 V
- Reference voltage: - 1.3 V
- Sampling frequency: 87.33 kHz
- Internal frequency: 1.048 MHz
- Analogue supply current: 30 µA
- Input sinus amplitude: 2.00 Vpp

The following figures were obtained by applying a 1024-point FFT to the digital output sinus signal. Figure 3-28 is the FFT of the digital output sinus with a frequency of 21.44 kHz (half the Nyquist frequency). The Signal to Noise and Distortion Ratio (SNDR) computation gives a result of 49.5 dB, and removing the harmonics gives a Signal to Noise Ratio (SNR) of 50.8 dB. If we add the 2.3 dB due to the fact that the analogue sinus is not full scale, we obtain an effective number of bits of 8.5 bit (see Equ. 3-8), which proves that the basic cell is able to meet the 8-bit level resolution requirement.

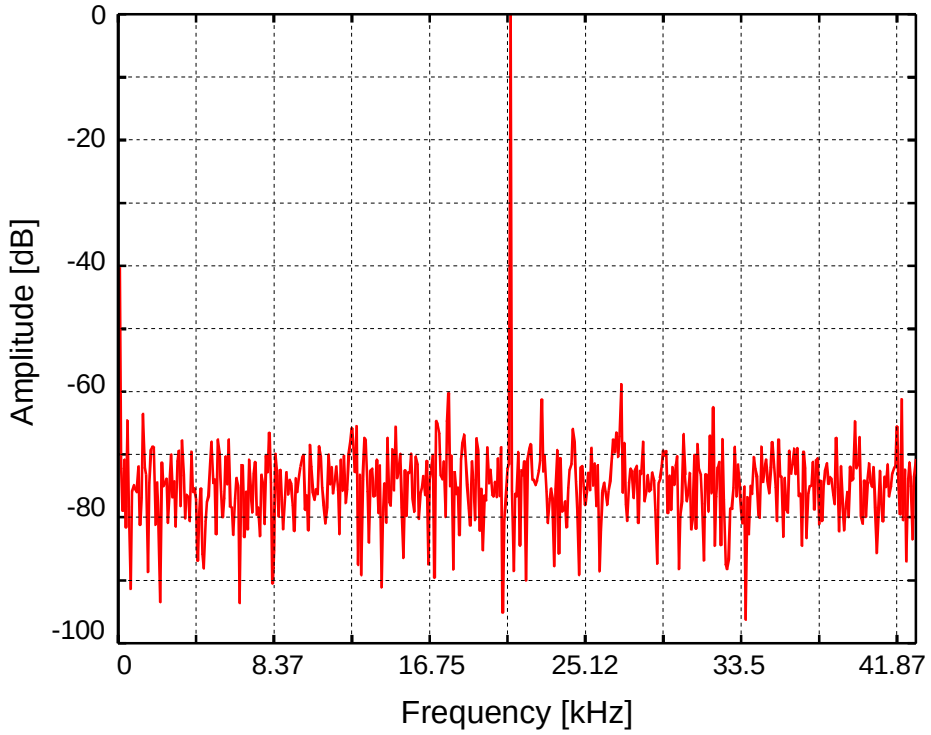


Figure 3-28: 1024-point FFT of a sinus sampled with the 12-bit ADC.

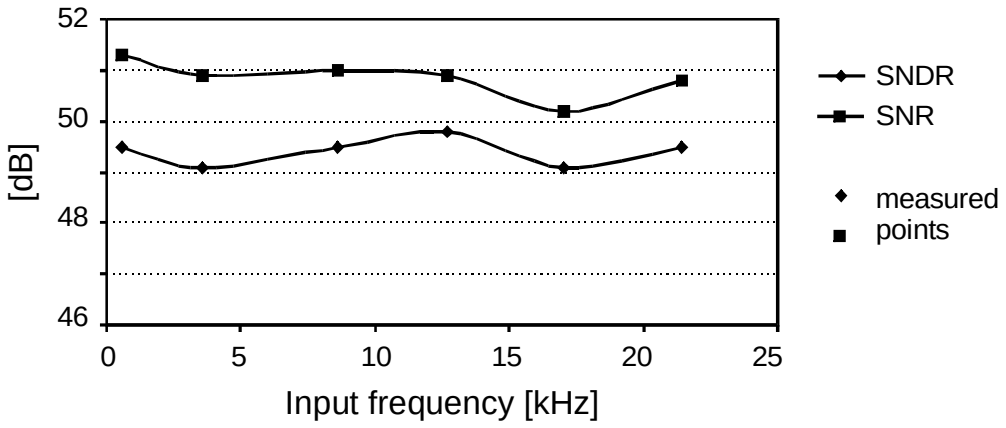


Figure 3-29: SNR and SNDR of the 12-bit ADC versus input frequency.

Figure 3-29 shows the behaviour of the SNR and SNDR in function of the input frequency in the same experimental conditions. In this figure, the lines connecting the points are not part of the measurement, but are used for a better vision. Those values are almost constant, showing that the cyclic converter has a short Sample & Hold phase compared to the duration of the whole conversion cycle.

Power consumption

Measurements of the chip power consumption were performed with a minimal exposure time, which leads to an effective working time of 45 % for the ADCs of the matrix. The following table gives the different current consumption of each block. Power supply voltage is ± 1.3 V, frequency is 4.2 MHz:

Block	Current consumption
ADC OTAs	1016 µA
ADC logic part	156 µA
ADC output part	115 µA
Logic for ADC and buffers	260 µA
Output buffers	660 µA
TOTAL	2.21 mA

Table 3-8: Current consumption of the different ADC blocks.

Excluding the power consumption of the output buffers, the total power consumption for the whole ADC array is about 4 mW @ Vdd = ± 1.3 V.

Power consumption of the circuit in function of the supply voltage has been measured, and is reported in Figure 3-30. The analogue power consumption has been fixed to a constant value for the whole power supply voltage range.

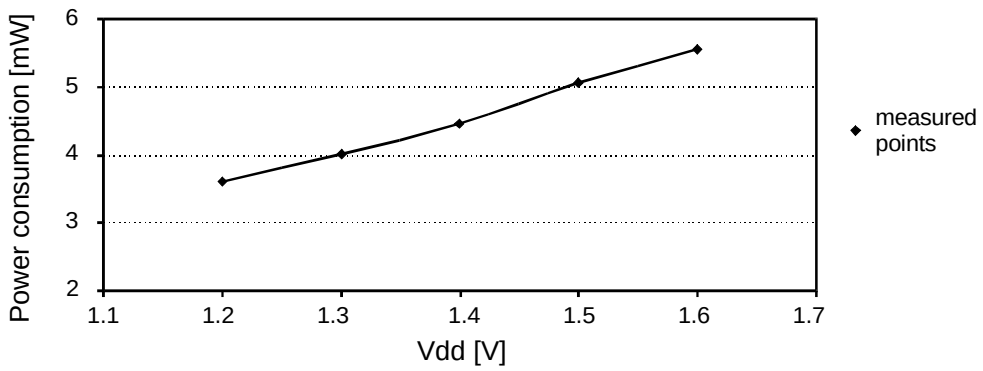


Figure 3-30: Power consumption versus supply voltage

3.6.4 Gain and offset variance

The variance in gain and offset between the 32 ADCs of the array has to be measured in order to calculate the equivalent SNR. The results are shown in Figure 3-31.

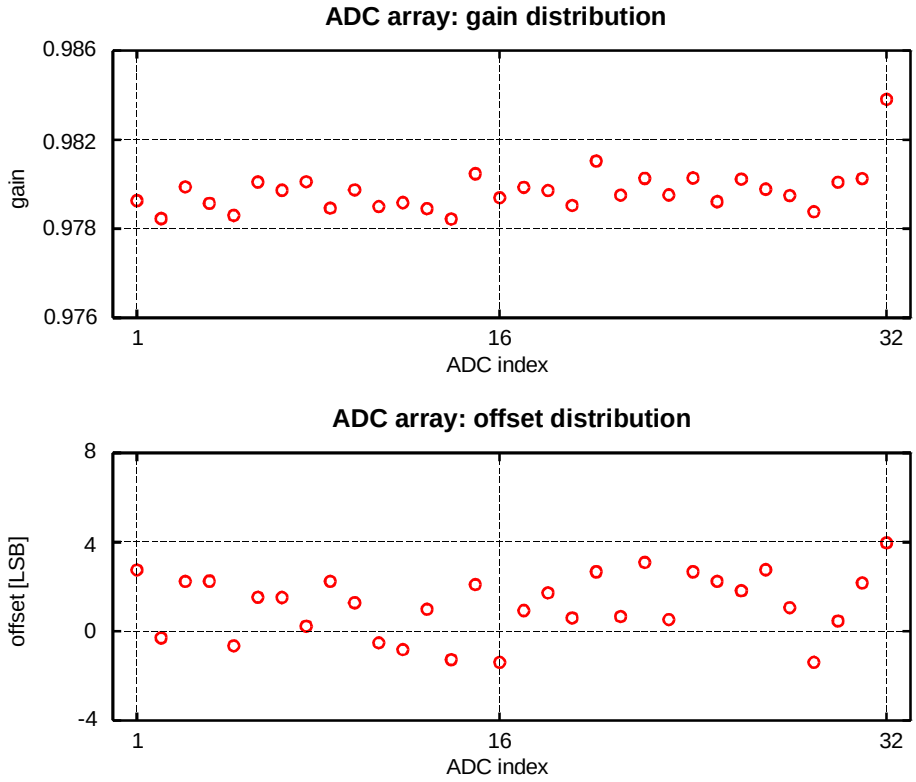


Figure 3-31: Gain and offset (in LSB) distribution.

The corresponding SNR can be calculated with the equations given in sub-section 3.4.2. We obtain an equivalent SNR of 60 dB for the gain variance, and 42 dB for the offset variance.

3.6.5 Conclusions of the parallel-serial realisation

The realised ADC array has a resolution limited mainly by the variance of the inter-channel offset to an effective number of bits of 6.7. If a digital offset correction is implemented, this value can be increased to reach 7.2 bit.

The use of a basic cell with 9 or 10-bit of resolution would achieve a resolution between 8 and 9 bit, at the expense of power consumption.

The parallel-serial solution shows a good power consumption budget, but is limited in resolution and occupies a large area. Therefore, another parallel approach was studied and realised.

3.7 Parallel-pipelined ADC

The second studied parallel ADC approach is based on a pipelined RSD A/D converter. The main advantage of a pipelined architecture is to allow a good optimisation of each stage: unlike the serial ADC approach, where all the bits are extracted by the same hardware, the pipelined conversion is distributed on several stages, each of them being optimised for the corresponding part of the result it has to convert. By scaling each stage, a gain in power consumption and area can be achieved.

3.7.1 Principle of the pipelined RSD conversion

The RSD conversion algorithm can be applied as well to a pipelined structure, resulting in the well known "1.5 bit/stage" pipelined ADC [Gray96]. The somehow ambiguous term "1.5-bit/stage" denotes the redundant nature of the RSD algorithm, which gives a ternary intermediate result for a final binary code.

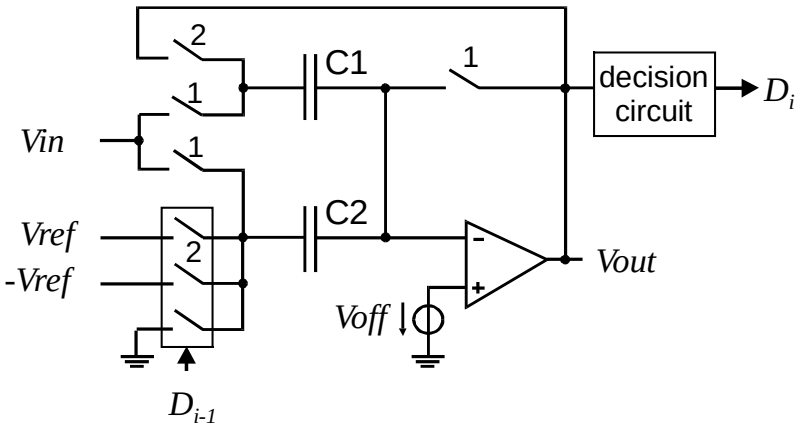


Figure 3-32: Conventional 1.5-bit/stage pipelined ADC (one stage shown).

The conventional switched-capacitor implementation of such a pipelined ADC is shown in Figure 3-32. It uses two capacitors (*C1* and *C2*), two complementary reference voltages (*Vref* and *–Vref*), an OTA and switches. A conversion cycle is decomposed into two phases; in the first phase (sampling), both input voltage *Vin* and OTA offset voltage *Voff* are sampled into *C1* and *C2*. During the second phase (amplification), the OTA gain is used to perform a charge transfer operation between *C1* and *C2*. Depending on the ternary digital decision D_{i-1} of the previous stage, three cases can occur:

1/ $D_{i-1} = 0$. The left plate of *C2* is connected to ground: $Vout = 2 \cdot Vin$.

2/ $D_{i-1} = -1$. The left plate of *C2* is connected to *Vref*: $Vout = 2 \cdot Vin + Vref$.

3/ $D_{i-1} = 1$. The left plate of *C2* is connected to *-Vref*: $Vout = 2 \cdot Vin - Vref$.

The resulting voltage *Vout* is used in the subsequent stages. A decision circuit (two comparators) is used to generate the conversion result D_i of the current stage.

3.7.2 Single-ended implementation

Usually, a differential implementation is used because it offers a better immunity against noise, especially the noise in the power supply lines. However, a differential structure requires more die area, and the differential amplifier consumes more power than the equivalent single-ended one.

The proposed solution, based on [Heu96], is to choose a single-ended implementation of a RSD pipelined stage. A gain in die area and power consumption can then be expected. For low-power, battery-powered systems, the noise in the power supply lines is less critical, and the single-ended approach can be sufficient for resolutions in the range of 8-12 bits.

The single-ended implementation leads to the following schematic, represented in Figure 3-33:

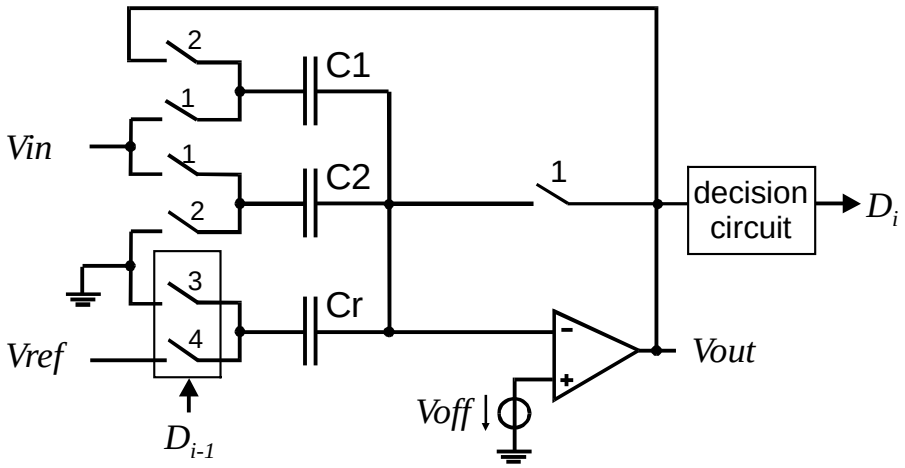


Figure 3-33: Schematic diagram of a single-ended RSD pipeline stage.

The symmetric voltage references + *Vref* and - *Vref* are replaced by a unique reference negative voltage *Vref* and a third capacitor *Cr*. Depending on the ternary digital decision D_{i-1} of the previous stage, three cases can occur:

1/ $D_{i-1} = 0$: The left plate of *Cr* is connected to ground during both phases 1 and 2: $Vout = 2 \cdot Vin$.

2/ $D_{i-1} = -1$: The left plate of *Cr* is connected to *Vref* during phase 1, and to ground during phase 2: $Vout = 2 \cdot Vin - Vref$.

3/ $D_{i-1} = 1$: The left plate of *Cr* is connected to ground during phase 1, and to *Vref* during phase 2: $Vout = 2 \cdot Vin + Vref$.

System equations with offset cancellation

If, during the first phase of the conversion, the common plates of the capacitors are connected to the output amplifier set in voltage follower configuration (see Figure 3-33), a cancellation of the amplifier offset is performed, and the output voltage is given by (see appendix A):

$$Vout = \left(\frac{a}{a + 3 + Cp/C1} \right) \cdot \left[\left(\frac{C1 + C2}{C1} \right) \cdot Vin + D_{i-1} \cdot \left(\frac{Cr}{C1} \right) \cdot Vref \right] + Vinj \qquad \text{Equ. 3-30}$$

where *Vinj* is the constant voltage generated by *Qinj*, *D* is the digital decision of the previous cycle, *Vref* is the reference voltage and *Cp* is the parasitic capacitor on the amplifier input node.

System equations without offset cancellation

If the amplifier is not available during the first phase, the offset cancellation can not take place, and the output becomes:

$$Vout = \left(\frac{a}{a + 3 + Cp/C1} \right) \cdot \left[\left(\frac{C1 + C2}{C1} \right) \cdot Vin + D_{i-1} \cdot \left(\frac{Cr}{C1} \right) \cdot Vref \right] + 3 \cdot Voff + Vinj \qquad \text{Equ. 3-31}$$

Simulation results

Based on the Equ. 3-31, simulations were performed for a 10-bit pipelined ADC without offset cancellation. The following errors were simulated:

- Capacitor mismatch randomly distributed between -0.2 and 0.2 %.
- OTA DC gain limited to 72, 69 and 66 dB, from stage 1 to stage 3. The remaining stages (4 to 8) have a DC gain of 60 dB.
- OTA offset with Gaussian distribution of variance = 1 mV.
- Noise in the comparators corresponding to 100 mV.
- Parasitic capacitor of about 20% of *C1*.

With those parameters, the obtained simulation results for the DNL and INL errors are plotted in Figure 3-34. We see that both DNL and INL are about 0.5 LSB, showing that a 10-bit resolution is achievable for this type of converter.

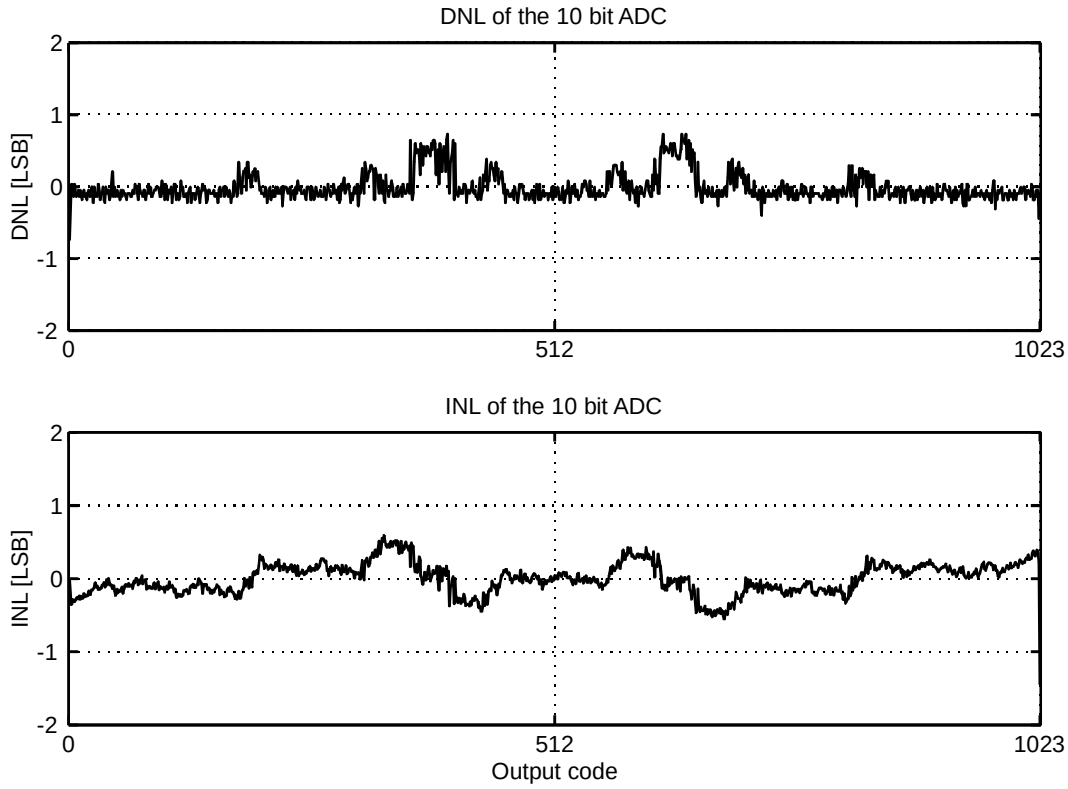


Figure 3-34: Simulated DNL and INL for a 10-bit pipelined RSD ADC.

3.8 Parallel-pipelined realisations and performance

Two parallel-pipelined RSD ADC have been designed and realised. For those designs, two improvement techniques are used. The first is based on an active element sharing technique, leading to a reduction in power consumption, while the second involves a DNL reduction technique.

3.8.1 Active element sharing technique

Various techniques have been applied in order to reduce the number of active elements in an ADC, like in [Naga97] and [Yu96] (duplication of the active element functionality and/or OTA sharing between two consecutive stages of a pipeline). The presented sharing principle has been proposed in [Naga97], and consists of an OTA sharing scheme between *two adjacent pipelines*, leading to a *dual-channel* ADC architecture. The OTA sharing technique relies on the fact that, if no OTA offset cancellation is requested during the first phase of a conversion cycle, the OTA can be used for another pipeline operating at that moment in the amplification phase. The OTAs are then working during the first half clock cycle on a first pipeline, and during the second half clock cycle on a second pipeline (see Figure 3-35). This simple sharing technique has the following advantages:

- Power reduction of about 30-40% compared to a conventional implementation (a reduction of 50% is not possible due to the increased OTA settling characteristic required when sharing is applied).
- The two channels show the same OTA offset, eliminating the need for an inter-channel offset correction.

Figure 3-35 shows a portion of a dual-channel pipeline with the OTAs being alternatively used by channel *a* for one half clock cycle, and by channel *b* for the second half clock cycle. The input sampling phases of channels *a* and *b* are then shifted by 180°.

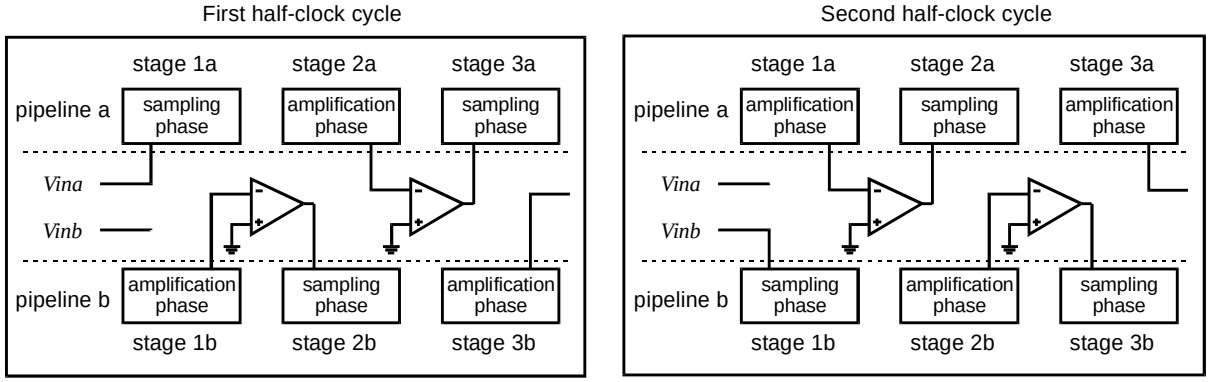


Figure 3-35: OTA sharing between two adjacent pipelines a and b.

Implementation with a single-ended RSD pipelined ADC

The implementation of the proposed sharing technique with the single-ended pipelined RSD stage is shown in Figure 3-36. Compared to the non-shared implementation (see Figure 3-33), only one more switch per stage is required. The timing diagram of the switching signals for capacitor *Cr* is shown in Figure 3-36. Depending on the logical value of Da_{i-1} of the previous stage, three cases are possible:

1/ Doubling of *Vin*: in this first case, *Cr* is not used and remains connected to ground.

2/ Doubling of *Vin* and subtraction of *Vref*: in this second case, *Vref* must be sampled into *Cr* during the sampling phase, and during the amplification phase *Cr* is connected to ground.

3/ Doubling of *Vin* and addition of *Vref*: in this last case, *Cr* is first connected to ground during the sampling phase, then connected to *Vref* during the amplification phase.

The fact that the digital result Da_{i-1} is used during the sampling phase forces the comparison to occur as early as possible. In practice, it happens in the middle of the sampling phase, when the input voltage, in our case *Vina*, has settled sufficiently (Figure 3-36).

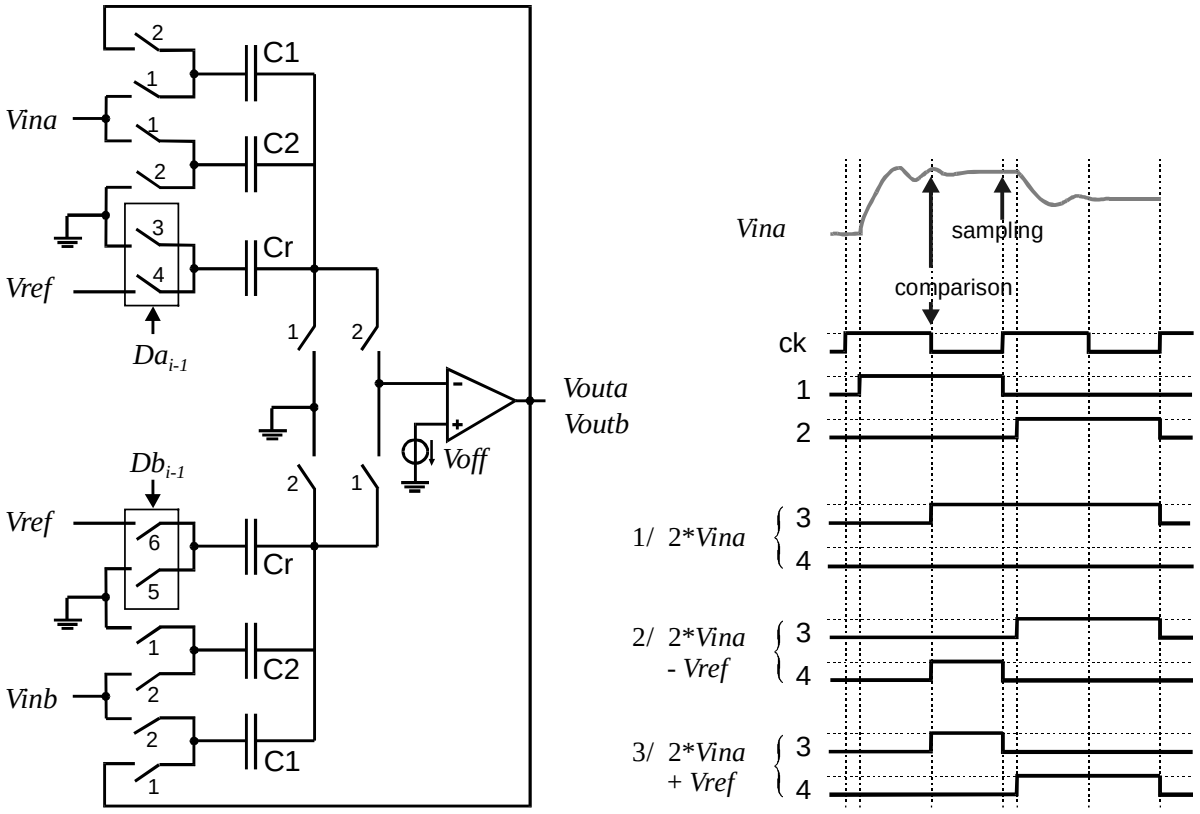


Figure 3-36: RSD implementation and corresponding switching signals for capacitor *Cr* (channel *a*) depending on the three different stage issues.

The generation of the switching signals must be carefully designed, especially for the timing of the switches connecting the OTA input. Non-overlapping signals with four different active edges were used to prevent any parasitic charge injection, which would have been catastrophic on the ADC accuracy.

3.8.2 DNL reduction technique

The second applied technique aims at reducing the Differential Non-Linearity (DNL). In [Yu96], the CFCS (Common Feedback Capacitor Switching) technique is described, allowing suppression of missing codes at MSB decision points, hence reducing the DNL errors. Unfortunately, this technique requires supplementary capacitors, and cannot be used with the proposed RSD implementation, which uses two decision levels instead of one, and three

capacitors per stage instead of two. The proposed idea is to apply the CFCS technique in the following way: depending on the RSD comparison result D_{i-1} (-1, 0, 1), a different feedback capacitor is used: *C1* is used as feedback capacitor if the result is 0, otherwise *C2* is used. This "data dependent" capacitor configuration does not fully compensate DNL as it is performed in [Yu96], but leads to a new transition error dependence in function of capacitor relative mismatches occurring between *C1*, *C2* and *Cr*.

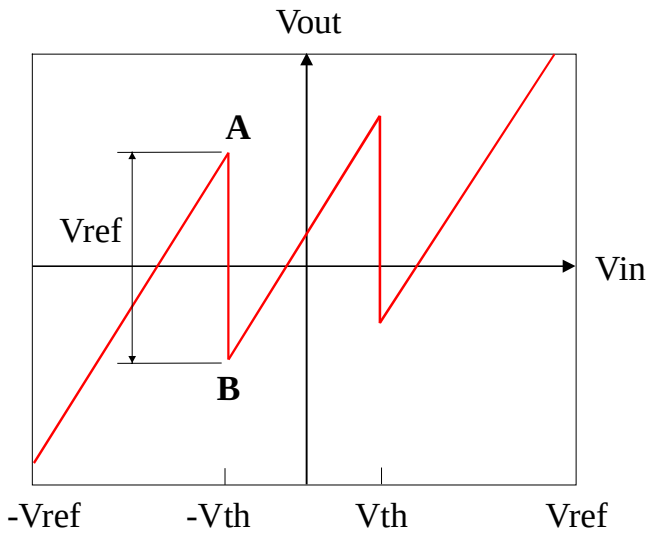


Figure 3-37: Transfer function of a pipelined RSD stage.

Figure 3-37 shows the transfer function of a pipelined RSD stage, corresponding, for the *i*th stage, to the following expression:

$$Vx_i = \alpha_i \cdot \left(\frac{C1_i + C2_i}{C1_i} \right) \cdot Vx_{i-1} + D_{i-1} \cdot \alpha_i \cdot \left(\frac{Cr_i}{C1_i} \right) \cdot Vref \qquad \text{Equ. 3-32}$$

where Vx_i and *Vref* represent the actual signal voltage and the reference voltage, respectively. The ternary output bit (-1, 0, 1) is given by D_{i-1}, whereas α_i denotes error factors induced by finite OTA gain of the *i*th stage.

Let us focus on the transition points A and B of Figure 3-37: Ideally, those points are separated by the exact value of *Vref*. Any error in that value will be amplified in the subsequent stages and will directly contribute to the DNL. If the feedback capacitor is always *C1*, the transition error is given by:

$$Verr = \left(\frac{Cr - C1}{C1} \right) \cdot Vref \qquad \text{Equ. 3-33}$$

If *C2* is used as the feedback capacitor instead of *C1* when and only when D_{i-1} is zero, the transition error is modified:

$$Verr' = \left(\frac{Cr - C1}{C1} \right) \cdot Vref - \left(\frac{C2^2 - C1^2}{C1 \cdot C2} \right) \cdot Vth \qquad \text{Equ. 3-34}$$

where *Vth* is the comparison voltage; its value is usually chosen to be a quarter of *Vref*.

It is possible to plot the transition error functions *Verr* and *Verr'* in function of the capacitor mismatches of *C1*, *C2* and *Cr* (ideally, *C1* = *C2* = *Cr*). Since we are interested in maxima, the absolute values |*Verr*| and |*Verr'*| are calculated. The two plots of Figure 3-38 show the absolute value of such errors in function of capacitor mismatches. *Cr* is assumed to be constant, while a mismatch of ± 0.5 % is applied to *C1* (left-horizontal axis) and *C2* (right-horizontal axis).

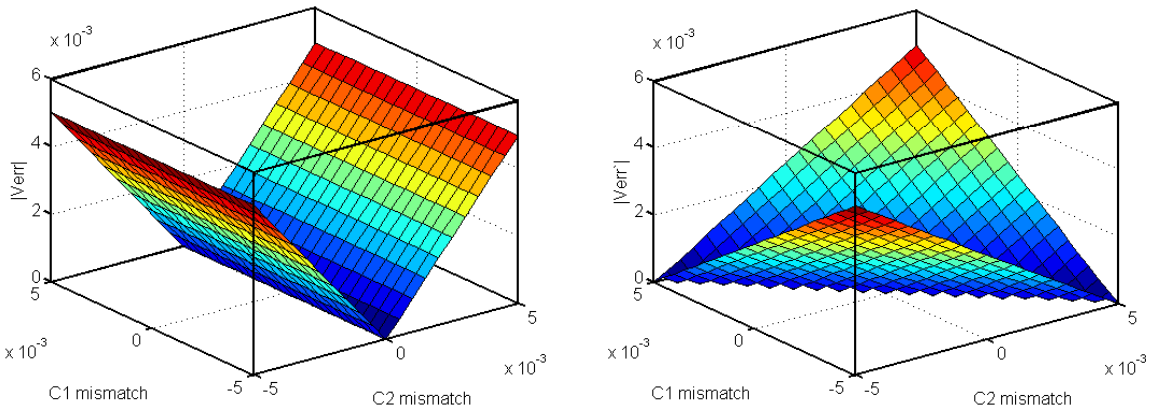


Figure 3-38: Transition Errors |*Verr*| (left) and |*Verr'* | (right) in function of capacitor mismatches of *C1* and *C2*.

The function |*Verr'*| shows an average error reduced by 35% compared to the function |*Verr*| with constant feedback capacitor implementation. The DNL is hence reduced by the same amount, without any significant supplementary hardware cost nor added power consumption. Only two supplementary switches are required.

The switched capacitor implementation of the DNL reduction technique is shown in Figure 3-39, with the OTA sharing technique. Switches 3 and 4 allow *C2* to be used as the feedback capacitor. Switches 11 and 12 have been added for avoiding oscillations in the common plate of *C1* and *C2* when *Cr* is switching.

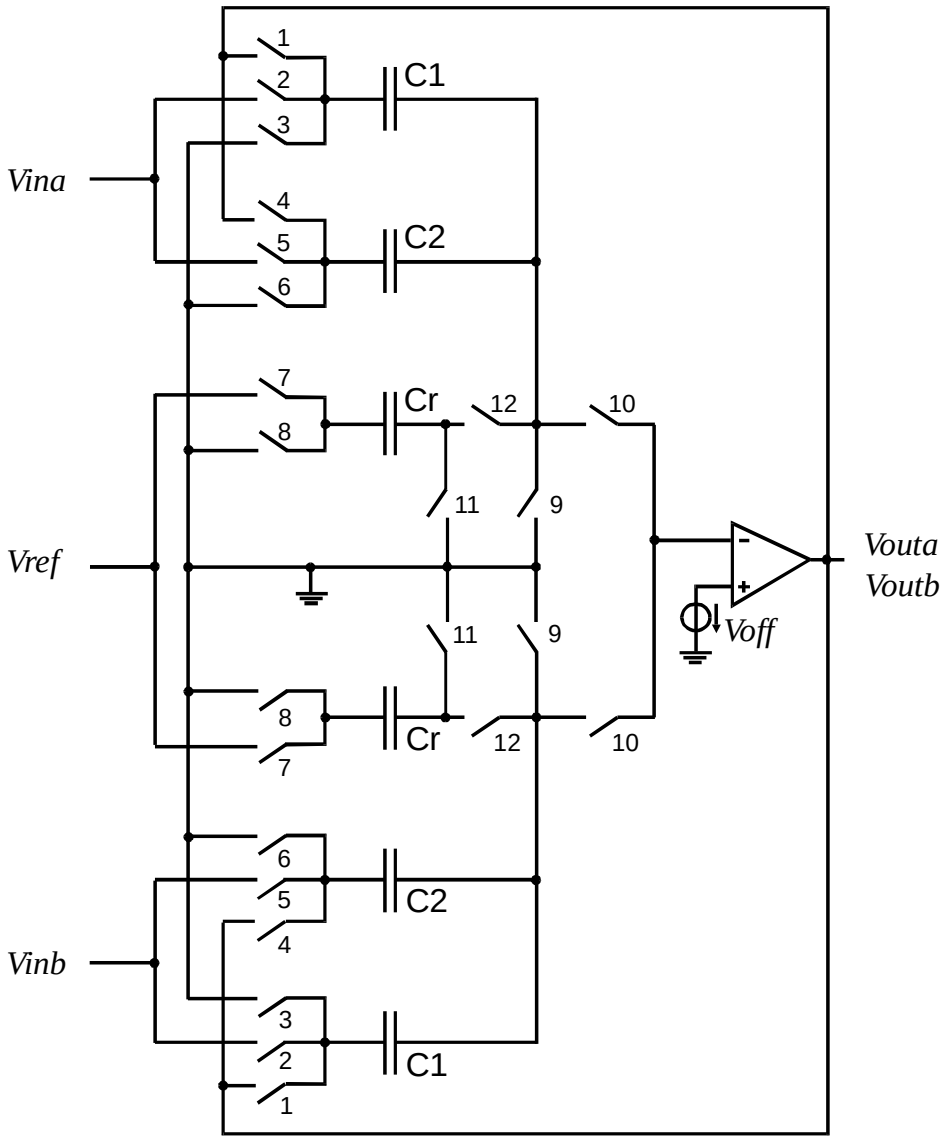


Figure 3-39: Schematic of a dual-pipeline RSD stage with OTA sharing and DNL reduction technique.

3.8.3 Pipeline architecture

The two proposed techniques are applied to a 10-bit dual-channel pipelined ADC. Since the RSD conversion produces *n* bit for *n-1* stages, whereas the last stage does not need amplification, only eight OTAs are required for the two channels.

The architecture of the dual-pipelined ADC is represented in Figure 3-40, with channel a on the top and channel b on the bottom. The shared OTAs are located between the two channels. $\phi 1$ and $\phi 2$ represent the two clock signals of the system, decayed each other by 180°. $\phi 1$ is clocking the odd stages of channel a

and the even stages of channel two, while ϕ2 is clocking the even stages of channel a and the odd stages of channel b.

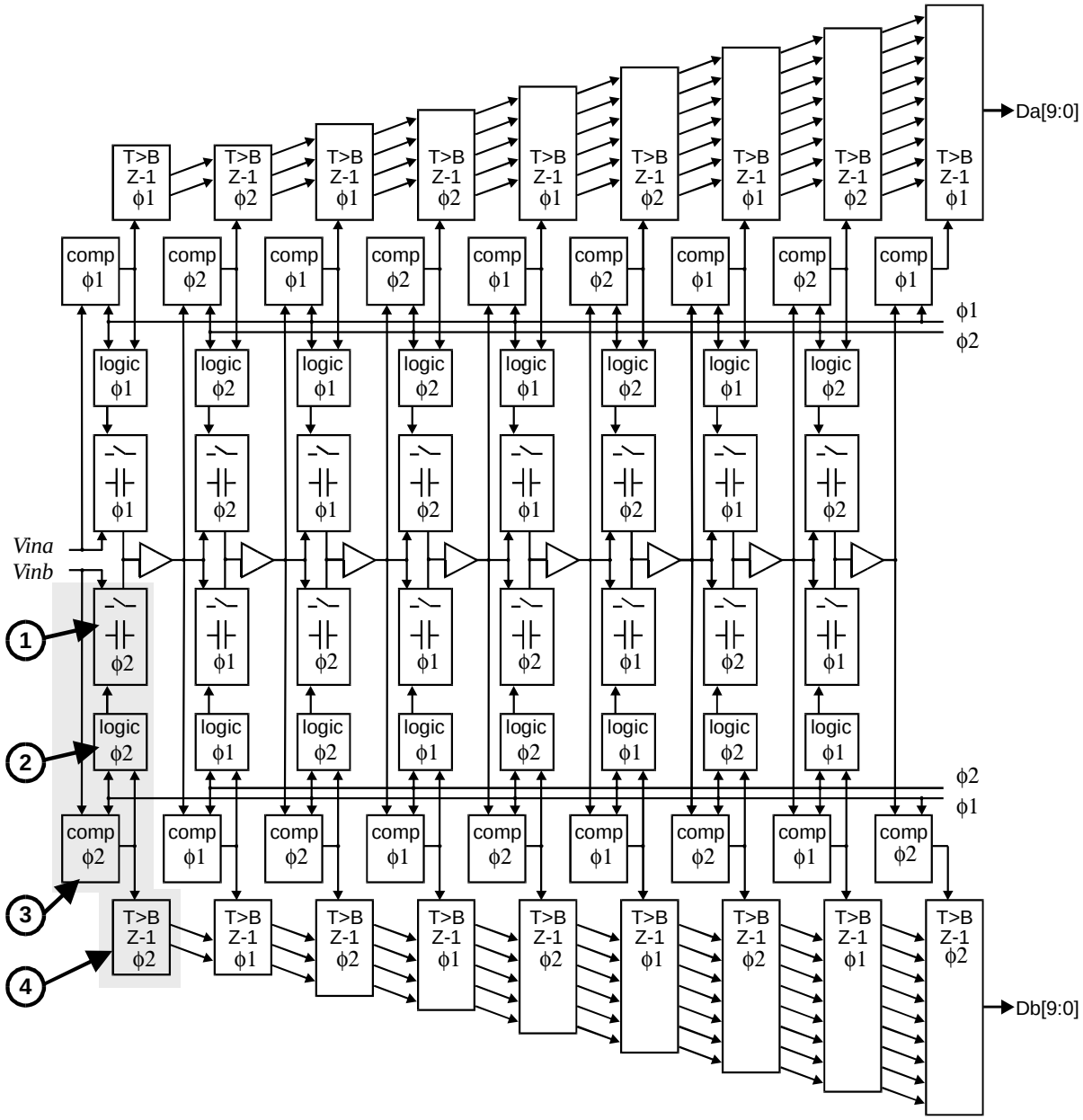


Figure 3-40: 10-bit dual-pipelined ADC architecture.

The structure of one channel stage is explained with the following numbers referring to the figure: (1) capacitors and switches, (2) control logic for the switches, (3) two comparators (comp) and (4) a digital pipeline (shift register) incorporating a ternary to binary conversion logic (T>B).

Comparators

Dynamic comparators presented in [Cho95] are used. They offer low power consumption and reasonable speed.

Digital pipeline with RSD to two's complement conversion

The same logic as the one used for the cyclic RSD converter (sub-section 3.6.1) is used, but it must be this time configured for a parallel implementation. The basic cell (Figure 3-41 a) includes a shift register and a half subtractor, with a carry in and carry out for carry propagation in the same stage.

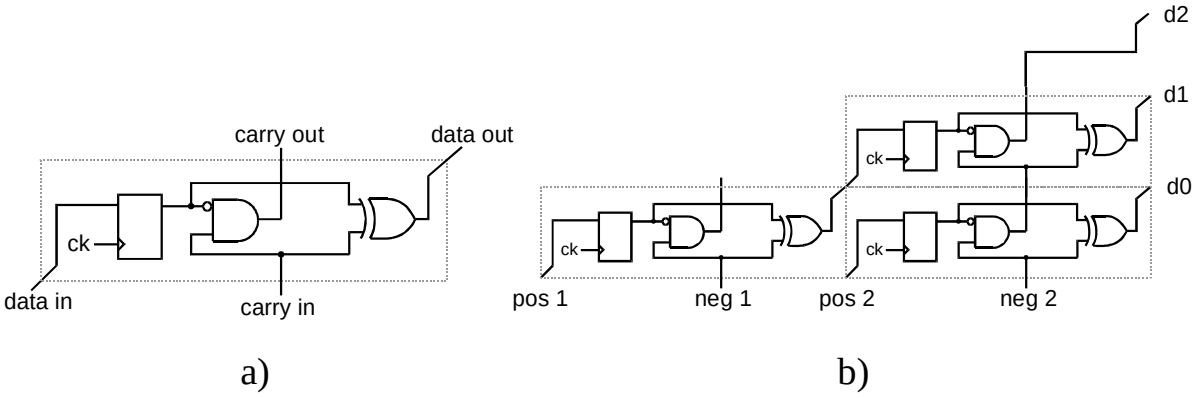


Figure 3-41: a) Digital pipeline basic cell and b) The first two stages of the digital pipeline with two ternary inputs and three binary outputs.

3.8.4 First parallel-pipelined ADC: four-channel, 10-bit ADC

A first parallel-pipelined, four-channel, 10-bit ADC was designed, whose sampling rate was targeted to be 1.25 Msample/s per channel. The corresponding settling time required for the amplifiers was about 300 ns.

The amplifiers used were 2-stage Miller OTAs (see sub-section 3.6.1). Stage scaling was used in order to minimise power consumption. Table 3-9 provides the current consumption and capacitor values for all eight stages. The capacitors were not chosen as small as they could have been for mismatch reasons.

Stage no.	1	2	3	4	5	6-8
Capacitor (pF)	1.8	1.5	1.2	1.0	0.8	0.5
Current (μA)	175	154	133	98	87	70

Table 3-9: Capacitor values and OTA current consumption of each stage.

The four-channel pipelined RSD ADC was integrated into the ALP1 1-µm double-poly CMOS technology from EM Microelectronic Marin SA, Switzerland. It has an active area of 2.4 mm x 0.9 mm. Figure 3-42 shows the layout of the ADC.

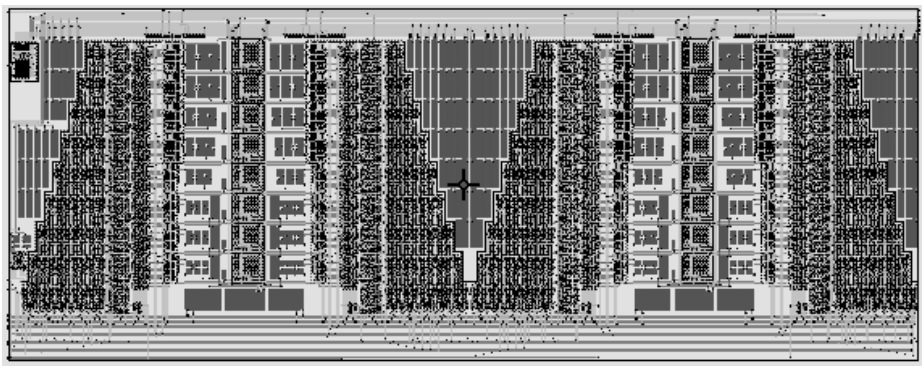


Figure 3-42: Layout of the four-channel ADC. Die area is 2.2 mm2.

3.8.5 Test results

The circuit was characterised, and the main measured parameters are summarised in Table 3-10 (single channel parameters) and Table 3-11 (whole ADC parameters). The circuit was fully operating over a voltage supply range of ±1.2 V to ±1.6 V. Concerning inter-channel errors, only offset degrades the overall ADC performance, and clearly must be corrected (digitally). Gain errors correspond to a limitation in SNR of 64 dB and can thus be neglected. Power consumption of the whole ADC corresponds to about 1.3 nJ/sample for a voltage supply of 3.0 Volt.

(T = 20° C, Vdd = ±1.5 V)

Input capacitance	3.6	pF
Nominal sampling frequency	1.25	MHz
DNL	± 0.5	LSB
INL	± 0.9	LSB
SNR (Fin = 7.14 kHz)	57	dB
SNDR (Fin = 7.14 kHz)	56.5	dB
ENB (effective number of bits)	9.1	bit
PSRR (1 kHz)	> 40	dB

Table 3-10: Measured parameters for each channel.

(T = 20° C, Vdd = ±1.5 V)

Channel number	4	
Analog input range	± (Vdd – 0.2)	V
Nominal sampling rate	5	MHz
Power consumption @ 5 MHz	6.6	mW
Inter-channel gain variance	0.063	%
Equivalent SNR	64	dB
Inter-channel offset variance	0.21	%
Equivalent SNR	44.6	dB

Table 3-11: Main measured parameters for the four-channel ADC.

DNL and INL measurements

There was no mean to switch off the DNL reduction technique in order to evaluate its real impact. But the measured DNL shows a good behaviour for a 10-bit converter that does not use any dummy capacitor, the priority being a minimal die area. Typical DNL and INL plots are represented in Figure 3-43.

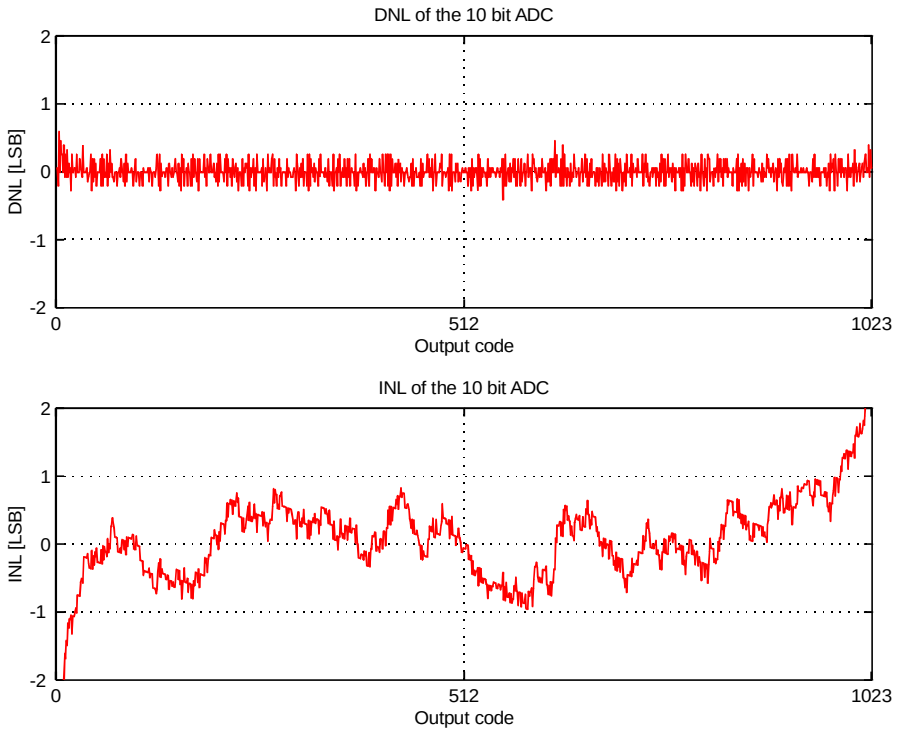


Figure 3-43: Measured DNL and INL plot (rail-to-rail input).

3.8.6 Second parallel-pipelined ADC: eight-channel 10-bit ADC

A second parallel-pipelined 10-bit RSD ADC was designed, but this time with eight channels in parallel. The overall targeted sampling rate was 10 Msample/s.

The same basic architecture as the four-channel version was used. Table 3-12 gives the different stage characteristics.

Stage no.	1	2	3	4	5-8
Capacitor (pF)	1.6	1.3	1.0	0.8	0.5
Current (µA)	164	144	112	84	64

Table 3-12: Capacitor values and current consumption of each stage.

This eight-channel ADC was integrated into a 0.5-µm double-poly triple-metal CMOS technology from IMEC (Belgium), featuring an active area of 2.98 mm x 0.61 mm = 1.82 mm^2. The layout is represented in Figure 3-44.

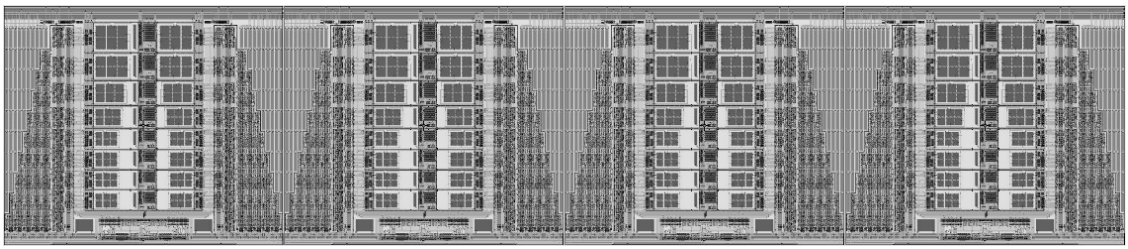


Figure 3-44: Layout of the eight-channel ADC.

3.8.7 Test results

Five circuits were tested and fully characterised. The extracted characteristics are based on the mean of 5 x 8 = 40 different ADC parameters, and are summarised in Table 3-10 (single channel parameters) and Table 3-11 (whole ADC parameters). The inter-channel errors are in the same order of magnitude as the first realisation, and thus require an offset compensation. Power consumption of the whole ADC corresponds to about 1.2 nJ/sample for a voltage supply of 3.0 Volt. Concerning frequency tests, it was not possible to fully characterise the chip at high frequencies due to the lack of Sample and Hold stage in the ADC input, this function being realised by the image sensor itself. The circuit was fully operating over a voltage supply range of ±1.2 V to ±1.6 V.

(T = 20° C, Vdd = ±1.5 V)

Input capacitance	3.2	pF
Nominal sampling frequency	1.25	MHz
DNL	± 0.5	LSB
INL	± 0.6	LSB
SNR (Fin = 28.07 kHz)	56	dB
SNDR (Fin = 28.07 kHz)	55.5	dB
ENB (effective number of bits)	8.9	bit
PSRR (1 kHz)	> 40	dB

Table 3-13: Measured parameters for each channel.

(T = 20° C, Vdd = ±1.5 V)

Channel number	8	
Analog input range	± (Vdd – 0.2)	V
Nominal sampling rate	10	MHz
Analog power consumption (@ Vdd = ±1.5 V, 10 MHz)	10	mW
Digital power consumption (@ Vdd = ±1.5 V, 10 MHz)	2.4	mW
Inter-channel gain variance	0.02	%
Equivalent SNR	74	dB
Inter-channel offset variance	0.22	%
Equivalent SNR	45	dB

Table 3-14: Main measured parameters for the eight-channel ADC.

3.9 Comparisons

The following table gives a comparison between the two parallel approaches studied, i.e. the parallel-serial and the parallel-pipelined approach, for the same technology (1 µm). The column describing the 10-bit parallel-serial ADC has been added for comparison only, and is obtained by adding two more conversion cycles to the 8-bit initial realisation, leading to an increase in power consumption of 25% and in die area of 8%.

	parallel-serial (8 bit) [Tann98]	Parallel-serial (10 bit)	Parallel-pipeline (10 bit) [Tann99]	Unit
Effective number of bit	7.2	8.5	9.1	bit
Power consumption	0.95	1.2	1.3	nJ/sample
Speed over area ratio	2.4	2.2	2.3	MHz/mm2

Table 3-15: Comparison between the parallel-serial and the parallel-pipelined realisation, both in 1µm technology (measurement results).

A comparison of those two realisations with state-of-the-art academic ADC equivalent realisations is presented in the Figure 3-7 (8 bit) Figure 3-8 (10 bit). The two realisations present a good power consumption budget, but occupy a bigger die area than other implementations.

The 0.5-µm realisation of the parallel-pipelined approach improves the "speed over area" ratio: its value is 5.5 MHz/mm^2.

Improvements

The speed of the parallel-pipelined implementation is mainly limited by the delays required by the non-overlapping clock generation. This delay is about 25 ns per half-clock cycle in the 0.5-µm version. Since a half-clock cycle lasts for 400 ns at a frequency of 1.25 MHz, 375 ns remain for the OTA to settle.

Therefore, the ADC clock can easily be doubled, leading to an OTA settling time of 175 ns, which is still easily achievable with a Miller OTA configuration. The resulting "speed over area" ratio would then exceed 10 MHz/mm2, giving a really competitive ADC implementation in terms of power consumption and die area.

References

[Abo99]: A. Abo, P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline ADC”, *IEEE J. Solid-State Circuits*, Vol. 34, No. 5, pp. 599-606, May 1999.

[Blac80]: W. C. Black and D. A. Hodges, “Time interleaved converter Arrays”, *IEEE J. Solid-State Circuits*, Vol. 15, No. 6, pp. 1022-1029, December 1980.

[Bult90]: K. Bult, G. J. G. M. Geelen, "A Fast-Settling CMOS Op-Amp for S-C Circuits with 90-dB DC Gain", *IEEE J. Solid-State Circuits*, Vol. 25, 25, No. 6, pp. 1379-1384, December 1990.

[Bult97]: K. Bult and A. Buchwald, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2", *IEEE J. Solid-State Circuits*, Vol. 32, No. 12, pp. 1887-1895, December 1997.

[Chan92]: A. P. Chandrakasan, S. Sheng, R. W. Brodersen, "Low-Power CMOS Digital Design", *IEEE J. Solid-State Circuits*, Vol. 27, No. 4, pp. 473-484, April 1992.

[Cho95]: T. B. Cho and P. R. Gray, “A 10-bit, 20-MS/s, 35-mW Pipelined A/D Converter”, *IEEE J. Solid-State Circuits*, vol. 30, No. 3, pp. 166-172, March 1995.

[Ding85]: A. G. F. Dingwall, V. Zazzu, "An 8-MHz CMOS Subranging 8-bit A/D Converter", *IEEE J. Solid-State Circuits*, vol. sc-20, No. 6, pp. 1138-1143, December 1985.

[Font83]: P. G. Fontolliet, "Systèmes de télécommunications", *Traité d'Electricité*, vol. XVIII, pp. 208-209, PPUR, Lausanne, 1983, ISBN 2-604-00020-2.

[Gine92]: B. Ginetti, P. Jespers, and A. Vandemeulebroecke, ”A CMOS 13-bit Cyclic A/D Converter,” *IEEE J. Solid-State Circuits*, Vol. 27, No. 7, pp. 957-965, July 1992.

[Gris96]: L. Grisoni, A. Heubi, P. Balsiger and F. Pellandini, "Micro-Power 14-bit RSD A/D Converter", *ISPAT'96*, Oct. 8-10, 1996, Boston MA, USA, pp. 510-514.

[Gris97]: L. Grisoni, A. Heubi, P. Balsiger and F. Pellandini, "Micro-Power 14-bit ADC: 45 µW at ±1.3 V and 16 kSample/s", *ISIC'97*, Sept. 10-12, 1997, Singapore, pp. 39-42.

[Heub96]: A. Heubi, P. Balsiger and F. Pellandini, "Micro Power 13-bit Cyclic RSD A/D Converter", *ISLPED'96*, Aug. 12-14 1996, Monterey CA, USA, pp. 253-257.

[Hoes94]: D. F. Hoeschele, "Analog-to-Digital and Digital-to-Analog Conversion Techniques", Chap. 4, pp. 99-117, John Wiley, New-York, 1994, ISBN 0-471-57147-4.

[Jenq88]: Y. C. Jenq, “Digital Spectra of Nonuniformly Sampled Signals: Fundamentals and High-Speed Waveform Digitizers”, *IEEE Trans. On Instrum. and Measurements*, Vol 37, No. 2, pp. 245-251, June 1988.

[Katt91]: K. Kattmann and J. Barrow, "A Technique for Reducing Differential Nonlinearity Errors in Flash A/D Converters", *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 1991, pp. 170-171.

[Kusu93]: K. Kusumoto, A. Matsuzawa, and K. Murata, “A 10-b 20-MHz 30 mW Pipelined Interpolating CMOS ADC”, *IEEE J. Solid-State Circuits*, Vol. 28, No. 12, pp. 1200-1206, Dec. 1993.

[Lee94]: H.-S. Lee, "CMOS Operational Amplifiers for Low-Power, Low-Voltage Circuits", *Workshop on Low-Power/Low-Voltage IC Design*, June 27 - July 1, 1994, EPFL, Switzerland.

[Mehr99]: I. Mehr, D. Dalton, “A 500-MSample/s, 6-bit Nyquist-rate ADC for disk-drive read-channel applications”, *IEEE J. Solid-State Circuits*, Vol. 34, No. 7, pp. 912–920, July 1999.

[Miel96]: J. A. Mielke, "Frequency Domain Testing of ADCs", *IEEE Design & Test of Computers*, Vol. 13, pp. 64-69, Spring 1996.

[Naga97]: K. Nagaraj, “A 250-mW, 8-b, 52-Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers”, *IEEE J. Solid-State Circuits*, Vol. 32, No. 3, pp 312-320, March 1997.

[Naut95]: B. Nauta, and A. Venes, “A 70-MS/s 110 mW 8-b CMOS Folding and Interpolating A/D Converter”, *IEEE J. Solid-State Circuits*, Vol. 30, No. 12, pp. 1302-1308, Dec. 1995.

[Pelg94]: M.J. Pelgrom, A. C. Jeannet, M. B. Dijkstra, “A 25-MS/s 8-bit CMOS A/D Converter for Embedded Applications”, *IEEE J. Solid-State Circuits*, Vol. 29, No. 8, pp. 879-886, August 1994.

[Pelu98]: V. Peluso, M. S. J. Steyaert, W. Sansen, "A 900-mV Low-Power ΔΣ A/D Converter with 77-dB Dynamic Range", *IEEE J. of Solid-State Circuits*, Vol. 33, No. 12, pp. 1887-1897, December 1998.

[Petr91]: A. Petraglia, S. K. Mitra, “Analysis of Mismatch Effects Among A/D Converters in a Time-Interleaved Waveform Digitizer”, *IEEE Trans. On Instrum. and Measurements*, Vol. 40, No. 5, pp. 831-835, October 1991.

[Raba94]: J. Rabaey, "Low-Power Design at Architectural and System Level", workshop on Low-Power/Low-Voltage IC Design, EPFL, Switzerland, June 27 - July 1, 1994.

[Rob89]: Jacques Robert, "Convertisseurs Analogiques/Numériques Incrémentaux de Haute Résolution à Capacités Commutées", *Thèse No. 779*, 1989, EPFL, Switzerland.

[Raza92]: B. Razavi, B. A. Wooley, “ A 12-b 5-MS/s Two-Step CMOS A/D Converter”, *IEEE J. of Solid-State Circuits*, Vol. 27, pp. 1667-1677, December 1992.

[Raza95]: B. Razavi, "Data Conversion System Design", Chap. 6, pp. 116-126, IEEE Press, Piscataway, 1995, ISBN 0-7803-1093-4.

[Sack90]: E. Sackinger and W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit", *IEEE J. of Solid-State Circuits*, Vol. 25, No. 2, pp. 289-298, February 1990.

[Shei86]: D. H. Sheingold, "Analog-Digital Conversion Handbook", Analog Device Technical Handbooks, Prentice Hall, NJ, USA, 1986, ISBN 0-13-032848-0.

[Song95]: W. C. Song, B-S. Song, “A 10-b 20-MS/s Low-Power CMOS ADC”, *IEEE J. of Solid-State Circuits*, Vol. 30, No. 5, pp. 514-521, May 1995.

[Tann98]: S. Tanner, , A. Heubi, M. Ansorge, F. Pellandini, “An 8-bit Low-Power ADC Array for CMOS Image Sensors”, *Proc. ICECS98*, September 7-10, 1998, Lisbon, Vol. 1, pp. 147-150.

[Tann99]: S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, “A 10-bit Low-Power Dual-Channel ADC with Active Element Sharing”, *Proc. ISIC99*, September 8-10, 1999, Singapore, pp. 529-532.

[Ti95]: Texas Instruments, "Undertanding Data Converters", Texas Instruments Application Report, SLAA013, 1995.

[Tsuk98]: S. Tsukamoto, W. G. Schofield, T. Endo, “A CMOS 6-b, 400-MSample/s ADC with error correction”, *IEEE J. of Solid-State Circuits*, Vol. 33, No. 12, pp. 1939–1947, December 1998.

[Vale93]: V. Valencic, "Micropower CMOS Data Converters", *Workshop on Integrated A/D & D/A Converters*, July 5-9, 1993, EPFL, Switzerland.

[Veen84]: H. J. M. Veendrick, "Short-Circuit Dissipation of Static CMOS circuitry and its Impact on the Design of Buffer Circuits", *IEEE J. of Solid-State Circuits*, Vol. 19, No. 5, August 1984, pp. 468-473.

[Vitt94]: E. Vittoz, "Limits to Low-Power, Low-Voltage Analog Circuit Design", *Workshop on Low-Power/Low-Voltage IC Design*, June 27 - July 1, 1994, EPFL, Switzerland.

[Vore97]: P. Vorenkamp, R. Roovers, “A 12-b, 60-MS/s Cascaded Folding and Interpolating ADC”, *IEEE J. Solid-State Circuits*, Vol. 32, pp. 1876-1886, December 1997.

[Wang99]: Jin-Sheng Wang; Chin-Long Wey, “A 12-bit 100-ns/bit 1.9-mW CMOS switched-current cyclic A/D converter”, *IEEE Trans. on Analog and Digital Signal Processing*, Vol. 46, pp. 507-516, May 1999.

[Yots95]: M. Yotsuyanagi, et. al., “A 2 V, 10 b, 20 MSamples/s, Mixed-Mode Subranging CMOS A/D Converter”, *IEEE J. Solid-State Circuits*, Vol. 30, No. 12, pp. 1533-1537, Dec. 1995.

[Yu93]: Paul C. Yu and H. S. Lee, "A High-Swing 2-V CMOS Operational Amplifier with Replica-Amp Gain Enhancement", *IEEE J. Solid-State Circuits*, Vol. 28, No. 12, pp. 1265-1272, December 1993.

[Yu96]: Paul C. Yu, H-S Lee, “A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC”, *IEEE J. Solid-State Circuits*, Vol. 31, No. 12, pp 1854-1861, Dec. 1996.

Chapter 4
Architecture optimisation

After having presented the CMOS sensor principles in chapter two and several low-power video ADC realisations in chapter three, we can proceed with combining those two blocks in order to get a single chip digital camera. This chapter presents the concept of the digital image sensor, and develops some important aspects, at the architectural level, of its design and practical realisation for a low-power, small die size implementation.

4.1 Low-power digital image sensors

4.1.1 The "camera-on-a-chip" concept

The conversion of an image sensor signal into the digital domain, while not being a new concept, has for a long time been kept separate from the image sensor itself. The concept of "camera-on-a-chip" [Foss93] relies on the idea of grouping the image sensor, the AD converters and the signal processing electronic (analog or digital) on the same integrated circuit. The image sensor chip is thus perceived as a totally digital unit, as a digital memory or a microprocessor is. Besides the reduction in costs and component count this approach brings, it eases the system design and facilitates the sensor interface and control.

4.1.2 Basic blocks

A general schematic representation of a single-chip digital image sensor is shown in Figure 4-1:

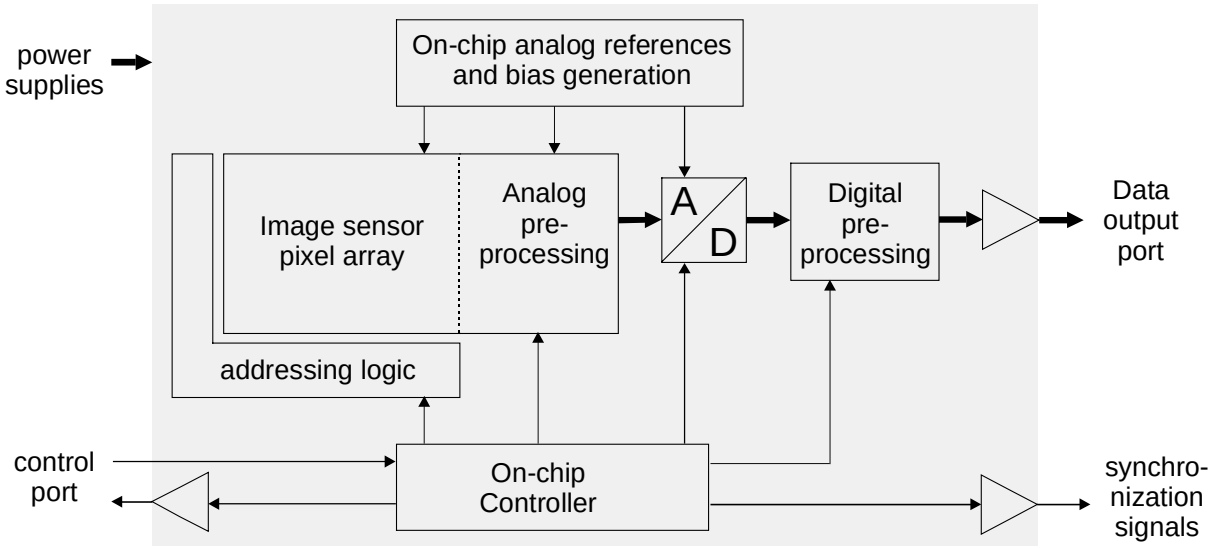


Figure 4-1: Schematic diagram of a digital image sensor.

Image sensor block

The pixel array, the associated addressing logic (horizontal and vertical) and the analog column processing stage form the image sensor block (see chapter 2).

Analog pre-processing block

An analog pre-processing stage may directly follow the sensor. Depending on the sensor architecture, this unit may as well be implemented in the analog column processing stage of the sensor and it becomes difficult to separate the image sensor and the analog pre-processing block into two distinct entities.

The analog pre-processing block possible operations are:

- Double sampling or correlated double sampling for noise suppression (especially FPN) [Nix95].
- Columns offset and/or gain correction.
- Black level subtraction.
- Gamma correction.
- Color space conversion (RGB to YUV, etc.).
- Filtering (anti-aliasing, etc.).

Digital pre-processing block

After the A/D conversion, the signal can be processed in the digital domain. The same operations as those in the analog pre-processing block may alternatively be applied in the digital domain, as well as other more complex algorithms not realisable in the analog domain. The type of algorithm and the specifications

(speed, resolution, power consumption) will decide between an analog or a digital implementation.

Analog references and bias generation block

In order to get rid of any external analog component, the digital image sensor incorporates as much on-chip circuitry as possible for reference or bias voltages generation.

Controller block

Finally, an on-chip dedicated controller (most often a dedicated state machine) pilots all the units present on the chip. The use of an on-chip controller has the following advantages:

- Reduction of the number of external connections.
- Ease of circuit manipulation: reduced need for dedicated external logic.
- Reduction in power consumption.

Interfaces

The digital image sensor has three main digital signal types:

- Control signals for communications between the on-chip controller and external control logic.
- Data output port.
- Synchronisation signals for the use of external acquisition logic with the data output port.

4.1.3 Low-power issues

The starting point for the design of a low-power digital image sensor is the optimisation of each individual block (sensor, ADC, etc.). However, those efforts may be fruitless if the combination of those blocks, at the architectural level, is not optimised. In particular, the following points are essential:

- Sensor and ADC interface.
- Sensor readout and ADC parallelism optimisation.
- Sensor pixel operation (impact on speed)
- Sensor addressing strategies.

4.2 Sensor and ADC interface

A good match between sensor and ADC performances is required for an optimal combination of those two blocks:

4.2.1 Sample & Hold function

Since the readout time of a pixel is usually much shorter than its integration time, the pixel acts as a memory element. Therefore, when a pixel is addressed and read out, an additional Sample & Hold function in the ADC is usually not required. This allows a reduction in power consumption. If the Sample & Hold function of the pixel is not efficient (due to the fact that the required ADC acquisition time is too long compared to the integration time), it can be realised by the Double Sampling stage usually present in the column analog processing stage.

4.2.2 ADC resolution

The ADC resolution should fit the sensor performance for optimum implementation. It would actually be useless to use a sensor with a SNR of 70dB if the following ADC has only 48dB of SNR (equivalent to 8 bit). However, the performance matching of the sensor and the ADC is not so obvious because two contradictory parameters are to be matched:

- First, the ADC resolution (the smallest analog input step corresponding to an LSB) should match the noise of the sensor. Since the noise increases with incident light (see chapter 2), the required ADC resolution decreases when the light increases.
- Second, the ADC SNR should match the output SNR of the sensor. Since the sensor SNR increases with light, the required ADC SNR (and consequently its resolution) will also increase with light.

Those two requirements are represented in Figure 4-2 for a typical pixel equivalent capacitor (50 fF) and output swing (1.5V). The noise floor is 0.3 mV.

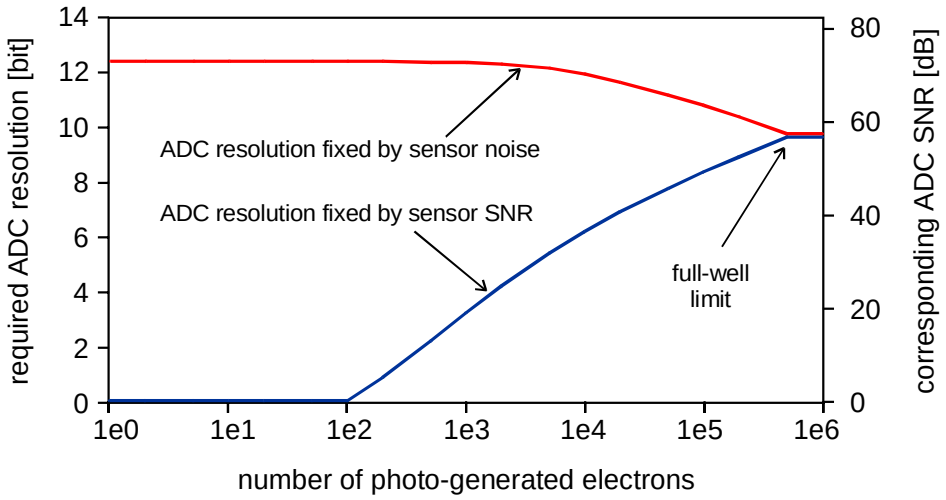


Figure 4-2: ADC resolution requirement in function of light intensity.

For full illumination (full-well limit), the sensor noise and SNR impose the same requirement for ADC resolution because both signal and noise are maximum. For a typical pixel, this requirement in resolution is about 9-10 bit.

The minimal required ADC resolution is then fixed by the sensor SNR at full illumination. With this choice, the sensor and ADC performances are matched for high illumination levels. However, for low light levels (less than 10% of the dynamic), the noise decreases and a higher ADC resolution should be required.

The first solution to this problem is to use an over-dimensioned ADC (typically 12 bit of resolution). Unfortunately, the increase in power consumption is important. Another solution is to use so-called floating point ADCs [Gris98] or relative precision ADCs [Heub96]. They show a limited resolution of 10 bit, but an input dynamic range of 13-14 bit.

4.2.3 Signal amplification before A/D conversion

A third solution to the above mentioned problem is to amplify the sensor output signal in order to increase its dynamic so that it will fully exploit the ADC resolution. A programmable amplifier with adjustable gain is used and the gain is adapted to the light conditions.

The effects of this amplification on the overall SNR performance were simulated and are shown in Figure 4-3, where the SNR after a 10-bit A/D conversion is plotted in function of light intensity.

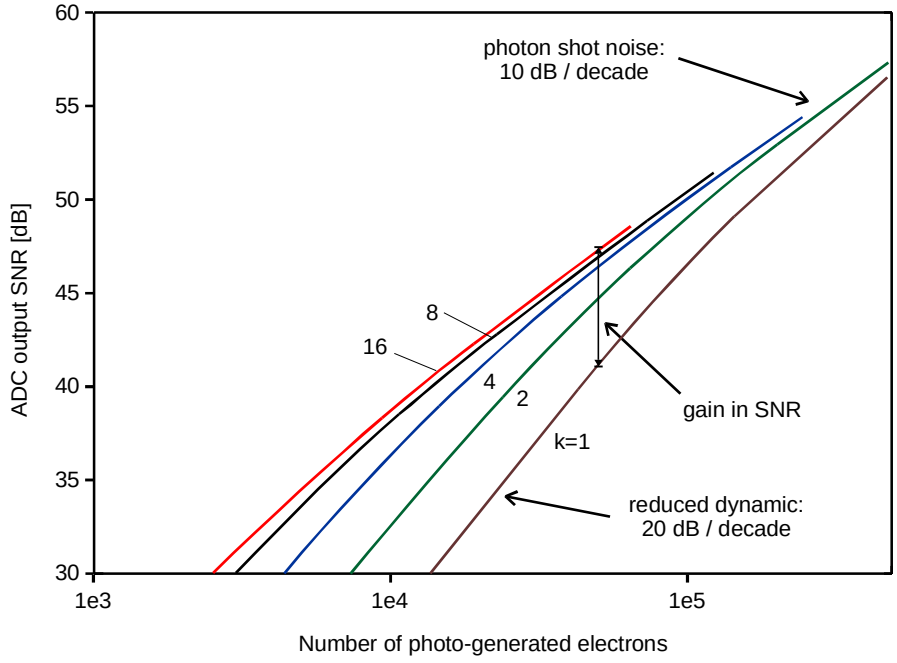


Figure 4-3: Overall SNR performance without pixel signal amplification (k=1) and with amplification (k=2, 4, 8, 16).

The same pixel as in Figure 4-2 was used, and the sensor electronic noise was set to 100μV (such a low value is obtained with a CDS stage).

- The SNR without amplification (k=1) is shown on the bottom right curve. For high illuminations, its slope is only 10dB/decade and is due to the dominant photon shot noise. For lower illuminations, the slope is 20dB/decade due to the loss of output swing.
- In the other plots, the sensor output signal was amplified by gains of 2, 4, 8 and 16 so that its output dynamic matched the ADC input range. The amplifier noise was set to 100μV and was then multiplied by its gain. In all plots the SNR for low light intensities is improved. As an example, the SNR is improved by 6 to 7dB with a gain of 16 and light intensities of 1/20 of the full well; even with such low intensities, the SNR is still reasonable (46 dB).

4.2.4 Sensor output dynamic and ADC input range

The last important issue regarding interfacing the sensor and the ADC is the control of their respective analog output and input dynamic range, thus avoiding any under -or overflow problems, and giving a controlled signal digital dynamic for subsequent electronics (memories, DSPs, etc.).

The ideal case is when the sensor output dynamic perfectly fits the ADC input range (Figure 4-4 a). However, this implies that the ADC reference voltages, defining the highest and lowest input voltages, are adjusted to the sensor signal top (black level) and bottom (white level) voltage limits. This may not always be easy to implement in practice, due to design constraints on the sensor and ADC, and on the difficulty of implementing on-chip low impedance programmable reference voltages for the ADCs.

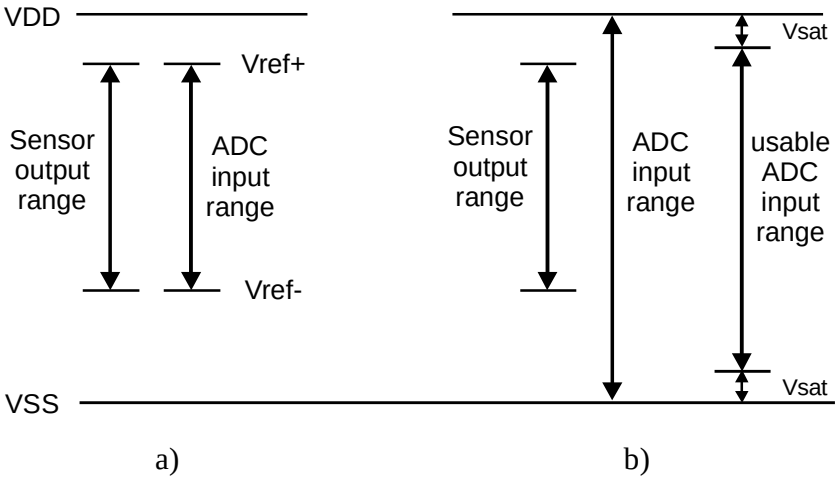


Figure 4-4: a) Ideally matched ADC input range and b) using VDD and VSS as ADC reference voltages.

An easier way to implement the sensor and ADC interface is to set the ADC reference voltages to their maximum (VDD and VSS, see Figure 4-4 b). The need for reference voltages is then avoided. This leads to a reduction in power consumption and a reserve on the ADC input range, solving overflow problems.

The drawback of this choice is that the ADC dynamic is not fully exploited, leading to a loss in SNR of about 3-6dB. This loss can be compensated with an increased ADC resolution of one bit.

4.3 Parallelism optimisation

One of the major degrees of freedom in the design of a sensor architecture is the parallelism of the readout circuitry: the inherent parallel architecture of an image sensor is very well suited for exploiting a variable degree of parallelism in its subsequent readout electronics. Since parallelism is a common way to compensate the loss of speed due to low-voltage operation [Heub97], its application to sensor readout architectures (including ADCs) is well suited for a low-power sensor design.

4.3.1 Principle

The degree of parallelism in digital sensor readout circuitry is given by the number of columns addressed at the same time during the scanning readout phase. Alternatively, this number corresponds also, in most cases, to the number of analog output lines (see sub-section 2.4.3) connecting the sensor to the ADC block. Figure 4-5 shows different parallel configurations in the readout circuitry and ADCs of an eight-column sensor. The parallelism can vary from only one (no parallelism) to the number of columns (maximal parallelism). In this case, all the pixels of a row are read out and digitised at the same time.

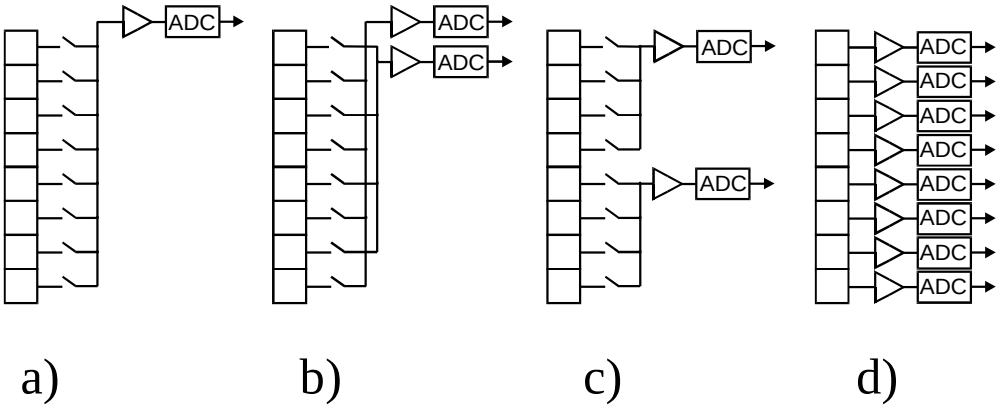


Figure 4-5: Sensor readout parallelism: a) no parallelism, b) two distributed paths, c) two non-distributed paths and d) maximum parallelism.

The parallelism configuration may be called "distributed" when an output path, reading columns, is evenly distributed all along the array (Figure 4-5 b). If the output paths connect each other to successive columns grouped in patterns (Figure 4-5 c), the configuration is "non distributed". The corresponding parasitic capacitors in the column amplifier outputs are in this case smaller than for the distributed configuration, but the ADCs are geometrically related to the pixels (constraints in pitch), which is not the case for the distributed approach.

As explained in sub-section 3.4.1, data multiplexing is performed in the digital domain at the ADC output in order to reconstruct the pixel flow.

4.3.2 Advantages and drawbacks

The main advantages of parallelism in the readout architecture are:

- Possibility to reduce the voltage supply due to reduced operating frequency. An important gain in power consumption is thus possible.
- Relaxed speed constraints of analog components in the readout circuitry (switches, amplifiers, etc.) due to the reduced operating frequency and the reduced capacitive load of each analog path.
- Low-power consumption in the sub-sampling modes due to the possibility of switching off the unused signal paths (see sub-section 4.5.1).

However, the following points may limit the use of parallelism:

- Increased die area (mainly due to the ADCs), giving an unacceptable final circuit area.
- Inter-channel mismatches between the different signal paths (offset, gain, etc.) leading to a reduction in overall SNR (see sub-section 3.4.2).
- Geometric constraints associated with the pixel pitch.

4.4 Pixel operation

Another degree of freedom in sensor architecture design is the pixel structure itself. An original pixel design, bringing new operation modes, has an impact on the overall sensor architecture, and can greatly improve some of its basic characteristics. The low-power sensor operation issue will be addressed in the following paragraphs and will be solved with the introduction of an original pixel structure.

4.4.1 Influence of readout speed on power consumption

In traditional photography, the exposure time has a strong impact on the picture quality. In standard conditions, its maximum is usually 1/50s (corresponding to 20ms). Beyond this value, the risk of blurred pictures is high.

This limit also holds for electronic image sensors. However, another parameter must be taken into account. This is the readout time of an image.

The usual shutter mode with APS sensors is the line shutter mode (see Chapter 2). In this mode, the exposition starts and ends row after row, as if a light aperture was sliding before the sensor and was immediately followed by the readout. If the subject is moving (translation, rotation, zoom), the image will be distorted even for very small exposure times. The sensor readout time must then be as fast as possible and should be in the same order of magnitude as the maximum exposure time. Usually, a value of 20-30 ms is chosen. The next table gives an overview, for different sensor sizes, of the minimum frequency to ensure a readout time of 1/20 second in line shutter mode:

Sensor format	Dimensions	Readout time	Corresponding frequency
CIF	352 x 288	20 ms	5.07 MHz
VGA	640 x 480	20 ms	15.36 MHz
SVGA	800 x 600	20 ms	24.00 MHz
XGA	1024 x 768	20 ms	39.32 MHz
UXGA	1280 x 1024	20 ms	65.53 MHz

Table 4-1: Readout frequencies for a fixed readout time of 20ms.

The necessary readout frequency becomes very high for big sensors, which is critical for battery-powered, still picture image acquisitions devices, where the peak current consumption has to be minimised.

4.4.2 Pixel with memory operated in global shutter mode

The requirement in high readout frequency can be relaxed if a special pixel with analog local memory is used (see sub-section 2.3.2). Jointly used with the global shutter mode, it allows not only all the pixels to be exposed at the same time (better image quality), but it also enables the sensor to be read out with a lower frequency. The information, stored in the pixel analog memory, can be read out more slowly. An important gain in peak current consumption is achievable.

4.5 Sensor addressing strategies

The last degree of freedom in the design of low-power sensor architectures is the way the sensor is horizontally and vertically addressed in special modes. This section presents a few concepts allowing a power consumption reduction in several common addressing modes.

4.5.1 Sub-sampling addressing

For sub-sampling modes (see sub-section 2.3.3), only a subset of the pixels is read out. Consequently, the required frequency and/or the hardware parallelism can be lowered, leading to a diminution in power consumption.

Row direction

Only one row over *n* is addressed and read out (Figure 4-6). The readout time can thus be divided by *n*, or the readout frequency lowered by a factor *n*, which allows decreasing the current consumption by the same amount. For both cases the image acquisition energy is divided by *n*.

Column direction

Only one column over *n* is addressed and read out (Figure 4-6). In this case, a "distributed" parallel readout architecture is suited and the power consumption can be reduced by a factor *n* by switching off all the unused paths (so *n* paths are required).

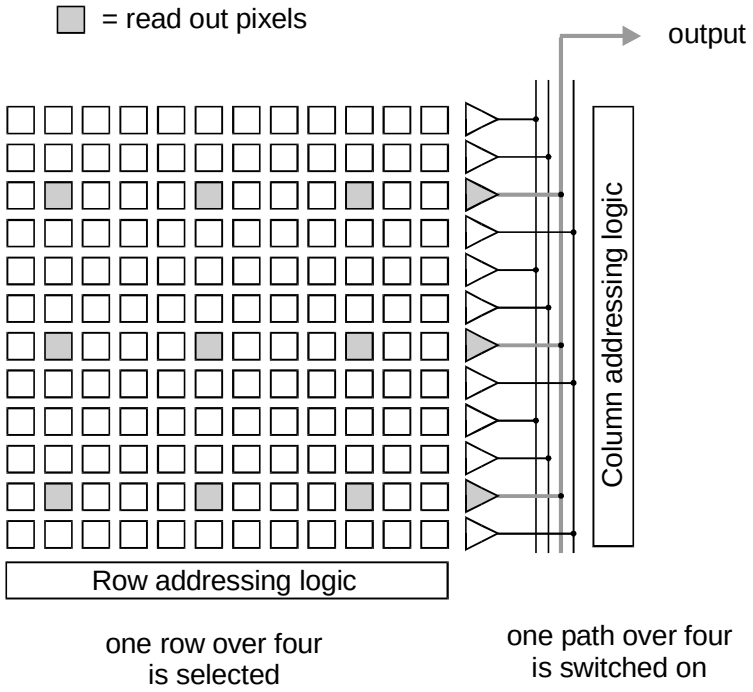


Figure 4-6: Sub-sampling mode with *n* = 4 in both directions

The overall number of read out pixels is divided by n^2 compared to the full resolution; the power consumption can thus be reduced by the same amount.

4.5.2 Windowing addressing

Another common addressing mode is encountered when only a given sensor area ("window") is read out. Only the rows and columns belonging to the window are addressed. The power consumption can be decreased if the unused column amplifiers are switched off. For distributed parallel architecture, the readout signal paths cannot be partially switched off as in sub-sampling addressing mode, and consequently all the output buffers and ADC channels are operating. However, if a non-distributed solution is chosen (see Figure 4-5 c), the unused readout paths can be switched off and the power consumption can be minimised.

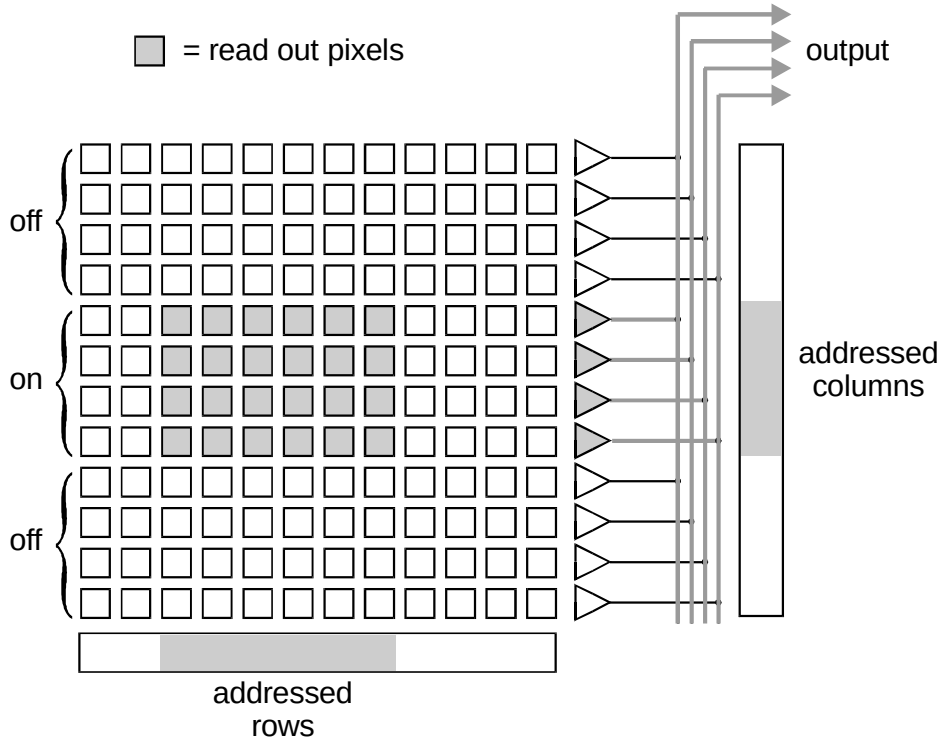


Figure 4-7: Windowing addressing mode with distributed parallel architecture.

4.5.3 Gated clock for active elements

Power consumption can be further reduced if the gated clock principle is applied to active elements, such as current sources, amplifiers, etc., whenever they are not used. In particular, the sensor is subject to a reduction in power consumption during the readout phase if the current sources for the in-pixel source follower (one every column) are not switched on all the time.

However, the effects of gated clock on the current consumption homogeneity have to be investigated for avoiding image artifacts (see sub-section 4.6.1).

4.6 Realisation issues

For a digital image sensor, the realisation phase (layout, floor-planning, routing) is determinant for the overall performance because of the following points:

- Like any mixed-mode design, noise-sensitive analog devices and noisy digital devices are combined on the same chip. Coupling problems are important.
- The important die size of an image sensor introduces not only signal propagation problems (as in digital designs), but also homogeneity problems in the technologic parameters and in the DC voltages.
- There are additional optical and Photon-related problems.

This section focuses on some important electrical issues, and points also out problems related to the floor-planning of the circuit in order to get a small final die area.

4.6.1 Homogeneity in time of DC voltages

In most APS pixel designs, the reset level is strongly dependent on the supply voltage. Any fluctuation in the VDD node (inside the pixel) during the reset phase will then cause artifacts in the image (level change, oscillations, etc.), even for "small" variations. For instance, a sudden change of 20mV on VDD in the middle of the image during reset operation corresponds to 2 LSB at the 8-bit level. This intensity-step in the image may be visible because the eye is very sensitive to such regular variations. The same observation may also be applied for the other DC voltages of the chip.

Modelling the effect of an increased current consumption on the reset level

The case of the reset voltage is studied by looking at a model of the sensor power supply lines (Figure 4-8). In this schematic are represented the three main power consuming blocks of the circuit: sensor, ADC and pads. All three have their equivalent current source. R_{sens} is the serial resistor of the sensor supply line, and V_{sens} is the resulting sensor supply voltage used for reset operation.

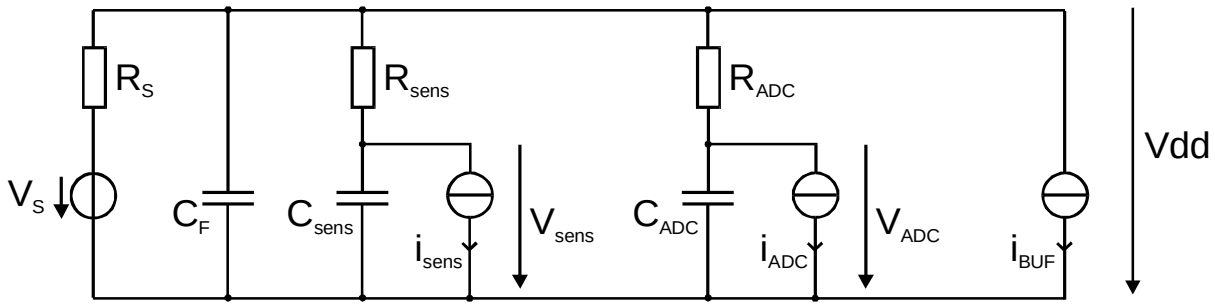


Figure 4-8: Model of the sensor power supply lines.

C_F is a de-coupling capacitor, and R_S is the internal serial resistance of the voltage source V_S. In this case, during the reset operation in line shutter mode, any increase in current (induced by the read phase) will affect the pixel reset voltage by a drop of:

$$\Delta V_{sens} = R_s \cdot \left(\Delta i_{sens} + \Delta i_{BUF}\right) + R_{sens} \cdot \Delta i_{sens} \qquad \text{Equ. 4-1.}$$

For instance, with R_s = 2 ohm and R_{sens} = 5 ohm, an increase of 5mA for both sensor and buffers during readout causes a drop of 45mV of the reset voltage. Figure 4-9 shows the corresponding timing.

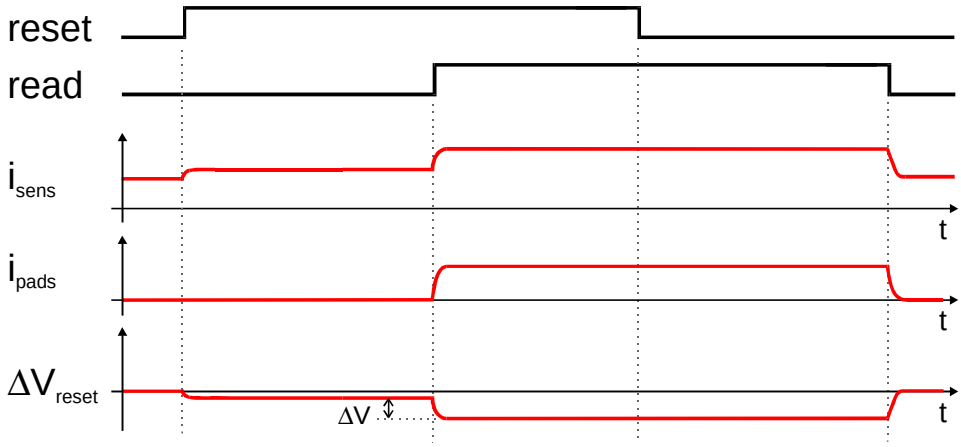


Figure 4-9: Effect of current changes (sensor and pads) on the reset voltage for the line shutter mode.

The changes in the DC voltages in function of time can be avoided by:

- Minimising the resistance of the corresponding lines.
- Ensuring a constant current consumption of all the elements throughout the image acquisition phases, and particularly during pixel reset. This includes also the external components of the system.

4.6.2 Homogeneity in space of DC voltages

Due to the important dimensions of the pixel array and of the final chip, constant voltage gradients may exist in the DC voltage lines (power supply, reference voltages) due to their internal resistance. If they are too important, those gradients can lead to non-uniformity in the image. The voltage gradients can be lowered by applying the traditional techniques of ASIC design:

- Minimising the resistance of the power supply lines.
- Avoiding asymmetric power supply lines (see Figure 4-10).
- Using as much connections to bulk as possible.

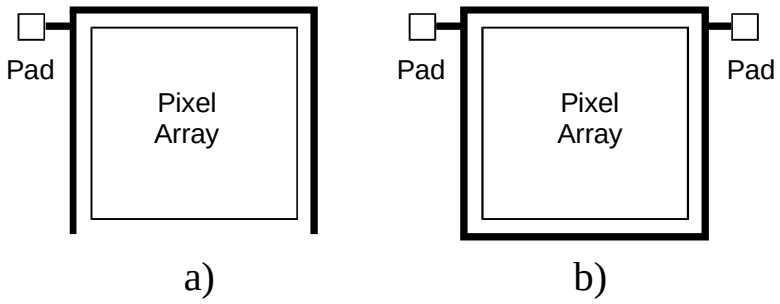


Figure 4-10: a) Asymmetric and b) Symmetric power supply layout.

4.6.3 Power supply noise

The noise present in the power supply lines can have an external origin, but is in most cases generated internally by the switching activity of the digital blocks and of the digital output buffers contained in the pads. It can be minimised by applying the following rules:

- Analog and digital blocks are supplied with different power lines and pads.
- Capacitive cross-talk is minimised if the superposition area of two crossing lines is reduced. In particular, the superposition of two lines of different nature (analog/digital) over a long distance should be avoided.
- On-chip de-coupling capacitors are used as much as possible, even for digital blocks. They are placed as near as possible to the current consuming devices.
- Guard-rings are systematically used around sensitive analog blocks in order to minimise substrate noise.
- The resistance of the power supply lines is minimised.
- The peak current consumption of digital output buffers is minimised using limited slew-rate cells and reasonable maximum speed.

- Off-chip de-coupling capacitors are intensively used.

4.6.4 Floor-planning

The placement of the different blocks must satisfy the following requirements:

- Smallest die area (avoid lost space!).
- Minimised connection lengths in order to avoid signal propagation problems and too high resistance of the power lines.
- Sensor sensitive area centred inside the chip (easing by the way packaging with the optic system).

Since their size is usually important, image sensors are core-limited designs and a simple way to save area is to use a reduced pad-ring. Depending on the application, the pad-ring can consist in three, two or even one row and may be placed so that the chip size will be minimised in a desired direction (Figure 4-11).

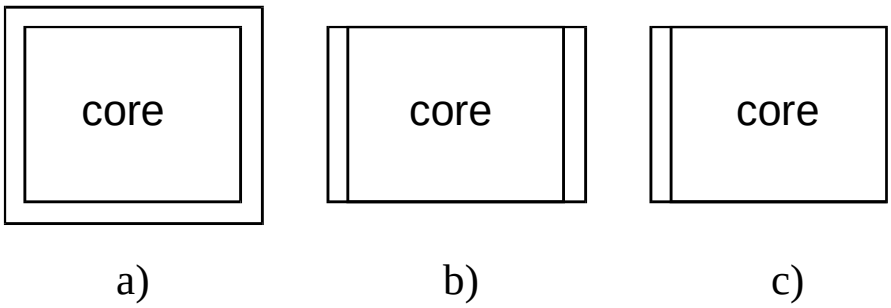


Figure 4-11: Pad-ring configuration. a) Four-sided, b) Two and c) One.

4.6.5 Testing

The individual test of each block of the circuit (sensor, ADC) can be performed if a supplementary circuitry is implemented, consisting in an analog output for the image sensor and an analog input for the ADC, both available on individual pads.

References

[Foss93]: E. R. Fossum, "Active Pixel Sensors - are CCDs dinosaurs?", in *CCDs and Optical Sensors III, Proc. SPIE*, vol. 1900, pp. 2-14, 1993.

[Gris98]: Louisa Grisoni, "Low-Power Floating Point A/D Converters for Audio Signals", *Ph. D. Thesis*, University of Neuchâtel, Switzerland, 1998.

[Heub96]: A. Heubi, P. Balsiger and F. Pellandini, "Micro Power 13-bit Cyclic RSD A/D Converter", *ISLPED'96*, Aug. 12-14 1996, Monterey CA, USA, pp. 253-257.

[Heub97]: Alexandre Heubi, "De l'algorithme de traitement numérique du signal à sa réalisation à faible consommation par un circuit intégré spécifique", *Ph. D. Thesis*, EPFL, Switzerland, 1997.

[Nix95]: R. H. Nixon, E.R. Fossum, "128 x 128 CMOS Photodiode-type Active Pixel Sensor with On-Chip Timing, Control and Signal Chain Electronic", *Proc. SPIE*, Vol. 2415, pp.117-123, 1995.

Chapter 5
On-Chip Controller

After having focused on the sensor, ADC and overall system architecture in the previous pages, this chapter emphasises the main required functions of the on-chip controller, and presents different solutions developed and realised in the frame of this thesis, grouped into four categories:

- Image acquisition control.
- Data processing.
- Exposure control.
- Interface.

5.1 Image acquisition control

5.1.1 State machine

A dedicated state machine is used for the generation of all the control signals involved in an image acquisition (Figure 5-1). Several programmable, successively cascaded counters are used for the generation of reset, exposure time and read operations.

An image acquisition procedure starts with a trigger event, either generated externally (on demand, through a frame request signal or command) or internally (automatic trigger generation for fixed frame rates). The trigger event launches the reset operation, which can be global or row-wise, depending on the shutter type. It also starts the exposure time counter. When the programmed exposure time has elapsed, the read operation is performed. The timing diagram for both line and global shutter modes were presented in Figures 2.7 and 2.9.

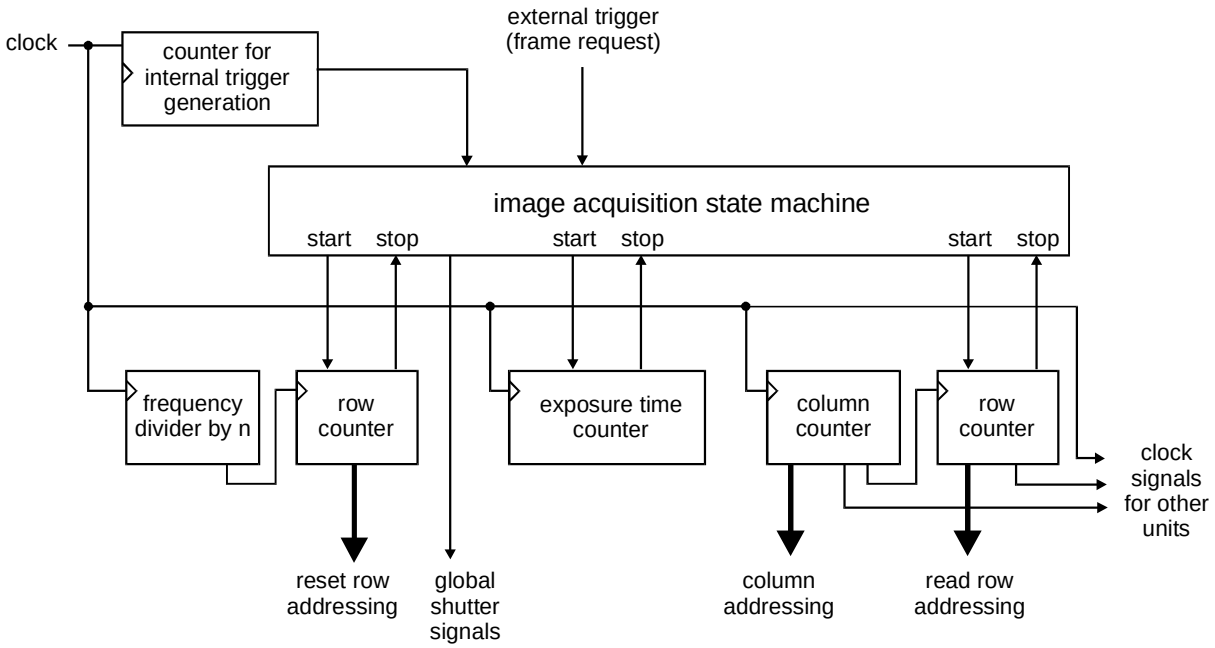


Figure 5-1: Image acquisition state machine for an *n* column sensor.

5.1.2 Video mode operation

In video mode, images are continuously requested with a fixed rate (frame rate). In line shutter mode, an overlap between the readout phase of the current image and the reset phase of the next image is possible because both operations are performed in a row-wise manner. A row, once been read out, can immediately be reset for the following frame (Figure 5-2 a).

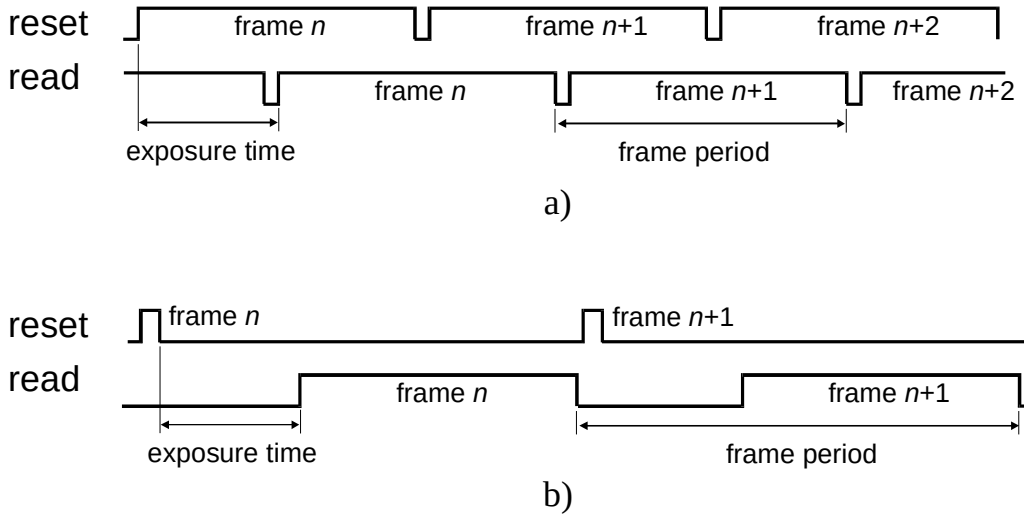


Figure 5-2: Timing in video mode for a) line and b) global shutter mode.

For exposure times shorter than the frame period (time to read out one frame), the frame rate is limited by the readout time. Above this value, the frame rate is limited by the exposure time.

For the global shutter mode, all rows are reset at the same time (Figure 5-2 b). An overlap between reset and read is then not possible, and the maximum frame rate depends directly on the exposure time.

The dependence of the maximum frame rate in function of the exposure time is plotted in Figure 5-3 for a sensor with a readout time of 30ms per frame.

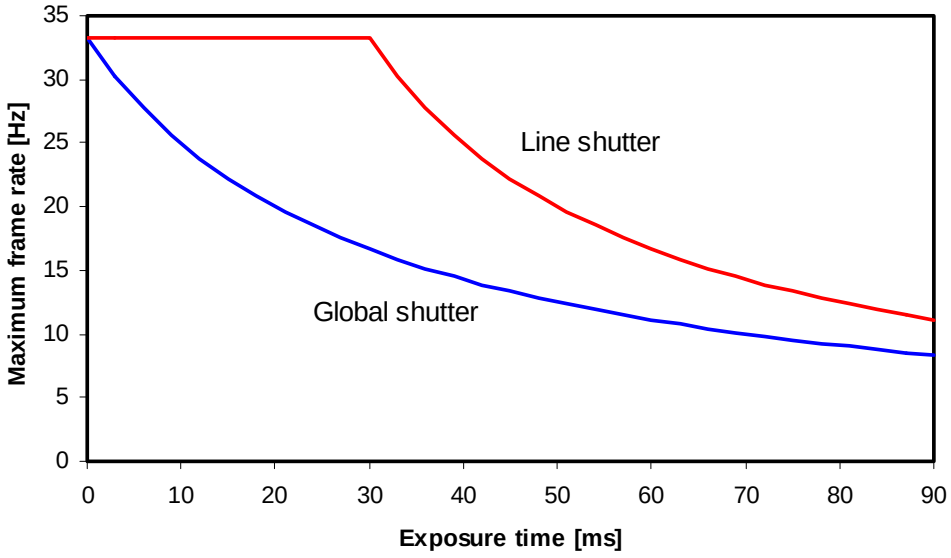


Figure 5-3: Maximum frame rate in function of exposure time.

The line shutter mode appears to be more appropriate for video mode than the global shutter mode. The reset/read overlap better exploits the available frame time.

5.1.3 Impact of the logic on constant current consumption

The image acquisition logic generates all the control signals for the units on the chip, and thus has an important impact on the current consumption of those units in function of time. In order to avoid any artifact in the image due to DC voltage changes in line shutter mode (see paragraph 4.6.1), this logic must be designed so that all the units on the chip consume at any time the same current. The following points will be observed:

Control logic for the sensor

The sensor addressing and readout circuitry should be working continuously, even if no image is requested. A solution consists of continuously reading out the last sensor row. In this way, the sensor consumes exactly the same current than in a "real" image acquisition situation.

A/D converter(s)

The ADCs should be working continuously. Particular attention should be taken if their current consumption is signal dependent.

Digital output buffers

Since their power consumption may be very high, the digital output buffers should be continuously operating. During the blank intervals (line and frame), they should be also activated. Since there is no signal during those periods, an arbitrary signal generator can be used (looped shift register, etc.).

5.2 On-chip digital processing

5.2.1 Sensor and ADC error corrections

The sensor block suffers from different fundamental limitations. They are:

- Pixel Fix-Pattern Noise (offset and gain).
- Column amplifier inter-channel errors (offset and gain).
- Defect pixels, defect rows or columns.
- Pixel and column amplifier non-linearity.

The ADC is considered to have an ideal transfer function. However, if several channels are used, the inter-channel errors (offset and gain) must be corrected.

Ideal correction logic

If we consider only the DC and first order term of the sensor error, the cumulated error in gain a and offset b of the pixel (a_{pix}, b_{pix}), the column amplifier (a_{col}, b_{col}) and the ADC (a_{ADC}, b_{ADC}) can be combined into two coefficients per pixel (a_{tot}, b_{tot}). The transfer function $h(ill)$ of a given pixel in function of the illumination ill becomes:

$$h(ill) = \left(\left(a_{pix} \cdot ill + b_{pix}\right) \cdot a_{col} + b_{col}\right) \cdot a_{ADC} + b_{ADC} = a_{tot} \cdot ill + b_{tot} \qquad \text{Equ. 5-1.}$$

An efficient digital correction logic implementation would then consist in two stages (Figure 5-4):

- The first corrects the gain and offset error of each pixel individually. The corresponding correction coefficients are stored into memories.
- The second replaces the defect pixels by an approximation based on the neighbourhood pixel values. The locations of the defect pixels are stored in a memory.

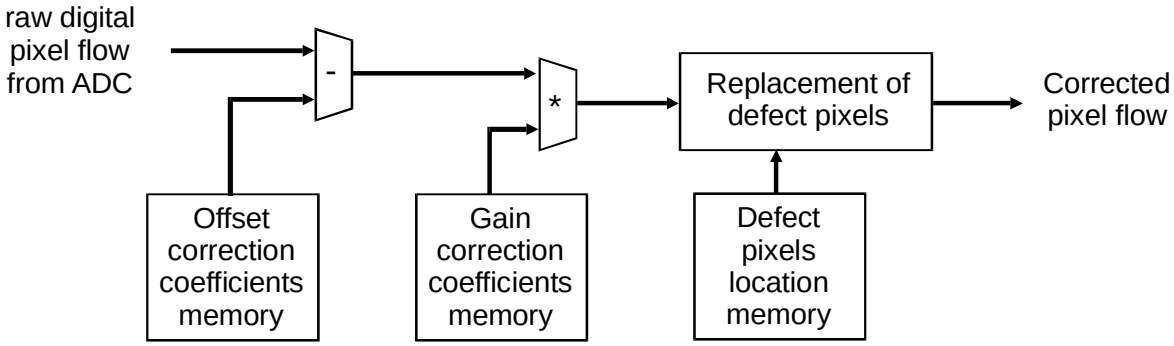


Figure 5-4: Ideal logic for the correction of sensor and ADC errors.

This correction logic has the advantage of an almost perfect correction of each individual pixel as well as all the inter-channel errors. However, it requires the computation and storage of two coefficients per pixels. The corresponding memory system would be too big and consume too much power to be taken into consideration for a low-power on-chip implementation.

Realised correction logic

A simplified version of the correction logic can be designed if there is no need to perform a gain correction. For this, the pixel array must show an acceptable gain variance and the column amplifiers and ADCs must be designed so that their inter-channel gain errors are small enough to be neglected.

If a pixel offset (FPN) suppression in the analog domain is added, the correction consists then only of an offset compensation between the different readout channels of the sensor. Following Equ. 5-1, the ADC offset suppression can further be added in the same correction coefficient, as well as the black level adjustment.

The correction algorithm begins with a calibration phase where the image black level is read out, digitised and stored into registers (coefficient *B*, one for each readout channel). Then, during an image acquisition, the following phases take place (Figure 5-5 a): (1) the pixel is reset to its black level. (2) It is exposed and

discharges to a given level. (3) The column amplifier and ADC offsets are added to the pixel signal, giving the digitised pixel signal *A*. (4) and (5) The difference *B* - *A* is computed and corresponds to the non-inverted, offset-free illumination value. Figure 5-5 b) shows the (very simple) correction logic.

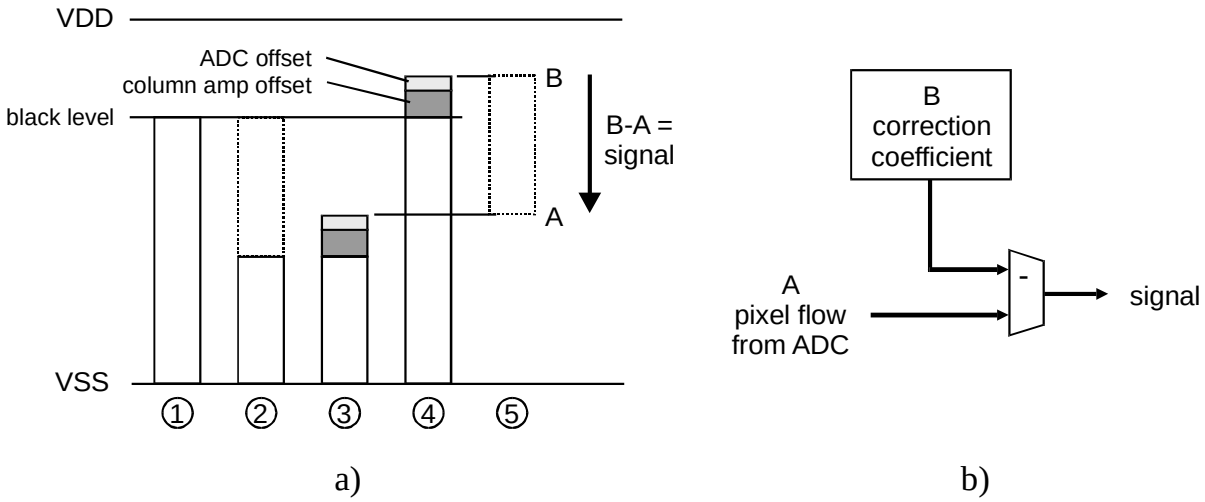


Figure 5-5: a) The phases of signal correction, b) the correction logic.

5.2.2 Digital bilinear filtering

A bilinear filtering on the image is very often required for several reasons:

- Anti-aliasing (low-pass) filter for sub-sampled images.
- Sharpening (high-pass) filter for improving the image sharpness.

Alternatively, other 2D operations might be necessary, like colour interpolation and space colour conversion (RGB to Y-Cb-Cr for instance).

The simplest on-chip implementation requires a digital buffering of *k* image lines, where *k* is the bilinear operator size. The filtering arithmetic unit must be able to process the stored image portion in real time.

The necessary hardware for a real-time 2D operation is very often not compatible with the constraints in die size and power consumption of the digital image sensor.

5.2.3 Low-power anti-aliasing filtering

For sensors operating in sub-sampling modes, the spatial sampling frequency is reduced: the Nyquist frequency limit is not respected any more, and the risk of

aliasing effects in the image is strong. Before sub-sampling, a bi-directional anti-aliasing (low pass) filtering operation has then to be performed.

For some applications in sub-sampling modes, low-power consumption is more important than image quality:

- In digital photography, sub-sampling image acquisition is used for the viewfinder mode on a low-resolution LCD; the image quality is of second importance, while the power consumption has to be minimised because this phase usually lasts for a long time.
- In autonomous security systems, the automatic image analysis occurs on a reduced resolution scene for saving computing requirements. The maximum image quality is only required for remote, occasional human visual inspection.

For those reasons, it may not be power-effective to acquire a full resolution image and then throw away most of the information by down sampling after filtering. Two alternative solutions are proposed and evaluated. Both rely on the fact that, in the column direction, addressing two pixels at the same time and summing their output currents can realise a simple low-pass filter function.

Anti-aliasing filtering for sub-sampling of factor 2

In the column direction, the rows are selected two by two and the pixel currents are summed (decimation by a factor 2). In the row direction, a digital mean of two adjacent pixels is performed, which is equivalent to a second order FIR filter, and one value over two is kept (decimation by a factor 2). In Figure 5-6, the corresponding amplitude response of a 1-D (mono-dimensional) mean filter is compared with 1-D FIR filters of orders 3 and 5.

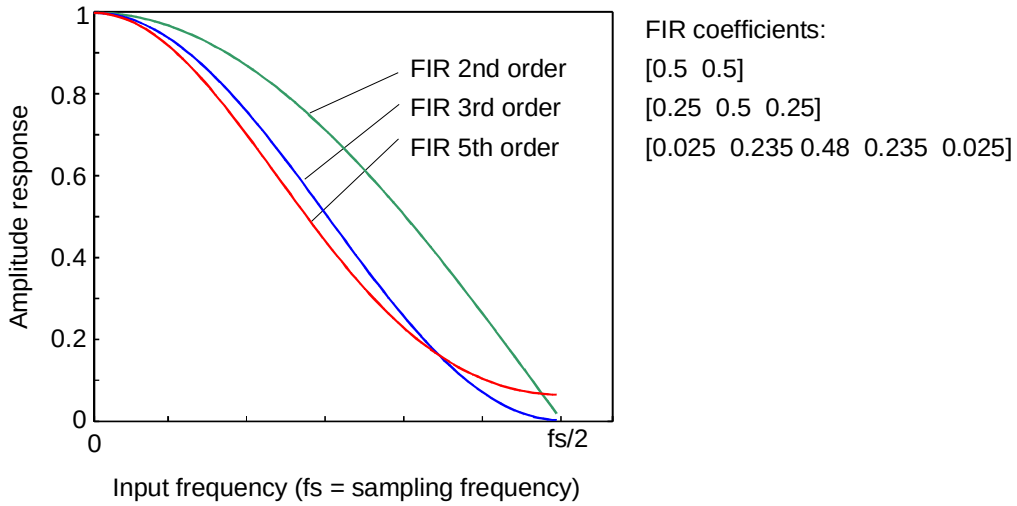


Figure 5-6: Comparison of the mean filter with FIR of orders 3 and 5.

We see that, although not as good as a 3rd or 5th order FIR filter, a mean has the advantage of simplicity. As an example, Figure 5-7 contains a test image on the left. The images in the middle and on the right were obtained by filtering and decimating the test image by a factor of two in both directions. In the middle, a mean filter was used, and on the right a 5th order FIR filter was used. The advantage of using an analog mean in the column direction is a reduction in energy necessary for processing an image.

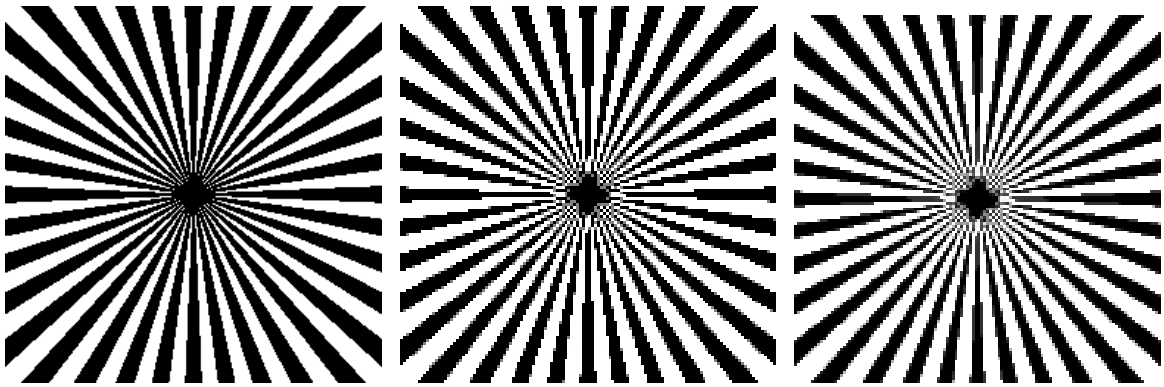


Figure 5-7: Left: original image. Middle: 2nd order FIR and 2x2 decimation. Right: 5th order FIR and 2x2 decimation.

Anti-aliasing filtering for sub-sampling of factor 4

For sub-sampling of factor 4, the proposed filtering method consists in:

- Sub-sampling the image by a factor 2 in both directions. This is naturally performed if only one row and one column over two are read out.
- Performing a mean of the adjacent pixels in both directions as described in the previous paragraph: digitally in the row directions, and by current addition in the column directions.
- Sub-sampling again the image by a factor 2 in both directions.

The resulting operation is shown in Figure 5-8, and is compared with a 5th order FIR filtering followed by 4x4 decimation. This method gives satisfying results only if the high frequency content of the initial image is not too important. In the practice, it can be limited by the spatial filtering properties of the optical system. The main benefit of this method is a reduction of the image acquisition energy by a factor of about eight.

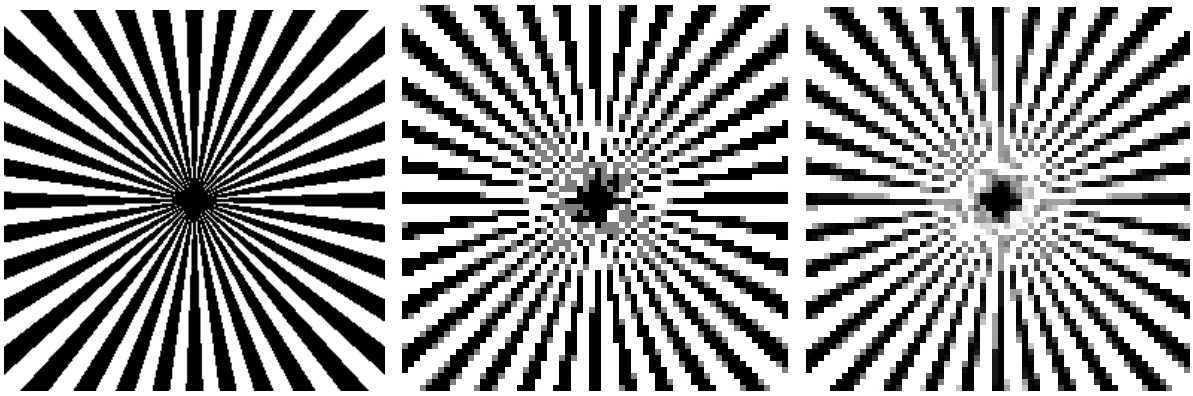


Figure 5-8: Left: original image. Middle: 2x2 decimation, 2nd order FIR and 2x2 decimation. Right: 5th order FIR and 4x4 decimation.

5.2.4 Signal amplitude control

Since for most imaging applications a dynamic of eight bit is sufficient, the interest of using 8-bit wide external memories will be obvious for power consumption and connection count reasons. The full digital dynamic has to be used for maximal image quality, and a control of the signal amplitude is necessary. This control consists in several operations:

- A down-clip to zero, eliminating possible pixel negative values.
- A gain correction for readjusting the dynamic to a 9-bit value.
- An up-clip to 511 (9 bit) for avoiding any over-range in the pixel values.

The realised overall digital data flow is represented in Figure 5-9. After the A/D conversion, the inter-channel offset correction and black level adjustment is performed, followed by the down-clip operation. Then the gain adjustment (four selectable values) and the (optional) digital mean between two adjacent pixels is made. The last operation is the up-clip.

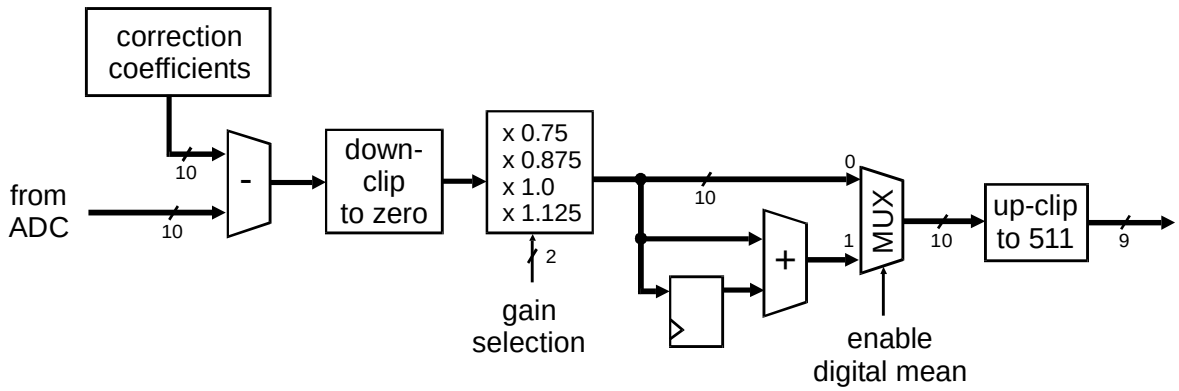


Figure 5-9: Digital data flow with amplitude control units.

In our present case, the selected ADC has a resolution of 10 bit and a rail-to-rail input range. The sensor block is optimised for having an output dynamic of 1.5 to 1.8 Volt, which represents about half the ADC input dynamic. The effective output digital dynamic is then around 9 bit, which is more than necessary. The supplementary bit is used in the digital processing units for improving the accuracy. At the end, only the eight most significant bits are kept.

5.2.5 Limitations of on-chip digital processing

The amount of on-chip digital processing is in our case limited by the small die area constraint. By using deep sub-micron technologies, the area occupied by the logic would dramatically decrease, but one is faced with the poor optical behaviour of such technologies for realising image sensors. It is thus preferable to use two distinct chips realised in different technologies. The first is dedicated to the sensor and has limited on-chip digital processing abilities, while the second is realised in a deep sub-micron technology and is optimised for digital signal processing.

5.3 Exposure time control

A simple on-chip exposure time controller has been designed. It is based on an adaptive and incremental proportional regulation loop whose principle is shown in Figure 5-10.

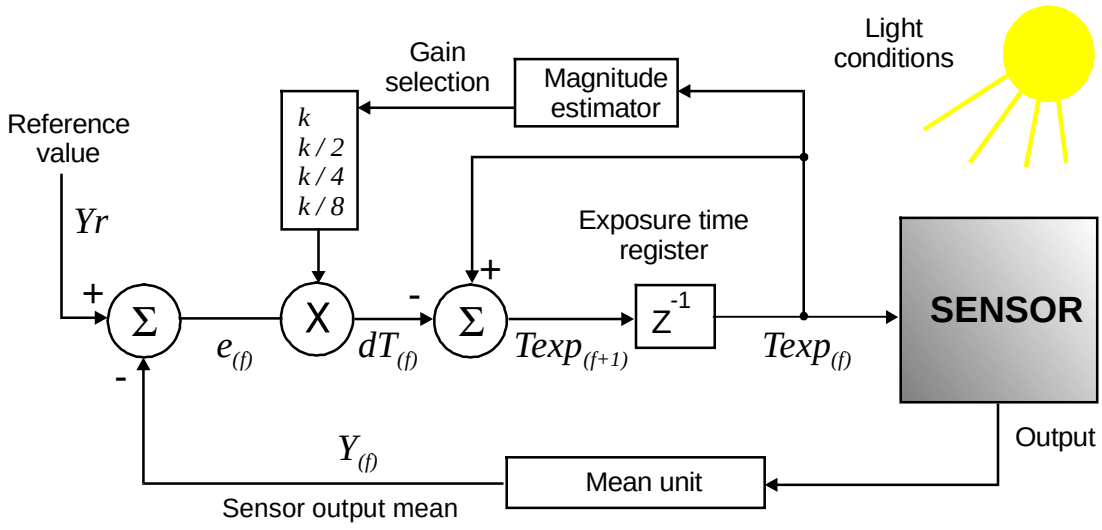


Figure 5-10: Exposure time controller principle.

After each frame acquisition, the mean value $Y_{(f)}$ of the current frame f is computed on a given number of pixels regularly distributed on the sensor array.

This mean value is compared to a programmable, reference image level *Yr*. The difference $e_{(f)}$ is multiplied by an adaptive gain *k* taking four different values depending on the magnitude of the exposure time $Texp_{(f)}$ used for exposing the present frame. This adaptive gain is useful for increasing the response speed of the regulator for long exposure times and avoiding oscillations for short values. Then, the product $e_{(f)} \cdot k$ gives the correction $dT_{(f)}$ that has to be applied on the exposure time for getting the exposure time $Texp_{(f+1)}$ used for the next frame f+1.

5.4 Interfaces

5.4.1 Control interface

An external control of the digital image sensor consists in reading and writing the circuit internal registers. For this, a serial link is sufficient and has the advantage of a low amount of pad and external connections. A synchronous, 3-wire slave interface is a simple and efficient solution and is retained. It consists in a clock line SCK and two data lines SDIN and SDOUT (input and output). It can be operated up to several MHz. The serial protocol consists in transmitting a frame of 16 bit containing a start bit, a read/write bit, the address (up to 6 bit) and the data (8 bit) (see Figure 5-11). At each rising edge of SCK, a bit is read on SDIN. In case of a read operation, the required data is returned on the output line SDOUT.

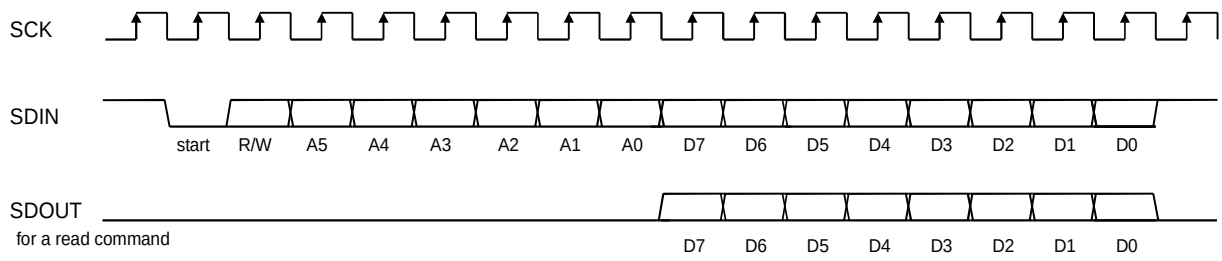


Figure 5-11: Signals of the 3-wire serial interface with 5 bit of address.

5.4.2 Data port

The image information represents a large amount of data and requires in most cases its own interface. A parallel port offers the advantage of the correlation in time between adjacent pixels, hence reducing the number of digital transitions.

Interface with an 8-bit data bus

At the system level, the digital image sensor can be directly connected to an 8-bit bus. A DMA controller with single address generation is required for transferring the pixel values directly into memory. Therefore, the sensor 8-bit data port requires tri-state output buffers.

5.4.3 Synchronisation signals

A certain number of synchronisation signals are necessary for triggering external logic when an image is read out. They were implemented for both analog and digital outputs.

- A horizontal synchronisation signal (HSYNC) indicating that a pixel row is being read out.
- A vertical synchronisation signal (VSYNC) indicating that a frame is being read out.
- A pixel clock (PCK), indicating on each rising edge that a data is valid on the data port. The pixel clock takes into account the reduced number of pixels in sub-sampling modes. It can either be continuous or present only if the HSYNC/VSYNC signals are active.

The timing of those signals is shown in Figure 5-12 for a non-continuous pixel clock.

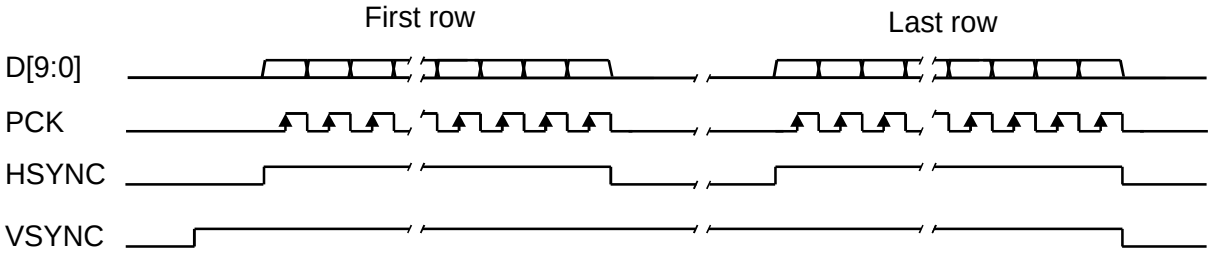


Figure 5-12: Timing diagram of the synchronisation signals.

Chapter 6
Realisations

The concepts and techniques developed in Chapters 2, 3, 4 and 5 were implemented and tested with two practical realisations of digital CMOS image sensors. Those realisations are the subject of this chapter.

For the two circuits, the same design procedure was applied. First, a general architectural approach, taking into account the specifications, as well as the main technological and practical limitations, was drawn. Then, the main blocks (sensor, ADCs, controller) were designed in parallel. Finally, all the components were carefully placed and routed in accordance with the architectural initial idea.

The sensor blocks of the two circuits (pixel array, row addressing logic, column readout logic and amplifiers, current references, voltage up-converters) were designed, realised and fully tested by the CSEM Image Sensing Group of Zürich. The essential practical contribution of this thesis is located in the design of the overall architecture, the remaining blocks (ADCs, controller) and in the place, route and verification operations, as well as the test of the final circuit.

6.1 First realisation: APS256D

For both design groups (CSEM and IMT), this circuit was the first experience of placing on the same chip a CMOS image sensor, an ADC and a dedicated controller. It was fabricated with the ALP1LV (1µm CMOS) technology from EM-Microelectronic Marin SA, Switzerland.

6.1.1 General specifications

Table 6-1 presents the general specifications of the circuit:

Parameter	Value
Technology	2-metal, 2-poly 1µm CMOS
Voltage supply range	2.7 to 3.3 Volt
Sensor resolution	256 x 256 pixels
Fill factor	> 30%
Pixel pitch	15 µm
Sensor dynamic	> 60 dB
Fixed Pattern Noise correction	No
ADC resolution	10 bit
Maximum pixel rate	4.2 MHz
Corresponding maximum frame rate	60 frame/s
Expected overall power consumption	10 mW
Exposure time control	on chip

Table 6-1: General specifications of the APS256D circuit.

6.1.2 Sensor

Pixel schematic diagram and operation modes

Due to the constraints of the technology and of the 15µm pixel pitch, the simplest three-transistor, n+ p-substrate photodiodes pixel structure was chosen (see Figure 2.4) for the best possible fill-factor. The operation modes of the pixel array were consequently reduced to the basic line shutter mode.

Pixel array addressing logic

A shift register combined to a 4-row decoder (see Figure 2-9 c) was retained for both reset and read row-addressing logic. This logic allows a sub-sampling addressing of one row over four (1/16-resolution of 64 x 64 pixels called "preview mode"). In the column direction, the columns were also selected by groups of four with a shift register.

Column amplifier and output buffer

The simple configuration of Figure 2-13 a) was chosen for the column amplifiers and output buffers, with a parallelism of four in the output lines (see Figure 6-1). This configuration does not allow any on-chip FPN correction, but has the advantage of a low-power consumption. The four output current sources (biased by Vp_{col}) can be switched on and off by signals /en1 and /en2. In Preview mode, only /en2 is active.

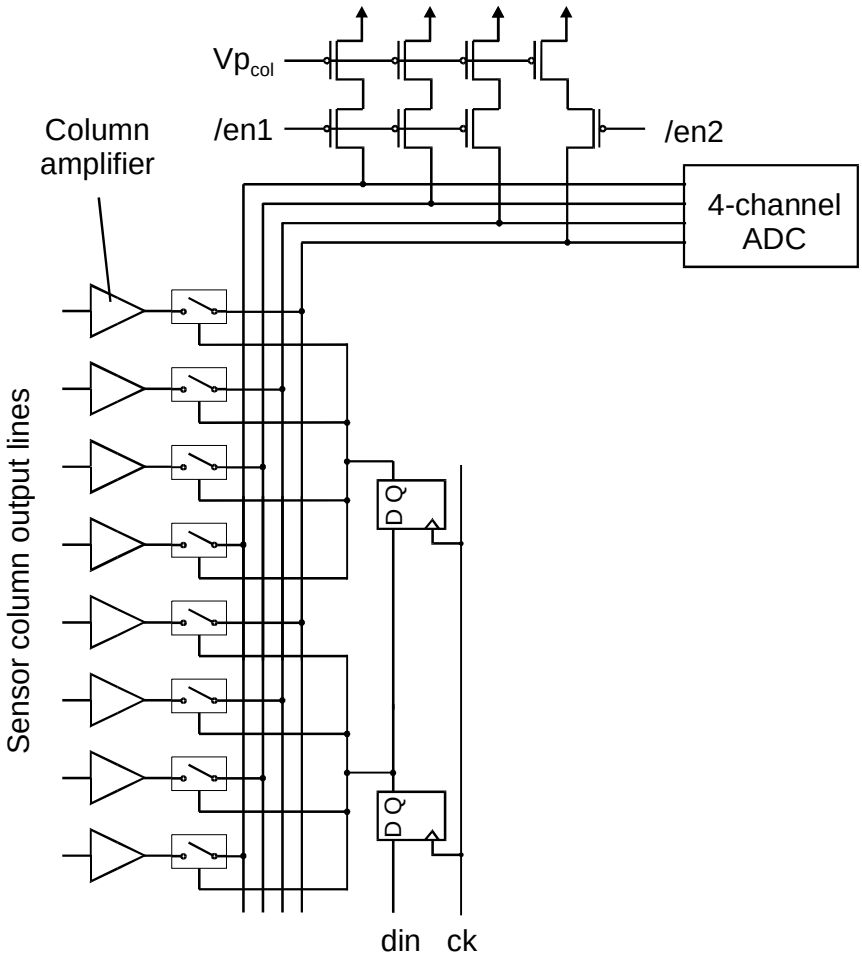


Figure 6-1: Readout architecture of the APS256D circuit.

Other sensor components

In order to increase the sensor output dynamic, the voltage applied to the gate of the pixel reset transistors was generated with an on-chip voltage multiplier (diodes and capacitors charge pump). The two bias voltages needed by the column and output buffer stages were also generated on-chip by a current reference.

6.1.3 ADC

The four-channel, 10-bit RSD pipeline ADC presented in sub-section 3.8.4 was implemented [Tann99]. Programmable current references as well as voltage generators for the comparators were also integrated on-chip.

6.1.4 On-chip controller

The on-chip controller is a full static synchronous state machine counting about 12600 transistors. It includes the following functions:

State machine for image acquisition

The most important function of the controller is the generation of all the control signals for the sensor and ADCs for the acquisition of images (in full resolution or preview mode). This corresponds to about 40 control signals.

Mean and saturation calculation

A set of 256 pixels homogeneously distributed on the image is used to compute a digital mean of the image. An other set of 4096 pixels are compared to a programmable threshold digital value and an automatic count of the values below the threshold is performed, giving the number of pixels in saturation of an image.

Offset and black level correction

Since the four-channel ADC may have two different offset values, and since the signal coming from the sensor is inverted and not referred to any black level, the pixels are inverted and their ADC offset and black level reference is corrected.

Exposure time controller

An exposure time controller based on the mean value of the image and on an adaptive proportional regulation loop enables an automatic control of the exposure time.

Serial interface and internal registers

All the functions of the on-chip controller are controlled via a bank of eight 10-bit registers. Those registers can be read and written externally via a three-wire serial synchronous interface.

6.1.5 Interfaces

Power supplies

Four different power supply pins are implemented for de-coupling and test reasons:

- Sensor power supply (analog and digital parts).
- ADC power supply (analog part).
- Logic power supply (controller, ADC digital part and padring).
- Digital output buffers power supply.

Data output port and synchronisation signals

The 10-bit pixel values are available on tri-state buffers. In order to indicate to external logic the presence of valid data, several synchronisation signals are generated by the controller and are available on output pads, as described in Chapter 5.

Control signals

The circuit is externally controlled through a few signals:

- Two input signals and one output for the three-wire synchronous serial interface.
- Two clock input signals: one for the main clock and one for the voltage multiplier.
- An active low hardware reset.
- A frame request input signal.

6.1.6 Circuit realisation

The core-limited circuit layout of the APS256D is shown in Figure 6-2. The dominant block is the sensor with related logic (reset addressing logic on the top, read addressing logic on the bottom and column amplifiers and other units on the right). On the top right of the circuit we have the ADCs and on the bottom right the controller (standard cells). Overall chip size is 6.4 x 4.8 mm, giving an area of 30.7 mm^2. The pads were placed on all four sides of the core in order to facilitate connections. The area occupied by the sensor, ADC, logic and pads are 61%, 8%, 6% and 15% respectively.

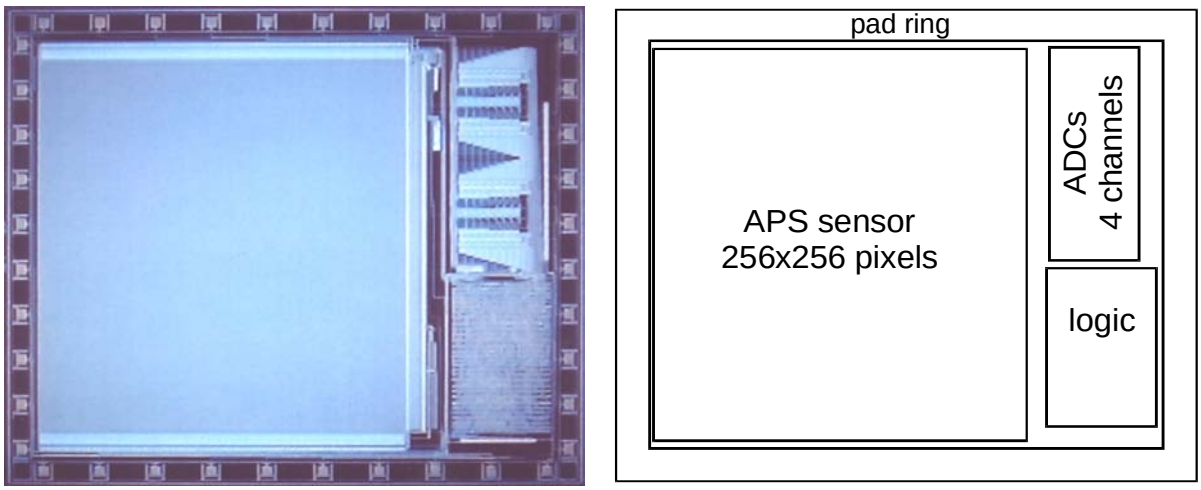


Figure 6-2: Photomicrography of the APS256D circuit (left) and floorplan (right).

6.2 APS256D: measurement results

6.2.1 Sensor characteristics

The main sensor parameters were measured by the CSEM-ZH team and are summarised in Table 6-2 [Blan99]:

Parameter	Value
Saturated output signal swing	1.2 Volt
Computed full well capacity	1'000'000 electrons
Conversion gain	1.5 µV/e
Fill factor	35%
Fixed Pattern Noise	8.5 mV rms
Noise floor	0.4 mV rms
Dynamic range	70 dB
Sensitivity @ 626nm [V/lux s]	0.84 V/lux·s
Dark current	150 mV/s

Table 6-2: APS256D sensor characteristics.

6.2.2 ADC characteristics

The test results of the ADC are presented in sub-section 3.8.5.

6.2.3 Power consumption

In full video-mode with a working frequency of 4MHz and a voltage supply of 3.0Volt, the current consumption of each block of the circuit is given in Table 6-3. The overall power consumption is 12.3 mW.

ADC	Sensor	Logic	Pads	TOTAL
1.4 mA	1.3 mA	0.6 mA	0.8 mA	4.1 mA

Table 6-3: Current consumption of the blocks of the APS256D.

6.2.4 Overall performance

Image quality

Figure 6-3: Two sample images taken with the APS256D. The image on the left was obtained with a test version of the chip with six different pixel areas.

The image cosmetic quality is good, but an important artifact has been reported: the image is split into two zones of different intensities. The location of the limit separating the two zones depends on the exposure time. The problem is due to a drop of the reset level when the readout phase occurs. The two zones have a level difference of about 10-15 mV, which represents 3-5 LSB.

Investigations were made in order to understand the reason of this voltage drop. It can be explained by the fact that, compared to the reset phase, an increase in current consumption exists during the readout phase. This increase is about 1.4mA (256 pixel current sources switched on + output buffers). For a drop of 10-15mV, the equivalent serial resistance is about 6-10 Ohm. The resistance of the power supply path is certainly responsible of this drop.

Overall Signal to Noise Ratio

A measurement was performed in order to evaluate the overall noise performance of the circuit. For this, the digital pixel-wise difference of several consecutive images, grabbed at constant illumination (50% of the dynamic) and constant exposure time, was computed. Then, the standard deviation of those pixels was computed and is expressed in mV rms in the last row of Table 6-4.

Noise	Remarks	Value
Sensor Electronic noise (noise floor)	Measured in analog mode in the dark with minimum exposure time.	0.4 mV rms
Photon shot noise	Calculated for an illumination of 50%.	1.06 mV rms
ADC related noise (including all ADC noise sources)	Based on the measured ADC SNR of 57 dB, with rail-to-rail input.	1.5 mV rms
Total estimated noise		1.87 mV rms
Total measured noise		2.1 mV rms

Table 6-4: Estimated and measured overall noise of the APS256D circuit.

The comparison between estimated and measured noise values give a difference in noise of about 1 mV rms. The origin of this supplementary noise can be imputed to the dark-current equivalent noise and to on-chip coupling noise. In particular, the presence of digital circuitry on the chip, especially the output buffers, may induce substrate noise.

Effects of parallelism on the overall performance

The readout architecture of the circuit (see Figure 6-1) does not include elements subject to significant offset variation. No column fixed pattern offset was measured. The ADCs, however, showed an inter-channel offset variation

corresponding to an SNR of 44.6dB (see paragraph 3.8.5). With digital offset calibration, this value can be increased to reach about 55dB.

6.3 Second realisation: VGACAM

6.3.1 General specifications

The circuit specifications are summarised in Table 6-5.

Parameter	Value
Technology	3-metal, 2-poly 0.5µm CMOS
Voltage supply range	2.7 to 3.3 Volt
Sensor resolution	648 x 488 pixels
Fill factor	> 30%
Pixel pitch	10.5 µm
Sensor dynamic	> 60 dB
Fixed Pattern Noise correction	Yes
Shutter type	line and global
ADC resolution	10 bit
Maximum pixel rate	10 MHz
Corresponding maximum frame rate	30 frame/s
Expected overall power consumption	50 mW at full speed
Exposure time control	on chip

Table 6-5: General specifications of the VGACAM circuit.

6.3.2 Sensor

Pixel schematic diagram and operation modes

The pixel schematic diagram is represented in Figure 6-4. Compared to the basic APS structure, it includes two more transistors. The first is the shutter (sh) transistor, whose function is to disconnect the photodiode from the source follower amplifier transistor gate (memory node) at the end of the exposure time. The second supplementary transistor is the "timer" (ti) transistor enabling the resetting of the photodiode independently from the memory node. The reset (rs) transistor is hence used for resetting the memory node.

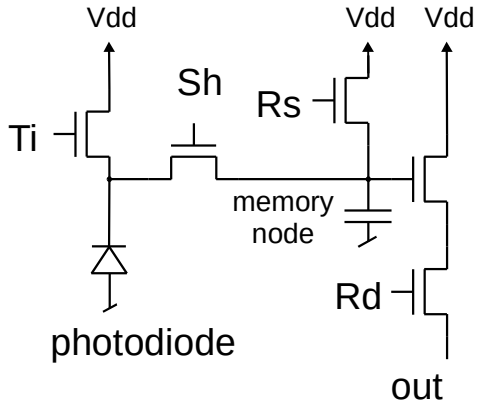


Figure 6-4: Schematic diagram of the VGACAM pixel.

The pixel can be operated in line shutter or global shutter mode, depending on the timing of the control signals. For the global shutter mode, the corresponding signals are given in Figure 6-5. In phase 0, the photodiode and memory nodes of all the pixels are reset. The exposition phase (1) begins when the photodiode node is released, and begins to integrate photo-generated charges. Then, at the end of phase 1, the memory nodes are released and a pulse is generated on all the shutter transistors (2), allowing charge transfer from the photodiode to the memory node. The exposure time stops with the end of phase 2. At this moment, all the pixel signals have been stored into the memory node, and the photodiode is not used any more and can consequently be reset. The memory nodes are then read out and reset row by row (phase 3) like in line shutter mode.

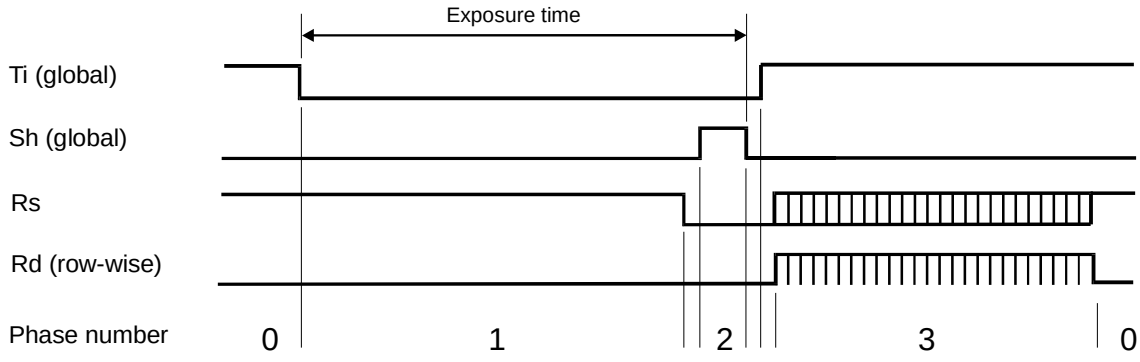


Figure 6-5: Timing diagram of the global shutter mode.

For the line shutter mode, the shutter and timer transistors are set to constant values of 1 (switched on) and 0 (switched off) respectively, and no global signal is used.

Row addressing logic

The logic for row reset and read addressing is schematically represented in Figure 6-6, where a basic block for the selection of four rows is represented, each of them having a reset (rs), a read (rd) and a shutter (sh) selection signal. This logic combines both global and row-wise addressing modes for the reset and the shutter transistors. Supplementary signals allow the selection of those two transistors during a read cycle (ena_rs_rd and ena_sh_rd respectively). This logic also allows sub-sampling addressing modes of factor 2 and 4.

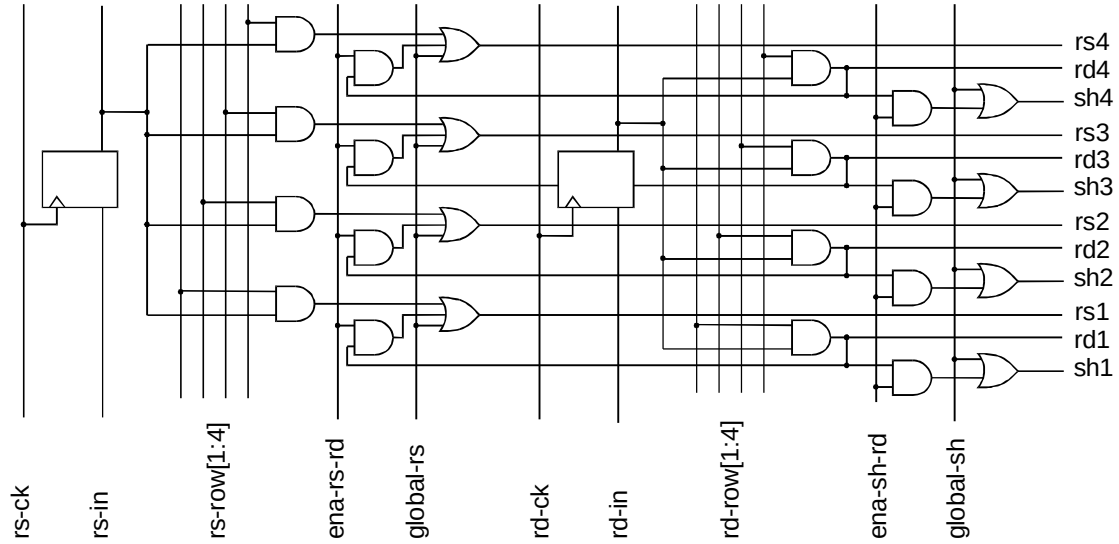


Figure 6-6: Row addressing logic of the VGACAM sensor.

Column addressing logic and FPN suppression stage

The output lines of the sensor are selected eight by eight by two blocks of four (Figure 6-7). For this, the column addressing logic includes a shift register with half of its flip-flops triggering on a first clock signal (col_ck_a) and the other half triggering on a second clock signal (col_ck_b) delayed by 180°. A special signal (sw_col_all) allows the selection of all the columns at the same time. The column signals are read out through FPN capacitors [Dier97] (one for each column) that perform storage of the signal value for the FPN suppression operation [Nix95]. When selected, those capacitors are connected to the output S-C amplifiers via eight analog output lines. Their charge is transferred into the feedback capacitors Cfb (of the same size than the FPN capacitor), and the pixel signals are available on the eight amplifier outputs.

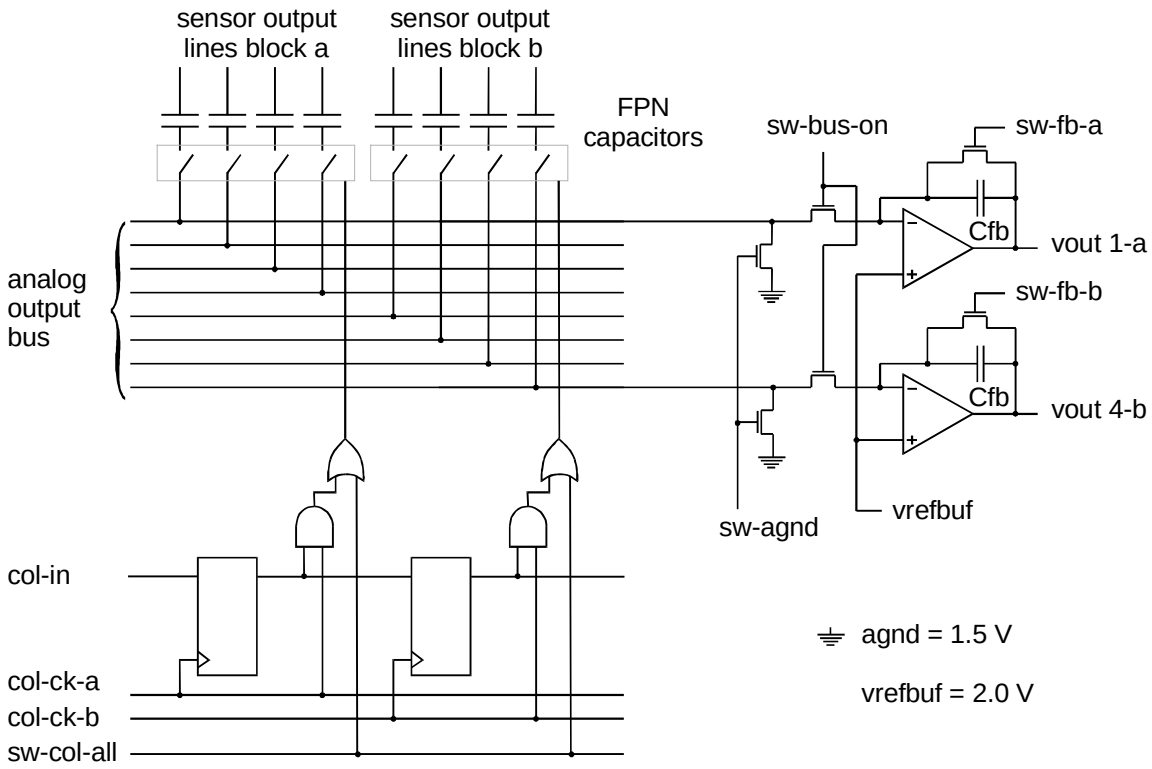


Figure 6-7: Column addressing logic with FPN stage and output buffer.

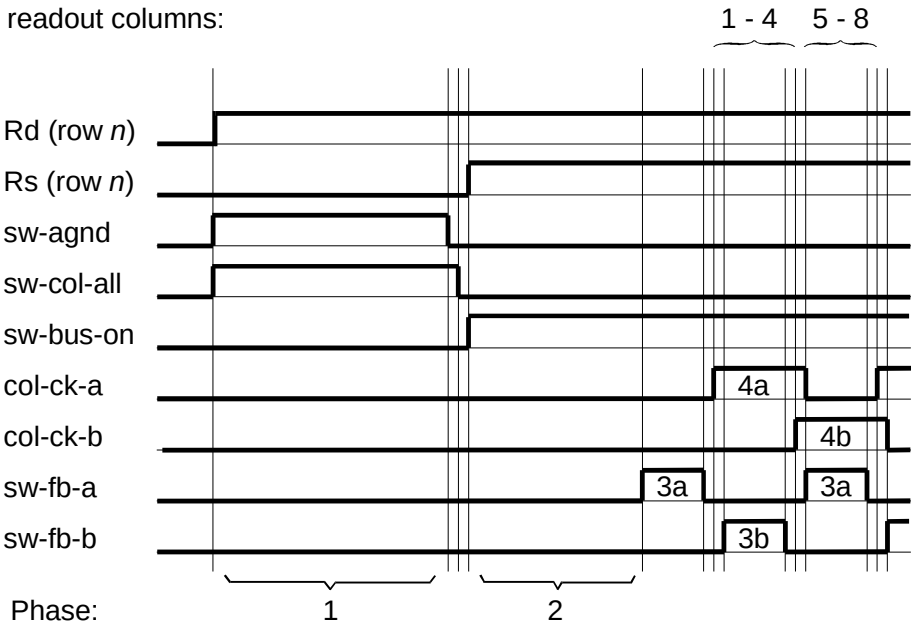


Figure 6-8: Timing diagram of a row readout operation with FPN suppression.

The row readout and FPN suppression timing diagram is represented in Figure 6-8. First, in phase 1, the row is selected (Rd signal), and the two signals sw_agnd and sw_col_all are active: the FPN capacitors are connected on one side to analog ground and in the other side to the pixel output voltages. At the end of phase 1, the capacitors are disconnected from analog ground and the stored charge into FPN capacitors is:

$$Q_1 = (V_{pix}) \cdot C_{FPN} \qquad \text{Equ. 6-1.}$$

During phase 2, the pixels are reset and the analog bus lines are connected to the amplifier inputs (signal sw_bus_on). Then, during phases 3, the feedback capacitors Cfb are reset; during phases 4, the columns are selected and the charge inside the FPN capacitors are transferred into the feedback capacitors. The output voltage is then given by:

$$Vout = \alpha \cdot (V_{pix} - V_{reset}) + \beta \cdot V_{refbuf} \qquad \text{Equ. 6-2.}$$

The difference between the pixel reset voltage V_{reset} and the pixel signal voltage V_{pix} has been performed and hence FPN suppression is realised. The offset voltage of the output is controlled with V_{refbuf}. Since the amplifier DC gain a is very high, the factors α and β can be approximated by:

$$\alpha = \frac{a \cdot C_{FPN}}{C_{fb} + C_{FPN} + C_x + a \cdot C_{fb}} \cong 1 \qquad \text{Equ. 6-3.}$$

$$\beta = \frac{a \cdot C_{fb} + a \cdot C_{FPN}}{C_{fb} + C_{FPN} + C_x + a \cdot C_{fb}} \cong 2 \qquad \text{Equ. 6-4.}$$

with C_x = parasitic capacitor of the analog bus lines.

6.3.3 ADC

The eight-channel, 10-bit RSD pipeline ADC presented in sub-section 3.8.6 are implemented with on-chip programmable current references.

6.3.4 On-chip controller

The on-chip controller includes nearly the same functions as the APS256D chip. 32 eight-bit registers are implemented, programmable via a 3-wire serial interface.

Logic for wafer test

A supplementary logic function was added to count the number of defective pixels of the sensor. This logic uses the saturation unit and sums, over the whole pixel array, the number of pixels whose output value exceeds a given level.

Output unit

The output unit performs several operations on the raw ADC codes:

- Black level and inter-channel offset correction.
- Image inversion.
- Down and up-clipping.
- Digital mean between two consecutive samples.
- Scaling with a constant coefficient for exploiting the full dynamic.

The implemented output unit is represented in Figure 6-9.

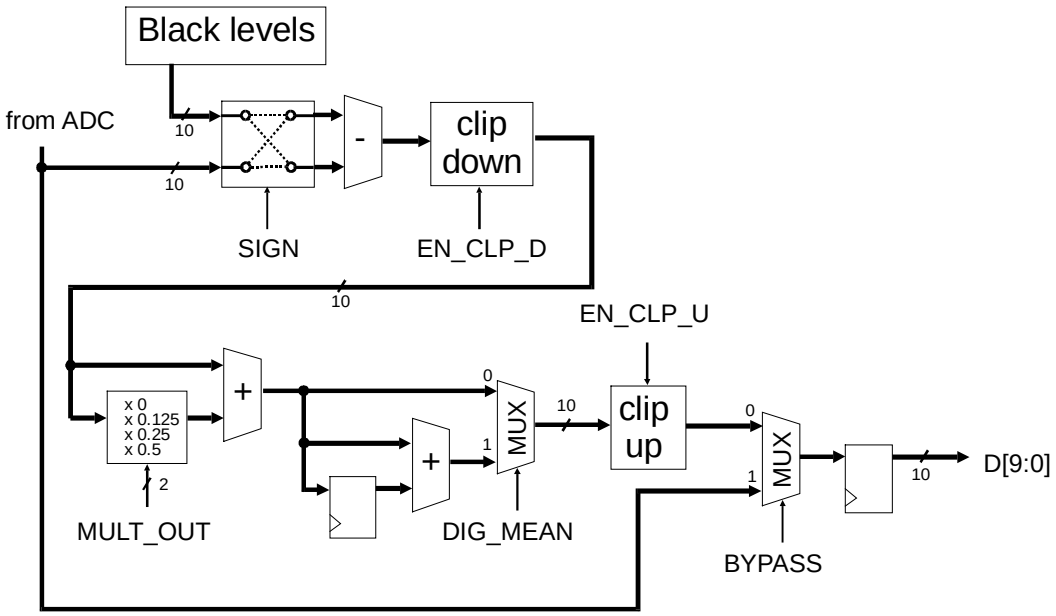


Figure 6-9: Output unit.

6.3.5 Interface

The interface signals of the VGACAM circuits are nearly the same as for the APS256D circuit (see sub-section 6.1.5).

6.3.6 Circuit realisation

The VGACAM floor plan is optimised for minimum die area and minimum die size in the vertical direction. For this, only two pad rows are used, one on the

left side and the other on the right side of the chip. The circuit photomicrography is shown in Figure 6-2. The sensor block occupies the left part of the chip, while the ADCs and the on-chip controller are located on the top-right and on the bottom-right respectively. Overall chip size is 9.28 x 5.94 mm, giving an area of 55.1 mm^2. The area occupied by the sensor, ADC, logic and pads represent 76%, 3%, 3% and 11% respectively. Routing channels occupy the remaining area (7%).

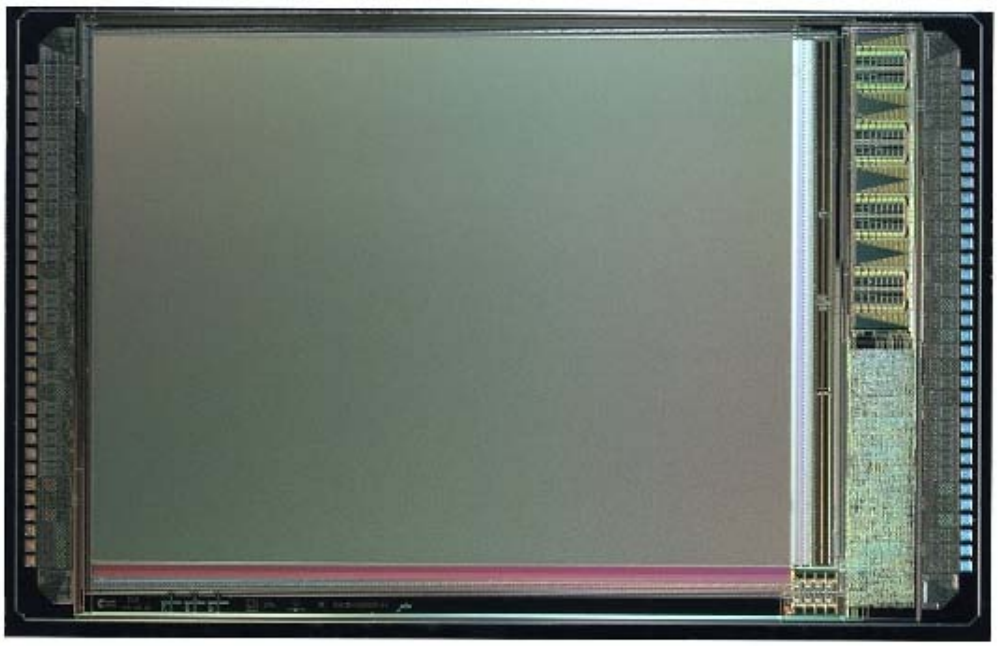


Figure 6-10: Photomicrography of the VGACAM circuit.

6.4 VGACAM: measurement results

6.4.1 Sensor characteristics

The main sensor parameters were measured by the CSEM-ZH team and are summarised in Table 6-6:

Parameter	Value
Saturated output signal swing	1.86 Volt
Computed full well capacity	266'000 electrons
Conversion gain	7 µV/e [23 fF]
Fill factor	32%
Fixed Pattern Noise	10 mV rms

Noise floor	< 1.6 mV rms
Dynamic range	> 60 dB
Sensitivity @ 626nm [V/lux s]	2.3 V/lux·s
Dark current	118 mV/s

Table 6-6: VGACAM sensor characteristics.

Those measurements show that the FPN suppression stage gives poorer results than expected, and that the on-chip electronic noise is important. However, the pixels are much more sensitive to light than for the APS256D.

6.4.2 ADC characteristics

All the experimental results of the ADC block are presented in Chapter 3.

6.4.3 Power consumption

Power consumption has been measured in full video-mode with a working frequency of 10 MHz and a voltage supply of 3.0 Volt. The current consumption of each block is given in Table 6-7.

ADC (analog)	ADC (digital)	Sensor (analog)	Sensor (digital)	Logic	Pads	TOTAL
3.3 mA	0.8 mA	10 mA	1.9 mA	0.72 mA	4.6 mA	21.3 mA

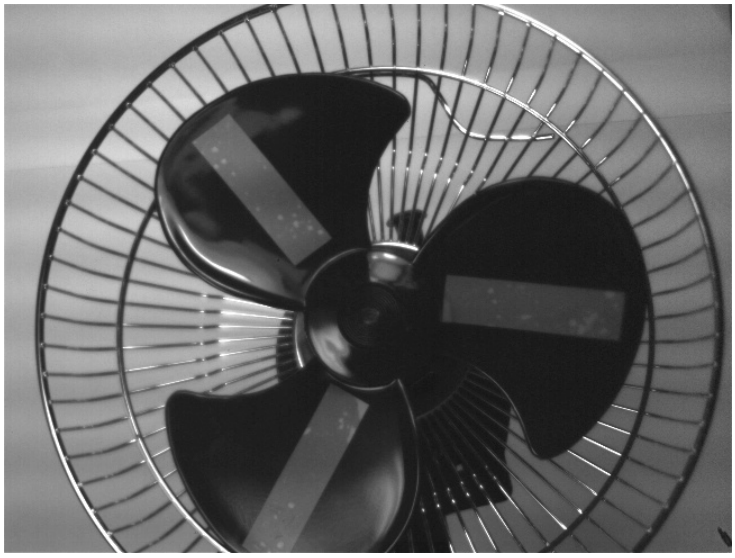
Table 6-7: Current consumption of the blocks of the VGACAM circuit.

The power consumption is higher than expected of about 28%. The reasons are:

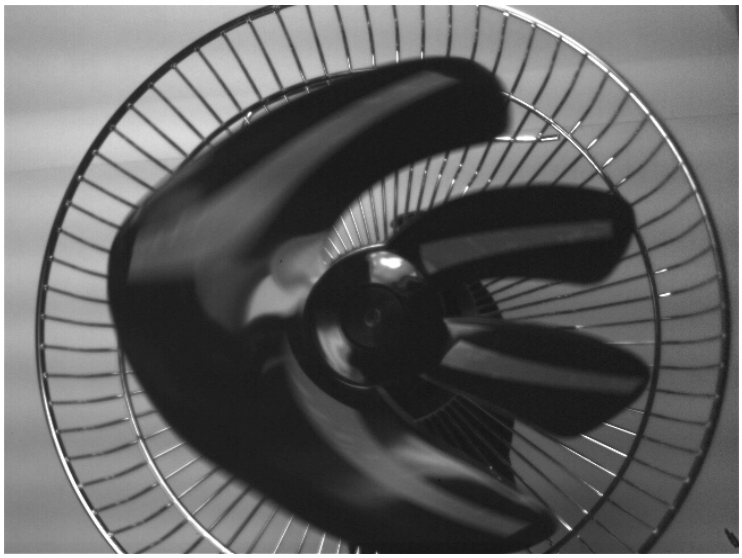
- An excessive current consumption of 1.2 mA in the charge pump block due to protection diodes in the pads.
- An excessive power consumption of about 2.6 mA in the digital output pad buffers.

6.4.4 Global shutter mode performance

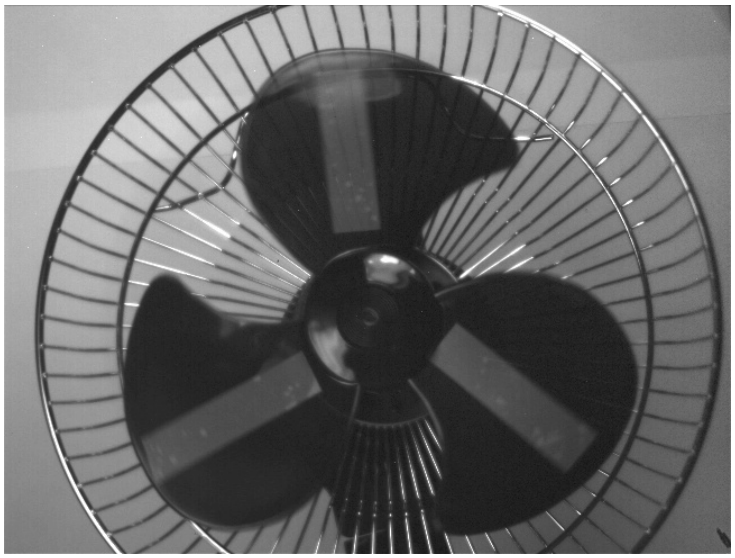
The global shutter mode was tested at a frequency of 4 MHz with the acquisition of a rotating fan. In Figure 6-11 a), the fan is immobile and has been captured with the line shutter mode. In b), the fan is spinning at about 200-300 rpm and was captured in line shutter mode (exposure time = 1 ms). The image is strongly distorted due to the important scanning time of 83 ms.



a)



b)



c)

Figure 6-11: Efficiency of the global shutter mode with a moving object.

In Figure 6-11 c), the fan was acquired in global shutter mode with identical exposure time and rotation speed than the picture b). No distortion is observed; the efficiency of the global shutter is demonstrated.

A closer look at the last image shows that:

- The image noise is stronger in global shutter than in line shutter mode; this could be due to charge injection fluctuation of the shutter transistor between the pixels.
- Many more white pixels (pixels with too strong leakage current) are observed. This shows the limits of the on-pixel memory node.

However, the behaviour of the in-pixel memory is remarkably good and allows the global shutter mode to be usable, even at a frequency of 4 MHz.

6.4.5 Image artefacts

An analysis of the image quality reveals some strongly visible artefacts and other less important ones. They are summarised below and the efficiency of the design measures to avoid them is discussed.

Variation of the reset voltage in line shutter mode

This effect (see paragraph 4.6.1) has been measured by acquiring a black image in line shutter mode where the readout cycle occurs approximately in the middle of the image (Figure 6-12). A voltage drop of about 4 LSB, corresponding to 25 mV, is observed.

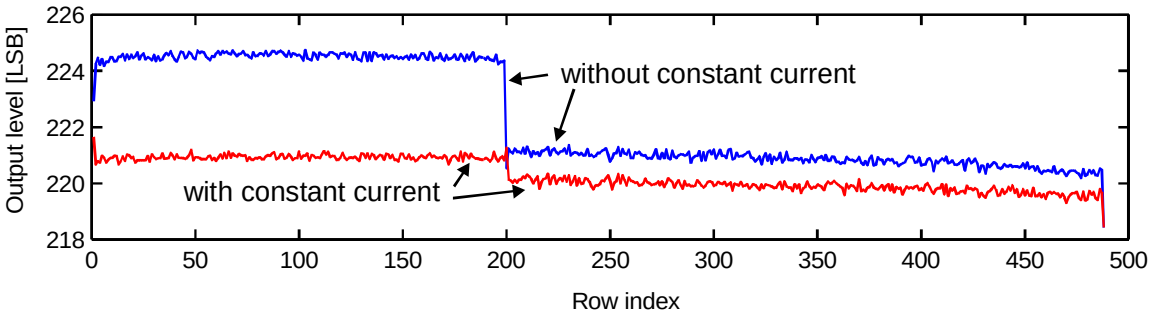


Figure 6-12: Reset voltage drop with and without constant current operation.

A mode allowing a constant current consumption for the sensor has been implemented and was switched on for the second curve of Figure 6-12. In this case, the voltage drop is reduced to 1 LSB (= 6 mV). The internal resistance of the sensor supply voltage has been indirectly measured and is about 20 ohm. It is responsible of the observed reset voltage drop occurring when the sensor current changes.

Effect of the digital output buffers on the image

The digital output buffers integrated into the pads are very power-consuming and their current consumption fluctuations cause artifacts in the image of two types:

First, in line shutter mode, the output buffers are active only during the readout phase, and the increase in current causes a drop in the sensor reset voltage for coupling reasons (substrate or power line coupling). This is proven by the fact that if the output buffers are forced to be active all the time, the reset voltage drop is decreased (Figure 6-13).

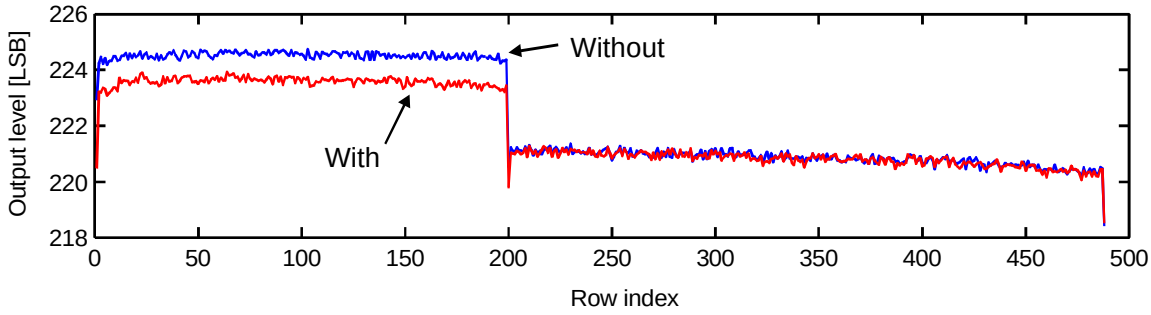


Figure 6-13: Reset voltage drop with and without constant output buffer activity.

Second, the switching activity variations of the output buffers between two consecutive rows cause transient regimes in the power supply voltages of the whole circuit. This directly affects the image level and causes a visible line in the column direction, as shown in the small image portion of Figure 6-14.

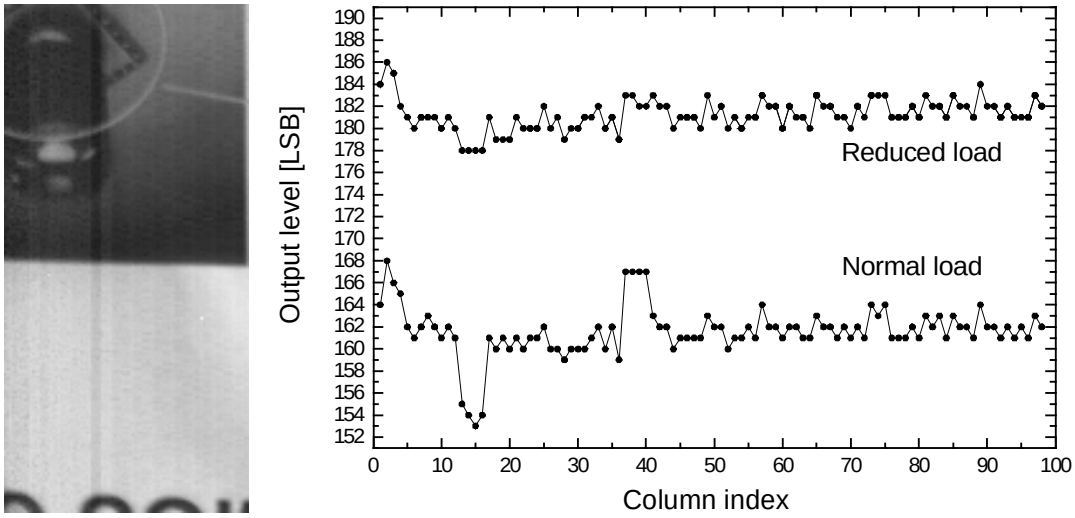


Figure 6-14: Image artefacts due to output buffers (left) are strongly reduced if the capacitive load of those buffers is reduced (right, courtesy of CSEM-Z).

These oscillations were decreased by:

- Reducing the output buffers capacitive load.
- Forcing the output buffers to switch continuously.

6.4.6 Sensor spatial frequency response

In order to evaluate the spatial frequency response of the sensor, a test pattern including high frequencies was acquired. The MTF for different frequencies was computed and the results are represented in Figure 6-15. Near the Nyquist frequency, the MTF is about 0.4 (loss of contrast of about 60%). Better results can be expected with the use of an infra-red filter.

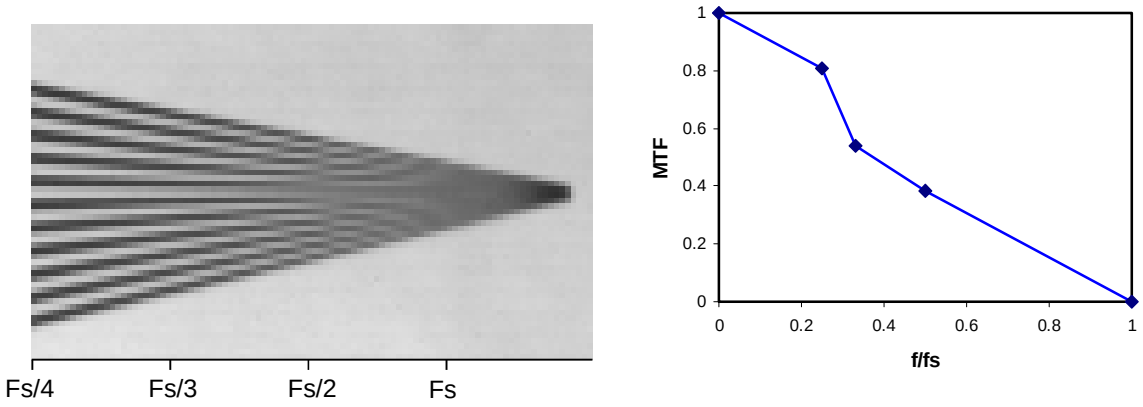


Figure 6-15: Test pattern of 100 x 60 pixels and corresponding MTF.

6.4.7 Sub-sampling modes

The voltage mode of the pixels does not allow to perform an analog mean between two pixels addressed at the same time. The obtained function is an analog "or" function.

Furthermore, due to a design error, one column over two was black in sub-sampling modes. It was then not possible to test the efficiency of the digital horizontal filtering (see sub-section 5.2.3). Figure 6-16 shows the comparison between an ideal sub-sampled image, obtained from filtering and decimation of a full-resolution image, and a sub-sampled image obtained with the sensor. This last image shows artefict effects, proving that no filtering function was operating.

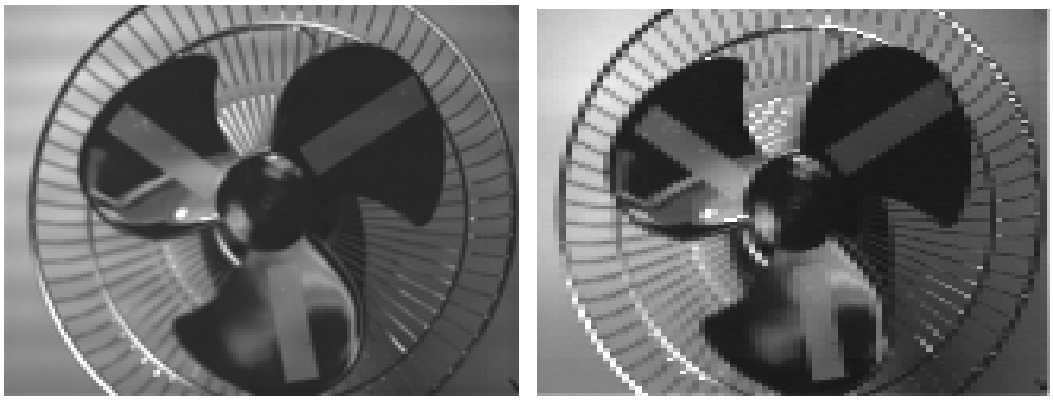


Figure 6-16: Sub-sampled images. Left: ideal sub-sampled image obtained from a full-resolution image. Right: raw image from the sensor.

6.4.8 Exposure controller

The exposure controller, based on the description of Section 5.3, was tested and is operating. In Figure 6-17 are represented the reference value, the image mean and the exposure time before and after image acquisition. Two strong changes in illumination were applied: an increased light after frame 7 and a decrease in light after frame 12. For both changes the controller adapted the exposure time in order to minimise the difference between image and reference levels.

No extended tests in video mode were performed and the dynamic behaviour of such a regulator (oscillations, stability) was not characterised.

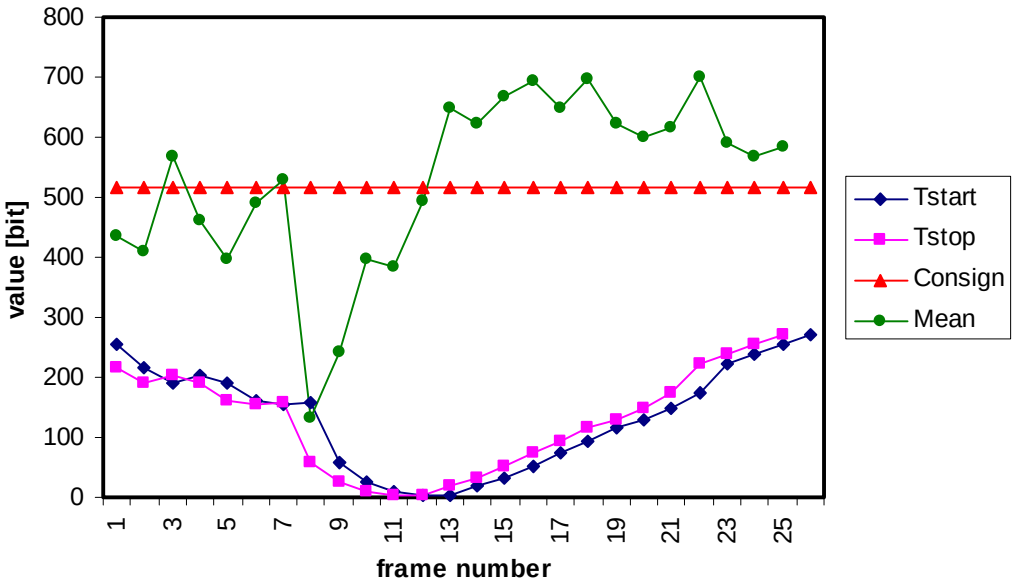


Figure 6-17: Qualitative behaviour of the exposure controller.

6.5 Realisations evaluation

The technical performances of the two realised circuits are compared with other digital CMOS image sensors (academics and industrials) in terms of power consumption, die size and overall SNR whenever available. Other points of comparison (image quality, sensor sensitivity, etc.) are more difficult to establish. Such a comparison should consider, in order to be valid, only circuits with relatively identical features. The chosen circuits are:

Academic realisations:

1. [Mans97]: a 1024 x 1024 sensor with 10-bit ADC.
2. [Deck98]: a 256 x 256 sensor with 10-bit ADC.
3. [Pain00]: a 512 x 512 sensor with 10-bit ADC.
4. [Yang99]: a 640 x 512 sensor with floating-point 8-bit pixel-level ADC.
5. [Cho00]: a 176 x 144 sensor with 8-bit ADC.

Industrial products:

6. CD5500 from STM Microelectronics (http://www.vvl.co.uk).
7. HDCS-2000 from Agilent (http://www.semiconductor.agilent.com).
8. PB720 from Photobit (http://www.photobit.com)

The comparison results are represented in Table 6-8, where the APS256D and VGACAM circuits appear under numbers 9 and 10 respectively.

Circuit No.	Overall power consumption [mW/MHz]	Supply voltage [V]	Sensor area [%]	Overall SNR [dB]	FOM (see below)
1	~20	3.0	65	~57	16.6
2	~25	3.0	40	56	8.1
3	~1.3	3.0	25	57.7	99.8
4	~1.5	3.0	55	< 45	148
5	~0.6	1.2	44	~42	44.3
6	~15	3.0	35	57	12.0
7	~30	3.0	~45	57.7	7.8
8	~5	5.0	32	55	88.0
9	2.9	3.0	48	56	**83.4**
10	5.25	3.0	64	55.4	**60.8**

Table 6-8: General comparison.

For this table, the value given for the sensor area is the ratio of the pixel array area over the chip area. The overall SNR is calculated from the ADC resolution, assuming that the sensor SNR is bigger. The overall power consumption includes digital output buffers, and was normalised with the pixel rate.

Factor of merit (FOM)

A factor of merit (FOM) was computed, taking into account the power consumption, the die area and the SNR:

$$FOM = \frac{Vdd^2}{Pcons_{norm}} \cdot A_{ratio} \cdot SNR \qquad \text{Equ. 6-5.}$$

Vdd is the supply voltage (in V). $Pcons_{norm}$ is the normalised power consumption. It is calculated by dividing the power consumption (in mW) with the corresponding pixel clock frequency (in MHz). A_{ratio} is the ratio of the sensing area (pixels) divided by the overall chip area. *SNR* is the signal-to-noise ratio (in dB).

Performance of the realised circuits in terms of power consumption

The two realised circuits show a good power budget compared to similar products in the industry and to equivalent academic circuits. However, some publications [Pain00], [Cho00] exhibit very low power consumption. In those circuits, the A/D conversion relies on charge-redistribution successive approximation ADC, featuring a power consumption of about 100-200 µW per Msample/s. Unfortunately, the corresponding die area of such converters is prohibitive compared to standard video ADCs.

In [Yang99], a pixel-level floating point ADC is implemented. This technique drastically reduces the power consumption, but the overall SNR is poor.

Performance in terms of die area

In the two realised circuits, the overhead in die area caused by the sensor addressing logic, the ADCs, the on-chip control and the pads remains small compared to industrial products or low-power academic realisations. This positive result is due to the chosen ADC conversion principle, which is relatively compact, at the expense of higher power consumption compared to a charge-redistribution successive approximation ADC.

Performance in terms of SNR

The SNR of the two realised circuits is comparable to all the other realisations. A 10-bit resolution is confirmed to be a standard in digital imagers.

References

[Blanc99]: N. Blanc, S. Lauxtermann, P. Seitz, S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, E. Doering, "Digital Low-Power Camera on a Chip", *Proc. of Int'l. COST254 Workshop on Intelligent Communication Technologies and Applications with Emphasis on Mobile Communications*, Neuchâtel, Switzerland, May 5-7, 1999, pp. 80-83.

[Cho00]: K. - B. Cho, A. Krymski, E. R. Fossum, "A 1.2V Micropower CMOS Active Pixel Image Sensor for Portable Applications", *2000 IEEE Int. Solid-State Circuits Conference*, San Francisco, February 7-10, 2000.

[Deck98]: S. Decker, R. D. McGrath, C. G. Sodini, "A 256 x 256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output", *IEEE J. Solid-State Circuits*, Vol. 33, No. 12, pp. 2081-2091, December 1998.

[Dier97]: B. Dierickx, G. Meynants, D. Scheffer, "Offset-Free Offset Correction for Active Pixel Sensors", *Proc. of IEEE Workshop on CCD and Advanced Image Sensors*, Bruge, Belgium, June 5-7, 1997.

[Mans97]: B. Mansoorian, G. Yang. E. Fossum, "Megapixel CMOS APS with Analog and Digital Readout", *Proc. of IEEE Workshop on CCD and Advanced Image Sensors*, Bruge, Belgium, June 5-7, 1997.

[Nix95]: R. H. Nixon, E.R. Fossum, "128 x 128 CMOS Photodiode-type Active Pixel Sensor with On-Chip Timing, Control and Signal Chain Electronic", *Proc. SPIE*, Vol. 2415, pp.117-123, 1995.

[Pain00]: B. Pain, G. Yang, C. Ho, "A Single-Chip Programmable Digital CMOS Imager with Enhanced Low-Light Detection Capability", *13th Int. Conf. on VLSI Design*, Calcutta, India, January 4-7, 2000.

[Tann99]: S. Tanner, A. Heubi, M. Ansorge, F. Pellandini, “A 10-bit Low-Power Dual-Channel ADC with Active Element Sharing”, Proc. ISIC99, Singapore, September 8-10, 1999, pp. 529-532.

[Yang99]: D. X. Yang, B. Fowler, H. Tian, "A 640 x 512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC", *IEEE J. Solid-State Circuits*, Vol. 34, No. 12, pp. 1821-1834, December 1999.

Chapter 7
Conclusion

The main objective of this work was the development of low-power architectures and building blocks for single-chip, low-power digital image sensors easily usable into a digital image acquisition micro-system. As a conclusion, we will first evaluate the realised work, having in mind the initial objectives, and we will then propose some possible investigations for further improvements.

The ADC block

The comparisons made regarding the performances of the developed ADCs (see section 3.9) show that their power consumption reaches the actual lower limit of today's main ADC families, which is about 1 nJ/sample.

Some ADC conversion principles consume less energy, like the charge-redistribution successive approximation ADC [Vale87], the charge-to-digital converter [Paul96] or some current-mode ADCs [Dong97]. Unfortunately, those techniques suffer from several drawbacks, like die area in [Pain00] or [Ols97]. However, they are showing the way for future realisations.

Another important factor is the supply voltage. Although most of the ADC conversion principles do not in appearance show an improvement in power consumption when the voltage supply drops below 2 Volt, some implementations allow it [Cho00]. A very low supply voltage should then not be discarded in order to further decrease the power consumption.

A factor of 10 in power consumption (corresponding to 0.1 nJ/sample) for the same performances in resolution might be achievable in a very near future.

Overall architecture

In this thesis, the emphasis on architecture was made on a medium parallelism approach on the sensor readout circuitry and ADCs. Furthermore, a distributed parallel approach was used (see Section 4.3), having two advantages. First, it allows the ADCs to be independent, in terms of geometric dimensions, of the pixel pitch. Second, it reduces power consumption in sub-sampling modes.

However, this architectural choice implies the use of two power-consuming elements:

- The first is the high capacitive charge of the analog output bus, connecting the column buffers to the output buffer. It forces to have column amplifier with important power consumption.
- The second is the output buffer itself, whose task is to drive the ADC input capacitance.

For those reasons, an approach using a massively parallel ADC architecture (one ADC for one, two or four pixel columns) might produce better results in terms of power consumption because in this case the long analog output bus and the output buffer are suppressed. The column amplifiers directly drive the ADC input capacity. Furthermore, the latter can be used advantageously for Double Sampling operation [Pain00], again reducing power consumption.

At the architectural level, other approaches can be investigated for lowering power consumption, like using in-pixel ADCs [Yang99]. In a general way, a huge gain in power consumption can be expected if the supply voltage is decreased. Recently, small sensors with a power consumption of a few tenths of micro-watt have been reported [Cho00], the reason for such a good result being the low supply voltage (1.2 Volt). Although getting quality images from a sensor working at 1.2 Volt is problematic, this direction has to be clearly investigated.

System integration

The two developed digital image sensors were and/or are on the way to being integrated into several micro-system prototypes. They proved to behave as expected. Very often, their power consumption is not the essential part of the system. This clearly shows that the low-power approach to imaging applications does not concern only the image sensor, but all the components of the system.

Digital signal buffering

A closer look at the power consumption contribution of each block of the two realised circuits shows that the digital output buffers consume a huge part of the overall power consumption. This contribution might even represent by far the biggest part in tomorrow's digital sensors [Cho00]. A solution to this problem

would be to reduce the amount of data to be transmitted to the external world by implementing on-chip data compression hardware. Another solution would be to work with reduced-dynamic logic levels, decreasing, incidentally, the required switching energy. Finally, other techniques might be developed, like chip-to-chip optical or magnetic transmissions.

On-Chip signal processing

Clearly, the approach followed in this thesis was to limit the on-chip signal processing hardware because the die area was important. However, for certain applications where die area is not critical, increasing the on-chip signal processing might result in lower power consumption at the system level. One then has to be aware that the optical properties of deep sub-micron technologies are for the moment not good enough for quality image sensor applications.

...And tomorrow?

The final limit in power consumption of a vision micro-system is fixed by the energy required for storing, displaying and/or transmitting the image content. If the system is designed to be autonomous, with a very small amount of transmitted data, then it is not difficult to imagine vision micro-systems requiring so little energy that they might be operating with the energy of the light they receive...

References

[Cho00]: K. - B. Cho, A. Krymski, E. R. Fossum, "A 1.2V Micropower CMOS Active Pixel Image Sensor for Portable Applications", *2000 IEEE Int. Solid-State Circuits Conference*, San Francisco, February 7-10, 2000.

[Dong97]: S. - C. Dong, B. S. Carlson, "10 Bit, 25MHz, 15mW CMOS Pipelined Subranging ADC", *Proc. IEEE Int. Symp. on Circuits and Systems*, June 9-12, 1997, Hong Kong, pp. 2024-2027.

[Ols97]: B. H. Olson, T. Shaw, E. R. Fossum, "A Single Chip CMOS APS Digital Camera", *Proc. of IEEE Workshop on CCD and Advanced Image Sensors*, Bruge, Belgium, June 5-7, 1997.

[Pain00]: B. Pain, G. Yang, C. Ho, "A Single-Chip Programmable Digital CMOS Imager with Enhanced Low-Light Detection Capability", *13th Int. Conf. on VLSI Design*, Calcutta, India, January 4-7, 2000.

[Paul96]: S. A. Paul and H. - S. Lee, "A 9-b Charge-to-Digital Converter for Integrated Image Sensors", *IEEE J. Solid-State Circuits*, Vol. 31, No. 12, pp. 1931-1938, December 1996.

[Vale87]: Vlado Valencic, "Convertisseurs A/N à approximations successives en technologie CMOS à capacités commutées", *Thèse No 708*, Ecole Polytechnique Fédérale de Lausanne, 1987.

[Yang99]: D. X. Yang, B. Fowler, H. Tian, "A 640 x 512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC", *IEEE J. Solid-State Circuits*, Vol. 34, No. 12, pp. 1821-1834, December 1999.

Acknowledgements

I would like to express my gratitude to my thesis supervisor, Professor Fausto Pellandini, for having given me, at my arrival at IMT, the opportunity to work in the very interesting field of image sensors. Despite my lack of experience in VLSI design in the beginning of this work, he fully trusted me. I also thank him for the very pleasant atmosphere and excellent conditions of work at IMT.

My warm thanks go secondly to my project leader and thesis expert Michael Ansorge, for his continuous support and availability during this work, and for his very constructive and enriching remarks. In particular, I thank him for the time he spent for reviewing my papers and the text of this report. I also thank him for his very positive and kind personality.

I would like to thank all my colleagues and ex-colleagues at IMT for the excellent work ambience and friendship we have been sharing together. Working at IMT was and is really a privilege, firstly because all of you. I would in particular thank Alexandre Heubi, whose strong experience initiated me to the world of mixed IC design when I arrived at IMT.

My thanks go to all the team of CSEM – Zürich for the excellent collaboration we had during the design of the circuits presented in this report. In particular, I would like to thank Nicolas Blanc, Stefan Lauxtermann, Martin Waeny and Michel Willemin. It was a real pleasure to work with you. I thank also Professor Peter Seitz for having taken the time to co-examine my work.

Many thanks go also to Professor Roland Siegwart (EPFL) and Doctor Joachim Grupp (Asulab) for their work of examination and their interest in this work.

I thank the industrial partners of the MINAST Microcam project and their respective representative (EM Microelectronics Marin SA, Asulab SA, Siemens-Cerberus SA) for the good collaboration and constructive attitude during the whole project.

The English content of this report has been kindly revised and corrected by Mrs. Georgina Cretegny. Thank you very much for your help and availability!

Finally, I would like to thank my family for their encouragement regarding my work, and my wife Martina for her continuous support and tireless attention towards my technical problems, questions and reflections.

Biography

Steve Tanner was born on July 10th, 1972 in Orbe, Switzerland. He received his Microtechnology engineer degree from the Swiss Federal Institute of Technology – Lausanne (EPFL) in March 1996. He then joined the Institute of Microtechnology (IMT) of the University of Neuchâtel in April 1996, where he was involve in the VLSI design of low-power imaging acquisition and processing devices. In September 2000, he defended successfully his PhD thesis in the domain of low-power digital image sensors.

Annex

Transfer function of a switched-capacitor ADC stage: general approach

Let us consider the general schematic diagram of a switched capacitor stage, made of capacitors *C1* to *Cn*, switches, analog voltages *V1* to *Vn*, common parasitic capacitor *Cp* and an amplifier with DC gain *a*, and offset *Voff*.

We can basically decompose the stage operation into two distinct phases:

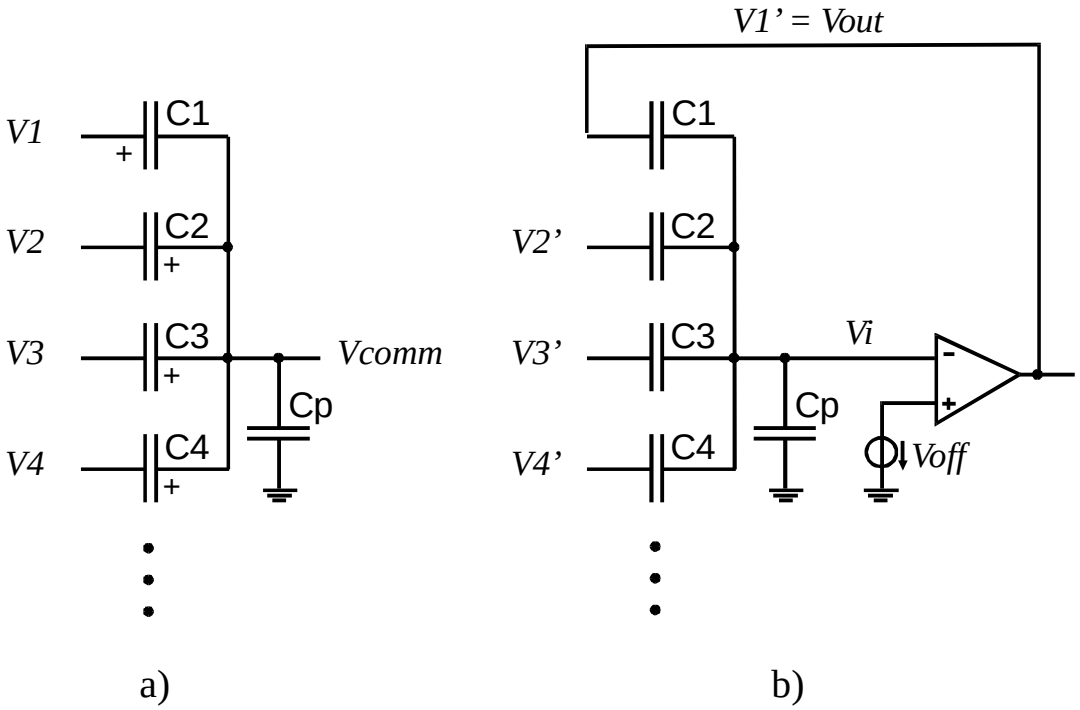


Figure A-1: a) Phase 1 and b) phase 2 of a switched capacitor ADC stage.

- Phase 1: sampling. The different capacitors *Cj* (*j* = 1 .. *n*) are connected on one side to analog voltages *Vj* (input or reference voltages), and on the other

side to a common voltage *Vcomm*. During this phase, the amplifier may be either unused, or used to generate a given voltage needed by the algorithm.

- Phase 2: amplification. The common capacitor plate is connected to the amplifier input *Vi* (floating node), and the other plates are connected to analog voltages *Vj'*. One capacitor (*C1*) is connected to the amplifier output and becomes the feedback capacitor. The capacitor charges are transferred so that the node *Vi* becomes a "virtual ground". The amplifier output voltage changes accordingly.

At the end of phase 1, the charges inside the capacitors are:

$$Q1 = C1 \cdot (V1 - Vcomm)$$ For the feedback capacitor Equ. A-1

$$Qj = Cj \cdot (Vcomm - Vj)$$ For the other capacitors Equ. A-2

During phase 2, the amplifier is connected and thus:

$$Vout = a \cdot (Voff - Vi)$$ Equ. A-3

where *a* is the amplifier DC gain and *Voff* is the amplifier offset.
The voltage *Vi* can be expressed as:

$$Vi = \frac{Q}{C} = \frac{\left(\sum_{j=2}^{n} Qj \right) + Qinj + \Delta Q}{\sum_{j=2}^{n} Cj}$$ Equ. A-4

where *Qinj* represents the switch injection charge (supposed constant), *n* is the number of capacitors and *ΔQ* represents the charge transferred to the feedback capacitor. If the voltages *Vj* are changing of ΔVj during phase 2 (they should be grounded otherwise), *Vi* becomes:

$$Vi = \frac{Q}{C} = \frac{\left(\sum_{j=2}^{n} Qj \right| + Qinj + \Delta Q + \left(\sum_{j=2}^{n} Cj \cdot \Delta Vj \right)}{\sum_{j=2}^{n} Cj} \qquad \text{Equ. A-5}$$

The output voltage is:

$$Vout = Vi + (V1 - Vcomm) + {\Delta Q}/{C1} \qquad \text{Equ. A-6}$$

From Equ. A-2 and A-5, we have:

$$\Delta Q = Vi \cdot \left(\sum_{j=2}^{n} Cj \right| - Qinj - \left(\sum_{j=2}^{n} Cj \cdot (Vcomm - Vj') \right| - \left(\sum_{j=2}^{n} Cj \cdot \Delta Vj \right) \qquad \text{Equ. A-7}$$

And, by using Equ. 6 and Equ. 7, we obtain *Vi*:

$$Vi = \frac{C1 \cdot (Vout - V1 + Vcomm) + Qinj + \left(\sum_{k=2}^{n} Ck \cdot (Vcomm - Vj) \right| + \left(\sum_{k=2}^{n} Ck \cdot \Delta Vj \right)}{\sum_{k=1}^{n} Cj} \qquad \text{Equ. A-8}$$

If Equ. A-8 is introduced into Equ. 3, we get:

$$Vout = \left(\frac{a \cdot \Sigma C}{a \cdot C1 + \Sigma C} \right) \cdot Voff + \left(\frac{a \cdot C1}{a \cdot C1 + \Sigma C} \right) \cdot V_Q - \left(\frac{a}{a \cdot C1 + \Sigma C} \right) \cdot Qinj - \left(\frac{a}{a \cdot C1 + \Sigma C} \right) \cdot \sum_{k=2}^{n} Ck \cdot (Vcomm - Vj) - \left(\frac{a}{a \cdot C1 + \Sigma C} \right) \cdot \sum_{k=2}^{n} Ck \cdot \Delta Vj \qquad \text{Equ. A-9}$$

where ΣC represents the sum of all the capacitors (including parasitic capacitor *Cp*), and V_Q represents the voltage across capacitor *C1* at the end of phase 1.

Example 1: cyclic RSD converter from [Heub96]

This cyclic RSD converter has the following characteristics:

- Three identical capacitors *C1*, *C2* and *Cr*, *C1* being the feedback capacitor.
- During phase 1, *C1* is used with the amplifier as a hold function of the previous analog result, and the common capacitor plate is grounded (*Vcomm = 0*).
- The feedback capacitor is reset during phase 1 of the first cycle, then is used as an integration capacitor in the next cycles.

If we assume that *a* is high, we obtain the following output voltage after the first conversion cycle (each conversion cycle being composed of phases 1 and 2).

$$Vout_1 = \left(\frac{a}{a + 3 + Cp/C1} \right) \cdot \left[Vin \cdot \left(\frac{C2}{C1} \right) + \frac{Qinj}{C1} \right] + 3 \cdot Voff \qquad \text{Equ. A-10}$$

And for the next cycles ($i > 1$), by taking into account the feedback capacitor charge:

$$Vout_i = \left(\frac{a}{a + 3 + Cp/C1} \right) \cdot \left[\left(\frac{C2}{C1} + \frac{a+1}{a} \right) \cdot Vout_{i-1} + D_{i-1} \cdot \left(\frac{Cr}{C1} \right) \cdot Vref \right] \qquad \text{Equ. A-11}$$
$$+ 2 \cdot Voff + Vinj$$

where *Vinj* is the constant voltage generated by *Qinj*, *i* is the current cycle number, D_{i-1} is the digital decision of the previous cycle, and *Vref* is the reference voltage.

Example 2: pipelined RSD stage with offset cancellation

This stage has the following characteristics:

- Three identical capacitors *C1*, *C2* and *Cr*.
- During the phase 1 of each conversion cycle, the amplifier is used to generate its own offset voltage. This voltage is supplied on *Vcomm*.
- Both *C1* and *C2* are charged with $Vout_{k-1}$ (output voltage of the previous pipeline stage) during phase 1.

We obtain, from Equ. A-9, the following output voltage for the stage *k*:

$$
\begin{aligned}
Vout_k = & \left(\frac{a \cdot 3C}{a \cdot C1 + 3C + Cp} \right) \cdot Voff \\
& + \left(\frac{a \cdot C1}{a \cdot C1 + 3C + Cp} \right) \cdot (Vout_{k-1} - Voff) - \\
& \left(\frac{a}{a \cdot C1 + 3C + Cp} \right) \cdot Qinj \\
& - \left(\frac{a}{a \cdot C1 + 3C + Cp} \right) \cdot (C2 \cdot (Voff - Vout_{k-1}) + \\
& Cr \cdot (Voff - D_{k-1} \cdot Vref) + D_{k-1} \cdot Cr \cdot Vref) - \\
& \left(\frac{a}{a \cdot C1 + 3C + Cp} \right) \cdot \left(\overline{D}_{k-1} \cdot Cr \cdot Vref \right)
\end{aligned}
\qquad \text{Equ. A-12}
$$

After simplification, we get:

$$
Vout_k = \left(\frac{a}{a + 3 + Cp/C1} \right) \cdot \left[\left(\frac{C1 + C2}{C1} \right) \cdot Vout_{k-1} + D_{k-1} \cdot \left(\frac{Cr}{C1} \right) \cdot Vref \right] + Vinj \qquad \text{Equ. A-13}
$$

where *Vinj* is the constant voltage generated by *Qinj*, D_{k-1} is the digital decision of the previous stage, and *Vref* is the reference voltage.