# MEMS-based Mirror Array for Astronomical Instrumentation

Thèse présenté à la Faculté des Sciences
Institut de Microtechnique (IMT)
Université de Neuchâtel
Pour l'obtention du grade de
*Docteur ès Sciences*

par

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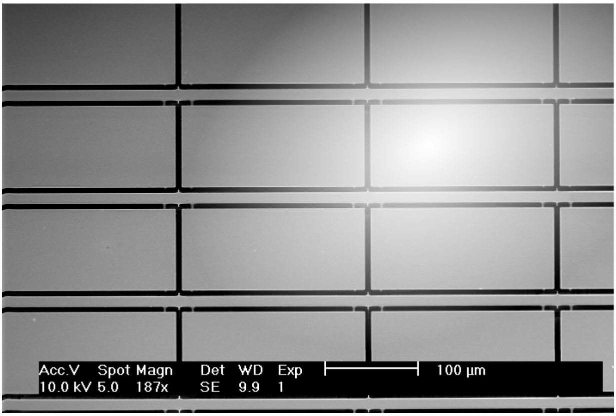

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Soutenue le 6 mai 2010

É. 6

Université de Neuchâtel

**FACULTE DES SCIENCES**
**Secrétariat-Décanat de la faculté**
- Rue Emile-Argand 11
- CP 158
- CH-2009 Neuchâtel

# IMPRIMATUR POUR LA THESE

## MEMS-based mirror array for astronomical instrumentation

## Severin WALDIS

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# MEMS-based Mirror Array for Astronomical Instrumentation

Dissertation submitted to the Faculty of Sciences of
the University of Neuchâtel, in fulfilment of the
requirements for the degree of
"*Docteur ès Sciences*"

by

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2010

Dedicated to Michèle

*Sans rime ni raison, remettre toujours tout en question,*
*douter meme en reve!*
E. M. Cioran

# Abstract

**Keywords** MEMS, MMA, micro-mirror array, astronomical instrumentation, multiobject spectroscopy, MOS, SOI, large tilt-angle, uniform tilt-angle, cryogenic operation, flat mirror

The NASA's and ESA's James Webb Space telescope program, the development of the European Extremly Large Telescope (E-ELT) and the European Cosmic Vision program bring into fashion what astronomy always wanted to do, explaining where we are coming from by studying the formation of the galaxies and their evolution. Two requirements become a necessity: multiplexing and high spatial resolution capabilities. Thanks to its multiplexing capabilities, Multi-Object Spectroscopy (MOS) is becoming the central method to study large numbers of objects by recording simultaneously hundreds of spectra and utilizing a target selection mechanism in the field of view.

Micro-electromechanical systems (MEMS) where identified by the major global astronomical and space societies as high-potential candidates for the use as reconfigurable target selection masks in future MOS: they are lightweight, remote-configurable, versatile and have the potential to be operated in cryogenic environment. Within the scope of this thesis the corner stones for a new class of MEMS mirror arrays (MMA) for the use in future MOS has been laid. The main requirements are: large tilt-angles of $\geq 20°$, feed-forward tilt-angle uniformity, large micromirrors of $100 \times 200 \mu\text{m}^2$ with a surface quality better than $\lambda/20$ and operation in cryogenic environment.

The device concept, conceived to tackle these challenges, include a two-chip architecture required to accommodate the large tilt-angle and mirror size. The micromirrors are made from $10\mu$m-thick bulk single crystalline silicon to provide maximum flatness. The micromirrors are suspended with polysilicon cantilever beams located on the mirror backside. A system of

landing and stopper beams has been implemented, which, together with intermediate supporting beams for uniform spacing between mirror and electrode, aimed to provide feed-forward tilt-angle uniformity over large arrays. The individual chips were fabricated utilizing a combination of bulk- and surface micromachining. An assembly scheme for mirror and electrode chip, allowing passive alignment with an accuracy of $\pm 5\mu$m, has been developed and demonstrated.

The mirrors of fabricated 5×5 arrays showed to have an excellent surface quality, with a peak-to-valley deformation of 35nm for gold-coated mirrors at room temperature and 50nm for gold-coated mirrors at cryogenic temperatures (100K). Electromechanical characterization showed micromirrors yielding a tilt-angle of 20° at an actuation voltage below 90V. The tilt-angle in ON-state was stable within 3arcmin over a voltage range of more than 10V, demonstrating the stopper and landing beam concept. Successful operation of the micromirror array *in vacuo* and cryogenic environment at temperatures below 100K has been showed and a preliminary demonstration of the object selection capabilities of the fabricated micromirrors has been carried out.

# Contents

# Chapter 1

# Introduction

## 1.1 Motivation and Background

“The Universe, yours to discover” was the theme of the International Year of Astronomy (IYA) 2009, launched by the International Astronomical Union (IAU)[1] and the United Nations Educational, Scientific and Cultural Organization (UNESCO)[2]. The IYA aimed to promote one of the oldest science and sensitize people to the beauty and necessity of the modern art of star-gazing. Not only in 2009, but probably since the dawn of religion and philosophy, two central questions related to astronomy preoccupy mankind: where are we coming from and, even more thrilling—is somebody else out there in space?

The scientific contribution of the astronomers to above questions is the quest for exo-planets or extra-solar planets and the study of the formation of the universe. One of the principal methods for studying the evolution of the universe is measuring the red-shift (allowing to determine the age) and the composition of very large numbers of remote (early) galaxies. This kind of research requires to analyze very distant and faint objects and probing very large fields of view and many objects.

Several transnational research and development programs are set-up to develop a new generation of telescopes and instruments that address these challenges. The James Webb Space Telescope (JWST) is a multinational program between NASA, the European Space Agency (ESA) and Canadian

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[1] http://www.iau.org/

[2] http://www.unesco.org

Space Agency (CSA), scheduled to be launched in 2014. The JWST is conceived to "examine every phase of cosmic history: from the first luminous glows after the Big Bang to the formation of galaxies, stars, and planets to the evolution of our own solar system"[3]. A prominent example of a ground-based telescope is the development of the European Extremely Large Telescope (E-ELT). The E-ELT is projected to have a huge primary mirror with a 40m-diameter, enabling the astronomers to look very far. One of the science cases is the research for extra-solar planets: according to ESO, "discovering and characterizing planets and proto-planetary systems around other stars will be one of the most important and exciting aspects of the E-ELT science programme"[4]. Another program, ESA's EUCLID, a space-based telescope to be launched in 2017, is conceived under the theme "How did the Universe originate and what is it made of?" [5].

The advent of these new and very sophisticated telescopes and associate instrumentation require the development of powerful subcomponents that enable the full use of the overall system. A common challenge is how to efficiently handle the incoming light, i.e. how to make the best out of the available information that is projected in the focal plane of the telescope. In particular the research of the origins of the universe relies on taking large samples of spectral data (red-shift surveys and composition of galaxies). One candidate that is commonly used for this kind of task is the Multi-object Spectrograph (MOS), enabling recording of many spectra in parallel. The performance of a MOS relies on how efficient objects in the focal plane of the telescope can be selected. The typical size of very distant galaxies is 0.1–0.5 arcsec[6]; depending on the plate-scale[7] of the telescope, this translates to a size of some tens to hundreds of micrometers in the focal plane.

An ideal class of candidates for manipulating light at the micron scale are optical micro-electro-mechanical systems (optical MEMS, also referred to as OMEMS or MOEMS). MEMS represent a device family that integrate optical and mechanical elements, actuators and sometimes sensors and electronics on one substrate. MEMS are fabricated on silicon substrates, using fabrication technologies that are based on semiconductor manufactur-

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[3] http://www.jwst.nasa.gov

[4] http://www.eso.org/sci/facilities/eelt

[5] http://sci.esa.int/euclid

[6] This is the angle under which the object is seen on the sky. As comparison, the moon is seen under an angle of about 30arcmin.

[7] The plate-scale is the projection of the angular size of the astronomical object on the telescope focal plane; for instance a plate scale of 1"/mm signifies that an object of 0.1 arcsec has a diameter of $100\mu$m in the focal plane

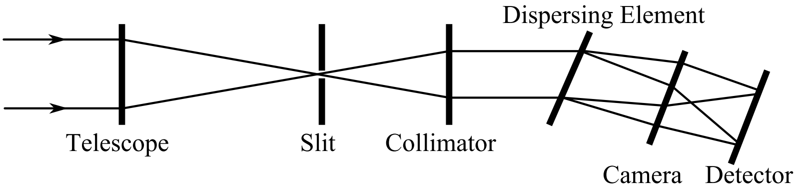

Figure 1.1: Schematic drawing of an astronomical slit spectrograph.

ing technology; typical fabrication steps include material deposition, photolithography and etching.

To address the particular challenge related to the efficient use of the focal planes in future telescopes a joint research activity (JRA) within the European Framework Program 6 was dedicated to the development of so-called smart focal planes: "Smart Focal Planes maximise the use of a telescope's focal plane to feed spectroscopic and imaging instruments" [12]. Within this JRA Optical MEMS was identified as potential key technology for the implementation of a smart focal plane for MOS. The Laboratoire d'Astrophysique de Marseille (LAM), part of the OPTICON consortium, initiated a collaboration with the Institute of Microtechnology (IMT) and laid the foundations for the subject of the present dissertation: The development of a MEMS-mirror array class that is suited for the use in future large-scale infrared MOS.

In this chapter the basics and state of the art of multiobject spectroscopy (Sec. 1.2), optical MEMS (Sec. 1.3) and MEMS-based MOS (Sec. 1.4) are given. The chapter concludes with the need and motivation for the development of a MMA-platform for future MOS and the scope of the present dissertation (Sec. 1.4.5).

## 1.2 Multiobject Spectroscopy

It is hardly contested that the astronomical spectrograph, besides the telescope itself, is the instrument that provided the most of new astronomical knowledge. Spectroscopic surveys provide an abundance of information on celestial objects, including their

- chemical composition and their abundance,
- temperature,

Table 1.1: Science cases and required resolving power of the spectrograph (Source [22])

| Resolving power | Science Case |
|---|---|
| $R = 500$ | Finding emission line objects (survey work)<br>Red shifts of faint galaxies |
| $R = 1000$ | Measuring red-shifts in faint quasars |
| $R = 2500$ | Stellar spectral classifications<br>Measuring line profiles of galaxies |
| $R = 10000$ | Measuring line profiles in broad line stars |
| $R = 25000$ | Element abundance analysis for a range of elements in solar type stars |
| $R = 100000$ | Very fine interstellar lines with multiple components to be resolved |

- radial velocity and
- distance.

The very first experience spectroscopic experience was carried out by Newton in the second half of the 17th century when he observed the spectrum of the sunlight. His spectrograph consisted of a pupil (a hole in the windows shutters), a prism and a wall 22ft away from the prism. Based on this very simple experience, which can be regarded as the fundamental starting point for the science of spectroscopy, he concluded that there is a relationship between refrangibility and color (of light), i.e. wavelength. It was Young in 1801 who first used a diffraction grating to demonstrate the wave nature of light; he made the observation that the wavelength can be obtained through the spacing of the grooves and found that the sines of the diffraction orders increased in accordance with the integers 1,2,3... Fraunhofer continued the experiments with gratings since 1820 and confirmed the law of diffraction orders $\sin\beta \propto m$. He used diffraction gratings to determine the wavelength of certain emission lines, that he used as wavelength standards; together with the law on refraction of Snell-Descartes he was able to establish a relationship between refractive index and wavelength (dispersion). This he used to systematically characterize the refractive index of different glasses of the Benediktbeuern glass works in Bavaria [22].

While Newton can be considered as spectrograph pioneer, the work of Young and Fraunhofer laid the foundation for the (quantitative!) science of spectroscopy. Using a prism in front of a theodolite telescope Fraunhofer recorded several hundreds of absorption lines of the solar spectrum and in 1823, using a larger telescope, he recorded the absorption lines of several bright stars and planets—the science of spectroscopy in astronomy was born[8] [ibidem].

In Fig. 1.1 a schematic of a basic astronomical spectrograph is shown; it consists of the telescope, an entrance slit, a dispersing element, a collimator, a camera and a detector onto which the entrance slit is imaged. Whereas in earlier times the prism was the preferred dispersing element, nowadays blazed gratings or also grisms, a combination of a prism and a grating, are preferably used as dispersing elements. The figure of merit of a spectrograph is determined by two quantities: the throughput and the spectral resolving power (or spectral resolution) $R$. The throughput is the fraction of source optical power that arrives on the detector, i.e. can be considered as measure for the efficiency of the system. The resolving power $R = \lambda/\Delta\lambda$ depicts the smallest wavelength difference that can be resolved. For a infinitesimal small slit $R$ is diffraction limited, in practice however the slit is always oversized in order to allow more source light to arrive on the detector—hence the resolving power is slit-limited. The required resolving power depends on the science case that the astronomer wants to pursue with the spectrograph; some exemplary science cases and the corresponding required resolving power are given in Tab. 1.1.

The above definition of the throughput refers to the light of one source; the light (in a single slit spectrograph) of all the other celestial objects is blocked, or, to express it a little bit more dramatically, wasted. Multiobject spectroscopy (MOS) is nowadays the answer to this problem—the following example illustrates the impressive advance in scientific efficiency utilizing multiobject spectroscopy (MOS): In 1912 Slipher at the Lowell Observatory carried out the first systematic red-shift survey. He recorded the red-shift of 25 celestial objects, for each one requiring three to six nights of observation time [36]. In contrast, 90 years later though, the spectra of 1546 much fainter objects were recorded in one single night. This observation was part of the 2dF Galaxy Redshift Survey at the Anglo-Australian Telescope (AAT) [9]. Whereas there were major advancements in the detector sensitivity (Slipher's photo-plate had a responsive quantum efficiency

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[8] Though it was only in 1858 when Kirchhoff found the true meaning of the absorption lines.

RQE of about 1%, nowadays state-of-the-art CCD's RQEs are in the 80%) and optical system throughput, the striking difference lies in the multiplexing: Slipher observed one object at a time, while the 2dF MOS was able to record the spectra of 400 objects simultaneously!

The first implementations of a MOS was the objective prism. Introduced in 1885 (at Harvard) this technique was the only means for multiobject spectroscopy for almost one century. The shortcomings of this method is overlap of spectra for densely spaced objects and sky background and a variable resolving power[9]; further, given such a slit-less configuration, the resolving power is generally very low, typically a few hundreds and sometimes even less. The sky background decreases signal to noise ratio and therefore the sensitivity. Consequently the objective prism is only suited when density of objects is low and no large resolving power, nor high sensitivity is required.

To overcome these limitations, a MOS must be able to operate in slit-mode for each observed source. In 1980 two different approaches for a multi-slit MOS were implemented. The first was the so-called aperture plate MOS. Here, instead of a single slit, a plate with many slits was introduced in the focal plane of the telescope, such that the light of the objects of interest pass through the slit mask and the rest of the light is blocked. The light that passes through the aperture plate is then, like in a classical slit spectrograph, dispersed and imaged on a detector. The second approach was to use optical fibers to pick off the light of the objects of interest from the focal plane. The simplest approach was to plug optical fibers in the aperture plate; the fibers where then used to guide the light to the spectrograph; herein lies the big advantage of a fiber-based MOS: the objects (fibers) can be arranged such that the use of the detector surface is optimum. The disadvantage are the increased system complexity (and effort required to setup the mask!) and the somewhat more involved sky background subtraction—this in contrast to the aperture plate MOS, where the sky background subtraction is straightforward through the use of long slits (rather than short slits).

The shortcomings of both approaches lies in the long preparation time that precedes an observation: First, in imaging mode, the distribution of the objects in the focal plane must be recorded; then the aperture plates or fiber assemblies must be fabricated and installed. This requires a large logistic effort and long preparation time. In order to overcome this drawbacks, several automatic reconfiguration mechanisms, for both aperture plate and fiber-based MOS, were developed. An aperture plate MOS with automatic punch plate system and plate exchanger mechanism was installed at the

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[9] In such a configuration the resolving power depends on the seeing $\theta*$ of the telescope.

Cassegrain Focus Grism Spectrograph of the Canada-France-Hawaii telescope (CFHT). Here the total time between CCD readout of the object position and installment of the punched plate was only ten minutes [22].

The 2dF fiber-based MOS, that was utilized to carry out AAT's red-shift survey mentioned above, is an example of a remote-reconfigurable robotic fiber placement system [9] (and references herein). It was conceived in the late-1980s and entered service at the AAT in 1997. The 2dF automatic fiber positioning system consists of a ferromagnetic base plate and 400 fibers terminated with a 90° microprism. A magnetic button underneath the microprism allows clamping it on to the ferromagnetic base plate in the focal plane of the telescope, having a diameter of 440mm; a robotic gripper system allows positioning of the individual field pick-off units at the desired positions within an accuracy of $20\mu$m. The positioning of one fiber took around six seconds; in order to avoid long wait times during reconfiguration, the system consists of two field plates: one of them can be reconfigured while observations are taking place with the other. The field plate exchange is done automatically with a robotic tumbler-mechanism.

Another approach of a multi-fiber positioning system was pursued with Echidna [7], a development of the Anglo-Australian Observatory (AAO), commissioned in 2004. The Echidna, named after the Australian mammal with movable spines on its back, is a 400-fiber multi-actuator system, in which every individual fiber is allocated a limited field-of-view in which it can be positioned within $10\mu$m accuracy. The fiber consists of a rigid part (spine); one end of the spine points to the focal plane, the other end sits on a piezo-electric actuator, allowing to tilt the spine so that the fiber tip can be placed within a patrol area of 7mm in the focal plane. The individual fiber spines are packed in a hexagonal pattern with 7mm centers. The Echidna approach has the advantage of being modular and scalable; as only one object within one 14mm-diameter fiber cell can be addressed, the Echidna instrument is best suited for observations where the density of objects is low.

A different approach of parallel spectroscopy is the so called integral field unit (IFU). Here, instead of selecting several individual objects over the field, the IFU provides the complete, position-resolved spectral information over a certain portion of the field of view. In a IFU the field needs to be subdivided into small portions (image slicer) that then are rearranged onto a linear slit and dispersed onto a detector. In one implementation the IFU consists of an array of closely packed fibers in the focal plane; this is in principle a fiber-MOS where all the fibers are concentrated in a certain region of the focal plane [38]. In order to get near-100% of fill-factor an array of quadratic micro-lenses focuses the light into the fibers. The IFU is best suited for assessing extended objects whose spatial structure is of interest, while slit-MOS performs best for point-like sources widely distributed over the field. Note that an IFU typically covers only a small field-of-view and in order to get a 3D spectroscopic map of large field-of-views, many pointings are required. Further, sky substraction is difficult in a IFU, whereas it is straightforward in a slit-MOS.

All of the above cited advanced MOS were and are utilized for the visible wavelength range. Astronomers demand now MOS with the same functionality and versatility for near-infrared (NIR) surveys and for space telescopes [18]. In terms of science the main driver for NIR MOS are large scale red-shift surveys for the exploration of the earliest periods of galaxy formation; here the spectrum of interest lies in the range from 0.6 $\mu$m to 5$\mu$m. Within this range thermal radiation of the instrument is a problem and hence, the components of a NIR MOS need to be cooled down to cryogenic temperatures. A new class of MOS that emerges from above drivers must therefore be light-weight, remote-reconfigurable and able to operate at cryogenic temperatures.

In terms of telescopes programs there are three main drivers for the development of new MOS instruments. First of all there is the James Webb Space Telescope (JWST). Given the evident need for lightweight, compact, reliable and remotely configurable components on a space mission, this program was pioneering in development of MEMS-based MOS slit-mask. The JWST and its MEMS-MOS development is further discussed in Sec. 1.4. Another important driver for the development of new instruments is the European Extremely Large Telescope (E-ELT). Initially conceived as an "overwhelming" large telescope (OWL) with a primary mirror diameter of 100m, it is now designed to feature a still extremely large primary mirror with a diameter of 42m and is scheduled for first light in 2018[10]. Given the massive effort and investment required to set up such a huge telescope, it is paramount that one makes the best out of the light that arrives in its focal plane. With a projected size of the focal plane of $0.5 \times 0.5\text{m}^2$ sampling of the focal plane is required for spectroscopy and even for imaging. With this perspective a Joint Research Activity (JRA5) under the European Framework Six OPTICON program (FP6)[11] was set up with the focus on so-called smart focal planes [11]. Smart focal planes aims to maximize the use of the focal plane, acting as smart link between the telescope and spectroscopic

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[10] http://www.eso.org/sci/facilities/eelt/

[11] http://www.astro-opticon.org/fp6-index.html

as well as imaging instruments. The developments of the JRA5 comprised amongst other [12] (and references herein):

- Replicated image slicers to enable more economic production of multiple IFUs
- "Starbugs"–miniature robots that carry fibres or pick-off mirrors to any given place in the focal plane, potentially at cryogenic temperatures.
- "Starpicker"–an alternative cryogenic, robotic positioner to place pick-off mirrors on a potentially curved, dual focal-plane that is tumbled into its observing position.
- Micro-mirror arrays fabricated in silicon that can be used to form multi-object slitlets with high densities of objects,

the latter development being the subject of the present thesis (see Sec. 1.4.5).

Another recent program that considers employing a MEMS-based slit-generator for a near-infrared MOS is ESA's EUCLID space telescope, set up within ESA's Cosmic Vision program [48] (see also Sec. 1.4).

Whereas MEMS seems to be a high-potential candidate for a new breed of slit generator for MOS, an example of a macro-mechanical alternative shall be mentioned: the mechanical slit generator conceived at CSEM, initially developed as fall-back option for the JWST NIRSPEC, continued to be developed within the Smart Focal Plane JRA5, now commissioned for the MOSFIRE instrument at Keck Telescope [39]. The slit-generator consists of several sliding bars (that can be remote-controlled) with a fixed width, allowing positioning 46 slits within a field of view of 267×267mm$^2$.

## 1.3 Optical MEMS

Micro-electro-mechanical systems (MEMS) first came up in the 80s and can be considered nowadays as an established technology. Prominent applications of MEMS are accelerometers in cars and in hand-held devices; optical MEMS are used in optical networks [56] and in projection devices—the optical MEMS flagship being the DMD of TI[12] [24, 25, 17].

An optical MEMS consists of an optical element that is attached to an actuator or electromechanical transducer, that allow to move ("actuate") the optical element in one or more degrees of freedom. The optical element may

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[12] http://www.ti.com

be a micro-mirror, grating, lens or a shutter; the most common transducer is based on electrostatic actuation, where the attractive electrostatic force between two charged capacitor elements is utilized. Other actuators use electromagnetic, piezo-electric or thermal forces [20].

One of the most appealing characteristic of MEMS is their fabrication process based on microelectronic manufacturing technologies. This has two major qualities: fist the devices are fabricated in batch mode, i.e. hundreds or thousands devices at the same time, and second, mechanical, optical, electrical and even electronic, features can be integrated on one substrate, yielding highly integrated multi-functional devices. A typical MEMS-fabrication scheme is based on adding material, photolithographic structuring and chemical or chemical-physical etching. The standard substrate that is used for manufacturing are single silicon wafers or silicon-on-insulator wafers, where two, or sometimes even more, silicon layer are stacked, separated by a silicon dioxide layer. The latter is commonly used for a so-called bulk-micromachining process, where structural elements are manufactured by deep-etching of bulk silicon—in contrast to the surface micromachining technology, where the structural layer consists of a previously deposited (thin) film material.

Whereas there is a class of devices, and corresponding applications, that consist of a single actuated element, the most of the MEMS-potential is exploited when it comes to arrays of actuated elements. Thanks to the microlithography-based fabrication process it is literally the same to integrate one or several hundreds or thousands of active elements within a device[13].

As prominent example for a single optical element device shall be mentioned the optical scanner. Here the optical device consists of a mirror element, typically a few millimeters in diameter that is suspended via a spring element to the device substrate. An actuation mechanism allows to tilt the mirror around one (1D-scanner) or around two (2D-scanner) axis. One example for a electrostatic driven 2D scanner is the one from Milanović et al. [41]. Here the actuator consists of so-called comb-drives that are arranged around a central gimbal. Electromagnetic actuation is employed in Microvision's two-axis resonant MEMS scanner [54] (and references herein). The device consists of gimballed mirror and a planar coil around the gimbal frame that interacts with an external magnetic field. By choosing the proper orientation of the external magnetic field and an excitation that corresponds

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[13] Addressing and driving of a large number of elements might not be straight-forward though; this is discussed further below.

to the resonance frequencies to the two axis, both axis can be driven in resonance with a single coil. MEMS scanner are commonly used for display applications, bar-code readers or imaging [53].

Other single-element optical MEMS-devices include scanning grating [46], which can be employed for selecting wavelengths, optical switch [35], used in optical circuits, and 2D in-plane positioners [47] for active alignment of optical components. A review on SOI-based optical MEMS may be found in [43].

Within the device family of arrays of optical elements the largest part makes out the micro-mirror array (MMA) devices; there are also arrays of actuatable gratings [5] for display applications and arrays of microshutters [29]; the microshutter array is visited in more detail in the next section, as it was conceived for the use in a multiobject spectrograph. Whereas typically the mirrors are segmented there are also continuous mirror membrane devices, such as Boston Micromachines' deformable mirror (DM); here an array of up to 4096 actuators is employed to deform a thin silicon layer [10].

The MMA devices family can be further subdivided according their functionality; there are MMAs that feature mirrors which can be tilted to two distinct positions (ON and OFF) [24] and such that allow tilting the mirrors analogously within a certain range; tilting can be around one axis [21] or two axis [2]. There are even MMAs that offer tilting around two axis and piston movement for each individual mirror, for instance irisAO's device [23].

MMAs are used for display applications [17], adaptive optics (AO) [23, 6, 10], mask less lithography [55, 21] and many niche applications. An example for MEMS used in astronomical AO is the Gemini Planet Finder[14], equipped with a Boston Micromachines deformable MEMS-mirror [6] and scheduled for first light in 2011.

A common challenge to all large MMA devices is the addressing of the individual mirrors. All mentioned MMAs utilize electrostatic actuation, requiring high drive voltages (20V and up). For a small number of elements the straight-forward approach is direct wiring of the individual actuators (electrodes) to an electronic driver component outside the MEMS. In-plane connection lines, typically on the same substrate or functional layers as the actuation electrodes, are utilized to connect the individual elements to the chip edges, from where wire-bonds can be employed as connection to the external driver electronics. As the in-plane wiring density is limited, with the approach of direct in-plane wiring typically only several tens to a few hundreds of active elements can be addressed. Using surface micromachining

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[14] http://planetimager.org

and several signal layers, this number can be increased to a few hundreds to thousands, such as in Boston Micromachines' DM [10]; for an even higher actuator count the use of through-silicon vias is proposed [15].

State of the art devices with a very high mirror count are built on a CMOS substrate, which seems to be the only practical way for handling very large numbers of actuatable elements (10k and up) at reasonable frame rates (1kHz and up)[15]. In the case of a digital mirror device the addressing and driving electronics are relatively simple, in principle it consists of one matrix-addressed switch (transistor) per mirror (or two in the case of TI's DMD as each mirror has two active states). The Fraunhofer institute IPMS employs a kind of analog DRAM CMOS substrate for their single degree of freedom analog MMAs; as example should be cited their 240×200 array of piston-type micro-mirrors; to each mirror, within a range of 400nm, an 8bit-resolved piston offset can be attributed [19]. Here a unit cell consists of a matrix addressed switch and capacitor, which is utilized to store the analog drive voltage (up to 30V). 48 analog channels are multiplexed over the 48000 mirrors (i.e. 1000 mirrors per analog channel) and are operated at a frequency of 1MHz each; therefore the voltage/charge of any cell is refreshed at 1kHz. IMEC's 11 million mirror array [21] features a similar driving approach.

The accuracy/stability of the analog DRAM driving scheme yields is limited by the voltage drop in between two refresh cycles; the voltage drop being dependent on the leakage current (that tends to discharge the storage capacitor) and the refresh rate. Put simply, in order to increase the accuracy by one bit, the number of analog channels must be doubled (assuming that the DACs operate at their maximum frequency); here the limiting factor at some point is the available footprint and wiring density. Another effects that limit accuracy/stability is clock feed-through.

The die size of the above cited large MMAs (large in terms of the number of mirrors) is in the range of 10mm to 20mm, IMEC's very large MMA measuring even $22\times46\text{mm}^2$. The typical mirror sizes that are employed range from $10\mu$m to $40\mu$m and the corresponding tilt-angle (measured from the neutral position) is around 10° for digital mirrors and a few degrees for the analog versions. These ranges for mirror size and mirror tilt seem to be what is reasonable to do with surface micro-machining on top of a CMOS substrate. Larger mirrors and larger tilt-angles require a larger air-gap (or

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[15] In the next section a device, NASAs shutter array [29], that does not rely on CMOS substrate for addressing a large number of actuators is presented; this approach, however is only suited for very slow frame rates (<1Hz).

spacing) between mirror and actuation electrode (in first approximation this gap is given with $l \sin \alpha$, where $l$ is the mirror size and $\alpha$ the tilt-angle); in order to achieve this gap, during fabrication a sacrificial layer is deposited, which thickness result the final air-gap. Typically, the thickness of these sacrificial layers is limited to a few micrometers[16].

Using surface micromachining technology, the mirror size is further limited by the maximum allowable mirror deformation. For large mirrors ( $100\mu$m and up) typically single-crystalline micromirrors are employed for yielding very flat mirrors, such as in irisAO MMA [23]. Utilizing thick single crystalline mirrors implies the use of bulk micromachining and some sort of joining technology, increasing the process complexity. Note that bulk-micromachining and wafer bonding is also required for achieving large (few tens to hundreds of microns) air-gaps. A nice combination of CMOS addressing substrate and single crystalline, though small, micromirrors has been shown by ZIMMER at IPMS [65].

## 1.4 MEMS for MOS

Given all the excellent properties of MEMS-based array as light-manipulator, it is self-evident that a MEMS-based object selection system has a large potential to boost the performance of a multiobject spectrograph and contribute to the scientific efficiency of celestial observations.

### 1.4.1 Basic Principles of MEMS-based MOS

In Fig.1.2 a schematic drawing of a MEMS-based MOS is depicted, here based on a micromirror array. The MMA is placed in the focal plane of the telescope and sends the light of wanted objects to the entrance pupil of the spectrograph and all the rest of the light (spoiler sources, sky background) to a light-trap or back to the telescope[17]. The MMA can be considered as a (reconfigurable) reflective slit-mask. When using a microshutter array (MSA), instead of a MMA, the optical design is similar to the one of a “classic” multi-slit spectrograph. Note that hereafter we use “slit” or “slitlet”, a

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[16] Of course thicker sacrificial layers exist, but then other, practical considerations, such as film stress and the etching of the sacrificial layer, finally limit the reasonable thickness in surface micro-machining

[17] In a more advanced design the rest of the light is sent to an imaging CCD, allowing parallel imaging and spectroscopy, see Sec. 1.4.4.

term also often used in conjunction with astronomical MOS, for both, the transmissive case (microshutters) and reflective case (micromirrors).

The conceptual difference between a MEMS-based slit-mask and a classic MOS is best illustrated with the way a certain object is selected: in a classic MOS the slit is placed wherever the light of the object of interest is located in the focal plane; in a MEMS-MOS the slit(s) *nearest* to the corresponding objects is opened. In a classic MOS the object is per definition centered in the corresponding slit, whereas in a MEMS-MOS the object may be anywhere within a certain slit, fall on the frame between two slits or be distributed over several slits. This has several consequences, geometrical and diffraction effects as well as increased stray-light may be the consequence. We define the following three key performance parameters for a MEMS-based MOS:

- Contrast
- Throughput
- Spectral photometric variation SPV

The contrast is a crucial parameter; for high signal to noise ratio a high contrast is required; note that high sensitivity is required in particular for observing faraway and faint galaxies. The contrast is the rejection ratio of wanted to unwanted light; it requires particular consideration for MMA-based MOS, as the transmissive (shutter-)solution has a higher ability to reject light. The throughput is mainly related to the fill-factor of the multi-slit or multi-mirror array and to global diffraction effects. Note that, whereas MSA may have an advantage in terms of contrast, MMA have the potential for near 100% fill-factor, which is not possible with MSA.

SPV is the unpredictable spectral photometric variation due to the random repartition of sources on the multi-slit device. The SPV is strongly affected by the object position (within the slit) and the wavelength, generating geometrical and diffraction effects. The impact of SPV is an error on the wavelength-resolved flux on the spectrometer CCD. This introduces an error on the weight of the different spectral components in the spectrum; whereas an elevated SPV would be tolerable for measuring red-shifts up to a certain degree, it is not acceptable for determining the type of galaxy, its composition and other relevant spectroscopic science. For the JWST NIRSPEC (see further below) a SPV requirement of <10% was set.

Zamkotsian et al. studied the influence of the object size relative to the unit size of MEMS-slit array (i.e. shutter size or mirror size) on the SPV for different wavelengths [59]. Three different plate-scales were considered:

0.66”/mm, 1”/mm and 2.5”/mm, called lean, standard and fat MEMS, respectively. It was found that the SPV requirement could not be met for any of the plate-scales over the whole wavelength range. On the other hand the throughput was identified to be superior for all wavelengths for the fat MEMS; at this plate scale a point like object is selected with a single slitlet (whereas in the two other cases several slitlets were required to select a single object). A dithering strategy was proposed that allowed to lower the SPV <10% for any case, involving different pointings of the telescope within a certain object selection area [61]. Anyhow, one generally avoids long exposure times and subdivides it rather into several smaller exposures—these sub-exposures could be utilized for the small repositionings of the telescope required for the dithering strategy.

As throughput is a key performance parameter and the SPV can be reduced utilizing the proposed dithering strategy it seems to be a good choice for choosing the unit-slit size of the MEMS such to accommodate one point-like astronomical object. Moreover, in the case of reflective slits, distributing a spatial coherent object (point source) over several tilted mirrors (in the tilting direction the mirrors would act as a blazed grating) would cause interferences. Ideally the mirror size is therefore adapted to spatially coherent point-like astronomical objects; extended objects can be distributed over several mirrors, as the spatial coherence is very low and interference is not a concern.

Besides being lightweight and configurable remotely, the big potential of MEMS-based MOS lies in its versatility and the vast number of conceivable operation modes, which are, unified in one single instrument, certainly unprecedented. A comprehensive but non-exhaustive enumeration is given below (based on MacKenty in [33])

1. Single slit

2. Multiple identical slits with a filter or Fabry-Pérot to define wavelength range

3. Custom slits tailored to targets; long slit for background subtraction, large slits (multiple single slits opened) for accommodating extended objects

4. Imaging and slitless spectroscopy (all mirrors in ON-state)

5. Blind pointing with large slits for background reduction at low dispersion without target acquisition overhead

6. Autonomous survey with onboard target selection and acquisition
7. Coronograph mode with multiple bright objects occulted by MMA slitmask
8. Slicing of brighter and extended sources for parallel acquisition of fainter objects
9. Integral field unit (IFU) mode, using Hadamard transformation masks

### 1.4.2 Ongoing and Past Developments

Since the late 90s NASA and ESA are pursuing the development of MEMS-based multiobject spectrographs. The earliest development is an infrared MOS using MEMS as object selection mechanism for the James Webb Space Telescope JWST (formerly named Next Generation Space Telescope NGST). Within a NASA Phase A study initially three different MEMS approaches where developed: a micromirror array based on polysilicon mirrors at Sandia, a micromirror array based on aluminum mirrors at GSFC and a microshutter array also at GSFC. For several reasons—we will consider them further below—the microshutter array development was selected to be continued [14]. It reached Technological Readiness Level 6 (TRL), i.e. readiness for flight, in beginning 2007; the JWST will be launched 2014. In parallel, several activities were pursued that employ the TI DMD as object selection mechanism in MOS. The Infrared Multiobject Spectrograph (IRMOS) using a 848x600-element TI DMD was conceived within the JWST community in order to explore the design and performance of MEMS mirror array based instruments [32]. The instrument is currently operated at the 4m Mayall telescope of the Kitt Peak National Observatory. Another development based on DMD is the Rochester Institute of Technology Multiobject Spectrometer (RITMOS), a small and light instrument designed for the Mees Observatory 24” Cassegrain telescope of UoR [40]. The most recent development is a prestudy for a DMD-based MOS for ESA’s EUCLID satellite [48]. Finally, a development of a MEMS shutter array using electrostatic actuation and intended for the use in future infrared MOS was reported by Takahashi of University of Toyko in 2006 [52].

### 1.4.3 Microshutters for the JWST NIRSPEC Channel

The driving science case for the JWST NIRSPEC channel is the exploration of red-shifts between 3 and 10. Observations with the Hubble space telescope

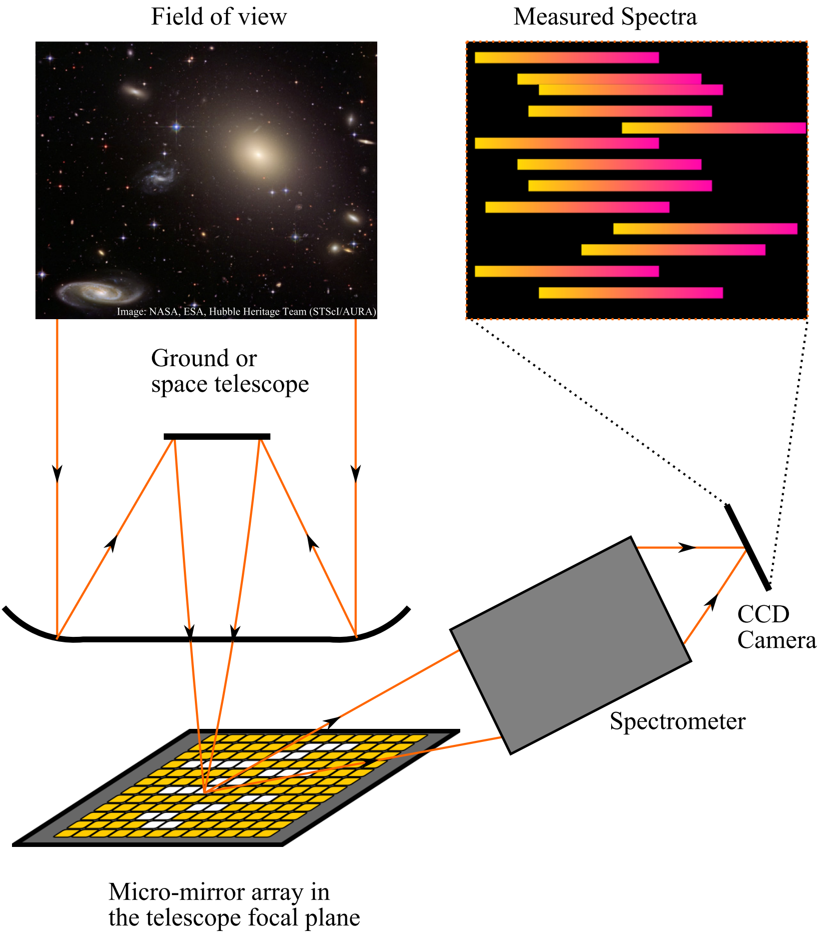

Figure 1.2: Principle of a Multi-Object Spectrograph with a Micro-Mirror Array.

Table 1.2: Key requirements for the MEMS-shutter array for the JWST NIRSPEC (Source [42])

| Item | Value |
|---|---|
| Object selection | Random Access Addressing<br>>200 objects simultaneously targeted |
| Field of view | 9 sq. arcmin |
| Contrast | >2000 (10,000 goal) |
| Lifetime | $9.4{\cdot}10^4$ with minimum failure |
| Operation Temperature | 37K |
| Mass | <10kg |
| Radiation | 48kRad |

have shown that most sources with high redshifts are both small and faint. Therefore excellent background rejection and high sensitivity is required. As the source density is low and long exposure times are needed, high spatial multiplexing and a large field of view is required. This implies the use of a reconfigurable slit-mask MOS, with the goal to select at least 200 objects at once. An optical MEMS seemed to be the ideal candidate for this task (if not the only one!). The general specifications of the JWST NIRSPEC and the requirements for the MEMS slit mask are summarized in Tab. 1.2.

Initially three competing MEMS-based slit-masks were developed in parallel: two MMA and one micro-shutter array (MSA). The first MMA development was pursuited by MacKenty and his team at NASA's Goddard Space and Flight Center GSFC. The device was oriented at TI's DMD technology: surface micromachined aluminum mirrors on top of a CMOS substrate. The mirror size was $100{\times}100\mu\mathrm{m}^2$ (much larger though than TI's DMD), the tilt-range ±10° and the projected device size 1024×1024 mirrors (which would result in an extremely large die size) [33]. Test arrays of 32×32 have been successfully fabricated and tested at 30K.

The second MMA development was carried out at Sandia National Laboratories, using their SummitV multi-layer polysilicon MEMS process[18]. Unfortunately very little information on this development is available through published literature.

The microshutter array development was also carried out at GSFC, ini-

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[18] http://mems.sandia.gov/tech-info/summit-v.html

tially under Moseley and will be described further below. In beginning 2002 the MSA was selected for continuation [14]. This decision was mainly based on the following three reasons:

1. Contrast: Shutters with adequate baffling provide inherently very high contrast between OFF and ON states and high transmission in ON state.
2. Transmissive solution could be interchangeable with a mechanical slit alternative, providing an efficient backup (CSEM's slit generator, see also [39]).
3. In case of a reflective solution the flatness and co-planarity (when using several mirrors per point-like source) of the mirrors is critical.

Note that these three reasons do not represent general show-stoppers for future MMA-based MOS developments. However one could guess that the two MMA developments at that time did not perform too well on point number three.

The microshutter array consists of $100\times200\mu\text{m}^2$-sized silicon-nitride (SiN) vanes, suspended via SiN torsion hinges to a single-crystalline silicon supporting structure. The SiN shutter vane features a metalized backside for electrostatic latching and ferro-magnetic stripes for magnetic actuation. The supporting structure is grid-like, i.e. each microshutter is entirely surrounded by a frame, the frame being $100\mu$m thick and $7\mu$m wide. The side-walls of the frame grid are metalized, providing a counter electrode for electrostatic latching. The projected array size for flight is 384×175 microshutters; four MSAs are mosaicked to cover a field of view of 3'.6×3'.6.

The microshutters are opened through magnetic actuation by sweeping a (macroscopic) tripole permanent magnet underneath the MSA and held in the open state by electrostatic latching. Addressing of individual shutters is done in a crosspoint-fashion: the shutters are electrically separated into rows and the counter electrodes on the frame are separated into columns. Initially all shutters are open; then row by row the desired slit-pattern is established by releasing the appropriate shutter. A shutter is held open when either of the two electrodes or both are set to a nonzero hold voltage[19] and similarly a shutter is released when both row and column electrode are at OV.

The fabrication process uses a combination of bulk and surface micromachining technology. The shutters, hinges, shutter electrodes and magnetic

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[19] Note that either row or column electrode must be set to a negative voltage; or alternatively, either row or column voltage is double the required hold voltage

stripes are processed, using thin film deposition and etching techniques, on top of a silicon-on-insulator (SOI) wafer. The stresses of the different thin-films of the shutter vane are adjusted such that it yields a near-zero deformation at the desired cryogenic operation temperature[20]. Then the handle layer of the SOI wafer is completely etched and the remaining 100$\mu$m-thick device layer (with the processed shutters on the topside) is etched from the backside using deep reactive ion etching (DRIE) to form the frame grid structure. In a final step the frame grid electrodes are deposited on walls of the frame grid using directional metal evaporation.

Life-time tests of earlier generations of 128 ×64 shutter arrays without light-shields have been conducted in cryogenic environment and demonstrated successful operation at 90K and 30K. The "failed open" (shutters that fail and stay in the open-position) failure rate increased logarithmically adding <2.3% failures at $10^6$ actuations, the specified mission life-time being $10^5$ cycles [26]. Contrast measurements showed a contrast of 7000 with lightshields; measurements on earlier devices without lightshields was 200 [29].

### 1.4.4 TI DMD based MOS Developments and Studies

IRMOS, an instrument conceived for the wavelength range 0.85$\mu$m to 2.5$\mu$m showed that TI's DMD can be operated at -45°C, well below the nominal operation temperature; further it has been shown that the mirrors do not get stuck, even after hours of static operation in either ON or OFF state. Many observation modes, including an integral field unit mode using a Hadamard transformation pattern, could be demonstrated. RITMOS, implemented a highly efficient instrument design, where the two states (ON and OFF) of the micromirrors were exploited: one state sent the light to a spectrograph and the other directed the light to an imaging CCD. Both, IRMOS and RITMOS utilized a early generation DMD with an array size of 848×600 [32, 40].

The prestudy currently being carried out for the EUCLID Near Infrared Channel (ENIS) states as main scientific goal to produce the largest three-dimensional evolutionary map of the Universe over the past 10 billion years. One instrument concept considers using a MEMS-based MOS, relying on a recent version of TI DMD, the TI Cinema chip with 2048×1080 micromirrors [48]. Within this prestudy extensive technical assessment of the TI Cinema chip has been carried out at Visitech (Norway) and LAM, including cold temperature characterization, and radiation tests [62]. It has been showed

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[20] This implies that the operation temperature range of the shutter device is limited

that the lower temperature limit for reliable operation is -40°; permanent failure of individual mirrors started to occur at -55°. The total ionization dose (TID) radiation test showed that the device starts to get affected at 10kRad, but still working with only minor artifacts up to a dose rate of approximatively 16kRad. It is suspected that the SRAM cells, located under each mirror, are the cause for radiation induced malfunctioning. Annealing at room temperature in a biased condition could be used to bring the DMD back to normal operation.

### 1.4.5 Development of a dedicated MMA: MIRA

MEMS shutter arrays and MEMS mirror arrays were identified by the major global astronomical and space societies as high-potential candidates for the use in future MOS: they are lightweight, remote-configurable, versatile and can be operated in cold environment. Moreover they offer a vast number of operation modes implementable with one single device, which is not conceivable utilizing classical approaches.

Though NASA's shutter device is an outstanding development and certainly superior to any other conceivable MEMS-based slit-mask in terms of contrast, it can't be regarded as general solution for all future applications. Due to its semi-macroscopic actuation mechanism it can't fully exploit the full potential in terms of versatility of MEMS-based solutions; for instance, real-time reconfiguration of the MSA or parts of it is hardly possible. Further, when covering of very large focal planes is intended, the present microshutter implementation is not optimum, as the device has a large lateral overhead, which makes mosaicking of individual arrays unattractive (low over-all fill-factor and consequently low throughput). A micromirror array has the potential to overcome this limitation, as all functional elements of the device (mechanical support, addressing, electronics, etc) can be hidden or stacked underneath the mirror array. Conceptually it is therefore possible to cover large focal planes by mosaicking of MMAs and reaching a near optimum over-all fill-factor. On top of that, in contrast to the microshutter approach, the intra-array fill-factor can be made near 100%, at least perpendicular to the dispersion direction, with a micromirror approach.

One limitation of TI's DMD is the small mirror size which for most plate scales and object sizes makes it impossible to set one object per mirror, which is an important prerequisite for efficient use of a MMA as reflective slit-mask. The second limitation is that reliable operation of TI's DMD is limited to -40°C; for proper suppression of instrument radiation for spectroscopy in the near-infrared regime, the device should be cooled at least to below 100K (1–5$\mu$m) (and below 30K for 5–28$\mu$m).

The goal of the MIRA development is to provide a MMA platform that is suited for MEMS-based MOS in future large ground-based and space telescopes, providing high versatility, high throughput and high sensitivity (sky-background limited instrument) for near infrared spectroscopic observations. MIRA, standing for Mirror Array and a class of "miraculous" pulsating stars, is a development between the Laboratoire d'Astrophysique de Marseille LAM and IMT[21], initially conceived within FP6 OPTICON Smart Focal Planes program[22].

The telescope class which we aim with MIRA has plate-scales of 1–2"/mm and fields of view larger than 3'×3'. This requires mirror-sizes in the range of 50–500$\mu$m and a MMA with low lateral overhead architecture enabling high-fill factor mosaicking of the large fields of view (e.g. for a field of view of 3'×3' and a plate scale of 1"/mm a surface of 180×180mm$^2$ must be covered with micromirrors). For a sky background limited instrument in the near infrared range, the MMA will be required to operate at least below 100K.

The goal of the present Ph.D work is to provide a conceptual and technological base for the MIRA MMA platform. In the following document the work carried out within the scope of this thesis is summarized. In Ch. 2 a few fundamentals on electrostatic actuators, MEMS microfabrication and the utilized characterization tools and methods is given. In Ch. 3 first the baseline MMA-MOS concept is presented and the requirements on the MMA are deduced. Then the MMA concept, conceived to fulfill the requirements is described. In Ch. 4 analytic and finite element modeling of the device are given, allowing to translated the requirements on the MMA into a design and a physical layout. Ch. 5 presents details on fabrication and assembly of the MMA and the resulting device. Finally, Ch. 6 summarizes optical, electromechanical and cryogenic testing and concludes with MOS-demonstration and contrast measurement of a fabricated MMA. For a quick overview, one may refer to Sec. 3.2 for the device concept, Sec. 5.3 for the fabrication results and Sec. 6.4 for a summary on the measured device performance.

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[21] Since 2008 incorporated at EPFL, Lausanne, formerly, and at the time where the presented work was carried out, belonging to University of Neuchatel

[22] For more information on Smart Focal Planes see Sec. 1.2

# Chapter 2

# Background

## 2.1 MEMS-Actuators

A MEMS-actuator consists of a movable element, e.g. a micromirror, that is suspended via a spring to a fix substrate and an actuation mechanism that allows positioning of the movable element.

Common actuation mechanisms are based on electrostatic, electromagnetic, piezo-electric or thermal forces. The choice of actuation mechanism depends on the requirements of the application, such as required stroke, speed, material or other restrictions (for instance maximum allowable actuation voltage). A comprehensive overview and comparison over the different actuation mechanisms and their limitations is given in [20].

We focus hereafter on electrostatic actuation. Given its simplicity and easy implementation with standard microfabrication technology it is certainly the most popular actuation mechanism in the MEMS-world. Further, it is particularly suited for actuation at small scales as the energy density increases with $1/d$ where $d$ depicts the separation between two charged electrodes.

### 2.1.1 Parallel Plate Electrostatic Actuator

The simplest model of an electrostatic actuator is depicted in Fig. 2.1 (a): A pair of electrodes each having a surface $A$, separated by an air-gap $g$, one of the electrodes being fixed and the other movable, suspended via a spring to a fix substrate. Applying a voltage potential $V$ between the two electrodes causes an attractive electrostatic force on the electrodes and thus, the movable electrode deflects towards the fixed electrode. The amount of deflection $z$ is given by the magnitudes of the deflecting electrostatic force $F_E$ and the restoring spring force $F_S$. With a few basic formulas we can determine the static system response and deduce the fundamental principles of a electrostatic closing gap actuator.

The electrostatic force can be derived using the principle of virtual work (e.g. from Feynman in [16]) and is given by

$$F_E = \frac{1}{2} V^2 \frac{dC}{dz} \tag{2.1}$$

The capacity $C$ of a parallel plate capacitor is given by $\epsilon_0 A/z$ and thus, $F_E$ becomes

$$F_E = \frac{1}{2} \frac{\epsilon_0 A}{(g-z)^2} V^2 \tag{2.2}$$

where $g$ is the initial separation of the two capacitor plates.

We assume a linear spring and thus, the restoring force is given by Hooke's law $F_S = -zk$, where $k$ is the spring constant. The system response is therefore given by

$$F = -k \cdot z + \frac{\epsilon_0 A}{2(g-z)^2} V^2 \tag{2.3}$$

For convenience we normalize above equation to

$$\widetilde{F} = -\widetilde{z} + \frac{\widetilde{V}^2}{(g-\widetilde{z})^2} \tag{2.4}$$

where

$$\widetilde{F} \equiv \frac{F}{gk^2} \qquad \widetilde{z} \equiv \frac{z}{g} \qquad \widetilde{V}^2 \equiv \frac{\epsilon_0 A}{2gk} \tag{2.5}$$

The equilibrium states of the system are given for $\widetilde{F} = 0$, i.e.

$$-\widetilde{z} + \frac{\widetilde{V}^2}{(g-\widetilde{z})^2} = 0 \tag{2.6}$$

or

$$\widetilde{V}^2 = (1-\widetilde{z})^2 \widetilde{z} \tag{2.7}$$

The stability of an equilibrium state is defined through the stiffness of the system, i.e.

$$K \equiv \frac{\partial \widetilde{F}}{\partial \widetilde{x}} = \frac{1 - 2\widetilde{V}^2}{(1-\widetilde{x})^3} \tag{2.8}$$

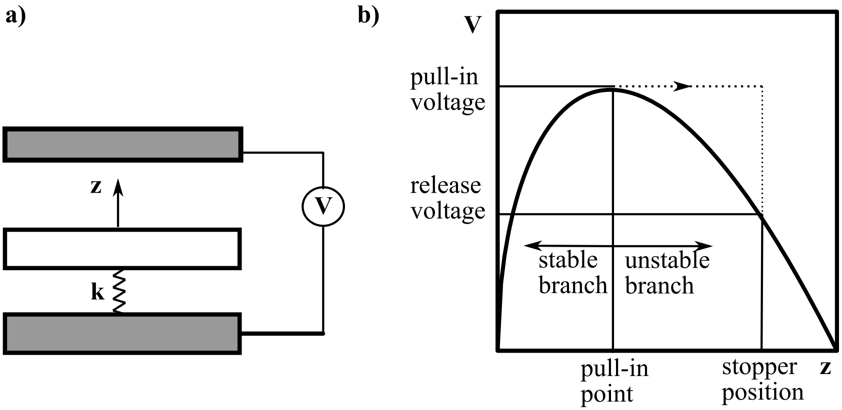

Figure 2.1: A simple example of an electrostatic closing gap actuator. (a) The actuator consists of a movable actuator, suspended with a spring to a fixed substrate, and a fixed electrode; applying a voltage between the two will cause the movable electrode to displace towards the fixed electrode. (b) Equilibrium states

For $K > 0$ an equilibrium state is stable, $K < 0$ unstable and $K = 0$ critically stable. The critically stable state is called pull-in. Posing $K = 0$ and substituting Eg. 2.7, solving for $\widetilde{x}$ and $\widetilde{V}$, respectively, and reusing the definitions in Eq. 2.5 we get

$$x_{\text{crit}} = \frac{g}{3} \qquad V_{\text{crit}} = \sqrt{\frac{8g^3k}{27\epsilon A}} \tag{2.9}$$

The square-root of Eq. 2.7 is plotted in Fig. 2.1 (b) and interpreted as follows: starting from zero and staying below the critical or pull-in point $\widetilde{x}_{\text{crit}} = \frac{1}{3}$ the displacement of the movable element is steady with the applied voltage. This regime is sometimes referred to as the *analog* range of the actuator. For any voltage above the pull-in voltage $\widetilde{V}_{\text{crit}} = (\frac{8}{27})^{1/2}$ the movable element makes a sudden transition towards the static electrode—in a real world device this sudden movement is stopped before the two electrodes come into contact, say at a position $x = s < g$, as depicted in the figure. Once in the state $s$ the movable element stays there for any voltages above the corresponding voltage $V_s$ and returns only to the analog branch for $V < V_s$.

### 2.1.2 Tilting Plate Electrostatic Actuator

Above considerations are qualitatively true for any closing-gap actuator. However when considering a tilting movement, e.g. a tilting micromirror, the parallel plate approximation of the electric field is inaccurate for finite tilting-angles. For that case Toshiyoshi [20] proposed a simple way of estimating the electric field strength by approximating it by coaxial arcs[1]. The radius of the arc at the rotation axis of the movable electrode ($x = 0$) is $R = (g - z)/\sin(\alpha)$, where $z$ depicts the piston movement towards the fixed electrode, which is always present for springs with finite stiffness in the $z$-direction. The corresponding arc length at position $x$ is therefore

$$a(x) = \left( \frac{g - z}{\sin(\alpha)} - x \right) \alpha \tag{2.10}$$

and the electric field

$$E(x) = \frac{V}{\left( \frac{g-z}{\sin(\alpha)} - x \right) \alpha} \tag{2.11}$$

The electrostatic force acting in $z$-direction and the force moment acting around the rotation axis is given by integrating the electrostatic pressure $w\epsilon_0 E^2/2$ and $wx\epsilon_0 E^2/2$, respectively, along the $x$-axis, i.e.

$$F = \frac{1}{2}\epsilon_0 V^2 \int_0^l \frac{1}{\left( \frac{g}{\sin(\alpha)} - x \right)^2 \alpha^2} wx \mathrm{d}x \tag{2.12}$$

and

$$M = \frac{1}{2}\epsilon_0 V^2 \int_0^l \frac{1}{\left( \frac{g-z}{\sin(\alpha)} - x \right)^2 \alpha^2} wx \mathrm{d}x \tag{2.13}$$

### 2.1.3 Reliability of MEMS-Actuators

Reliability is a very broad topic and at this place we only touch on this subject. Reliability is commonly understood as the probability that a device will perform a required task for a set amount of time. A very comprehensive introduction to MEMS Reliability is NASA's *MEMS Reliability Assurance Guidelines for Space Applications* from the year 1999 [51]—though some

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[1] The assumption of a radial electric field in a tilted capacitor plate arrangement in principle only holds true for a perfect conductor; in silicon, having a finite conductivity, this must be considered as an approximation...

of the contents may be outdated, most of the considerations certainly still hold true. A more recent review on MEMS reliability, focusing on space applications, is found in [50].

Amongst statistical considerations, reliability involves the careful analysis of potential failure modes of a given system, device or structure. A broad numbers of mechanisms can cause a MEMS to fail at a certain time; a failure mode of particular interest for microstructures operated in contact mode is stiction.

Under stiction we understand the phenomena when a movable element gets into contact with another element of the MEMS (for instance the substrate) and can not be released from this state by the restoring force. Given the small structure sizes, surface forces can easily dominate all others, in particular the restoring force. The predominant surface forces that may cause stiction are:

- capillary forces in presence of liquid (for instance due to local condensation of humidity)
- van der Waals force
- electrostatic forces due to trapped surface charges
- hydrogen bridging between hydrophilic surfaces due to adsorbed water layers

Further reading on stiction and its causes may be found in [57]. Generally these forces depend on the area and roughness of the surfaces in contact. In order to minimize stiction, minimizing the contact area is an efficient approach. Other approaches include applying special coatings or operation in a conditioned environment [24].

Cyclic fatigue failure, a failure mode that is of concern in macroscopic structural elements (mostly ductile materials), is barely encountered in the MEMS-world—bulk mono-crystalline silicon is literally immune against cyclic failure. However, it shall be noted, that micron-scale (poly-)silicon structures might *be* susceptible to cyclic fatigue failure under certain conditions [3, 4]—these conditions being very high stresses and an oxidizing environment. As in our application the device is operated in vacuum, this (rare) failure mode is not of concern.

## 2.2 Microfabrication Technology

MEMS are commonly fabricated starting from a single-crystalline silicon substrate (silicon wafer) or a substrate that contains two (or sometimes more) silicon layers separated by an silicon dioxide layer (silicon on insulator or SOI wafer). Similar to integrated circuit (IC) fabrication, the fabrication process consists of adding material through a deposition process and structuring the added material layer using a masking layer that was obtained through photolithography and chemical and/or physical etching. In some cases the substrate itself (especially when using SOI wafers) is utilized as structural layer and processed/etched accordingly using deep etching techniques. The latter technique is referred to as *bulk* micromachining, whereas the former is called *surface* micromachining.

During bulk and surface micromachining (which often include repeated deposition/structuring cycles) the mechanical, electrical, optical and sometimes even electronic elements of the MEMS are structured. In a final step the device needs to be released (and singulated/separated from the substrate), i.e. the mechanical structures are liberated such that the device is functional, and packaged, i.e. a mechanical and electrical interfaces must be added that allow the integration of the MEMS device into a working system.

In order to increase the integration density/vertical stacking of functional elements, it is sometimes required to process certain elements on different substrates and join the elements at a later stage; if the elements are joined before the individual devices are singulated we refer to wafer level bonding, else this technology is called chip level bonding. An example of such a stacking of functional elements through wafer level bonding is the irisAO MMA, where the actuators are processed through surface micromachining one substrate and the micromirrors, utilizing bulk micromachining on another and the two are joined through an wafer level bonding process to form the complete device [23].

Hereafter the most relevant fabrication steps required for bulk and micromachining are shortly described. A good reference for MEMS-fabrication technologies is for instance Madou's *Fundamentals of Microfabrication* [34]. For further reading on the steps involved in photolithography, a comprehensive collection of application notes can be found on MicroChemicals' website[2]; an excellent reference book on the particular subject of photoresist and its processing may be found in [13].

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[2] http://www.microchemicals.com/technical_information/index.html

### 2.2.1 (Deep) Reactive Ion Etching

In Reactive Ion Etching (RIE) both chemical and physical etching takes place. A RF reactor is employed to create a plasma and breaking the precursor gas mixture into reactive ions; the ions are accelerated towards the substrate and react with the substrate material, creating volatile species. If the arriving ions have enough energy also physical etching takes place, i.e. surface atoms of the substrate are ripped out due to the impact of the ions. RIE is suited to dry-etch a large variety of materials and offers limited anisotropic etching for a limited etch depth.

A specialized RIE process destined for etching deep structures at high aspect ratios into silicon is the Deep RIE (DRIE) process invented by Robert Bosch GmbH [28]. The DRIE process derives advantage of the physical and chemical etching effects taking place in a RIE system and consists of three steps: in a first step a passivation layer is conformally deposited; in a second step the passivation layer is physically etched by ion bombardment—this step is highly directional and consequently surfaces perpendicular to the ion acceleration direction are etched much faster. In a third step the exposed silicon is etched by a chemical reaction. The gas mixture that is commonly used is $SF_6$ and $C_4F_8$, the first component supplies fluorine radicals for silicon etching and the second is the precursor for the polymeric passivation layer. The cycle and ratio between the different steps is controlled through the cycling of the acceleration energy of the ion bombardment, partial gas pressures and other parameters. This cycled process yields high etch speed of $10\mu$m/s and beyond, very high aspect ratios of up to 1:30 and can also be tuned to yield very smooth side walls.

As masking materials resist can be employed (etch selectivity to silicon around 1:40) and for deep (long) etches an oxide masking layer may be required (selectivity of thermal oxide up to 1:150). The etching can either be timed controlled or stopped by a buried oxide layer, the latter being common for bulk micromachining based on SOI wafers. Both approaches have certain drawbacks that ultimately are related to a non-uniform etch speed. The etch speed depends on the position within the wafer (non-uniform plasma, acceleration field, etc); a realistic value here is 10% uniformity error accross the wafer (though smaller values are possible when restraining to the "sweet spot" of the machine and trading-off with other etch parameters). Further, the etch speed depends on the lateral dimensions of the structures to be etched (diffusion limited etching): smaller trenches etch slower than larger trenches—the latter fact is impressively exhibited in Fig. 2.2 and also shows

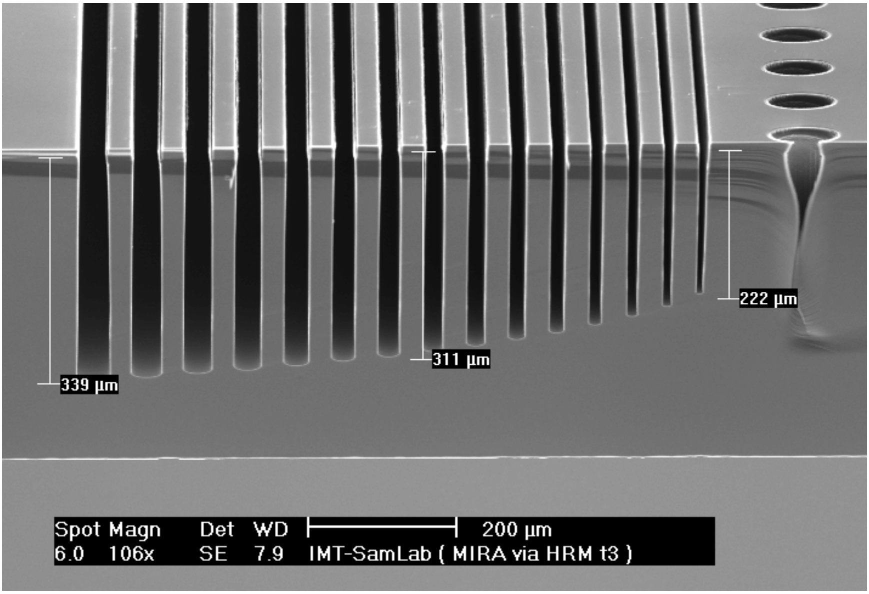

Figure 2.2: Dependence of etch speed of feature size to be etched in DRIE. In this example the trench width varies from 4$\mu$m to 32$\mu$m in 2$\mu$m steps.

the limitation of timed-etch. Whereas using the burried oxide layer of a SOI as etch-stop yields uniform etch depths, another effect related to non-uniform etch speed takes place: the so-called notching, illustrated in Fig. 2.3, related to charging of the oxide and field concentration at the structure edges.

A combination of timed-etch and oxide-stop etching can be used for the so-called delay mask process, yielding structures with more than two height levels [27].

### 2.2.2 Thermal Oxidation

Thermal oxidation of silicon is carried out in quartz furnaces at temperatures between 600°C and 1250°C in either water steam (wet oxidation) or $O_2/N_2$ (dry oxidation) atmosphere. Whereas wet oxidation yields higher growth rates, dry oxidation forms denser films. The ratio of silicon thickness converted to resulting oxide thickness is 0.46, i.e. for a 1$\mu$m-thick oxide layer 0.46$\mu$m of silicon will be consumed [34] (this value may slightly vary with

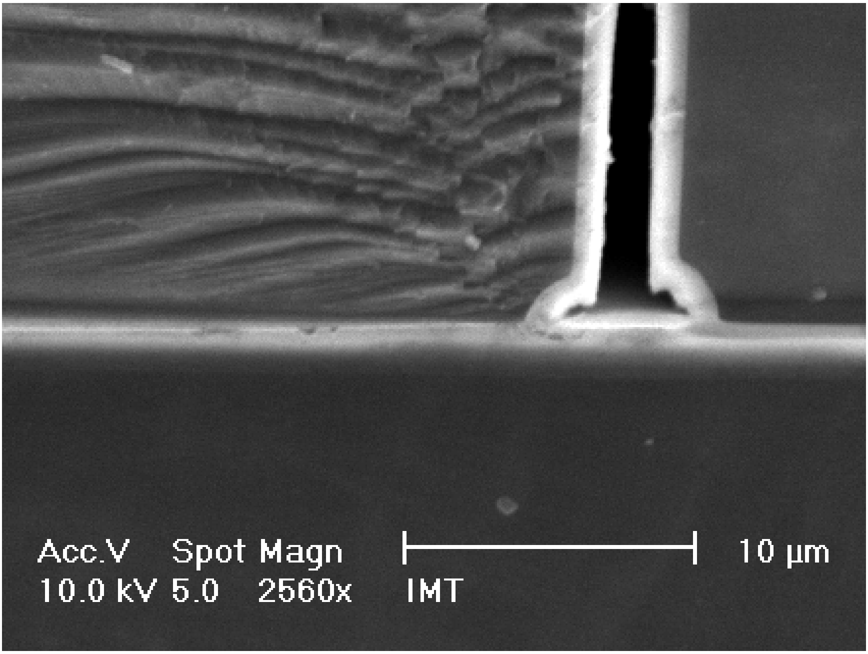

Figure 2.3: Notching in DRIE process

the actual oxide growth method and temperatures). Due to molecular volume and CTE mismatch to the underlying silicon substrate, silicon oxide is compressively stressed (depending on the thickness of the layer this may be up to several hundreds of MPa). This needs particular consideration when removing a thermal oxide layer on only one side of the wafer: warping of the wafer may occur, which is problematic for subsequent fabrication steps where clamping of the wafer on a chuck is involved (e.g. photolithography or DRIE).

Thermally grown $SiO_2$ can be used as electrical insulating layer, diffusion barrier for common Si-dopants, mask for subsequent DRIE or other etching steps and as sacrificial layer. Besides that, thermal oxidation can also be employed for filling trenches with high-aspect ratios, rounding sharp edges, smoothing surfaces or removing silicon residues after a delay mask DRIE.

### 2.2.3 Low Pressure Chemical Vapor Deposition of Polysilicon

The polysilicon film is formed through pyrolysis of silane ($SiH_4$), typically at pressures of 200mTorr and temperatures around 600°C and above. The deposition parameters determine the morphology and material properties of the material. The parameters used for the present work are 200mTorr and 610°C, yielding fine-grained polysilicon films (the transition from amorphous to poly-crystalline films happens at around 580°C) with predominant 110 crystalline orientation and a Young modulus near the bulk silicon value of 169GPa [30]. Intrinsic stress of the deposited layer can in principle be controlled by the deposition parameters, varying from tensile to compressive, but always needs to be traded-off with other material properties and deposition characteristics. For most applications a near stress-free layer is desirable; this can be achieved by a post-deposition annealing step, for instance one hour at 1050°C in a nitrogen atmosphere.

Doping of the polysilicon layer is for instance achieved by deposition of a doped oxide layer on top of the polysilicon layer and a subsequent diffusion step; the diffusion step can be carried out at the same time as the annealing step. Doping levels of around $10^{19}\text{cm}^{-3}$ and a resistivity below $10^{-1}\Omega\text{cm}$ are achieved with this method [ibidem].

Inherently LPCVD layers are very conform, i.e. even structures with a high aspect ratio (for instance deep trenches) are uniformly coated with a polysilicon film. This results from the large diffusion coefficient of the reactants at low pressures, leading to a growth rate limited by the rate of surface reactions rather than mass-transport. A high conformity is advantageous for many applications (for instance filling of deep trenches for through silicon vias or when good step coverage is required for anchored structural elements) but may also be a disadvantage, as will be seen in Sec. 5.2.1.

### 2.2.4 HF Vapor Phase Etch

In a final fabrication step the sacrificial layers that have been utilized to build up the functional structures needs to be etched in order to liberate the movable structures; in most of the cases the sacrificial layer is either silicon dioxide that was deposited during surface micromachining or the buried oxide layer of a SOI wafer in the case of bulk micromachining[3]. Hydrofluoric acid (HF) or buffered HF (BHF) is commonly used for wet-etching of $SiO_2$, showing an excellent selectivity towards single-crystalline silicon and polysilicon. Utilizing a liquid phase etchant for releasing delicate micro-scale movable structures is very challenging and requires sophisticated techniques such as critical point drying for avoiding stiction and destruction of the movable elements. Another approach is to avoid the liquid phase by employing HF in its vapor phase (see [64] and [45] and references therein).

Based on SOI substrates, front- and backside DRIE etching and HF vapor phase release etch, Overstolz proposed a chip singulation process [45], avoiding the rather harsh die saw process (dicing) that is normally employed to singulate the individual chips (or dies) and separate them from the substrate. In the dice-free approach, trenches delineating the chip are etched using DRIE into the device and the handle layer (front-and backside) of the SOI during device processing[4]. The front-and backside trench are horizontally offset by several micrometers to some tens of micrometers, such that device is still held within the wafer frame by the buried oxide layer that separates the device and handle layer. In the final HF vapor phase release etch the BOX between the trench in the device layer and the trench in the handle layer is etched, releasing the chip from the wafer. This approach not only avoids dicing but also enables the implementation of different chip shapes and sizes on one substrate, which particularly in R&D is of great advantage.

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[3] Other sacrificial materials are conceivable and utilized as well—in principle any material that is compatible with the fabrication process and that can be etched selectively towards the other materials present on the device could be employed.

[4] In many cases the trench etching can be done at the same time as the etching of the active structures, such that no additional process step is required.

## 2.3 Measurement Methods and Setup

The main measurement methods that were used in the present work were white light interferometry (also referred to as vertical scanning interferometry VSI) and phase shift interferometry. The first method can be employed to record two-dimensional images of large height scale topography, it was in particular used for determining tilt-angles of micromirrors. The second method is employed to get topographic information with sub-nanometer vertical resolution; this method is particularly suited to measure the surface quality (deformation and roughness) of micromirrors. Two setups, incorporating above measurement methods, have been utilized: a commercially available optical profilometer, Wyko NT1100, from the Veeco Corporation and a custom built setup at the Labratoire d'Astrophysique de Marseille. A third setup, also at LAM, has been utilized for MOS demonstration and contrast measurement of fabricated mirror arrays; this is presented in Sec. 6.5.

### 2.3.1 Phase Shift Interferometry

Consider illuminating an object of certain shape $h(x, y)$ with a plane wave as depicted in Fig. 2.4. The topography of the object will introduce a phase delay to the reflected wavefront, the phase-delay at point $(x, y)$ depending on the optical path difference introduced by the height $h$ of the object. The optical path difference is given with $2h(x, y)$ and the corresponding phase delay is $\frac{2\pi}{\lambda}2h(x, y)$. Thus, the reflected wavefront contains the topographic information of the object:

$$\phi(x, y) = \frac{4\pi h(x, y)}{\lambda_0} \tag{2.14}$$

The phase information $\phi(x, y)$ can be retrieved using an interferometer, where the reflected wavefront of the object is superimposed by the wavefront reflected by a reference mirror; the resulting interference pattern $I_i(x, y)$ is imaged on a detector and given by

$$I_i(x, y) = I_0(x, y)\left[1 + V(x, y)\cos(\phi(x, y) + \delta_i)\right] \tag{2.15}$$

where V(x,y) is the visibility or contrast of the fringes and $\delta_i$ is an additional phase shift that can be introduced by shifting the reference mirror parallel to the optical axis. Inducing phase shifts corresponding to $\delta_i = 0, \pi/2, \pi, 3\pi/2$

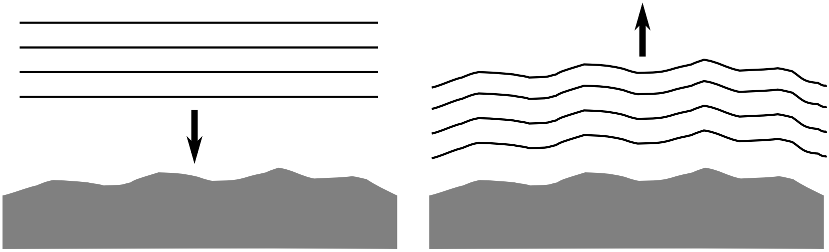

Figure 2.4: The topographic (height-) information $h(x, y)$ of an object is contained in the phase distribution $\phi(x, y)$ of the reflected plane wave. The phase information and thus, the topographic information can be retrieved using phase-shift interferometry.

and measuring at each time the resulting intensity $I_i(x, y)$ yields

$$I_1(x, y) = I_0(x, y) + I'(x, y) \cos(\phi(x, y) \tag{2.16}$$

$$I_2(x, y) = I_0(x, y) - I'(x, y) \sin(\phi(x, y) \tag{2.17}$$

$$I_3(x, y) = I_0(x, y) - I'(x, y) \cos(\phi(x, y) \tag{2.18}$$

$$I_4(x, y) = I_0(x, y) + I'(x, y) \sin(\phi(x, y) \tag{2.19}$$

which can be solved to

$$tan(\phi(x, y)) = \frac{I_4(x, y) - I_2(x, y)}{I1(x, y) - I3(x, y)} \tag{2.20}$$

from which we can extract the height information $h(x, y)$ according to Eq. 2.14. In practice the procedure is some more involved and limitations apply; a treatise on phase shift interferometry can be found in [31]. Under ideal condition the vertical resolution (ability to resolve a height difference in the topography of a sample) may be as low as 0.1nm; the accuracy ultimately depends on the planarity of the reference flat and the calibration of the displacement mechanism that introduces the $\pi/2$ phase shift. Single wavelength PSI is limited to topographies with abrupt steps lower than $\lambda/4$, where $\lambda$ is the central wavelength of the utilized light source. For large steps or very rough surfaces a more adapted method is white light or vertical scanning interferometry.

### 2.3.2 White Light Interferometry

White light interferometry or vertical scanning interferometry employs light with a short coherence length. In this case the contrast (or visibility) of the interference fringes is maximum when the path difference between a location on the object and the reference mirror is zero. Therefore, by scanning the reference mirror (or object) over a range of interest and monitoring the fringe contrast at each point on the object, the height information can be retrieved by mapping the maximum of the contrast to the z-position of the scanned mirror [31].

The vertical resolution of vertical scanning interferometry can be a few nanometers. The accuracy depends on calibration and linearity of the scanning mechanism and is generally a function of the total scanned length.

### 2.3.3 Measurement Setup

#### Veeco Wyko NT1100

The Veeco Wyko NT1100[5] is a micro-interferometer incorporating both, phase shift and vertical scan interferometry. Moreover it offers a dynamic measurement option (DMEMS) allowing reconstruction of periodic dynamic movements employing a stroboscopic light source. It features a pattern recognition software, in conjunction with a Matlab interface, allowing an automated measurement and data extraction mode.

The VSI mode of the Wyko NT1100 has been extensively used for tilt-angle characterization throughout the present project; hereafter the error on these measurements is estimated: The absolute measurement error of the VSI measurement is specified to be 2% of the scan range. Assuming a tilt-angle of $20°$ and a mirror length of $100\mu$m, the minimum scan range to detect the mirror tilt is $\sin(20°) \cdot 100\mu\text{m} \approx 35\mu\text{m}$. The absolute error is therefore about $0.7\mu$m. Using $\arcsin(0.7/100)$ we have an absolute error of about $0.4°$. The repeatability between two measurements is specified to be better than 10nm. Using $\arcsin(0.01/100)$ we get a repeatability of approximative $0.006°$, which is about half of one arcminute.

#### Interferometry Bench at LAM

An interferometric bench specialized for characterizing optical MEMS devices has been developed at LAM [31]. The modular Twyman-Green in-

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[5] www.veeco.com

terferometer allows high in-plane resolution ($4\mu$m) or large field of view (40mm)—the large field option is particular interesting for assessing global device characteristics. The utilized light source is an incandescence lamp with an interference filter (typical example: $\lambda_0$=650nm, $\Delta\lambda$=10nm). By monitoring the temporal light coherence, this illumination avoids all extraneous fringes that would be induced by classical high coherence sources such as lasers. Out-of-plane measurements are performed with phase-shifting interferometry showing very high resolution (standard deviation $<$1nm). Range is increased without loosing accuracy by using two-wavelength phase-shifting interferometry authorizing large steps measurements.

# Chapter 3

# Concept

## 3.1 MOS with Micromirrors

### 3.1.1 Considerations on System Layout

Fig. 3.1 shows the optical layout of a MMA-based MOS that was proposed by Garzon during the SMART-MOS studies for the E-ELT [18]. Whereas no such instrument is currently considered for being implemented in the E-ELT, we assume this optical layout as baseline for the MIRA MMA development. The MMAs are placed in the focal plane such that the neutral or OFF position is parallel to the focal plane, consequently sending unwanted (blocked) light back to the telescope. The tilted state of a micromirror element is defined as the ON state and conceived such that the light is sent through a collimator onto the entrance pupil of the spectrograph. The focal plane of the telescope is not planar but curved; the MMAs must be arranged such that all elements are imaged on the detector of the spectrograph. As the depth of focus is limited, it may be required to arrange the individual MMAs on a polygonal surface approaching the curved focal plane.

For convenience and further reference we set the coordinate system to be defined by the dispersion of the spectrograph and the optical axis: the y-axis is parallel to the dispersion direction of the grating in the spectrograph, the z-axis is perpendicular to the mirror in the OFF-state and points toward the telescope and the x-axis is defined through y and z to form a right-hand Cartesian coordinate system. The tilt-axis of the mirror is conceived to be parallel to the x-axis (perpendicular to the dispersion direction). The micromirror array is oriented such that the array principal axes are parallel to the x- and y-axes. The array architecture must be conceived such that no intermediate frame is located between two adjacent mirror in the y-direction, enabling the use of a long slit for background subtraction.

For maximizing throughput and minimizing interference between tilted mirror facets (see Sec. 1.4.1), one object is set to fit one mirror, assuming as a starting value an object size of 0.1" and a plate scale of 1"/mm. The considered wavelength range is 1–5$\mu$m, with the option to extend to below 1$\mu$m and above 55$\mu$m. For a sky background limited instrument the MMA must be cooled to below 100K if the considered wavelength is 1–5$\mu$m and below 30K for the range 5–28$\mu$m. The following top-level requirements are essential for the usefulness and applicability of the MMA in future MOS: The MMA slit-mask must be able to provide

- pure, undisturbed spectra of the objects of interest
- high scientific efficiency (parallelization) and maximum flexibility
- robust and simple system and capability of remote configuration.

### 3.1.2 Requirements

In this section the requirements for a MEMS-based slit mask are developed and the specifications for the MMA deduced. The requirements are partially based on the JWST-NIRSpec studies, which have been carried out at LAM [60, 59] and the studies within the Smart Focal Planes JRA [18].

**Undisturbed spectra** Only light that origins from the object of interest shall arrive at the detector and furthermore this light must not be altered. The rejection ratio between wanted and unwanted light originating from the sky background or other light sources is defined as the contrast. According to the density of objects (stars and galaxies) in the field of view and their magnitude, a contrast requirement of 3000:1 has been established during JWST NIRSpec studies. A DMD made by TI has been used for first experiments, and contrast values for 10° as well as 20° tilt-angles between ON and OFF position have been measured. The 3000:1 contrast requirement could be fulfilled only with the tilt angle of 20° [60]. Hence the tilt-angle requirement for the MMA is set to $\geq 20°$ between ON and OFF state of the micromirrors.

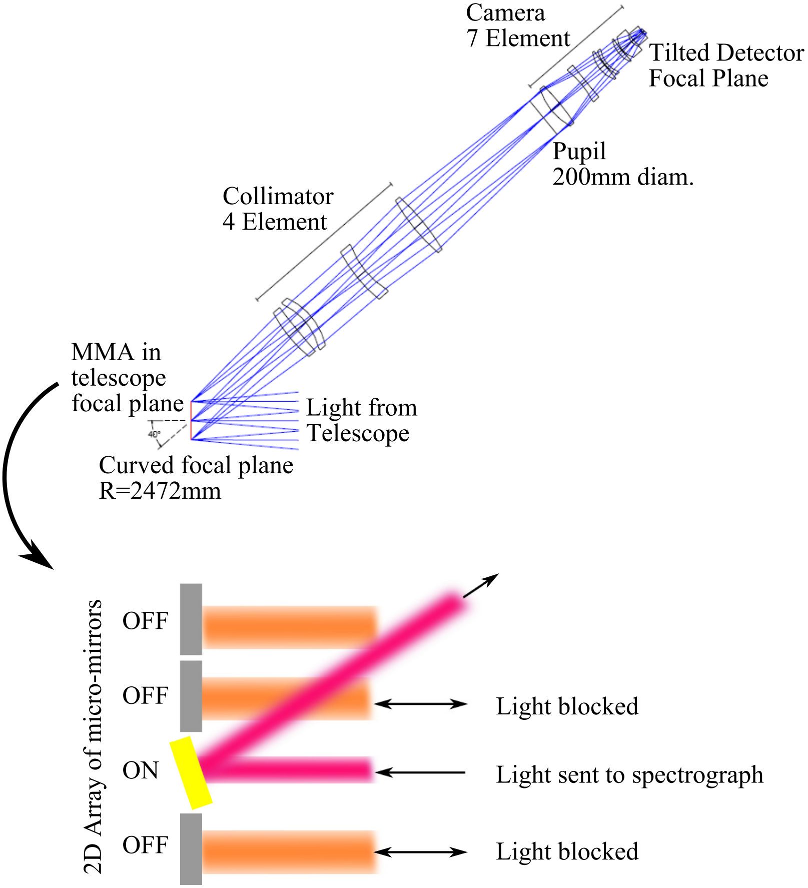

Figure 3.1: SMART-MOS with MMA: general optical system layout (from [18]) and working principle of the micro-mirror array as reflective slit-mask.

The point spread function (PSF) of the selected objects must be preserved; aberrations of the mirror in the medium and low spatial frequency spectrum change the shape of the PSF and high frequencies add a halo and consequently reduce the signal to noise ratio; to minimize all these effects we specify the contribution to the waveform error to be below $\lambda/20$, with $\lambda > 1\mu$m, and the roughness (high frequency) to below 1nm RMS.

The above contrast definition accounts only for incident light on the MMA and assumes that no other light sources, in particular the MMA itself, are present. Therefore it is required to avoid black-body radiation in the wavelength range of interest of any elements in or near the optical path. This implies that the elements must be cooled to cryogenic temperatures; for a sky background limited instrument operating in the near infrared range, i.e. $1\mu\text{m} \leq \lambda \leq 5\mu\text{m}$, the operation temperature of the component must be below 100K and for $5\mu\text{m} < \lambda \leq 28\mu\text{m}$ the MMA must be cooled to below 30K. This requires that the MMA is functional and fulfills all specifications at these temperatures.

**Scientific efficiency** The scientific efficiency is driven by the demand for maximizing the acquired information within given observation time. The amount of information is related to the light throughput of single objects and the number of objects that can be accessed and the flexibility with which the objects can be selected.

One astronomical object is set to fit one mirror in order to maximize throughput and complying with the considerations in Sec. 1.4. This implies a mirror size of at least $100 \times 200\mu\text{m}^2$, in order to correspond with the projected plate scales of 1"/mm to 2"/mm. The throughput is further related to the geometrical fill-factor of the array; a fill factor of more than 90% within one array is essential, at least along the long slit direction.

The number of objects that can be accessed by the MEMS-MOS system depends on the active surface, i.e. the percentage of the field of view of the MOS that is covered with actuatable micromirrors. According to [18] it should be possible to select sources from within at least 50% of the nominal MOS FOV. SMART-MOS was conceived as an instrument adressing a large FOV, which for E-ELT implied a field of over one arc minute [ibidem]. This would suggest that a surface of about $0.5 \times 0.5\text{m}^2$ would need to be covered with micromirrors. Covering this, in MEMS terms huge, surface is only feasible using a mosaicking approach, where “small” arrays are used as paving stones or tiles to cover an “arbitrary” large surface. Such a mosaicking approach requires an advanced concept for mechanical and electrical interfacing of the individual tiles to each other and to the substrate. The trade-off to make in terms of the size of an individual tile is fabrication yield (which generally drops with increasing die size) versus over-all fill-factor (increasing with increasing tile-size) and effort for assembly (decreasing with increasing tile size). We set the size of one individual MMA to 200 × 100 micromirrors; this corresponds to an approximate chip size of $20 \times 20\text{mm}^2$, which is in the range of the largest state-of-the art MMA (see Sec. 1.3). Approximating a curved focal plane with $R = 2$m tiles of $20{\times}20\text{mm}^2$ would require a minimum depth of focus of $2.5\mu$m, which can easily be obtained (see further below).

Further related to the scientific efficiency is the time needed to establish a certain selection pattern; in order to distinguish the MIRA approach from other approaches (micro-shutter array, semi-classical reconfigurable masks) we set the reconfiguration for the complete array to be less than 1s and demand the ability to reconfigure subsets of the array at even shorter times, enabling a scanning slit mode.

**Robust and simple system** Uniform tilt angle must be guaranteed over the whole array in order to send the light through a common pupil in the MOS. The tilt angle accuracy requirement is fixed by the F-number of the light ray on the array and the admissible oversizing of the pupil in the spectrograph; for F/10 and pupil oversizing of 20% a maximum slope error (peak-to-valley tilt-angle variation) of 17arcmin is admissible. For F/6 with the same pupil oversizing 30arcmin would be admissible. Note that this trades-off with the depth of focus. F/10 would yield a depth of focus of $139\mu$m and F/6 $50\mu$m (allowing a maximum wavefront error of $\lambda/20$ for $\lambda = 1\mu$m). A depth of focus of $50\mu$m should still be suffisiant if the curved focal plane is approximated by polygonal approximation (the minimum required depth of focus for a focal plane radius of curvature of 2m and tile size of $20{\times}20\text{mm}^2$ being around $3\mu$m). For comparision, with the same oversizing, F/20 would imply a maximum slope error of 8arcmin and a depth of focus of $554\mu$m. For MIRA we set the goal to below 10arcmin tilt-angle uniformity and the minimum requirement to 30arcmin.

The tilt-angle uniformity in ON position must be achieved without feedback and in particular without individual mirror control. This requirement is a necessity given the very large total number of micromirrors that will be employed in a real MOS and the particular operation environment. Furthermore, the mirror actuation should be conceived such that the switch characteristic is common for all micromirrors, e.g all mirrors can be switched with the same voltage magnitude to the ON state, which enables the use of rather simple driving electronic.

Concerning the driving of the MMA two requirements are imposed. In order to minimize thermal input in the cryogenic environment the power consumption of the MM actuation mechanism should be minimized—with a special focus on the power consumption in the hold mode, as this is the moment, where the measurements are taken and all thermal spoiler sources must be minimized. There is no precise specification on the power consumption of one MM for the switch and the hold operation. However, considering the different actuation methods, one can clearly distinguish between high and low power consumption actuators. E.g. in steady-state electromagnetic actuation is considered as a high power mechanism, whereas electrostatic actuation is a low power consumption mechanism. The second requirement relates to the actuation voltage magnitude. Especially electrostatic actuation often requires high driving voltage. From a system point of view there are two reasons to limit the driving voltage. First, the design rules for spacing between conducting lines increases drastically above 150V—this means important restrictions on wiring density. Second, several CMOS technologies with reasonable transistor size exist that go up to around 100V. Beyond that value, the available (standard) technologies feature much larger transistor size, which leads to increased device size and cost. The maximum allowable driving voltage is set to 100V.

The reconfiguration time, i.e. the time needed to change from one certain slit pattern to another one was set to 1s. This requires an actuation and addressing scheme with a certain degree of parallelization; for a line-by-line switching scheme and assuming 200 mirror lines, a switching time of 5ms for an individual mirror is allowable. The first resonance frequency is set to >1kHz, which should be sufficient to yield the required switching time. Note that the first resonance frequency can also be considered as degree for the shock-resistivity of the device; however at this point no explicit acceleration levels for shock resistivity are specified.

**MMA Specifications** Based on the above considerations a set of specifications for a MMA suited for the use in a future MOS is given in Tab. 3.1. The specifications must be considered as working base and may be adapted in function of the target instrument. Note that the contrast value is not a direct specification on the MMA component but a requirement on the MMA-MOS system performance. It is explicitly translated into the tilt-angle specification. Implicitly this requirement specifies that potential stray-light sources

Table 3.1: MIRA Requirements

| Item | Value |
|---|---|
| Contrast[a] | $\geq$1000, goal: $\geq$3000 |
| Tilt-angle OFF-ON | $\geq 20°$ |
| Tilt-angle uniformity ON state[b] | 30arcmin, goal: 10arcmin |
| Mirror Flatness | $\lambda/20$ with $\lambda > 1\mu$m |
| Surface Roughness[c] | $\leq$1nm RMS |
| Mirror Size | $100\times200\mu\text{m}^2$[d] |
| Array Size | $200\times100$ |
| Fill Factor | 95% along the long slit direction |
| Resonance frequency | $\geq$1kHz |
| Actuation Voltage | $\leq$100V |
| Operating Temperature | $\leq$100K, goal: $\leq$30K |

[a] Requirement on the MMA-MOS system performance

[b] Maximum tilt-angle deviation of any two mirrors within the array in ON-state with respect to an external reference plane. The absolute value of the tilt-angle in the ON state depends on the optical design of the target system. Note that the uniformity of the tilt-angle in the OFF state is not specified.

[c] AFM roughness on a $10\times10\mu\text{m}^2$ measurement field

[d] Typical value; smaller and larger mirrors should be conceivable

within the MMA must be minimized.

## 3.2 Micromirror Device

In order to accommodate for the required large out-of-plane movements of 20° for the relatively large $100\mu\text{m} \times 200\mu\text{m}$ micromirrors a two-substrate device configuration has been chosen. To comply with the requirement on micromirror flatness and operation in cryogenic environment, bulk micromirrors and an all-silicon (single crystalline and poly-crystalline) architecture for mirrors and structural elements has been implemented. Silicon has a low CTE value of around $2.5\cdot10^{-6}$ at room temperature and near zero below 150K which makes it an excellent material for minimizing thermal expansion and related thermal strains, required for operation at low temperatures.

The first substrate of the two-level architecture contains the movable mirror elements, a static frame and flexible beam elements connecting the individual mirror elements to the common frame. The mirrors are according to the requirements of rectangular shape and the structural frame is arranged such that it runs along only the long side of the mirror, which makes near 100% fill-factor possible along this direction. This is particularly useful for implementing the long-slit mode. Note that the long-slit must be perpendicular to the diffraction direction from the spectrograph, thus, the frame is parallel to the micromirror tilt-axis. We shall denote this first substrate the mirror chip.

The second substrate, referred to as the electrode chip, contains the actuator elements, which are used to deflect the mirrors to the desired tilt-angle, wiring elements, which interconnect the actuator elements to an outside control entity and spacer elements, which provide an adequate spacing and mechanical interface to the mirror chip. The two chips are fabricated separately and joined afterwards to yield a functional device.

According to the requirements the ON position must be accurate—hence we define the OFF state as the idle (unactuated) state and the ON state as the active (actuated) state, as the actuation mechanism can be used to force the mirror in a well defined position. On the other hand, the idle position is underlying a certain statistical distribution which is defined by the architecture of the device and the control of fabrication processes. The OFF-ON switching is done with an electrostatic actuator consisting of the mirror itself and the counter electrode on the electrode level. The ON state is hold by the same actuation mechanism and the OFF-ON transition is carried out with the elastic energy stored in the mirror suspension spring.

Figure 3.2 (a) shows schematically the architecture and functioning of one micromirror element.

### 3.2.1 Mirror Element

According to the requirements one micromirror must be $100\mu$m × $200\mu$m in size. This requirement depends on the plate scale of the considered telescope—conceptually, smaller and larger mirrors are possible with the current approach. We set the $100\mu$m × $200\mu$m-size as baseline—larger mirrors of $250\mu$m × $500\mu$m in size have been implemented for showing feasibility.

In order to have mirrors with a planarity better than $\lambda/20$, the mirrors must be inherently flat and strain-free. Therefore single crystalline silicon is chosen as mirror substrate. The substrate must be sufficiently thick such that the mirror is not deformed due to strains that occur during actuation

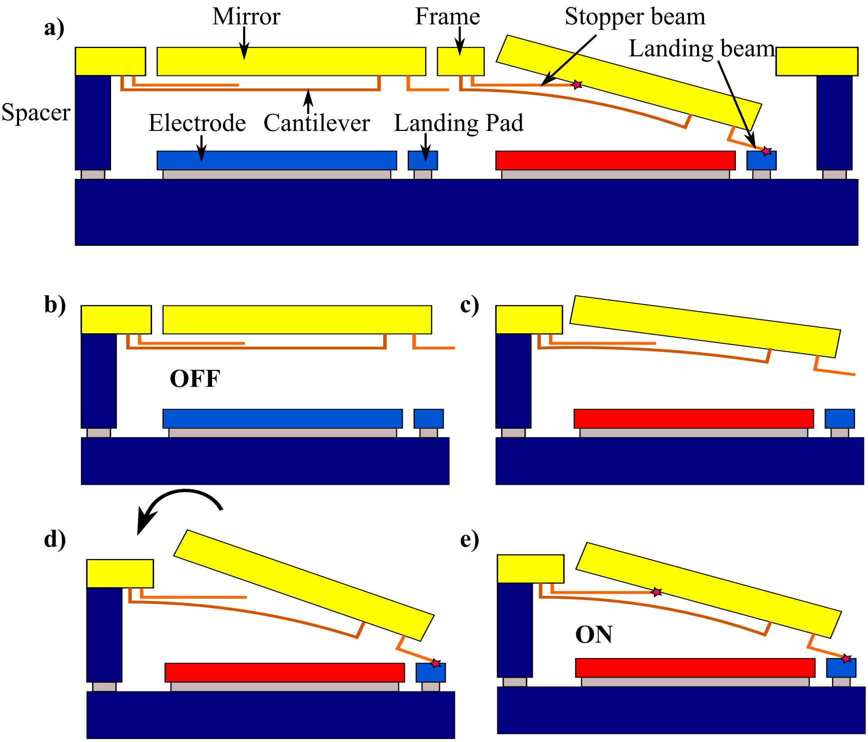

Figure 3.2: Schematic view of the MEMS-mirror concept. a) The device consists of a mirror element suspended via spring elements to a fix frame. On a second level an electrode and a landing zone is located. The two levels are separated by a well defined spacer element situated on the electrode level. b)-d) Actuation concept: The mirror element is tied to zero volt and a positive voltage is applied to the electrode. Due to the electrostatic force the mirror rotates upwards (c) until the first stopper beam, which is attached to the mirror, hits the electrode (d). Then the mirror starts rotating in the inverse direction until it hits the second stopper beam, which is attached to the mirror frame (e), and remains electrostatically fixed in this position.

nor due to the intrinsic stress of a reflective coating or thermal stresses arising when cooling down the device to the cryogenic operation temperatures. A gold coating is needed for good reflectivity in the infrared range since bare silicon is transparent for $\lambda > 1.1\ \mu$m. The effect of the metal coating on the mirror planarity can be minimized by using a sandwich-style coating, that is coating the front and the back side of the mirror with the same thickness of the same material. Note that the minimum required thickness to achieve a certain flatness increases with the mirror size.

While a maximum mirror-thickness is desired for maximum flatness, thin mirrors are preferred in order to minimize their inertia and the gap size between the mirrors. The inertia is related to the resonance frequency; less inertia means a higher resonance frequency for a given spring stiffness. The minimal achievable gap width is related to the substrate thickness by the maximum aspect ratio imposed by the etching technology. A gap size as small as possible is desirable for maximizing the fill factor and minimizing stray light originating from below the mirror array.[1] A reasonable thickness for the $100\mu$m $\times$ $200\mu$m-sized mirrors is in the range of $5\mu$m to $15\mu$m.

### 3.2.2 Spring Suspension

The spring suspension holds the micromirror in its idle position (OFF). It acts as restoring mechanism to switch the mirror from the OFF to the ON position. The spring suspension is quantified in terms of stiffness values for the different degrees of freedom: in-plane, out-of-plane, tilt around x-axis and tilt around y-axis. Ideally the spring suspension is compliant with respect to the nominal movement, i.e. tilt around x-axis, and stiff with respect to all other degrees of freedom, suppressing the unwanted movements. Below we refer to the stiffness around the x-axis as the spring stiffness.

Two requirements define the limits of the stiffness of the spring suspension. The lower limit is imposed by the requirement on the resonance frequency: for a given inertia of the mirror the resonance frequency is proportional to the square root of the stiffness value of the spring suspension. The upper limit is set by the maximum force/torque that the actuator can provide.

The spring suspension might be a flexion (or cantilever) type or a torsion

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[1] In the TI DMD based applications the gap size is also of concern related to instrument black body radiation; in our approach by concept the black body radiation is sufficiently suppressed by cryogenic cooling, which is only possible to a certain extend in the case of TI DMD MOS [62].

type spring or a combination of these. Figure 3.3 shows schematically the two suspension spring configurations. Principally any stiffness value, within a certain design range, can be reached with both spring-types by adapting their geometrical dimensions. The upper and lower limit for the stiffness design range is imposed by the design rules, which depend on the fabrication technology and materials used.

Concerning the above functional requirements towards the spring suspension, the torsional suspension can be considered as near-ideal. It blocks all degrees of freedom to a great extend except for the (wanted) rotation; furthermore the axis of rotation coincides in good approximation with the long side of the torsion beam and is thus, geometrically well defined. Although a cantilever (or flexion beam) suspension can also be conceived such that the in-plane degrees of freedom are blocked, it will allow a certain flexibility towards the piston movement, as the piston stiffness is coupled to the (wanted) out-of-plane tilt stiffness. In both configurations the stiffness of the spring system towards the (parasitic) piston motion defines the final position (and thus the tilt-angle); a variation of the spring stiffness across a mirror array (yielding from process variations) will therefore lead to a variation of the tilt-angle. Thus in order to comply with the uniform tilt-angle requirement the piston stiffness of the spring must be independent of process variations. This can be achieved by introducing additional structural beams, hereafter denoted as stopper beams, that block the piston degree of freedom of the mirror at a certain point. This concept is described further below in the actuator section and illustrated in Fig. 3.2. As the stopper beams are structural elements (i.e. do not have to provide flexibility as the suspension beams) they can be conceived such that its stiffness towards piston movement is orders of magnitude larger than the stiffness of the suspension spring and thus tune the vertical stiffness such that the process-induced variations on the tilt-angle variation are within the uniformity requirement.

In order for such a concept to work, the intrinsic stiffness of the spring suspension towards the piston movement must be sufficiently low such that it allows the mirror to settle on the stopper beams. Practically, this is only conceivable with a cantilever suspension type. Thus, even though the torsion beam has intrinsically a higher stiffness towards the piston movement the cantilever suspension is the preferred option for achieving stable and uniform tilt-angles using the stopper beam system. The cantilever suspension with stopper beams is illustrated in Fig. 3.3 (c).

The cantilever spring suspension is situated on the back of the mirror plane. This hidden or stacked suspension configuration is a necessity to achieve the required fill-factor and contrast value. As the suspension is covered by the mirror (except for the small gap between mirror and frame), we have no stray light originating from the bent beams, which means less degradation of the contrast. Figure 3.3 (d) visualizes the hidden spring suspension. A special fabrication technology, a combination of bulk and surface micromachining, is required to accomplish this hidden suspension configuration.

### 3.2.3 Actuator

The actuator or actuation mechanism must provide the force on the micromirror to overcome the spring suspension stiffness and switch the mirror into a well defined position. Furthermore the actuation mechanism must hold the mirror in said position. Electrostatic actuation is well suited to fulfill the requirements. It combines low power dissipation, high stroke and simplicity on system level. Other actuation methods are conceivable for actuating micro-mirrors, but none of those would be suited for our application. Thermal and electromagnetic actuation are not conceivable as no heat sources are allowed in the system (and especially not in the proximity of the mirrors). Even though high strokes at low power consumption could be achieved with piezo-electric bending beams, piezo-electric actuation is not preferred as the technology for processing efficient piezo-electric layers is not easily available and above all, the risk of delamination from the silicon substrate in cryogenic environment due to a large CTE difference is high.

Electrostatic actuation requires (at least) two electrodes, at least one of them being movable. Applying a voltage between the two electrodes causes the mobile electrode to move, the type of movement being defined by the electrode arrangement and the suspension spring of the mobile electrode. The electrostatic actuator in our case consists of the mirror element itself, representing the movable electrode and fixed counter-electrode located on the electrode chip.

As the actuator is only used to switch and hold the mirror in one defined position, the electrostatic actuator can be operated in pull-in mode. Operation in pull-in is advantageous for switching binary actuators:

1. The actuator is used in the regime where it provides the largest force per applied volt
2. Sharp transition/step in the tilt-angle versus voltage curve → binary actuator

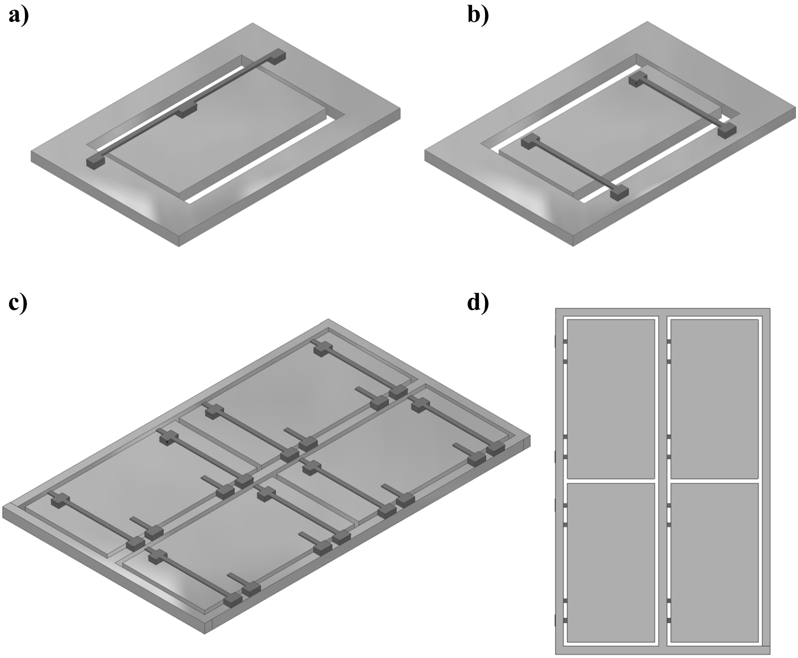

Figure 3.3: Suspension beam configuration and hidden spring concept. (a) Torsion beam suspension. (b) Flexion beam or cantilever suspension—this is the baseline suspension concept. (c) Cantilever suspension and stopper beam arrangement, illustrated on a 2×2 mirror array. (d) Hidden spring concept: here showing the optical side of a 2×2 mirror array—the cantilever suspension and stopper beams are hidden on the back side of the mirrors, thus, minimizing potential stray light originating from these structures.

3. Hysteresis: lower OFF-ON transition voltage than ON-OFF

The first point is a pre-requisite for the required low voltage (below 100V) requirement. The second and third property, the particular displacement versus voltage curve, enables the implementation of very efficient mirror addressing and actuation scheme. This scheme is proposed in Sec. 3.3 and is a crucial requirement for the implementation of very large mirror arrays in a MOS.

Operation in pull-in mode implies that the micromirror actually touches the electrode substrate. In order to avoid electrical short-circuit between the micromirror and the electrode and mechanical damage to the mirror substrate, a landing beam fixated on the mirror and a corresponding landing site on the electrode substrate is implemented. The landing beam on the mirror is less rigid than the mirror and damps the impact of the mirror on the electrode substrate. Furthermore it serves as anti-stiction feature: first it reduces the contact surface between mirror and electrode substrate, second by preloading the stopper spring it can be used to release the mirror 'by force' if the mirror sticks nevertheless[2]. The landing zone on the electrode provides the required electrical insulation between the electrode and the mirror.

The tilt-angle after pull-in (i.e. in the ON state) is primarily defined by the spacing between the mirror and electrode and secondarily by the spring suspension geometry. In order to achieve a tilt-angle of 20° a vertical gap of approximate $35\mu m$ is required for the $100\mu m \times 200\mu m$ sized micromirror[3]. It is obvious that for achieving a uniform tilt-angle over the MMA a uniform spacing between mirror and electrode layer is a mandatory (but not sufficient) condition. In order to achieve uniform spacing, distributed spacer elements are integrated on the electrode chip. By fabrication, the height of these elements must be very uniform. As introduced in the previous section, a system of stopper beams located on the mirror frame is required to eliminate process-induced tilt-angle variations (given a uniform spacing). The functioning of the stopper beams during mirror switching is shown in Fig. 3.2: Once the mirror (i.e. the landing beam located on the mirror) touches the electrode, it will not stop moving but start to turn into the opposite direction around this new rotation axis. That is, the tilting angle tends to decrease once the mirror has landed, provided a sufficiently low stiffness of the suspension spring towards piston movement. This is due

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[2] This feature is utilized in TI's DMD; additionally they use a special forming atmosphere reducing the occurrence of stuck mirror to near zero [24].

[3] This value is obtained using a simple trigonometric relation $h = c \cdot sin(\alpha)$ where $\alpha$ is the tilt-angle, $h$ the vertical spacing between electrode and mirror and $c$ the mirror length.

to a non-zero (and opposite to the mirror tilting motion) torque around the point where the landing post is attached to the mirror. The reverse turning movement is stopped at a well-defined tilt-angle by the stopper beam attached to the frame adjacent the mirror. The mirror is now electrostatically latched in a position defined by the geometry of the landing and stopper beams and the spacing between electrode and mirror.

### 3.2.4 Array and Device Architecture

Large arrays are required as building blocks to cover large surfaces in the focal plane of the telescope. Conceiving an n×m array of micromirrors is a fundamentally different task than conceiving a single micromirror and multiplying it by n×m. In other words the device concept differs for a micromirror device with single mirrors (or very small arrays) and for large arrays. The development of a large micromirror array is separated in two phases:

- Develop and implement the concept for single mirrors and small arrays that fulfill the specifications on the single micromirror elements (MIRA1)
- Develop and implement the concept for large arrays of micromirrors composed of micromirror elements that have been validated in a small array architecture (MIRA2)

**MIRA1** Single mirrors and small arrays of 5 × 5 are used to validate the device concept and provide a technological and conceptual base for the large array device. The device architecture is optimized for easy assembly and controlling, still providing the required single mirror performance. Large self-aligning spacers on the electrode (and a counterpart on the mirror chip) enable assembly "by hand" (see further below). The electrodes are wired one-to-one to the outside world, enabling single mirror addressing without decent actuation scheme.

**MIRA2** The second generation of MMA feature array sizes, according to the requirements, of 200 × 100 (and some smaller arrays for test purposes). The main challenges going from small arrays towards large arrays are the tilt-angle, i.e. spacing uniformity over large surfaces, the handling and assembly of large chips and the driving/interconnectivity of a very large number of micromirrors. To provide a uniform spacing and support for the large micromirror surface, a multitude of supporting columns located on the

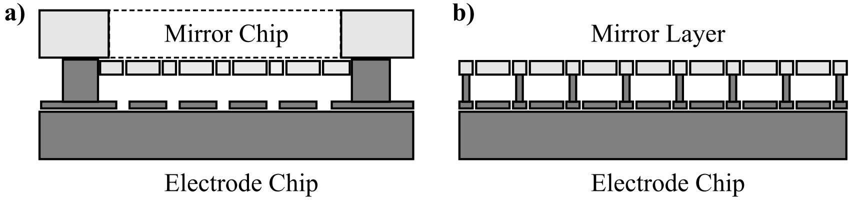

Figure 3.4: Array architecture. (a) Small arrays (MIRA1) (b) Large Arrays (MIRA2)

electrode chip is proposed. The columns support the mirror frame at two or more locations per mirror, i.e. for a 200×100 mirror array over 40'000 integrated columns are used. The location of the supporting columns on the (narrow) frame between the mirrors implies very challenging tolerances for the assembly of the mirror chip to the electrode chip. Furthermore, in order to avoid any mechanical constraints and resulting deformations, the mirror layer is conceived such that it is mechanically decoupled from the mirror chip handle layer before joining with the electrode spacer columns. A scheme for driving a large number of mirrors is proposed in the next section. This driving scheme enables the use of line electrodes and column electrodes. While line and column subdivision is implemented in smaller test arrays of 42 × 21 micromirrors, the 200 × 100 arrays of MIRA2 only feature line electrodes and thus just line-wise actuation is possible. Figure 3.4 illustrates the main difference in array architecture between MIRA1 and MIRA2.

## 3.3 Mirror Addressing and Actuation Schemes

The most elegant solution for addressing and actuating a large number of micromirrors would be using integrated CMOS circuitry—but, though not impossible from a technological point of view, it would be very challenging to implement such an approach regarding the many concurrent requirements (process compatibility with bulk micromachining, very large die sizes, high driving voltages, cryogenic environment, large temperature range, possibly ionizing radiation). A preferable solution is to have the driving electronics outside the cold environment such it can be optimized independent from the operation temperature of the MMA (which may be at room temperature, below 100K or even below 30K). This implies that the actuation voltages must wired to the micromirror arrays located in the focal plane of the telescope.

Direct wiring, that is one wire per mirror is not practical due to the huge number of micromirrors that will be used to cover large areas; for instance, for a surface of 0.5m x 0.5m, 25 arrays of 200 × 100 micromirrors, thus a total of 12.5 millions micromirrors, would be needed[4]. Using a column-line actuation scheme reduces the number of required individual voltages from $n \cdot m$ to $n + m$ for an array size of $n \times m$. Here a voltage $V_i$ is set to line i and $V_j$ to the column j, where $|V_i|, |V_j| < V_a$, $|V_i| + |V_j| > V_a$ and $V_i \cdot V_j < 0$, $V_a$ being the voltage needed to switch the mirror into the ON state. Hence all the mirrors remain unactuated except for the mirror in the intersection of line i and column j where we have $V_{ij} = |V_i| + |V_j|$. Technically the electrodes are electrically separated into lines and the mirrors into columns. Instead of using positive and negative voltages for lines and columns, one could use $V_i^{'} = V_b - V_i$, $V_j^{'} = V_b - V_j$, where $V_b$ is a bias voltage with $V_b > V_i, V_j$. In this case all the unused lines and columns must be set to $V_b$. The above actuation scheme holds true for actuating a single mirror at a time - exploiting the hysteresis of the electrostatically actuated mirror enables the generation of arbitrary patterns.

Fig. 3.5 (a) shows a tilt-angle versus voltage hysteresis of an electrostatic actuated micromirror. The steep transition at 90V is considered as the switching between the OFF and the ON state, the corresponding voltage is the (minimum) actuation voltage $V_a$. The voltage where the mirror switches back from the ON in the OFF state is referred to as the release voltage $V_r$. Consider now a voltage $V_c$ with $V_r < V_c < V_a$. Imposing $V_c$ to a mirror will preserve its binary state; for switching the mirror from the OFF to the ON state a voltage pulse of $2\delta$ is added to $V_c$ and for the ON-OFF transition $2\delta$ is subtracted from $V_a$, with $V_c + 2\delta > V_a$ and $V_c - 2\delta < V_r$. For generating an arbitrary pattern, the following algorithm is proposed: First the voltage $V_c > 0$ is set to all the lines. Then a voltage $V_\delta < 0$ is set to the first column and $-V_\delta$ is added to all the lines corresponding to the mirrors to be actuated in the first column, having $V_c + 2V_\delta > V_a$ for the mirrors to be actuated and $V_c, V_c + V_\delta < V_a$ for all the others (Fig. 3.5 (b)). Next the voltage of the first column is set to 0 and all the lines again to $V_c$. This cycle is then effectuated for the columns 2 through n, yielding the desired actuation pattern. For resetting all the mirrors to the OFF state, all lines and columns are reset to 0V; for resetting a single line, the corresponding voltage is reset to 0V and in the case of a column, the corresponding column voltage is first pulled down to $-V_c$ and then reset to 0V.

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[4] Assuming the current micromirror dimensions of $100 \times 200 \mu\text{m}^2$ and a focal plane size similar to the one of the E-ELT.

This actuation scheme implies that the tilt-angle in the OFF position is not necessarily zero but corresponds to the tilt-angle at the $V_c$ voltage, which in above example would be around 3°. Similarly, the tilt-angle in the ON state does not correspond to the tilt-angle at the snap-in or $V_a$ voltage, which here would be 20°, but to the lower $V_c$ voltage (21°).

Thus, once the desired mirror pattern is established, the voltage $V_c$ of all lines must be set to a hold-voltage $V_h$ such that the tilt-angle difference of the mirrors in the ON and in the OFF state is $\geq 20°$ for all mirrors. Furthermore, in order to achieve a uniform tilt-angle across the whole array, the proposed stopper beam system must also work "left" of the pull-in point, ideally the mirror should be in a fixed position down to the release voltage. It is clear that although the ON tilt-angle would be uniform for all mirrors over the array (given the functioning of the stopper beams and a uniform spacing), the OFF tilt-angle will be subject to variation over the array. As there is no hard specification on the uniformity of the OFF angle, this is not an issue, as long the above condition on the hold-voltage $V_h$ and tilt-angle difference ON-OFF is met.

In order to be able to implement this and other driving schemes, a dedicated driver electronic board was conceived. The driving electronics feature 64 independently addressable high voltage channels (up to 200V). The HV channels can be controlled through an USB interface and custom software, such that easy control with a simple PC is possible.

## 3.4 Fabrication and Assembly

The overall fabrication concept includes the following elements:

- Processing of the mirror chip
- Processing of the electrode chip
- Assembly of the mirror chip to the electrode chip
- Packaging of the assembled mirror device

Whereas the fabrication technology of the individual elements is the same for the small and the large array architecture, the assembly and packaging process is different for the two array generations.

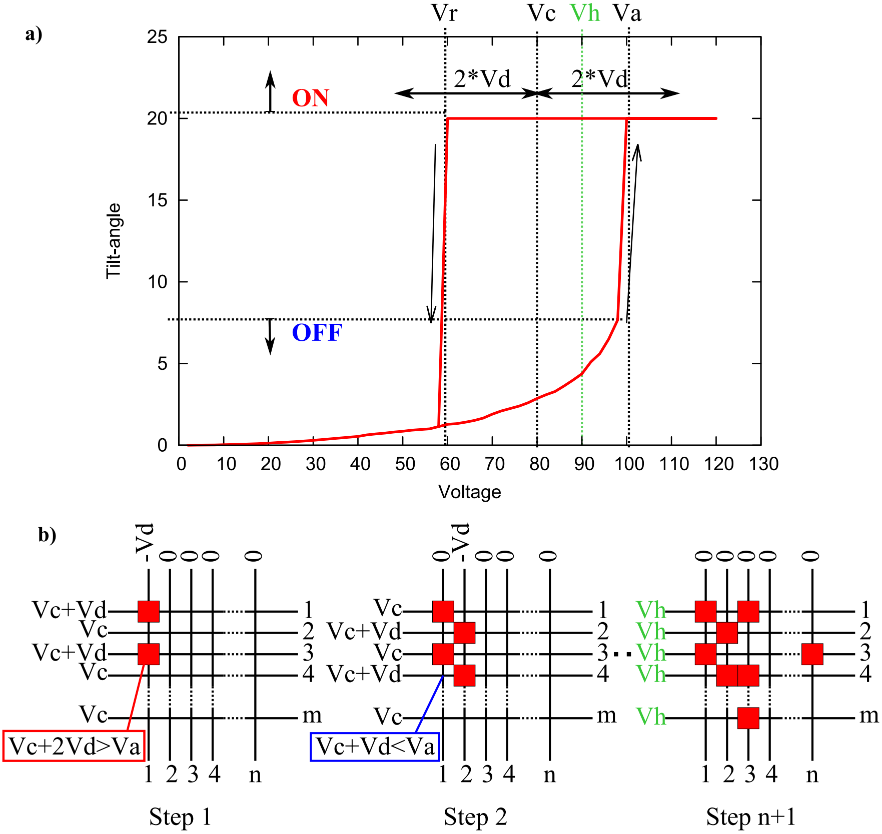

Figure 3.5: Electrostatic hysteresis of a micromirror without. The column-line addressing scheme is used to generate random patterns on large arrays—requiring only n+m voltages exploiting the electrostatic hysteresis of the micromirrors.

### 3.4.1 Mirror Chip

The mirror chip is made out of a silicon on insulator (SOI) wafer. The 10$\mu$m thick silicon on insulator layer (or, device layer) is structured into (horizontal) mirrors and frame by bulk micromachining. The optical active side of the mirror is the backside of the device layer, which must be released during fabrication. Intrinsically the device layer backside is optically flat in terms of roughness and, when released, optical flat in terms of planarity. The suspension structure and the landing posts are realized by surface micromachining of a deposited and doped polycrystalline silicon layer underneath the mirror and frame. Poly-silicon is used rather than another material as it has a thermal expansion coefficient similar to single crystal silicon. This is important for the operation in cryogenic environment. Physically, the polysilicon layer is deposited on the device layer after the trenches between the mirrors have been etched by deep reactive ion etching (DRIE). This implies that these trenches must been refilled before deposition of the polysilicon layer. A basic refill technique is the use of a thermal oxidation step.

### 3.4.2 Electrode Chip

In order to assure the thermal expansion compatibility with the mirror chip, the electrode chip is also based on a SOI wafer. Beside the electrodes, connecting lines and connecting pads, the electrode chip also contains the spacer elements, which ensure a constant gap between the electrode and the mirror chip. The spacer height is fixed and defined by the thickness of the device layer of the electrode chip, therefore the uniformity of the spacer height (and the uniformity of tilt-angle) depends on thickness-uniformity of the device layer.

A two step-DRIE (or delay mask process, see Sec. 2.2, is utilized to yield two height levels; the upper level is utilized for the spacer (having the height of the initial thickness of the device layer) and the lower level (height controlled by timed-etching) is utilized for the electrodes, connecting lines and bonding pads (in MIRA1 also for the landing pads).

### 3.4.3 Assembly

Table 3.2 summarizes the requirements on the assembly procedure imposed by the concepts of the small and large array architecture. The assembly of the mirror part and the electrode part is done on chip level, i.e. on released devices rather than on wafer level. Even though a wafer level assembly

| | Small Array | Large Array |
|---|---|---|
| Assembly technique | Passive possible | Active |
| Alignment precision | $10\mu$m | $1\mu$m |
| Chip max. dimensions | <5mm | >20mm |

Table 3.2: Requirements on assembly technique

or bonding approach would be advantageous in terms of device fabrication throughput, the required alignment precision for the large array architecture is very difficult to achieve with the available equipment. Developing a wafer level bonding technique for the small array architecture would not be sensible, as the small MMA is meant as an intermediate development step towards the large array device.

In the spirit of rapid prototyping, the small array device is conceived such that the assembly procedure requires no dedicated tooling and setup, i.e. the alignment can be done passively. Due to the different device architecture of the large arrays, imposed by the size of the array, passive alignment here is not possible.

### Small arrays

Once the two chips are brought into contact, where the mirror chip is put upside down on the electrode chip such that the handle layer of the mirror chip lies on the spacers of the electrode chip, guiding structures allow passive alignment of the two chips. A clip system, integrated in the device layer of the mirror chip, snaps in once the mirror chip is in the aligned position and holds it there. For permanent fixation a small amount of glue dispensed on the spacer elements before assembly may be necessary.

### Large arrays

The assembly of the large arrays relies on the fact that the mirror membrane is mechanically decoupled from the mirror chip substrate. The basic idea is that the mirror layer is completely freed of any mechanical constraints, such that it can be posed seamlessly on the column array of the electrode, without incorporating new strains and stresses (as it would be the case when forcing the two layers together). In technological terms the device layer part of the mirror membrane must be completely released from the handle layer before assembly and only loosely held within a handle layer frame. Once the mirror layer is bonded to the electrode chip, this handle frame must be removed from the assembly. This is done through the use of thin polysilicon latches that loosely ties the mirror layer to the handle frame during assembly and that can easily be cut, by electrical glowing or mechanical shock, after assembly. Alternatively, the mirror handle frame could be left as a protection on the assembled device during further post-processing (e.g. packaging).

Such an assembly procedure requires high-accuracy alignment tooling and special chip holder to handle the fragile structures. For this purpose a custom assembly setup was conceived which allows relative positioning of the two chips with high accuracy in six degrees of freedom (DOF). The setup comprises further specialized vacuum grippers for handling the very fragile, released mirror chip and a hot-plate for the bonding operation. A white-light interferometer is used for 6-DOF position feedback.

For the bonding of the two chips a thin glue layer at the chip edges is utilized; conceptually, the mirror layer should then be flattened, i.e. pulled against the supporting columns of the electrode chip *in operation* (due to a net electrostatic force on all mirrors; utilizing the row-column actuation scheme a constant force bias is present on all mirrors). At a further stage, a complete bonding of the columns to the mirror layer frame could be envisioned. This could be for instance a gold-silicon eutectic bonding, which would require the deposition of a metal layer either on the mirror frame or the electrode columns.

# Chapter 4

# Modeling and Design

## 4.1 Parameters and Boundary Conditions

The geometrical parameters of the micromirror device are depicted in Fig. 4.1 and summarized in Tab. 4.1. The schematic layout of the micromirror design presented in Fig. 4.1 descends from the conceptual considerations in the previous chapter and only geometrical features are represented that are relevant for device modeling—the complete layout is presented in the last section of this chapter. The global coordinate system is right-hand Cartesian and defined as follows: z is the surface normal to the mirror (top side) in the OFF-state. y is parallel to the long-slit direction, i.e. parallel to the tilt-axis of the micromirrors. +y is defined such that the nominal rotation around the tilt-axis is positive (right-hand rule). x is defined through y and z. The parameter notation convention is the following: the main symbol indicates dimension: $w$ for width, $l$ for length, $t$ for thickness, $h$ for height and $o$ for offset; the subscript indicates the concerned element (e.g. $c$ for cantilever).

The boundary conditions for the geometrical parameters (indicated in Tab. 4.1) are given by common MEMS-design rules, specific technological limitations, geometrical and conceptual implications. The technological related design rules and boundary conditions are summarized in Tab. 4.2. The alignment accuracy between two photolithography steps is based upon personal experience on the available equipment at the COMLAB (see Sec. 5); the minimum polysilicon thickness was determined by experiment: structures thinner than 0.5 $\mu$m showed a low fabrication yield. The condition on the maximum design stress of bending structures (which applies here to the cantilever suspension) is deduced from the fracture strength (or yield stress) of polysilicon: we impose a maximum design stress of 25% of the fracture strength. Yield stress and other properties of the utilized materials are summarized in Tab. 4.3 and Fig. 4.2.

In the next three sections the requirements given in 3.1.2 are translated, using the micromirror concept established in the previous chapter, into a set of geometrical parameters. First, the model and the physics are elaborated, which link the geometrical parameters to the device performance parameters. Second, a device design, which consists of a set of geometrical and corresponding device performance parameter values, is chosen such that it fulfills the requirements. The last section presents the physical layout descending from the device design and the device concept.

## 4.2 Modeling

### 4.2.1 Surface Quality

The surface quality or flatness is characterized by the (local) roughness and the topography (or deformation) of the surface. In this section we focus uniquely on the surface deformation, i.e. the peak-to-valley deformation $\Delta$[1]. The maximum allowable peak-to-valley deformation is $\Delta \leq \lambda/20$ with $\lambda \geq 1\mu$m, thus we have an allowable "deformation budget" of 50nm. Intrinsically a mono-crystalline and polished silicon surface is supposed to be flat. There are a variety of factors that may degrade the flatness of the micromirror surface and contribute to the deformation budget:

1. Initial non-uniformities of the silicon substrate due to polishing errors
2. Partial plastic deformation during fabrication
3. Stress at the interface between single-crystalline micromirror and polycristalline suspension
4. Intrinsic stress of the reflective layer on top of the mirror
5. Thermal stress due to the mismatch of the coefficient of thermal expansion (CTE) between silicon and reflective layer in cryogenic environment

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[1] The local roughness of a polished silicon wafer is around 0.3nm RMS and thus sufficiently smooth. During fabrication of the micromirrors, the surface of the mirror remains protected by the buried oxide of the silicon-on-insulator (SOI) wafer and thus no defects should be created.

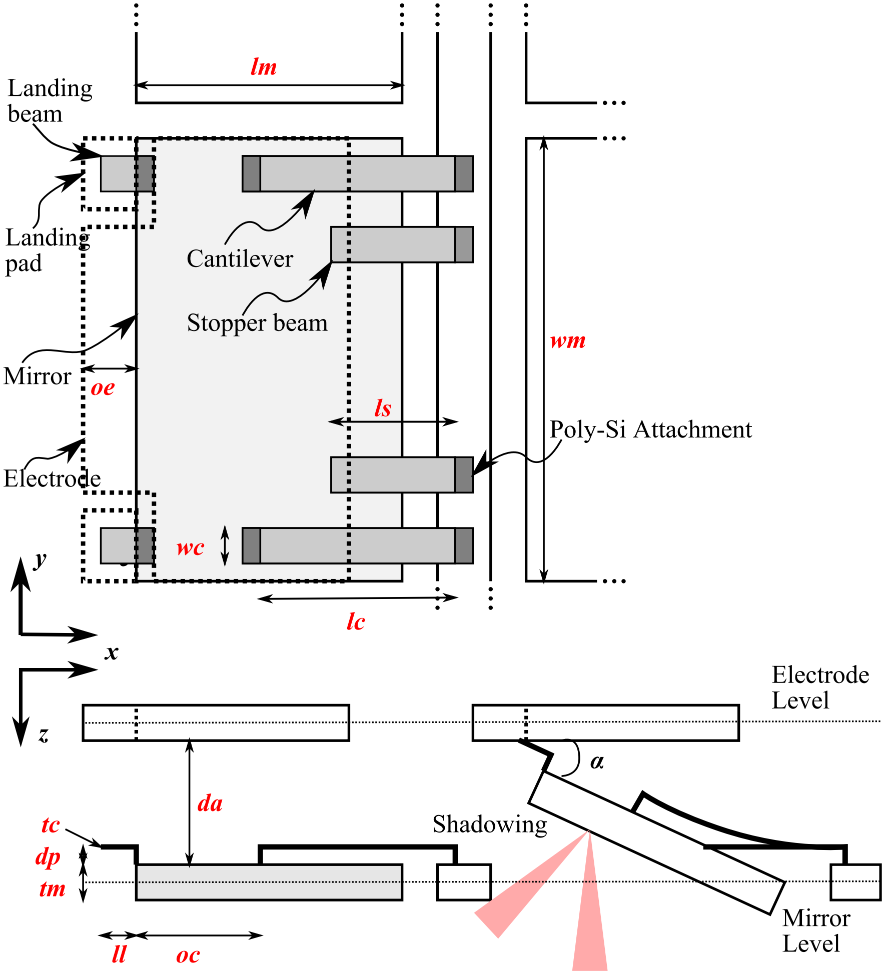


Figure 4.1: Geometrical parameters and coordinate system

Table 4.1: Geometrical parameters of the micromirror device

| Item | Symbol | Min [$\mu$m] | Max [$\mu$m] |
|---|---|---|---|
| Mirror | $m$ | - | - |
| Width | $w_m$ | 100 | 250 |
| Length | $l_m$ | 200 | 500 |
| Thickness | $t_m$ | 5 | - |
| Cantilever | c | - | - |
| Width | $w_c$ | 1 | 100 |
| Length | $l_c$ | - | 100 |
| Thickness | $t_c$ | 0.6 | 2 |
| Offset | $o_c$ | 5 | 100 |
| Vertical dist. to mirror layer[a] | $d_c$ | 1 | 3 |
| Anchor width on frame | $w_{ca}$ | | |
| Anchor length on frame | $l_{ca}$ | | |
| Stopper Beam | $s$ | - | - |
| Width | $w_s$ | 1 | - |
| Length | $l_s$ | - | - |
| Thickness | $t_s$ | $= t_c$ | |
| Landing Beam | $s$ | - | - |
| Width | $w_l$ | 1 | - |
| Length | $l_l$ | - | - |
| Thickness | $t_l$ | $= t_c$ | |
| Landing offset | $o_l$ | - | - |
| Electrode | | | |
| Electrode offset | $o_e$ | - | - |
| Electrode height | $h_e$ | - | - |
| Spacer (column, pillar) height | $h_p$ | - | - |
| Various | | | |
| Air height (spacing) [b] | $d_a$ | - | - |
| Gap (or trench) width | $w_g$ | 1 | - |
| Frame width | $w_f$ | | |

[a] Vertical distance between mirror and polysilicon structures

[b] Vertical distance between mirror and electrode

Table 4.2: Technological boundary conditions and design rules

| Item | Unit | Value |
|---|---|---|
| Alignment accuracy photolithography | $\mu$m | 3 |
| Min thickness of LPCVD polysilicon | $\mu$m | 0.6 |
| Generic process variation for material thicknesses[a] | % | 20 |
| Generic process variation for structure widths[b] | % | 20 |
| Minimum feature width on photolitho mask | $\mu$m | 1 |
| Maximum allowable bending stress[b] | MPa | 500 |

[a] Peak-to-valley variation across a 4-inch wafer; worst case assumption for thickness variation of deposited materials (e.g. polysilicon layer) and for substrate thicknesses (e.g. device layer total thickness variation)

[b] Peak-to-valley variation across a 4-inch wafer; worst case assumption for variation of lateral underetching and dimensional reduction of structures

Table 4.3: Physical and material constants used for mechanical and electrical modeling. The coefficient of linear thermal expansion (CTE) for gold and silicon is given in Fig. 4.2

| Item | Unit | Value |
|---|---|---|
| Silicon | | |
| Young Modulus (110 plane) | $10^9 \cdot Pa$ | 169[a] |
| Density | $10^3 \cdot kg/m^3$ | 2.3[a] |
| Fracture Strength | $10^9 \cdot Pa$ | 7[a] |
| Linear Thermal Expansion T=300K | $10^{-6}/K$ | 2.6[b] |
| Linear Thermal Expansion T=100K | $10^{-6}/K$ | -0.5[b] |
| Polysilicon | | |
| Young Modulus | $10^9 \cdot Pa$ | 170[c] |
| Fracture Strength | $10^9 \cdot Pa$ | 2–3[d] |
| Air | | |
| $\epsilon \equiv \epsilon_0$ | $\frac{As}{Vm} \cdot 10^{-12}$ | 8.854 |

[a] Source: [34]

[b] Source: [1]

[c] Source: [30]

[d] Source: [51]

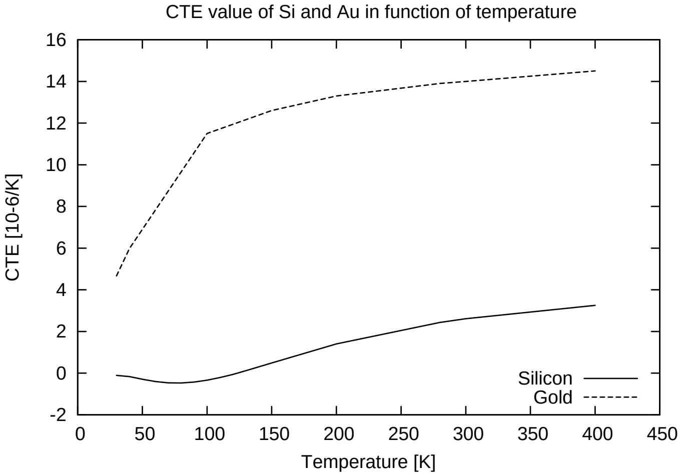


Figure 4.2: Coefficients of linear thermal expansion of gold and silicon in function of temperature. Sources: [1] (Si), [49] (Au)

6. Induced strain in the ON state of the micromirror

Factors one through three can be summarized into technology related, four through five into coating related and six into operation related deformation contributions. Measurements on completely processed and released micromirrors showed that the technology related factors contribute with roughly 10nm to the deformation budget (for 10$\mu$m-thick mirrors). The contribution of the forces acting on the mirror in the ON-state is below 0.5nm and therefore negligible, as finite element modeling showed (assuming a mirror thickness of 10$\mu$m and pressure levels extracted from coupled electromechanical simulations of the device, see Sec. 4.2.2).

The deformation of the substrate due to stressed thin film can be expressed to a good approximation by Stoney's formula [44]:

$$R \approx \frac{1}{6\sigma_f} \frac{E_s d_s^2}{(1-\upsilon_s) d_f} \tag{4.1}$$

where R is the resulting radius of curvature of the substrate, $\sigma_f$ the stress in the thin film, $E_s$ Young's modulus of the substrate, $\upsilon_s$ Poisson's ratio of the substrate, $d_s$ the thickness of the substrate (which equals $t_m$ the mirror height) and $d_f$ the thickness of the thin film. Eq. 4.1 is valid for $d_s >> d_f$. The peak-to-valley deformation $\Delta$ is obtained from the radius of curvature $R$ by a simple geometric relation:

$$\Delta = R\left(1 - cos\left(\frac{l_m}{2R}\right)\right) \tag{4.2}$$

where $l_m$ is the length of the mirror. For infrared operation the reflective coating is an evaporated 60nm thin film consisting of a 10nm chrome adhesion layer and a 50nm gold layer. Three different substrate thicknesses are considered: 5$\mu$m, 10$\mu$m and 15$\mu$m; Fig. 4.3 (a) shows the plots of the peak-to-valley deformation versus the stress in a 60nm thin film for the different substrate thicknesses.

The intrinsic stress for an evaporated gold film is reported to be around 260 MPa and for very thin chrome layer 1.6 GPa (both from [44] and at room temperature). These values of the intrinsic stress depend strongly on the thin film deposition system and the deposition parameters and consequently vary strongly across the literature. Therefore they are used here for estimation purpose only. We approach the yielding intrinsic stress of the Cr/Au bilayer by taking the weighted average of the individual contributions of the two layers: $\sigma_i = (\sigma_{Cr} + 5\sigma_{Au})/6 \approx 480$MPa. Using Eqs. 4.1 and 4.2 gives a peak-to-valley deformation of about 33nm for the 10$\mu$m substrate and about 15nm for the 15$\mu$m substrate, both at room temperature. The 5$\mu$m substrate would be deformed far beyond the maximum allowable peak-to-valley deformation of 50nm. Even though the chrome adhesion layer is very thin it adds a considerable amount of stress; chrome was chosen as adhesion layer as it is supposed to withstand the final HF vapor phase release step in the current fabrication process. However in a modified process, where the coating is applied as very last fabrication step, a titanium adhesion layer could be used instead. The intrinsic stress of very thin titanium films is reported to be near zero [44]. The total intrinsic film stress of a 10nm Ti/50nm Au bilayer would be then about 220MPa and the resulting deformation on the 10$\mu$m substrate 15nm at room temperature.

For predicting the mirror deformation at cryogenic temperatures the thermal stress in the thin film has to be taken into account. The thermal stress originates from the different shrinkage behavior of the thin film and the substrate when cooling down, i.e. from their CTE mismatch. Ansys FEM simulation has been used to study this effect. The mirror has been modeled by a thick substrate (mirror) and a thin layer on top of the substrate (coating). The linear coefficients for thermal expansion for silicon in function

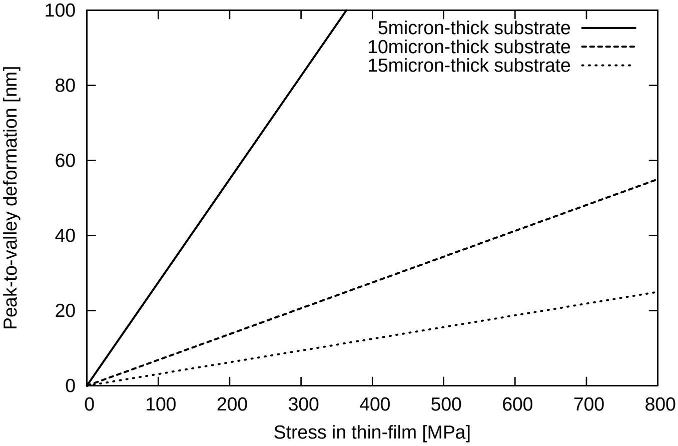
Table 4.4: Mirror deformation due to a stressed thin-film reflective coating at different temperatures.

| | Def.at temp. | | |
|---|---|---|---|
| Layer Stack | 300K [nm] | 100K [nm] | 30K [nm] |
| 10nm Cr / 50nm Au / 10$\mu$m Si | 33nm | 52nm | 57nm |
| 10nm Ti / 50nm Au / 10$\mu$m Si | 15nm | 34nm | 37nm |
| 10nm Cr / 50nm Au / 15$\mu$m Si | 15nm | 23nm | 26nm |
| 10nm Ti / 50nm Au / 15$\mu$m Si | 8nm | 15nm | 17nm |

of the temperature is found in [1] and the CTE($T$) for gold in [49]. The values are plotted in the inset of Fig. 4.3. For simplicity the thin-film is assumed to consist of gold only. As the CTE of chrome lies between gold and silicon, this assumption leads potentially to a slightly higher thermal film stress than in reality. The reference temperature is set to 300K and thus the thermal stress set to zero at this temperature. The thermal stress induced by the deposition at $T > 300$K is incorporated in the above values of the intrinsic stress. The simulated values of thermal film stress for temperatures between 30K and 300K is plotted in Fig. 4.3. Note that the thermal film stress goes almost linearly with the temperature—this is due to the fact that the difference between the two individual CTEs is almost constant with the temperature.

The total film stress is assumed to be the sum of the intrinsic stress (at 300K) and the thermal stress. The yielding peak-to-valley deformation of the micromirror is given by Eqs. 4.1 and 4.2 (graph in Fig. 4.3 (a)). Tab. 4.4 summarizes the peak-to-valley deformation for different substrate/coating combinations and temperatures. As stated in the beginning of the section, the contribution of the coating-induced effects (points five and six) to the total mirror deformation is almost an order of magnitude larger than all the other effects. According to the values from Table 4.4 the peak-to-valley deformation of the 10$\mu$m thick mirror is still within the specs at 30K using a titanium/gold bilayer as reflective coating. Using the chrome/gold coating the mirror deformation is still in the specs down to 100K. Therefore we set the minimum mirror thickness to 10$\mu$m.

a) Peak to valley deformation in function of stress in thin-film



b) Thermal stress of a gold layer on silicon

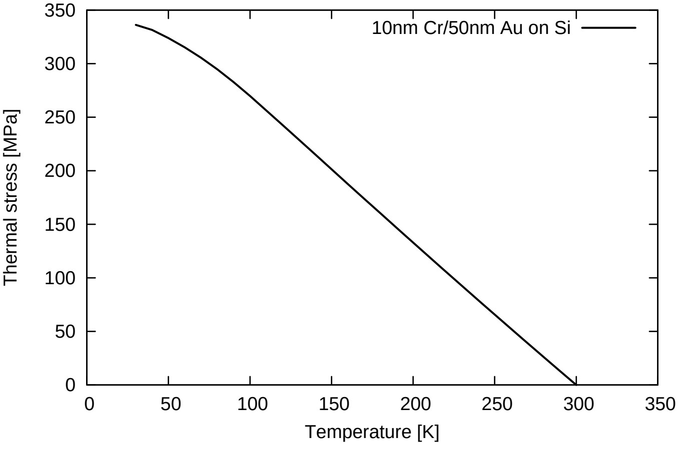


Figure 4.3: (a) Peak-to-valley deformation for a 100 × 200$\mu$m$^2$ mirror in function of the intrinsic stress of the mirror coating. (b) Thermal stress of a 50nm-thick gold layer (10nm chrome adhesion layer) on a silicon substrate; note that the zero-thermal stress temperature is set to 300K.

### 4.2.2 Electromechanical Performance

By concept the mirror movement is restricted to two degrees of freedom: out-of-plane translation or piston movement and out-of-plane rotation around an axis perpendicular to the cantilever suspension. We can restrain the modeling of the micromirror actuator to two dimensions—assuming the following conditions:

- The (parasitic) movement of the mirror in other degrees of freedom (DOF) is arbitrary well suppressed or is not performance-relevant

- The mirror-electrode system can be approximated as ideal parallel plate capacitor (no fringe fields) in the third dimension, i.e. $l_m >> d_a$.

The in-plane DOFs can be suppressed sufficiently well by adjusting the cantilever geometry such that the in-plane stiffnesses are orders of magnitude higher than the out-of-plane stiffness. The third out-of-plane DOF, the tilt around the axis that is perpendicular to the nominal tilt-axis, cannot be suppressed in a similar general fashion, as it is coupled to the wanted out-of-plane DOFs. However, this is of minor importance, as in operation the mirror is forced into a statically determined position. This position is given by the geometries of the landing and stopper beams and the parallelism between the mirror and electrode layer.

The second condition, i.e. the perfect parallel plate capacitor in y-direction, must be considered carefully; Feynman proposed a simple rule of thumb to correct for the effects at the plate edges: assume the real length (and width) of the plate capacitor to be extended by $\frac{3}{8}$ of the separating distance between the two plates [16]. We will estimate the error in the case of tilted plates using finite element modeling in Sec. 4.2.2.

The reduction of the three dimensional physical device to a two-dimensional model is schematically shown in Figure 4.4. The electromechanical behavior is modeled with an electrostatic and a mechanical model. The electrostatic model consists of a parallel (in operation tilted) plate capacitor which is used to calculate the electrostatic force and evaluate the electrostatic moment at the virtual attachment point of the cantilever to the mirror. The main element of the static mechancial model consists of a single-sided clamped cantilever, its free end corresponding to the mirror attachment point. Note that gravity effects are neglected throughout the modeling; a justification is given further below.

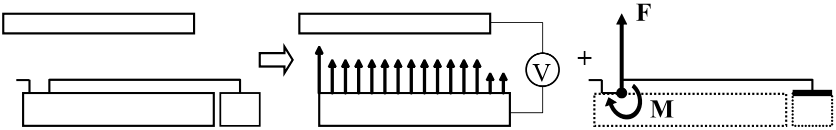


Figure 4.4: Modeling of the micromirror unit. The 3D model is reduced to a 2D model and split up into an electrostatic and mechanical model. The electrostatic forces acting on the mirror are replaced by a resulting force and moment acting on the endpoint of the suspension cantilever.

### Static Model

We consider the case of a cantilever suspension as shown in Fig. 4.4. The in-plane stiffness is assumed to be much higher than the out-of-plane stiffness, i.e.

$$\frac{k_y}{k_z} >> 1$$

$$\Longrightarrow \left(\frac{w_c}{t_c}\right)^2 >> 1 \qquad \text{(From Sec. 2.1)}$$

Thus, we assume the width of the cantilever to be much larger than its thickness. Furthermore if we consider that the mirror is much thicker and larger than the cantilever, we can assume the mirror to be rigid[2]. The electrostatic forces acting on the mirror can then be reduced to a resulting force and moment acting on the point where the cantilever is attached to the mirror, as shown in Fig. 4.4. The resulting piston movement $\delta$ and tilt-angle $\alpha$ due to the force $F$ and the moment $M$ is obtained by linear superposition, i.e. summation of the two individual contributions. Considering small deflections we can write for the z-deflection of the cantilevers end

$$\begin{aligned} \delta &= \delta_F - \delta_M \\ &= \frac{l_c^2}{EI_y}\left(\frac{Fl_c}{3} - \frac{M}{2}\right) \end{aligned} \tag{4.3}$$

---

[2] The deflection $\delta$ due to a force $F$ of a beam with rectangular section $wh$ can be written as $\delta \sim F/wh^3$. Assuming a beam with 10x0.5 $\mu$m section and a mirror with a 200×10 $\mu\text{m}^2$ section, having the same length, a force $F$ would deflect the mirror $20^4 = 160000$ times less than the cantilever.

and for the angle

$$\begin{aligned} \alpha &= \alpha_F - \alpha_M \\ &= \frac{l_c}{EI_y}\left(\frac{Fl_c}{2} - M\right) \end{aligned} \tag{4.4}$$

where $E$ is Young's modulus and $I_y$ the moment of inertia around the y-axis [58]. The moment of inertia is given with $I_y = w_c t_c^3/12$. Eq. 4.3 represents the (vertical) piston movement of the mirror and Eq. 4.4 the tilt angle. Inversely we can express the restoring (or reaction) force and moment of the cantilever in function of $\delta$ and $\alpha$ by rearranging Eq. 4.3 and Eq. 4.4:

$$F_c(\alpha,\delta) = \frac{6EI_y}{l_c^2}\left(\alpha - \frac{\delta}{l_c}\right) \tag{4.5}$$

$$M_c(\alpha,\delta) = \frac{3EI_y}{l_c}\left(\frac{2\alpha}{3} - \frac{\delta}{l_c}\right) \tag{4.6}$$

The electrostatic force $F_E$ is given by (Eq. 2.12, Sec. 2.1)

$$F_E = \frac{1}{2}\epsilon_0 w_m U^2 \int_{-o_c}^{l_m - o_c} \frac{1}{\left(\left(\frac{d_a-\delta}{\alpha} + x\right)\alpha\right)^2} dx \tag{4.7}$$

$$= \frac{1}{2}\epsilon_0 w_m U^2 \frac{l_m}{((l_m - o_c)\alpha + d_a - \delta)(-o_c\alpha + d_a - \delta)} \tag{4.8}$$

Consistent with the small deflection approximation we use $\sin\alpha \approx \alpha$.[3] In the initial position (and for small angles), i.e. $\alpha, \delta = 0$ $F_E$ becomes

$$F_E = \frac{1}{2}\epsilon_0 w_m U^2 \frac{l_m}{d_a^2} \tag{4.9}$$

which is the simple expression for the force in a parallel capacitor. Note that the required vertical spacing between mirror and electrode for a given tilt-angle in the ON state is given with the geometric relation $\sin(\alpha_{\mathrm{ON}}) \cdot o_c + \delta_{\mathrm{ON}} = d_a$; in a first approximation (assuming the rotation axis of the mirror going trough one end of the mirror) we pose $d_a = sin(\alpha_{\mathrm{ON}}) \cdot l_m$. Setting $\alpha_{\mathrm{ON}} = 20°$ and assuming a nominal mirror with $w_m = 200\mu$m and $l_m = 100\mu$m we can estimate the electrostatic force (in the initial position) using Eq. 4.9: For 100V we obtain a force of about 2.5$\mu$N. For a mirror with

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[3] For an angle of 20° this results in an error of about 4% for the sine function.

a thickness of $t_m = 10\mu\text{m}$ the maximum gravitational force that the mirror exerts on the cantilever suspension is $F_g \approx 5\text{nN}$ and thus insignificant.

For the electrostatic moment (or torque) we can write similarly (Eq. 2.13, Sec. 2.1)

$$M_E = \frac{1}{2}\epsilon_0 w_m U^2 \int_{-o_c}^{l_m - o_c} \frac{x}{\left(\left(\frac{d_a-\delta}{\alpha} + x\right)\alpha\right)^2} dx \tag{4.10}$$

Considering the special case $\alpha, \delta = 0$ we can simplify to

$$\begin{aligned} M_E &= \frac{1}{2}\epsilon_0 w_m U^2 \int_{-o_c}^{l_m - o_c} \frac{x}{d_a^2} dx \qquad (4.11)\\ &= \frac{1}{2}\epsilon_0 w_m U^2 \frac{l_m}{d_a^2}\frac{l_m - 2o_c}{2} \\ &= \frac{(l_m - 2o_c)}{2} F_E \qquad (4.12) \end{aligned}$$

**Condition of operation** It is obvious from Eq. 4.4 that for a mirror motion as shown in Fig. 3.2 (b) (in Sec. 3.2), we must have $Fl_c > 2 \cdot M$. If we have $Fl_c < 2 \cdot M$ the mirror tilts in the opposite direction.

Up to now it was assumed that the electrode and the mirror are congruent, i.e. $o_e = 0$. The case of $o_e \neq 0$ we model by multiplying the expressions 4.8 and 4.11 for $F_E$ and $M_E$, respectively, with a step function

$$e(x) = \begin{cases} 1 & \text{for } -o_c < x \leq l_m - o_c + o_e, \\ 0 & \text{else.} \end{cases} \tag{4.13}$$

i.e. we set the electrostatic pressure zero where no overlap between mirror and electrode exists. Note that only a shift of the electrode to the left, i.e. $o_e < 0$ is considered. Evaluating the condition $Fl_c > 2 * M$ using 4.8, 4.11 and 4.13 yields in

$$lc > l_m - 2o_c + o_e \tag{4.14}$$

According to the suspension concept (see Fig. 4.1) the cantilever length can be expressed by

$$l_c = l_m - o_c \tag{4.15}$$

assuming that the gap width $w_g$ is negligible compared to $l_m - o_c$. Using Eq. 4.15 we can re-write Eq. 4.14 to the operation condition:

$$o_c - o_e > 0 \qquad \text{(Operation condition)}$$

It follows that the suspension and electrode offset $o_c$ and $o_e$ are key parameters for the device performance. This impact is illustrated on the example of $o_c$, posing $o_e = 0$. By combining Eqs. 4.3, 4.4, 4.9, 4.12 and 4.15 we can estimate the influence of $o_c$ on the mirror angle $\alpha$ for a given gap height: in the ON-state the gap height can be approximated by $\delta + \alpha \cdot o_c$ and thus we can write the tilt-angle versus gap height ratio as

$$\frac{\alpha}{\delta + \alpha \cdot o_c} = 6 \frac{o_c}{6o_c^2 - o_c l_m + l_m^2} \tag{4.16}$$

In Fig. 4.5 Eq. 4.16 is plotted with $l_m = 1$. Note that the plotted function does not represent the angle at pull-in but gives solely an indication on the influence of the cantilever attachment offset on the force/moment ratio evaluated at the cantilever attachment point on the mirror and its impact on the tilt-angle/vertical displacement ratio. For a given position of the electrode there is a value for $o_c$ where the resulting tilt-angle/vertical displacement ratio is maximum (at $o_c = 1/\sqrt{6}$). The tilt-angle at a given air-gap is related to the bending shape of the cantilever; this is depicted in Fig. 4.5 (b). Note that the curvature of the bent beam and consequently the maximum bending stress are lower (maximum bending radius) for $o_c = (1/\sqrt{6}) \cdot m_l)$ than for $o_c = 0$.

**Pull-in behavior and stopper beam concept** Analytic modeling of pull-in modeling of our coupled degree of freedom model is rather involved; in order to promote basic understanding of the stopper beam concept we will rather utilize a strongly simplified approach. We transform our cantilever-suspended micromirror into two closing gap actuators, suspended with a spring of $k_1$ and $k_2$, respectively and a common fixed electrode and applied potential, as depicted in Fig. 4.6. The displacement of the two actuators are denoted as $z_1$ and $z_2$; the tilt-angle $\alpha$ we define then as $\alpha \propto (z1 - z2)$ and the piston movement $\delta$ as $\delta \propto (z_1 + z_2)/2$. We claim that $k_1$ and $k_2$ can be chosen such that they reflect the coupling between the two degrees of freedom (and also the geometrical coupling); the spring constants may be arbitrary complicated functions and in particular they might depend on $z_1$, $z_2$ and on each other, i.e. $k_1 = f(z_1, z_2)$ and $k_2 = f(z_1, z_2)$. Without knowing the exact functions we pose, translating the condition of operation (see above), $k_2 > k_1$.

As first approximation and strong simplification we assume that $k_1$ and $k_2$ are constant. Thus, we can calculate the normalized characteristics of the

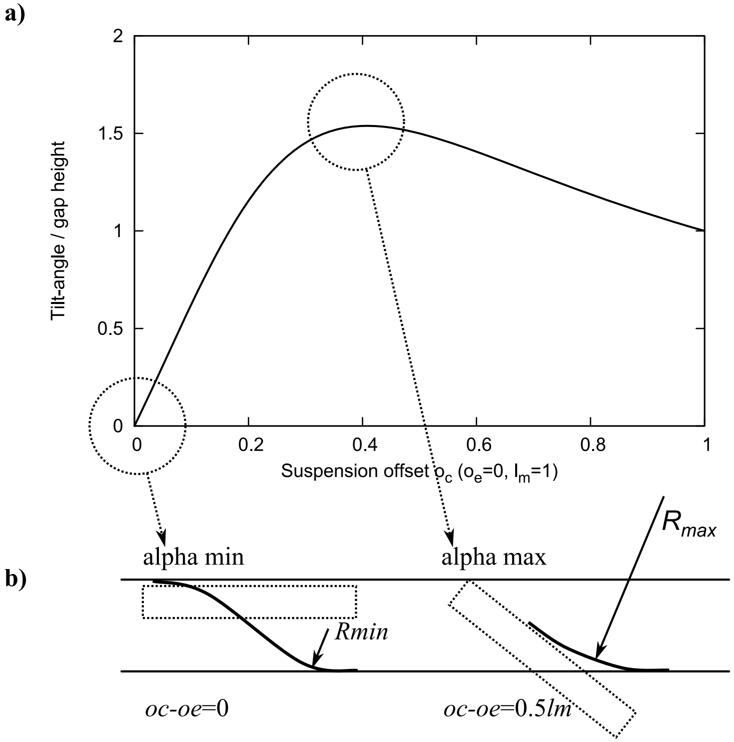

Figure 4.5: Analytic estimation of the influence of the suspension offset $o_c$ (a) on the tilt-angle versus gap height ratio, here for $o_e = 0$. The plot is normalized. (b) depicts the bending state in function of the resulting force/moment applied to the cantilever attachment point. Note that the force/moment ratio depends on $o_c$ *and* $o_e$.

two actuators according to Sec. 2.1 and we get

$$\widetilde{V}^2 = k_1(1 - \widetilde{z_1})^2 \widetilde{z_1} \tag{4.17}$$

$$\widetilde{V}^2 = k_2(1 - \widetilde{z_2})^2 \widetilde{z_2} \tag{4.18}$$

The square roots of the above functions are plotted in the graph in Fig. 4.6 (b) with $k_2 = 2k_1$ and exploited hereafter.

When the actuation voltage is set to $V_{a1}$, the actuator $z_1$ enters into pull-in state; we assume that a landing beam stops $z_1$ at a position $s_1$ ($1/3 < s_1 < 1$). The resulting tilt-angle $\alpha_a^+$ at this point is then $\propto s_1 - z_2(V_a)$. When we lower the voltage $V$ from this point on, $z_1$ will remain at position $s_1$ until $V = V_r = V(s_1)$ (recall that the states $1/3 < z_1 < s_1$ are not stable). At the same time the actuator $z_2$, not being in the pull-in state, changes its position from $z_2(V_a)$ to $z_2(V_r)$; as $V_r < V_a$ we have $z_2(V_r) < z_2(V_r)$ and consequently the resulting tilt-angle $\alpha_r^+$ before snap-back (at $V_r$) is larger than the tilt-angle at pull-in, i.e. $\alpha_r > \alpha_a$!

We deduce therefore that the ON-tilt-angle $\alpha_{\text{ON}}$ is a tilt-angle within the range $\alpha_a$ to $\alpha_r$. We can now introduce a second stopper beam (referred to as *the* stopper beam hereafter) in order to select a particular value out of this range; consider again Fig. 4.6: when we insert a stop for $z_2$ at a certain value $s_2$ (corresponding to the voltage $V_s$) we have consequently a constant tilt-angle $\alpha_{\text{ON}} \propto s_1 - s_2$ within a voltage range $V_a$ to $V_s$. By careful design, this (second) stopper beam can be utilized for accounting for process variations; this is further discussed in the next section.

At one point this simple model is not accurate or even misleading; it suggests that the mirror would hit the stopper beam $s_2$ in any case first and then $s_1$. Simulations using a finite element model (FEM, see Sec. 4.2.2) suggests that if the stopper beam $s_2$ is set within certain limits, $s_1$ is hit first and then $s_2$. The evolution of quasi-static states during the transition from the OFF to the ON state shows that a maximum tilt-angle $\alpha_a$ is reached before the mirror is settled in the actuated state $\alpha_a^+$ (the state $s_1 - z_2(V_a)$ in the simple model): see Fig. 4.7 (a); the maximum angle occurs at the instant when the landing beam (first stopper beam, $s_1$) hits the electrode (state at which simulation indicates initial contact).

The inverse case, when lowering the voltage starting from $V_a$, is explained correctly with the simple model, as simulation confirmed: In Fig. 4.7 the simulated tilt-angle versus voltage characteristics is depicted. Clearly, the mirror settles to a minimum ON-tilt-angle $\alpha_a^+$ at the pull-in voltage $V_a$[4]

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[4] Note that the tilt-angle would further decrease when considering voltages larger than

and increases when decreasing the voltage from this point on, until at a certain voltage $V_r$ it snaps back (or is released); the maximum tilt-angle $\alpha_r^+$ is reached before snap-back. The accessible tilt-angles for $V \leq V_a$ lie in between $\alpha_a^+$ and $\alpha_r^+$ and therefore we impose the second condition of operation

$$\alpha_a^+ < \alpha_{\mathrm{ON}} < \alpha_r^+ \qquad \text{(Second Operation Condition)}$$

The second operation condition is a constraint on the length of the stopper beam. When $\alpha_{\mathrm{ON}}$ would be set to be lower than $\alpha_a^+$, this state would only be accessible for voltages larger than $V_a$, which would be incompatible with the Row Column Addressing driving scheme RCA (see next section). If $\alpha_{\mathrm{ON}}$ would be set to be larger than $\alpha_r^+$, this state would not be accessible at all under normal operation conditions[5].

The existence of a second pull-in voltage $V_{a2}$ that is larger than the nominal pull-in voltage $V_{a1}$, as suggested by the simple model (consider Fig. 4.6) (b)), could also be verified with FEM simulations. It was even shown that for certain positions of the suspension attachment point $o_c$ (and electrode offset $o_e$) the second pull-in coincides with the first, resulting in a zero tilt-angle after pull-in. This was observed for combinations of $o_c$ and $o_e$ that were near the limit of the operation condition $o_c - o_e > 0$, i.e. for small $o_c - o_e$. This is further discussed in Sec. 4.3.

### ON and OFF tilt-range

Fig. 4.8 summarizes the succession of relevant mirror states as considered so far; the corresponding states are also depicted in the simulated mirror behavior in Fig. 4.7 (b). Note that a mirror state is defined through $\alpha_x, \delta_x, V_x$; the use of one of these parameters hereafter implicitly includes the others.

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$V_a$.

[5] Indeed, by a pure geometrical point of view one could impose a tilt-angle even larger than $\alpha_r^+$ by setting the length of the stopper beam accordingly; however, in this case the mirror must be forced to turn or slide around the tip of the stopper beam, which according to this position of the stopper beam and the distribution of forces and moments is only possible when the stopper beam bends through; this would require very high voltages and would not yield a constant ON-position. It is possible though, that during OFF-ON switching the mirror might touch the stopper beam *first* and the electrode after, even for stopper beams that fulfill the Second Operation Condition. As a matter of fact, the maximum tilt-angle during OFF-ON switching $\alpha_a$ might be somewhat smaller than $\alpha_r^+$, as indicated by the simulations depicted in Fig. 4.7; moreover dynamic effects may further alter $\alpha_a$. In any case it would be sufficient for the $\alpha_a < \alpha_{\mathrm{ON}} < \alpha_r^+$ to lower the voltage after pull-in to access the state $\alpha_{\mathrm{ON}}$.

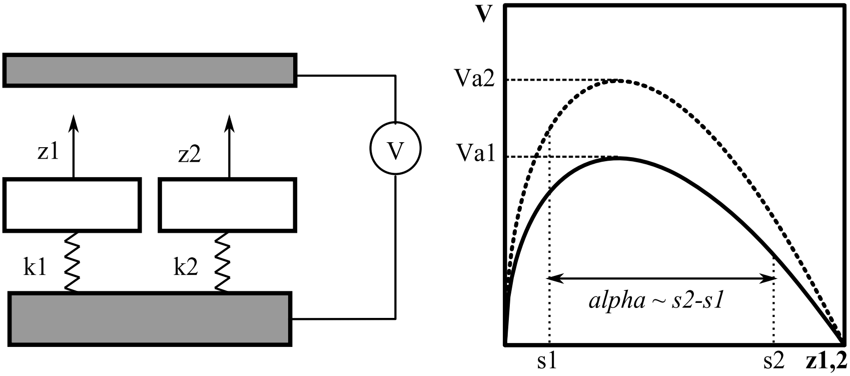

Figure 4.6: Simplified two degree of freedom model (a) and equilibrium states (b)

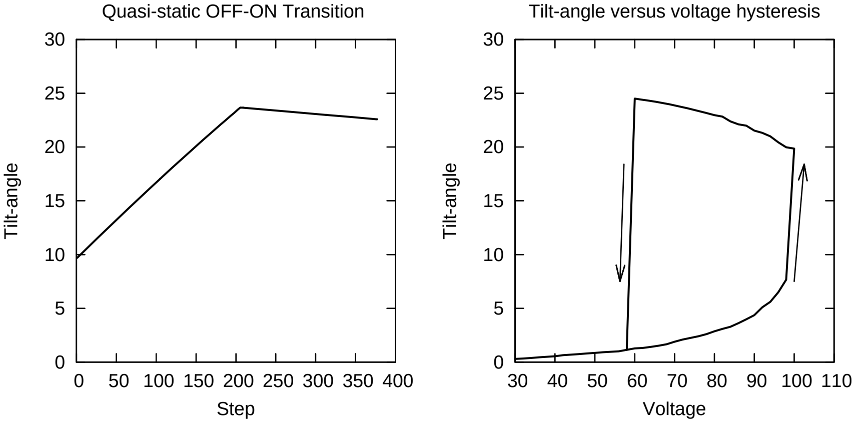

Figure 4.7: Simulated OFF-ON (quasi-static) and hysteresis behavior

The first two positions delimit the tilt-range that we refer to as the OFF-state, whereas positions three through five delimit the ON-state tilt-range. The lower limit of the OFF range is given with the tilt-angle $\alpha_0$ at zero actuation voltage, i.e. $\alpha_0 = 0$ in the model[6]. The upper limit $\alpha_a^-$ is given with the last equilibrium state before pull-in. The usable ON tilt-range is limited at the lower end by the position $\alpha_a^+$ after pull-in, and the upper end by the tilt-angle $\alpha_r^+$ before pull-back. We define further the tilt-angle $\alpha_r^-$ at voltage $V_r^-$, which corresponds to the position in OFF state after pull-back. Position four does not indicate a stable state but the transition between the OFF and the ON state at the instant where the landing beam comes into contact with the landing pad[7]. We refer to this tilt-angle as $\alpha_a$ and the corresponding voltage is the pull-in voltage $V_a$.

The stopper beam must halt the mirror at an intermediate state between $\alpha_a^+$ and $\alpha_r^+$; this position, defined as $\alpha_{\mathrm{ON}}$ is given with the stopper beam length $l_s$ through the following geometrical relation (see Fig. 4.1 and Tab. 4.1):

$$\tan \alpha_{\mathrm{ON}} = \frac{d_a - 2d_p}{l_c + o_s + l_l - o_l - l_s} \tag{4.19}$$

Unlike the other states, $\alpha_{\mathrm{ON}}$ is not related to a distinct voltage value but rather to a voltage range. This voltage range is delimited with the pull-in voltage $V_a^+$ and a voltage $V_s$. The voltage $V_s$ corresponds to a state between the states $\alpha_a^+$ and $\alpha_r^+$, i.e. between pull-in and snap-back (ON-OFF transition) that has the tilt-angle $\alpha_{\mathrm{ON}}$. Physically, this voltage corresponds to the moment when the mirror detaches from the stopper beams when lowering the voltage from $V_a^+$ towards $V_r^+$. In other words this signifies that the mirror stays in position $\alpha_{\mathrm{ON}}$ within the voltage range $V_a^+$–$V_s$.

The row-column actuation scheme (RCA)[8] relies on the fact that a hold voltage $V_h < V_a$ can be utilized to hold the mirrors in the ON-state. More precisely, $V_h$ must be set between $V_a$ and $V_s$, i.e. $V_s < V_h < V_a$ in order to make sure that the mirror is in the ON-state defined by the stopper beam.

As the hold voltage is applied to all mirrors, the mirrors in the OFF-state have a non-zero tilt-angle that depends on $V_h$ (depicted in Fig. 4.7). The voltage range $\{V_s, V_a\}$ can therefore be regarded as tuning range for the tilt-angle in the OFF-state $\alpha_{\mathrm{OFF}}$. In summary, the range $\{\alpha_a^+, \alpha_r^+\}$ is the tuning

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[6] In the real case the tilt-angle might not be zero at zero volts due to a stress gradient in the polysilicon layer.

[7] Note that even though it is not a stable state we still refer to it as quasi-static in modeling; dynamic effects are not considered as they are not believed to be relevant for the operation of the device.

[8] See Sec.3.3

range for the angle in the ON-state $\alpha_{\mathrm{ON}}$; through the length of the stopper beam $l_s$ $\alpha_{\mathrm{ON}}$ and correspondingly $V_s$ is set. $\{V_s, V_a\}$ is then the range for setting $V_h$, which in turn defines $\alpha_{\mathrm{OFF}}$. This is schematically depicted in Fig. 4.9

### Tilt-Angle Uniformity and Process Variations

Considering process variations we make the following assumptions:

- Process conditions are stable within the surface of one micromirror (i.e. no process variations within one micromirror);
- Only systematic and no statistic variations are considered (i.e. the effect of local defects, e.g. due to a dust particle, are neglected);
- Dimensional uniformity errors on the photomasks used for microfabrication are assumed to be negligible[9].

The process variations that are taken into account are

- Variations of lateral dimensions due to non-uniform dimensional reduction during pattern transfer (photolithography, etching) affecting the performance-relevant parameters $w_c$, $l_s$ and $l_l$;
- Variations of thicknesses (and heights) affecting the performance-relevant parameters $t_c$, $d_c$ and $d_a$.

We consider now the total variation $\Delta\alpha_{\mathrm{ON}}$ of the ON tilt-angle across the mirror array due to process variations. According to Eq. 4.19, the only parameters that influence $\alpha_{\mathrm{ON}}$ *and* are subject to process variations are $l_s$, $l_l$, $d_c$ and $d_a$[10]. Variations of the length of $l_s$ and $l_l$ are canceled out in Eq. 4.19 as the deviation of $\Delta l$ from the nominal lengths (and widths) is assumed to be constant within one mirror. Note that this signifies also that

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[9] Critical dimension (CD) uniformity can be specified to be below 70nm for quartz-photomasks used for MEMS-fabrication; this is less than 1% of the typical dimensions in our micromirror architecture (lenght of cantilever $l_c \approx 100\mu$m, length of stopper beam $l_s \approx 20\mu$m, see Sec. 4.3)

[10] $l_c$ and $o_s$ are not altered due to pattern transfer (lateral dimensional reduction) but only depend on CD uniformity on the photomask, which was assumed to be sufficiently well. $o_l$ depends in first degree on the tilt-angle (and in second degree on the shape of the bent cantilever). It is therefore not considered as *cause* for process-induced tilt-angle variation; it might however cause a slight error on the estimated tilt-angle variation given further below.

an absolute (or global) deviation of $l_l$ and $l_s$ from the design value do not alter the absolute value of the design ON tilt-angle[11].

Therefore only variations of $d_a$ and $d_c$ cause a variation of the ON tilt-angle across the mirror array. We denote these variations as $\Delta d_a$ and $\Delta d_c$ and correspondingly the tilt-angle variation $\Delta\alpha_{\mathrm{ON}}$ is given by

$$\tan(\Delta\alpha_{\mathrm{ON}}) = \frac{\Delta d_a + 2\Delta d_p}{l_c + o_s + l_l - l_o - l_s} \tag{4.20}$$

Note that the impact of the variation of the spacing between mirror and electrode $\Delta d_a$ will be predominant, as we have $d_a >> d_c$ and we assume the process variations $\Delta$ to be proportional to the absolute values.

In above considerations we assumed the stiffness of the landing and stopper beams to be infinite and thus, not susceptible to process variations; for the real case of finite stiffness we impose that the stiffness of the stopper and landing beam must be, by design, a factor $x$ higher than the stiffness of the cantilever suspension, where $x$ is determined through the expected stiffness variation of polysilicon structures and the requirement on tilt-angle uniformity.

The condition for the hold voltage $V_h$ of the RCA scheme is extend in consideration of process variations: the hold voltage must be within the range $V_s^i$ to $V_a^i$ for all mirrors $i$ (uniform tilt-angle condition). This is depicted graphically in Fig. 4.9. The usable range for setting $V_h$ is therefore delimited at the lower end by the maximum value of $V_s^i$ and at the upper end by the minimum value of $V_a^i$. The minimum and maximum values of $V_x$ across a mirror array are given by the stiffness variation of the polysilicon cantilever suspensions within that array. If $k$ is the nominal stiffness and $\Delta_k$ the peak-to-valley stiffness variation within one array (induced by geometrical variation of the cantilever suspension, in particular its thickness) then $V_a^{\min} = V_a(k - \Delta_k)$ and $V_s^{\max} = V_a(k + \Delta_k)$. Within the usable range $\{V_s^{\max}, V_a^{\min}\}$ $V_h$ can be set to adjust the angle $\alpha_{\mathrm{OFF}}$. Naturally, one wants to minimize the tilt-angle of the mirrors in the OFF-state (ideally zero), i.e. minimizing $V_h$, in order to maximize $\alpha_{\mathrm{ON}} - \alpha_{\mathrm{OFF}}$. For that a large tuning range is desirable, ideally the stopper beam is set such that $V_s = V_r^-$—this also maximizes the tilt-angle in the ON-state for a given spacing between mirror and electrode.

In order to account for absolute dimensional errors of the stopper beam (modeling errors, global over-etching, etc), it is also desirable to maximize

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[11] As long the deviation $\Delta l$ is smaller than the absolute length of $l_l$ and $l_s$.

the tuning range in terms of tilt-angle, i.e. the range $\{\alpha_a, \alpha_r\}$ within which the ON-tilt-angle must be set, and thus, providing design margin for $l_s$.

### Finite Element Model

For quantitative analysis of the electromechanical behavior of the cantilever suspended micromirror, simulations using the finite element method (FEM), taking into account geometrical nonlinearities, were carried out. The above key parameters are calculated from a set of geometrical parameters using a custom finite element model, which is described hereafter.

The modeling of our micromirrors demands three major capabilities of the used simulation environment:

- Coupled mechanical and electrostatic simulation
- Large out of plane displacements (in the same order of magnitude as the lateral dimensions of the considered structures)
- Contact simulation

The integration of all this elements in one model is not efficient and subject to convergence issues due to large mesh-deformation, combined with highly non-linear contact simulations. Therefore a custom script-based simulation model for ANSYS has been developed; the basic philosophy of this approach was to tackle the above challenges by separating the problems within the simulation environment and couple them again outside the simulation space. ANSYS was chosen as FEM engine as it allows complete script control and is well established. The script-based model is separated into three submodels:

- Electrostatic model
- Mechanical model
- Mechanical model with contact simulation ability

Fig. 4.10 depicts the custom coupled simulation flow. The electrostatic model represents the mirror-electrode configuration; the position of the mirror is an input coming from the mechanical model. The electrostatic model is used to calculate the electrostatic pressure on the mirror for a certain voltage and a certain position of the mirror. The electrostatic pressure distribution is summed to a resulting force and moment value evaluated at the attachment point of the suspension. This value is passed to the mechanical model. The

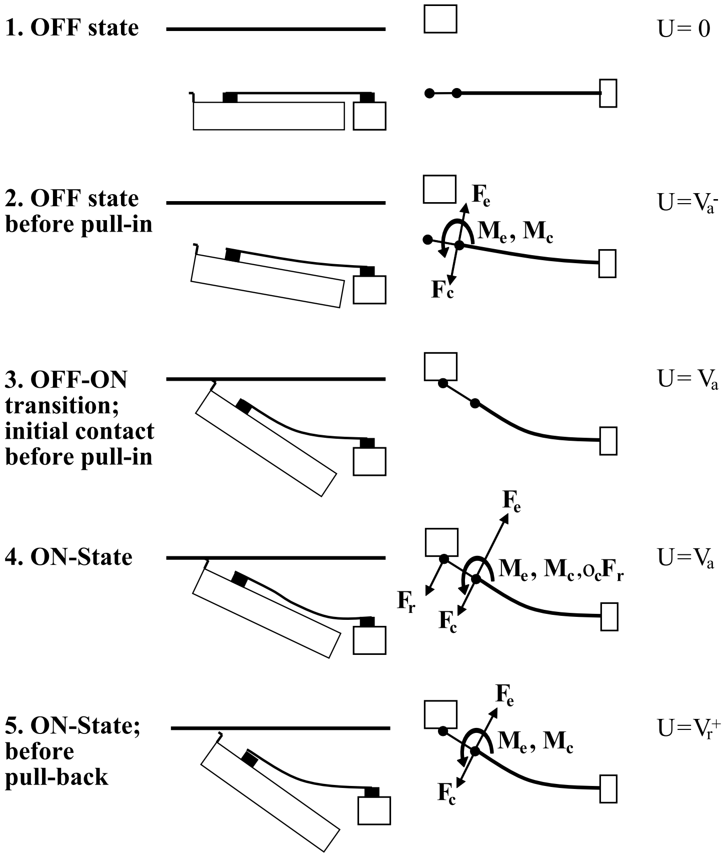

Figure 4.8: Key States

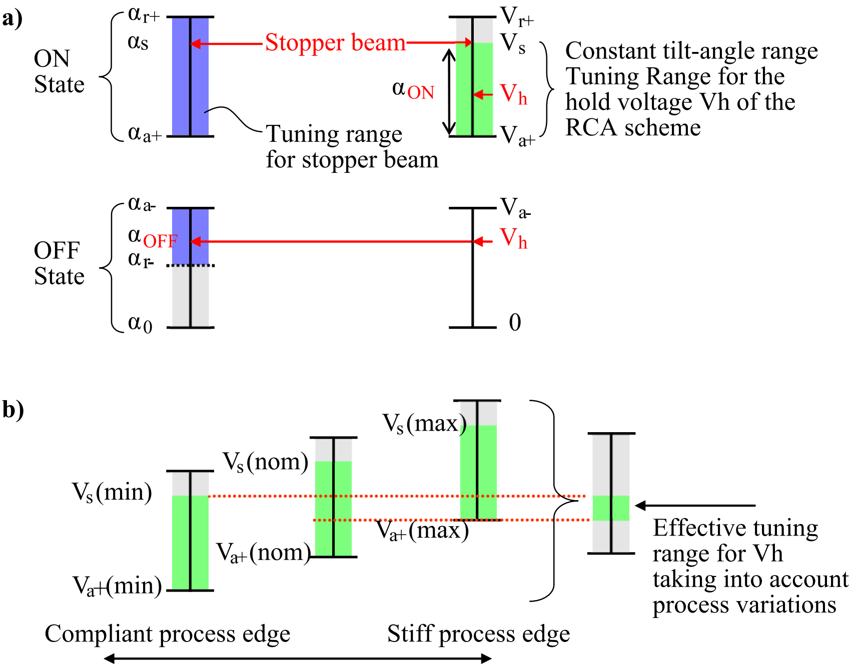

Figure 4.9: OFF and ON ranges (a) and the implications of process variations (b).

mechanical model consists uniquely of the suspension beam, which is fixed at one end. The torque and force value from the electrostatic simulation is applied to the free end of the suspension cantilever and the deformation of the suspension beam is simulated. From that the resulting mirror position is calculated and the value is passed to the electrostatic model for the next iterations. This cycle is repeated until the mirror position converged for a certain voltage value. Then the voltage value is increased and the cycle starts again; this steps are repeated until the mirror goes into pull-in state which is detected by the fact that the displacements between two iterations increase without increasing the voltage value. At this point the information on the mirror position and the force and torque values of a position near the theoretical contact position is evaluated and passed to the mechanical model featuring contact simulation ability. This mechanical model features an additional landing post, which is attached via a rigid link to the suspension beam, and a corresponding landing pad. This model is used for further iterations until a contact between the landing beam and landing pad is detected by the simulation engine and a equilibrium position is reached. Optionally, after that point a post pull-in simulation is possible, which is required to determine the complete electrostatic hysteresis of the micromirror.

The individual three individual FE models are all based on 2D elements. Even though this implies that certain effects are neglected, it increases calculation speed drastically and enables searching large solution spaces.

The electrostatic model is based on 2D electrostatic triangular shaped finite elements. The elements are not used to model the physical electrode-mirror geometry but the "air" between the different elements: see the illustration and sample simulation, showing the effect of charge oxide near the electrodes, in Fig. 4.11 (a). This implies that the air must be re-meshed for each mirror position; this has the advantage that the mesh is always best adapted to the current mirror position and no mesh-deformation related convergence issues occur. On the other hand, certain mesh-induced effects can occur: there is a certain influence of the mesh morphology on the resulting electric field and charge distribution and thus on the electrostatic force/momentum; the relative error between simulations due to a changed mesh was around 2%.

The reduction of the 3D case to a 2D model implies that fringe field effect in the third dimension are neglected. A comparison between the 2D model and a corresponding 3D model revealed that the resulting electrostatic force on the micromirror is around 4% higher in the 3D case than in the 2D case, signifying that we rather overestimate the required actuation voltage in the

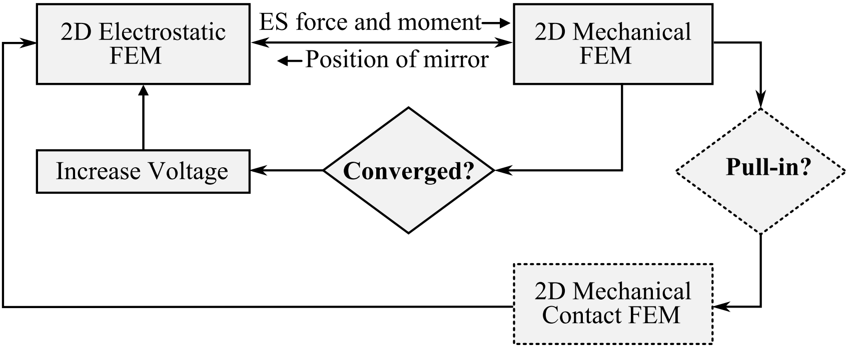

Figure 4.10: Schematic representation of the custom FEM based on an ANSYS script.

2D model. The gain in calculation time is important: the 2D simulation took less than one second, compared to about 30s for the 3D simulation (in both cases including automatic building the model, meshing, simulation and value extraction).

For the mechanical model an finite element type is used that is specialized for modeling bending beams. The element is 2D but can be attributed three dimensional physical parameters, such as the beam width. It supports large deflections; that means that geometrical non-linearities are taken into account for large beam deformations.

In addition to a simple cantilever, the mechanical model with contact simulation ability features a landing beam attached to the free end of the cantilever and a corresponding landing pad. A predefined contact zone between the landing beam and the landing pad is modeled using surface contact elements. The landing beam consists of a rigid link, corresponding to the mirror part between cantilever attachment point and landing beam attachment point (parameter $o_c$), and a short bit of cantilever with length $l_l$, width $l_w$ and thickness $t_c$. A visualization of the beam model is given in Fig. 4.11 (b).

The geometrical parameters and material constants used in the FE model correspond to the conventions proposed in the first section of this chapter. The outputs of the FEM are the key performance parameters, plus additional parameters, such as maximum stress and resonance frequency.

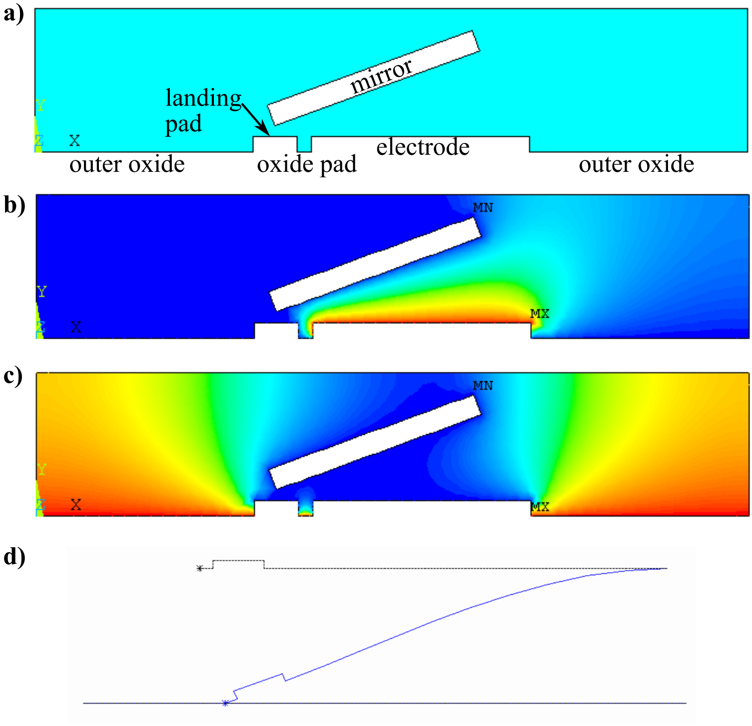

Figure 4.11: 2D electrostatic (a-c) and mechanical FEM (d) used for the custom coupled simulation script. The geometry in (a) was utilized to study the impact of charged oxide around the electrode: in (b) the electrode is set to zero and the oxide surfaces are set to 100V; the impact of the charged small oxide pad between electrode and landing pad showed to be negligible. The charged large oxide surface around the electrode induced rather a repulsive force on the mirror, tending it to release it from the ON-state and thus, not to be to considered as potential cause for "sticking" of the mirrors. In the normal simulations, the effects of the oxide and landing pad geometry were, given their low impact, neglected. (c) shows the potential distribution with the electrode set to 100V. The electrostatic force and moment on the mirror is evaluated at the cantilever attachment point and sent to the mechanical model. (d) The mechanical model consists of a simple cantilever and a landing beam, connected to the cantilever via a rigid link. For contact simulation, a landing zone at the height of the electrode landing pad, is added.

## 4.3 Design

In this section we identify the requirements on the micromirror device related to the electromechanical performance and link them to the geometrical parameters of a micromirror unit.

### 4.3.1 Translating the Requirements

Implicitly the dependencies are given by the modeling of the device, i.e. the physics that relate the geometrical parameters to the device performance. Hereafter the requirements imposed by the application from Sec. 3.1.2 are translated into performance parameters and their mutual influence on the geometrical parameters are exhibited.

**Contrast** The contrast requirement is a system requirement; it is translated into a device performance parameter by the requirement on the tilt-angle. Furthermore it implies that by architecture the stray-light must be minimized. From that we deduce that the gap width $w_g$ must be minimized.

**Tilt-angle OFF-ON** The OFF-ON tilt-angle $\alpha_{\mathrm{OFF-ON}}$ is given with the performance parameters $\alpha_{\mathrm{OFF}}$ and $\alpha_{\mathrm{ON}}$; the maximum value that $\alpha_{\mathrm{OFF-ON}}$ can take for a given set of parameters equals $\alpha_r^+ - \alpha_r^-$ and the minimum $\alpha_a^+ - \alpha_a^-$. A usable value will be in-between (taking into account the tilt-angle uniformity conditions, see below) and therefore we specify

$$\alpha_{ON} - \alpha^-(V_h) \geq 20^\circ \tag{4.21}$$

The geometrical parameters with the biggest influence on $\alpha_{\mathrm{OFF-ON}}$ are the spacing $d_a$, the cantilever attachment offset $o_c$. A working point for elaborating a solution space is set, based on the considerations in the previous subsection, by using $d_a = 35\mu\mathrm{m}$[12], $o_c = 0.15 l_m$ and $o_e = 0.1 l_m$.

**Tilt-angle uniformity in ON state** The uniform tilt-angle conditions, defined before, apply:

$$\alpha_a^+ < \alpha_{ON} < \alpha_r^+ \tag{4.22}$$

and for the hold voltage of the row column actuation scheme

$$V_s^{\max} < V_h < V_a^{\min} \tag{4.23}$$

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[12] Using, as first approximation, $d_a = \sin(20^\circ) \cdot l_m$ with $l_m = 100\mu$m.

where (min) and (max) depict the process edges within an array. The tuning range $\{\alpha_a^+, \alpha_r^+\}$ must therefore be designed such that above conditions can be fulfilled—ideally the tuning range is maximized.

The third uniform tilt-angle condition implies that the stiffnesses of the landing and stopper beam $k_l$ and $k_r$ are much higher than the stiffness of the cantilever spring $k_c$. As design value we impose $k_l, k_r \geq 1000 \cdot k_c$[13].

Provided that above conditions are fulfilled, the tilt-angle uniformity solely depends on the variation of spacing between mirror and electrode chip $d_a$ and polysilicon layer and mirror layer $d_p$; by simple geometrical reflexion (and using Eq. 4.20), the tilt-angle uniformity requirement $\Delta^{\text{req}}\alpha_{\text{ON}}$ is therefore translated into

$$\Delta d_a + 2\Delta d_p < \Delta^{\text{req}}\alpha_{\text{ON}} \cdot l_m \tag{4.24}$$

$\Delta d_a + 2$ and $\Delta d_p$ can't be influenced by design but must be assured through concept and careful process (assembly) control. A requirement of 10arcmin is translated into a maximum allowable $\Delta d_a + 2\Delta d_p$ of 300nm.

**Mirror flatness and surface roughness** The requirement on mirror flatness defines the minimum mirror thickness $t_m$; according to Sec. 4.2.1 we have $t_m \geq 10\mu$m. The surface roughness is not related to an electromechanical performance or geometrical parameter but depends uniquely on the choice of a substrate and the fabrication process.

**Mirror Size** The requirement on the mirror size defines the values $l_m$ and $w_m$, i.e. $l_m = 100\mu$m and $w_m = 200\mu$m.

**Array Size** The array size requirement defines the surface over which the uniform tilt-angle requirement must be fulfilled. The maximum process variations are in first approximation proportional to the array size (surface) m×n. According to Tab.4.2 we assume a worst-case edge-to-edge variation of 20% (including some safety margin) accross a 4-inch wafer for thickness of deposited materials, thickness of substrates, etch-depths (or heights) of time-etched structures and for in-plane dimensions (lateral overetch). Assuming a

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[13] This value was estimated with following simple reflexion: the cantilever with stiffness $k_c$ is deflected to 20° and consequently a 1000 times stiffer stopper beam will allow only a deflection of $20°/1000 \approx$ 1arcmin; as the stiffness variation is expected to be below 10%, the resulting tilt-angle variation is below 10 arcseconds and thus, negligible. Note that for MIRA2 a landing/stopper beam design with matched $k_l$ and $k_s$ is implemented, theoretically completly suppressing any variations.

linear distribution this translates into about 1‰/mm (applies to the longer side of a rectangular array). For the small array (5×5) this translates into 1‰and for the large array (200×100) into about 4%.

**Fill Factor** The effective fill-factor is given by $\mathrm{f}_{\parallel} \cdot \mathrm{f}_{\perp}$, where $\mathrm{f}_{\parallel}$ is the fill-factor parallel and $\mathrm{f}_{\perp}$ perpendicular to the long-slit (or frame) direction. A hard limit is imposed on the fill-factor parallel to the frame, given by $f_{\perp} = \frac{l_m}{l_m + w_g} \geq 0.95$; this implies a maximum value on $w_g$: $w_g \leq 0.05 l_m$. The minimum value is imposed by the fabrication technology and is discussed in the next section. The fill-factor perpendicular to the long slit direction $\mathrm{f}_{\perp}$ is given by the projection of the usable mirror width on a plane perpendicular to the incoming light and the gap- and frame-width, $w_g$ and $w_f$. The usable mirror width is the geometrical mirror width reduced by a length $o$, which represents the part of the mirror that is obscured by the mirror frame; the obscuration $o$ is schematically represented in Fig. 4.1:

$$\mathrm{f}_{\perp} = \frac{(w_m - o)\cos\alpha}{2w_g + w_f} \qquad \text{with} \qquad o = \frac{\sin(\pi - \alpha - \arctan\frac{d_a}{l_o})}{\sin(\pi - \alpha - \gamma)} \sqrt{l_o^2 + d_a^2} \tag{4.25}$$

where $\gamma$ is given with the numerical aperture, i.e. $\sin\gamma = \mathrm{NA}$, and $\alpha$ with the tilt-angle in the ON-state, i.e. $\alpha = \alpha_{ON}$. Even though there is no hard limit for $\mathrm{f}_{\perp}$, the requirement states that this value must be maximized. This implies that the frame width, the tilt-angle in the ON-state and the spacing between the mirror and electrode must be minimized—under the condition that concurrent requirements are still met. Thus, for a given tilt-angle (set by the requirements), the gap-height must be minimized. The minimum frame width is given by technological and structural boundary conditions and is discussed in Sec. 4.4.1.

**Resonance frequency** The resonance frequency requirement is imposed as measure for shock resistivity and determines the minimum stiffness values of the cantilever suspension (the mirror mass being fixed through dimensional requirements and the requirement on surface quality).

**Actuation Voltage** The actuation voltage corresponds to the performance parameter $V_a$; as such $V_a$ depends on all geometrical parameters (cantilever dimensions, mirror dimension, air gap between electrode and mirror). The actuation voltage requirement specifies $V_a < 100V$ and therefore sets the maximum available force for a given mirror/electrode surface and mirror-electrode spacing. This implies a maximum allowable stiffness of the cantilever spring—therefore this is a concurrent requirement to the minimum resonance frequency.

### 4.3.2 Design Space

The design space was spanned using the custom coupled physics FE model and the working point set before. Note that all simulations consider the mirror only with landing and not with stopper beams. The stopper beam will be added further below.

In Fig. 4.12 the tilt-angles $\alpha_a^+$ and $\alpha_r^+$, the actuation voltage $V_a$ and first resonance frequency $f_r$ are plotted in function of the basic cantilever parameters $w_c$ and $t_c$ and the spacing $d_a$. The cantilever length was set to $l_c = 0.9 \cdot l_m$ (mirror length $l_m = 100\mu\text{m}$), the suspension offset to $o_s = 0.15 \cdot l_m$ and the electrode offset to $o_e = -0.1 \cdot l_m$. A reasonable set of cantilever parameters, which fulfills the resonance frequency, actuation voltage requirements and technological requirement is $w_c = 3\mu\text{m}$ and $t_c = 0.6\mu\text{m}$. The minimum gap size to achieve $\alpha_a^+ \geq 20°$ is $35\mu\text{m}$. The maximum bending stress in the cantilever suspension is around 500MPa for these parameters, which is somewhat high compared to the assumed fracture strength of 2GPa. A lower maximum bending stress could be achieved with a lower thickness of the cantilever but this would contradict the minimum thickness requirement: a test run with thinner beams showed that the fabrication yield is very low with $t_c < 0.5\mu\text{m}$ and therefore the safe minimum thickness was set to $0.6\mu\text{m}$.

In Figs. 4.13–4.14 the impact of the cantilever attachment offset $o_c$ and the electrode offset $o_e$ on the the maximum and minimum tilt-angle $\alpha_r^+$ and $\alpha_a^+$ and corresponding voltages and resonance frequency are plotted. As predicted by analytic modeling the influence of the parameters $o_c$ and $o_e$ on the pull-in tilt-angle $\alpha_a^+$ is considerable. For $o_c$ below $0.1 \cdot m_l$ (for $o_e = -0.1 \cdot m_l$) simulation suggests that the resulting tilt-angle after pull-in is zero, i.e. a second-pull-in coinciding with the first takes place; the same effect is observed for $o_e \geq 0$ (here with $o_c = 0.15 \cdot m_l$). In reality, the mirror would not be pulled-down to a zero tilt-angle position but would rather be stopped by the cantilever suspension itself (and for the nominal case, naturally, by the stopper beams) as depicted in Fig. 4.15. That implies that not the full range $\{\alpha_a^+, \alpha_r^+\}$ can be utilized for setting $\alpha_{\text{ON}}$; the angle at which the cantilever suspension would stop the mirror depends on the spacing between the mirror and the cantilever $d_c$ and for the present set of

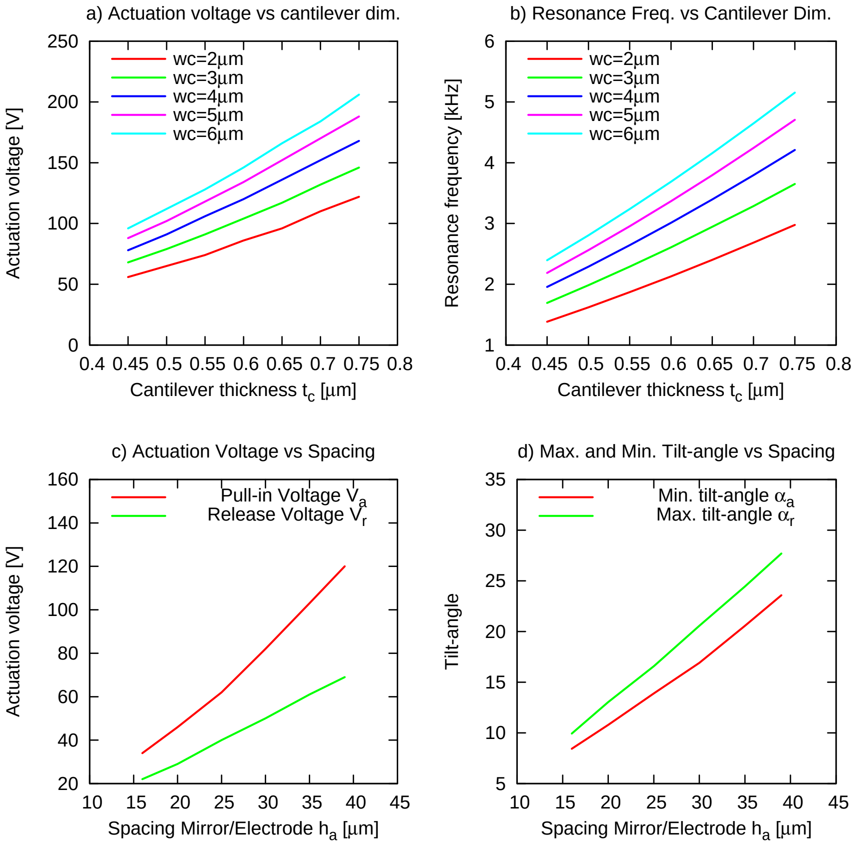

Figure 4.12: Simulation results exhibiting the influence of the basic geometrical parameters. Common parameters are the cantilever offset $o_c = 15\mu$m, the cantilever length $l_c = 90\mu$m and the electrode offset $e_o = -10\mu$m. In (a) the pull-in voltage and in (b) the resonance frequency for a gap height $d_a$ of $35\mu$m in function of the cantilever thickness $t_c$ and cantilever width $w_c$ are plotted. (c) Dependence of actuation voltage and (d) dependence of tilt-angle on the gap height $d_a$ (using $w_c = 3\mu$m and $t_c = 0.6\mu$m).

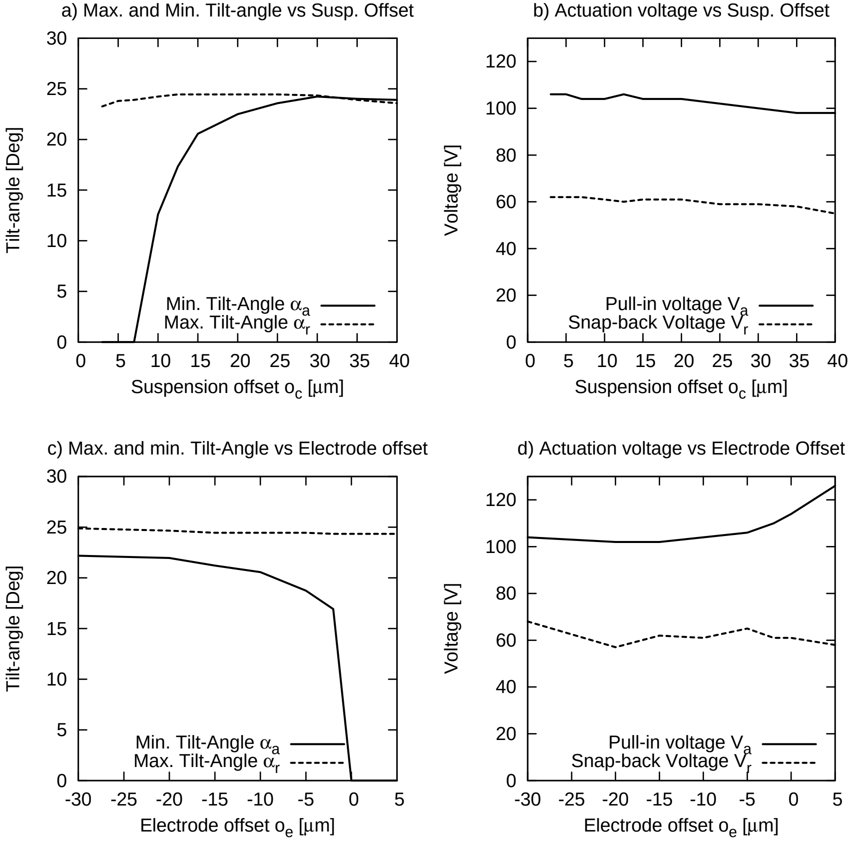

Figure 4.13: Simulation results exhibiting the influence of the suspension offset $o_c$ (a,b) and the electrode offset $o_e$ (c,d) on the maximum and minimum tilt-angle and the actuation voltages. Common parameters are $w_c = 3\mu$m, $t_c = 3\mu$m and for (a,b) $o_e = -10\mu$m and for (c,d) $o_c = 15\mu$m. The cantilever length is set to $l_c = 105 - o_c$

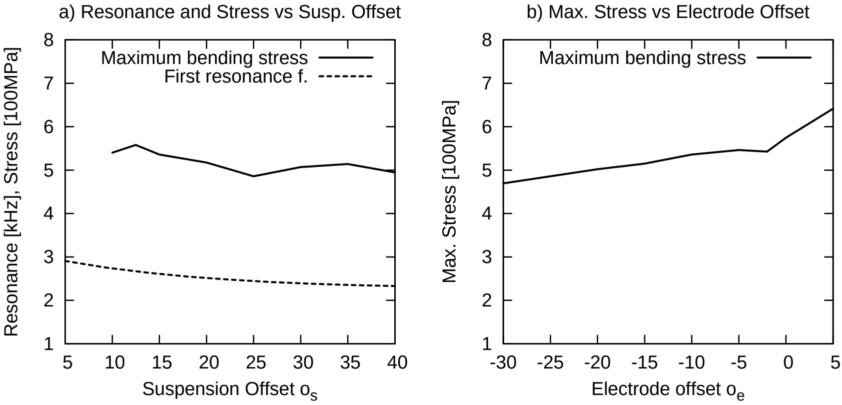

Figure 4.14: Simulation results exhibiting the influence of the suspension offset $o_c$ (a) and the electrode offset $o_e$ (b) on the first resonance frequency and the maximum bending stress. Common parameters are $w_c = 3\mu$m, $t_c = 3\mu$m and for (a) $o_e = -10\mu$m and for (b) $o_c = 15\mu$m. The cantilever length is set to $l_c = 105 - o_c$

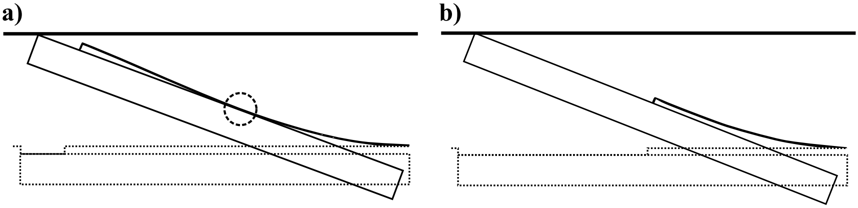

Figure 4.15: Mirror position after pull-in for two different cantilever length; a) long cantilever $l_c = 95\mu$m, $o_c = 10\mu$m b) short cantilever $l_c = 75\mu$m, $o_c = 30\mu$m. In the case of the long cantilever, in absence of stopper beams, the mirror is prevented from collapsing into the second pull-in state by the cantilever suspension itself (the mirror touches the cantilever at the position indicated with a circle); in the case of the short cantilever the mirror position after (first) pull-in is inherently stable

parameters this value is around 4° lower than the maximum tilt-angle $\alpha_r^+$. This new lower limit for setting $\alpha_{\mathrm{ON}}$ is indicated with a dashed line in the graphs of Fig. 4.13. Note that if required this limit could be pushed lower by increasing $d_c$.

Thus, the maximum tuning range for $\alpha_{\mathrm{ON}}$ is obtained for a cantilever attachment offset $o_c = 10\mu$m (at an electrode offset of $o_e = -10\mu$m; note that the tuning range can also be adjusted for a fixed $o_c$ with the electrode offset $o_e$). It is noteworthy that the actuation voltages remain almost constant with a changing suspension offset (and thus, changing cantilever length). This was implicitly predicted by Eq. 4.16, in principle stating that for a given gap the voltage is independent of $o_c$ (and also of $o_e$). A similar behavior is observed for the resonance frequency which, despite a stiffer (shorter) cantilever suspension, is almost independent of $o_c$—this is attributed to the rotational mass of inertia that increases with increasing $o_c$ and thus, counterbalances the increased stiffness.

Note that the electrode offset has a considerable impact on the maximum bending stress. The maximum bending stress is related to the shape and particularly to the maximum curvature of the cantilever in the ON-position. The bending shape, as depicted in Sec. 4.2.2 (recall Fig. 4.5) depends on the the magnitude and orientation of the resulting electrostatic moment (and force) evaluated at the cantilever attachment point, which again depends on $o_c$ and $o_e$ (Sec. 4.2.2). The maximum bending stress increases with decreasing $\alpha_a^+$ and for a *given* $\alpha_a^+$ the maximum bending stress increases with decreasing cantilever length $l_c$, i.e. increasing cantilever suspension offset $o_c$.

### 4.3.3 Trade-Off, Tolerances and Design Values

We set the nominal cantilever dimensions to $t_c = 0.6\mu$m and $w_c = 3\mu$m and the nominal spacing $d_a$ to $35\mu$m such that the resulting actuation voltage $V_a$ is around 100V. Further, $o_c$ is set to $10\mu$m and $o_e$ to $-10\mu$m for maximum tuning range and, following above considerations, minimizing the maximum bending stress and actuation voltage (at maximum tuning range)[14].

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[14] For the purpose of completeness also the reasons that would favor $o_c > 10\mu$m shall be mentioned here. The first reason is that from a layout point of view it might be desirable to shift the electrode to the right, i.e. increase $o_e$, in order to leave more room for the landing pad on the electrode layer; this is particular true for the large array design. Increasing $o_e$ requires increasing $o_c$ according to the condition of operation $o_c - o_e > 0$ and above design considerations. The second argument that would speak for increasing $o_c$ is increasing the restoring force for switching from $\alpha_r^+$ to the OFF state (which at this point and under normal conditions depend on the stiffness, i.e. the length of the cantilever).

The process edges for the largest array size (MIRA2, 200×100), based on the assumptions at the beginning of this section, are

$$w_c^{\min} = 2.88\mu\text{m} \tag{4.26}$$

$$t_c^{\min} = 0.59\mu\text{m} \tag{4.27}$$

and

$$w_c^{\max} = 3.12\mu\text{m} \tag{4.28}$$

$$t_c^{\max} = 0.61\mu\text{m} \tag{4.29}$$

The resulting actuation voltage of the most compliant design (from Fig. 4.12) is 5V lower than the nominal actuation voltage and correspondingly 5V higher for the stiffest process edge. In consequence, the voltage range for setting $V_h$ must be at least 10V-wide in order to account for process variations (recall Fig. 4.9, p.84).

We chose the length of the stopper beam such that the resulting tilt-angle in the ON-state is

$$\alpha_{ON} = \frac{\alpha_a^+ + \alpha_r^+}{2} \tag{4.30}$$

i.e. in the middle of the tuning range $\{\alpha_a^+, \alpha_r^+\}$. Whereas this does not provide the maximum tilt-angle for the given gap-size, it provides maximum safety margin. Recall that for proper operation in the final device we must imperatively have $\alpha_a^+ < \alpha_{\text{ON}} < \alpha_r^+$.

The resulting tuning range magnitude $V_a - V_s$ is consequently $(V_a - V_r)/2 = 20$V and thus, should be sufficient to account for process variations (10V minimum requirement). Setting $V_h$ to $(V_s + V_a)/2$, a OFF-tilt-angle of 5°.8 is obtained, yielding a ON-OFF tilt-angle of $\alpha_{\text{ON}-\text{OFF}} = 16°.5$. In one design variant the stopper beam length is increased in order to yield a ON-tilt-angle of 22°.8 and a OFF-tilt-angle of 4°.5. Note that the maximum ON-OFF tilt-angle would be reached for setting $\alpha_{\text{ON}}$ to $\alpha_r^+$; here the corresponding $\alpha_{\text{OFF}}$ would be 1.3 and thus, $\alpha_{\text{ON}-\text{OFF}} = 22°.9$.

Beside the baseline design, several variations of it were also implemented in the final layout. A selection of implemented designs is given in Tab.4.5.

## 4.4 Layout

In this section the design parameters are translated into a device layout, which can be fabricated using the process sequence presented in Ch. 5. Ge-

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An increased restoring force would increase the chances for releasing a stuck mirror.

Table 4.5: Design device performance

| Geom. Param. | | | | | Performance Param. | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $l_c$ [$\mu$m] | $l_s$ [$\mu$m] | $o_s$ [$\mu$m] | $V_a$ [V] | $V_r$ [V] | $V_s$ [V] | $\alpha_a^+$ [°] | $\alpha_r^+$ [°] | $\alpha_{\mathrm{ON}}$ [°] | $\alpha_{\mathrm{OFF}}$ [°] |
| 95 | 10 | 27.3 | 104 | 61 | 84 | 12.6 | 24.2 | 22.2 | 5.8 |
| 95 | 10 | 25.3 | 104 | 61 | 90 | 12.6 | 24.2 | 21.7 | 6.1 |
| 95 | 10 | 29.3 | 104 | 61 | 76 | 12.6 | 24.2 | 22.8 | 4.5 |
| 85 | 20 | 31.4 | 104 | 61 | 86 | 22.5 | 24.4 | 23.5 | 7.3 |
| 75 | 30 | 34.4 | 104 | 61 | 83 | 24.2 | 24.3 | 24.3 | 7.8 |

[1] Design Identifier

[2] Design value

[3] Measured value

[4] Tilt-angle variation within stopper angle regime

ometrical parameters that are implemented in the layout of the photomasks for fabrication are denoted with $m$, e.g. the parameter $w_g^m$.

### 4.4.1 Technology related Parameters

#### Trench width

The trenches between individual mirrors and frame must be refilled before the structural polysilicon layer can be deposited. The proposed refill technology is based thermal oxidation. Therefore the trench width must be adapted with respect to the limits of this technology. The filling of a trench using thermal oxide is illustrated in Fig. 4.16 (a). According to Sec. 2.2 it takes 0.45 $\mu$m silicon for a 1$\mu$m-thick layer of thermal oxide. Thus, filling a trench with a width of $w'_g$ would require a layer of thermal oxide with thickness $w'_g/1.1$; the resulting trench width in the final device would then be $w'_g/0.55$. The trench width $w'_g$ corresponds to the trench width after the deep reactive ion etching step; photo-lithography and DRIE adds about 400nm to the layout value $w_g^m$. The relation between layout value and design value is therefore given with $w_g = (w_g^m + 0.4)/0.55$ (in $\mu$m).

The thickness of the thermal oxide should be minimized in order to minimize induced wafer bow and process time (see Sec. 2.2). The minimum trench width is given by the maximum aspect ratio that the DRIE process can provide, the substrate thickness and the minimum feature width. The base-line aspect ratio is 1:15; for a 10$\mu$m-thick substrate the minimum layout trench width would be about 0.7 $\mu$m. The minimum feature width given the used photomask-technology is 1$\mu$m, being therefore the limiting magnitude[15]. The layout trench width $w_g^m$ is thus set to 1$\mu$m and the resulting trench width after fabrication $w_g$ is about 2.5 $\mu$m.

Given the nature of this refill process, the trenches throughout the mask must have the same width everywhere. The first implication is that for having larger gaps anywhere within the device multiple trenches (or multi-slits) must be used. The concept of multi-slits is illustrated in Fig. 4.16 and explained exemplary for the case of a double-slit hereafter: Two parallel trenches, both having a width of $w_g$, are arranged such that the remaining bar in between is completely oxidized. The width of the bar is given with $\frac{0.45}{0.55}w_g$. Note that this value must be achieved with great exactness: if the bar is too small it is difficult to completely fill the trenches[16], if it is too wide, the bar cannot be completely oxidized and thus a thin residual stripe of silicon remains between the trenches after release of the device.

The resulting total width in the final device is two-times the minimum design width, i.e. 2·2.5 $\mu$m. The available design trench widths are thus $n$·2.5 $\mu$m with $n = 1, 2, 3...$. For the spacing between individual mirrors and frame single slits have been chosen. A couple of devices, serving as fall-back option, have been equipped with double-slits. For the spacing between mirror layer and outer handle frame (MIRA2) even quintuple-slits were implemented. In order to avoid buckling of the middle-bars during oxidation, due to the compressive nature of thermal oxide, the middle-bars were interrupted with small trenches as exhibited in Fig. 4.16 (b).

The second implication is that the individual trench itself must have an uniform width. This is not easy to achieve in corners and intersections, i.e. at mirror edges. Two solutions were implemented. The first applies to ⊤-intersections between mirrors: here a middle-bar with width $\frac{0.45}{2 \cdot 0.55}w_g$ between the $^{-}$ and the | was inserted (see Fig. 4.16 (c.1)), which, similarly to the bars between the multiple slits, is completely oxidized. Mirror edges at the array corners and corners of the chip edge were rounded off such that an uniform trench width could be assured (see Fig. 4.16 (b)).

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[15] For substrate thicknesses of 15$\mu$m and up, the limiting magnitude is the aspect ratio that the DRIE process can provide.

[16] Though it is still possible for a double slit by over-oxidizing; the trenches left and right of the former middle-bar is then filled from the bulk. In the case of multiple slits $> 2$ it is no longer possible to completely fill the trenches.

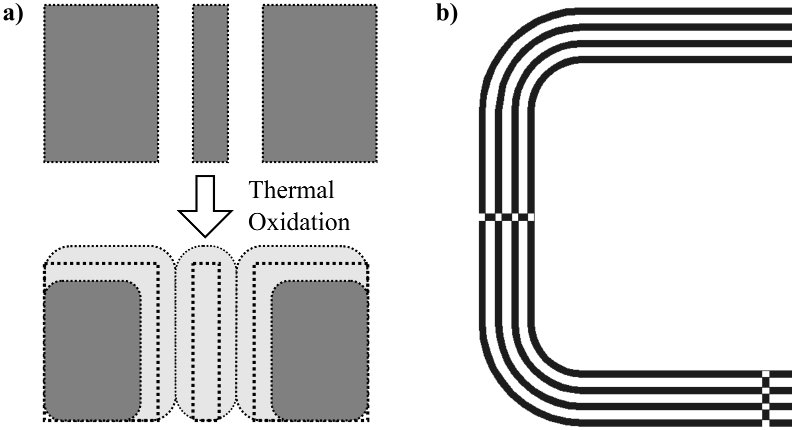

Figure 4.16: Trench refill principle and layout.

### Frame Width

From a performance point of view the frame width needs to be minimized. The frame serves as structural element and attachment site for the static end of the cantilever suspension beams. As for the function as structural element the requirement for small arrays we pose that the frame element bends less than 200nm in the z-direction under full load. Full load is achieved when all mirrors are in ON-state, i.e. a force of $F_{\mathrm{ON}} \approx 1\mu$N applies per mirror. We approximate the maximum z-deflection assuming a central load and a double-side clamped beam; the deflection of a double-sided clamped beam of length $l_f$, with a force $F$ applied at its center is given with

$$\delta_f = \frac{F l_f^3}{192 E I_y} \tag{4.31}$$

with $I_y = w_f t_f^3/12$. Using $F_{\mathrm{ON}} = 5 \cdot 1 \cdot 10^{-6}$N, $f_l = 5 * l_m$ and $f_t = 10\mu$m, we get a minimum frame width of $w_f = 10\mu$m.

In the large array architecture the frame is supported and attached locally to pillars and therefore the z-deflection requirement no longer applies. The minimum frame width is imposed by the minimum attachment surface of the polysilicon and alignment error of the chip assembly. From MIRA1 fabricated devices a width of $6\mu$m for the attachment surface (and a length of $20\mu$m) seemed to be sufficient.

The alignment error for the chip assembly of large arrays was specified to be ±3$\mu$m. Thus, the minimum frame width is set to $w_f = 6 + 6 = 12\mu$m and correspondingly the layout frame width to $w_f^m = w_f + 2\frac{0.45}{0.55}w_g \approx 14\mu$m.

### Polysilicon structures

In order to account for the overetching during the structuring of the polysilicon layer (see Ch. 5) the structure widths and lengths must be adapted. For the process base-line that was used for MIRA1 and MIRA2 an over-etching corresponding to 150% of the thickness of the polysilicon layer was foreseen; for $t_c = 0.6\mu$m this corresponds to a lateral underetching of about one micrometer (using RIE). Therefore for MIRA1 and MIRA2 the mask layout parameters for the polysilicon structures are given with $x_y^m = x_y + 1\mu$m for lengths (except for $l_c$, as the cantilever length is not affected by the overetching) and $x_y^m = x_y + 2\mu$m for widths. Note that in principle the only parameter that is affected by lateral dimensional reduction is the stiffness of the cantilever (reduced width); the stopper beam concept and thus, the ON-tilt-angle is not affected as long as within one mirror the underetch is uniform.

### Landing pads

The landing pad dimensions are implied by the alignment tolerance chain between the landing beams and landing pad: ±3$\mu$m for the alignment between the polysilicon structures and the alignment features etched in the device layer of the mirror chip, plus ±5$\mu$m for the assembly of mirror and electrode chip. An additional 2$\mu$m margin accounts for errors in the modeling, yielding in a landing pad size of $10 \times 10\mu\text{m}^2$. The landing pads reduce therefore the maximum usable electrode surface by about 1% and as consequence increases the required voltage by about 0.5%—this is negligible and therefore minimizing the landing pad surface by minimizing the aligment tolerances is not an important lever for optimizing the design performance.

## 4.4.2 Small Arrays

Layout specifics of the small array architecture (MIRA1) are presented hereafter.

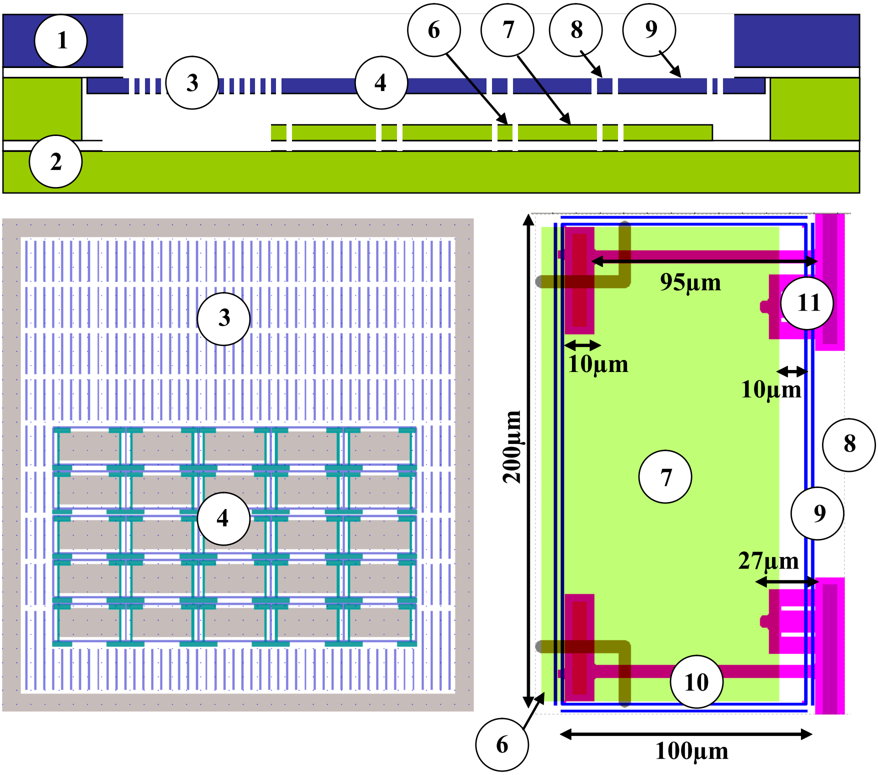

Figure 4.17: Layout MIRA1 of baseline design. 1. Mirror Chip 2. Electrode Chip 3. Opening for unobstructed illumination and release slits for device release 4. 5×5 Mirror Array 6. Landing Pad on electrode side and landing beam on mirror side 7. Electrode 8. Supporting frame 9. Mirror 10. Cantilever suspension 11. Stopper beam

### Device layout

The device layout of MIRA1 is illustrated in Fig. 4.17. The mirror chip is placed upside down on the integrated spacers of the electrode; the design of the spacers and the counterpart on the mirror chip side, serving for assembly of the two chips, is described further below. A large opening in the handle layer of the mirror chip allows for unobstructed illumination of the micromirrors: the minimum width of the opening on the array edge (perpendicular to the tilt-axis) is given with $h/\tan(\frac{\pi}{2} - 2\alpha_{\mathrm{ON}} - \arcsin(NA)/2)$, where $NA$ is numerical aperture of incoming light and $h$ the handle layer thickness. With $h = 350\mu$m and $NA = 0.16$ the minimum width of the opening is $350\mu$m. During fabrication this relatively large device-layer membrane (to this adds the surface of the actual mirror array!) is protected with a solid handle layer block, that falls out during release of the device[17].

The chip assembly concept implies that the handle and not the device layer of the mirror chip is posed on the spacers. The spacing between the two chips is therefore given by $h_p - t_m$, where $h_p$ is the spacer height. The spacer height equals the device layer thickness of the electrode chip and the mirror height equals the device layer thickness of the mirror chip. The air height $d_a$, i.e. the spacing between mirror and electrode, is given with $d_a = h_p - t_m - h_e$, where $h_e$ is the electrode height and can be tuned by timed etching (see Ch. 5). Given the nature of the timed etching process, the variation of the electrode height across the wafer is about 10% of the total etch height and therefore, as a rule of thumb, the designed height should be somewhat larger than 10% of the device layer thickness. The mirror height and air height are given by design with $10\mu$m and $33\mu$m, respectively; the device layer thickness of the electrode wafer is set to $50\mu$m and thus, the target electrode height is $7\mu$m.

In Fig. 4.17 the electrode and mirror layout is presented. According to the assumptions that were made in the device performance modeling, the landing and stopper beams must be very stiff compared to the suspension cantilever. The landing beams are two ultra-short cantilevers, having the same width as the suspension cantilever and a length $l_l \approx l_c/20\mu$m; the out-of-plane stiffness of the landing beams is therefore about 4000 higher than the stiffness of the cantilever suspension. The length of the stopper beams is imposed by design and in the range of 20-30$\mu$m. The reduced stiffness (compared to the landing beam) is partially compensated by an increased width $w_s = 30\mu$m. The resulting stiffness ratio between suspension

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[17] For more insights on the chip release process refer to Sec. 2.2.

cantilever and stopper beam is about 1 : 750. Even though this value is lower than required by modeling, it is still acceptable for very small arrays, where the process variations are negligible.

According to the electromechanical design, the electrode is shifted $10\mu$m relative to the mirror in x-direction. The landing pads, serving as contact zone for the landing beams, are electrically isolated from the electrode. The landing pads are centered around the nominal touch-down point of the landing beams; by modeling the touch-down point is located about $5\mu$m in x-direction[18] (parameter $o_l$, extracted from FEM) relative to the OFF-position of the landing beam tip.

The electrodes (and landing pads) are electrically separated from the substrate (handle layer of the electrode) by the buried oxide; the electrodes (and landing pads) are electrically isolated amongst them by trenches stopping on the oxide[19]. The electrodes (and landing pads) are connected through $40\mu$m-wide bars to bond pads in the chip periphery.

### Assembly

Fig. 4.18 shows layout and functioning of the guiding and clip system required for passive aligning of the two electrode and mirror chip. The guiding system consists of four angled cuboids on the electrode side and a counterpart on the mirror chip (etched into the device layer). The clip-springs, etched in the device layer of the mirror chip, engage whenever the mirror chip is arrived at the aligned position and prevent, when engaged, backwards and limit sidewards movement; forward movement is restricted in the aligned position by two stoppers located on the electrode chip.

The clip springs must hold the mirror chip in place under moderate accelerations; in particular it should be able to hold the mirror chip when the assembly is turned upside down. For the estimation of the mirror chip mass we approximate the chip as solid silicon cuboid, i.e. $m_C \approx w_c l_c t_c \rho_{\mathrm{Si}} \approx= 10^{-8}$kg. Assuming a friction coefficient of 0.05 the spring must push with a force of $2\mu$N. With the implemented spring dimensions of $10 \times 5 \times 200\mu\mathrm{m}^3$

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[18] By modeling no lateral movement (in y-direction) are present; for the non-ideal case, where also slight lateral movements may occur, a margin is included in the landing pad dimensions.

[19] A dielectric layer that is situated between electrodes can potentially degrade the electromechanical performance. However in our case the portion of uncovered $SiO_2$ is shielded to a great extend by the sidewalls of the electrodes. In the large array architecture the oxide layer situated between the electrodes is completely etched and therefore dielectric charging is no longer an issue.

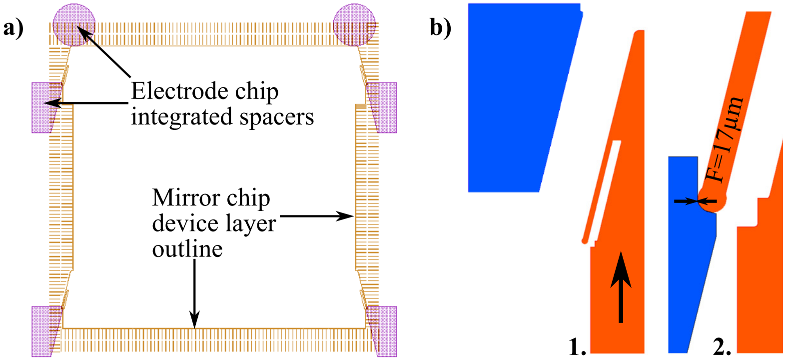

Figure 4.18: Guide and clip-system for passive aligning of the electrode and mirror chip. The angled cuboids on the electrode chip form together with the springs on the mirror chip the guide-and-clip system used to passively align (b.1) the electrode and the mirror chip with a precision better than 5$\mu$m. Once aligned, the clip-springs snap into the indentation on the angled cuboid and hold the two chips in the aligned position (b.2). Note that the cuboids act also as spacers between electrode and mirror chip.

and a displacement of 5$\mu$m in the engaged state, a force of 17$\mu$N is obtained.

### 4.4.3 Large Arrays

Layout specifics of the large array architecture (MIRA2) are presented hereafter.

#### Device Layout

The fundamental differences of the device layout compared to MIRA1 are that, first, the handle layer of the mirror chip is no longer present in the final device and, second, the mirror frame is supported locally by pillars. During fabrication the mirror chip is separated into the actual mirror chip (consisting only of the device layer of the SOI substrate) and a handle chip, supporting and protecting the mirror layer during assembly. A detailed description of the assembly procedure is given in 5.2.4; the layout features specifically designed for the assembly process are described further below.

Fig. 4.19 shows the device layout of MIRA2 and an exemplary mask layout depicting the arrangement of the pillars and the stopper and landing beams. The pillars on the electrode chip are arranged such that they support the mirror frame between the anchor sites of the cantilever suspension and stopper beams. The shape of the pillars is elliptical and the ellipse is oriented such that its long axis is parallel to the frame. The width of the ellipse (or the short axis half-diameter) and the width of the frame determine the requirements on the alignment tolerance of the assembly process. The width of the frame was set to 10$\mu$m (see Sec. 4.4.1). The minimum diameters of the pillars were determined experimentally: see Sec. 5.2.2. The pillar shape that proved to show an acceptable fabrication yield had a short axis half-diameter of 3.5 $\mu$m and a long axis half-diameter of 7$\mu$m. That implies that an alignment tolerance of ±1.5$\mu$m is allowable for that the pillar is still placed completely under the frame; allowing the pillar to be partially uncovered, another ±1.5$\mu$m can be granted without the pillar touching the mirror. The requirement on the maximum alignment error that is imposed on the assembly setup is therefore ±3$\mu$m.

On the electrode side, the pillars are surrounded by a foundation that has the same height level as the electrodes and electrically interconnects all pillars to a fixed potential. In contrast to the MIRA1 layout, the landing beam no longer hits a landing pad that is located on the same height level as the electrodes, but the substrate (i.e. the handle layer) of the electrode chip. Therefore a clearance, where the device layer is completely etched, between

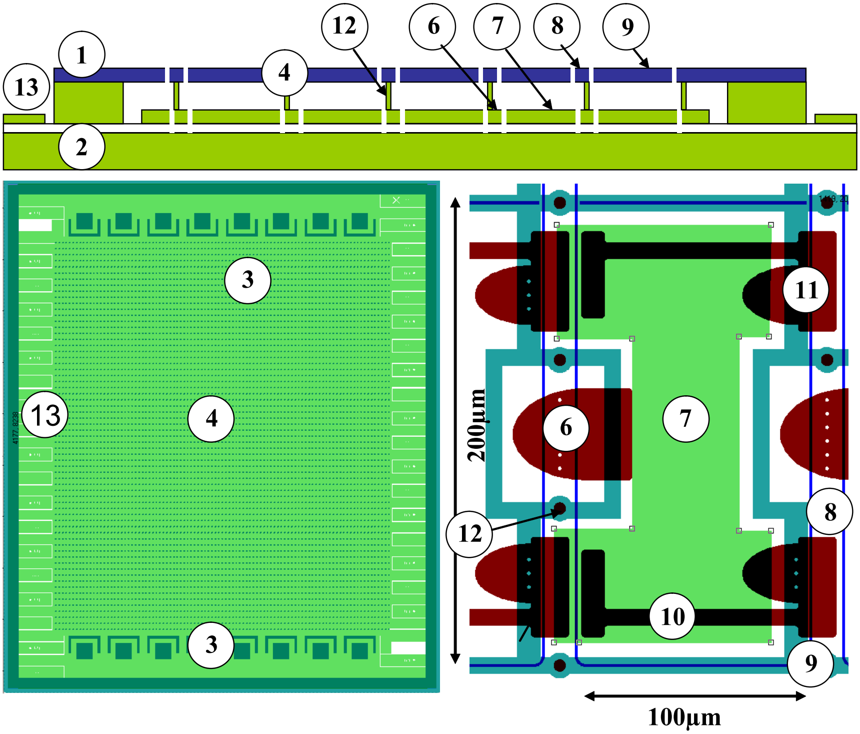

Figure 4.19: Layout MIRA2; example of 64×32 array. 1. Mirror Chip 2. Electrode Chip 3. Lateral spacers and alignment features for chip assembly (see also Fig. 4.21) 4. 64×32 Mirror Array 6. Landing Pad on electrode side and landing beam on mirror side 7. Electrode 8. Supporting frame 9. Mirror 10. Cantilever suspension 11. Stopper beam 12. Spacer column (or pillar) 13. Bonding pads

the pillars and the electrode is provided; we refer to it as a landing zone. Note that the buried oxide layer (BOX, the layer that separates the handle and device layer) is completely etched during release process; therefore no trapped-charge effects can occur.

The spacing that determines the tilt-angle is therefore purely given by the spacer height, i.e. by the thickness of the device layer of the electrode. The landing beams are adapted such that the lowest edge of the mirror in the ON position is still above the electrode height level. This situation is illustrated in Fig. 4.19. The distance of the lowest mirror edge to the electrode surface is designed to be $2\mu$m at least in order to prevent electrical breakthrough.

The landing beam shape is adapted to account for the reduced stiffness caused by the increased length (see Fig. 4.19). Furthermore, the stiffness of the landing beam and the stiffness of the stopper beams are matched such that the impact of polysilicon thickness variation is minimized: As the thickness variation of the polysilicon is rather a global than a local effect, the local thickness variation (within one mirror) can be considered as negligible, which makes it possible to fix the stiffness ratio between stopper and landing beam.

Given their size, release holes with $2\mu$m have been placed across the landing and stopper beams in order to facilitate the release process. The anchor, i.e. the attachment site of the landing and stopper beams and cantilever suspension has been adapted to minimize constraints on the mirror layer imposed by a stressed polysilicon-silicon interface. Instead of a continuous anchor surface, the polysilicon-silicon interface is engineered as a "‘riveted"’ surface: this is illustrated in Fig. 4.19. The slanted sidewalls between the riveted sites can absorb a part of the intrinsic stress after release of the mirror layer.

The above device architecture implies that, by modeling, $\alpha_{\mathrm{ON}}$ underlies no longer non-uniformities across the MMA caused by process variations. The only source that may cause a tilt-angle variation is a non-uniform thickness of the electrode SOI substrate or a non-uniform interface spacing that occurs during assembly. The instrument-dependent tilt-angle uniformity requirement is therefore translated directly into a specification on the Total Thickness Variation (TTV) of the device layer of the electrode substrate (and the uniformity of the interface spacing yielding from the assembly process). According to the calculations in Sec. 4.3.1 the TTV (assuming no other contributions to spacing variation) must be less than 300nm over the large array surface ($20\times20\mu\mathrm{m}^2$); assuming a wedge-type TTV, we can extrapolate this value to a TTV of about $1.5\mu$m for the device layer of a 4-inch wafer—which is a reasonable value for a total thickness of $35\mu$m of the device layer.

Different array sizes have been implemented: 42 × 21, 64 × 32 and 200 × 100 micromirrors. The 42 × 21 micromirror array supports row-column actuation (see below), the 64 × 32 and 200 × 100 array feature line-electrodes and therefore only line-wise actuation. The electrodes of all arrays are conceived such that all mirrors can be accessed by the 64-channels custom driving electronics. Thus, in the 200 × 100 array several line electrodes are clustered—a slightly different electrode surface from line to line within one cluster enables, at least in one direction, line-by-line switching of 200 line-electrodes.

### Row-Column Actuation

The implementation of the row-column algorithm (RCA) requires a special device architecture. Two different array architectures were designed, that enable row-column addressing. In the first architecture the mirrors, along the long-slit direction, are electrically separated into rows and the electrodes correspondingly into columns. On the array edge a bar etched in the handle layer of the mirror chip supports and belts the individual mirror frames. Beyond the supporting bar the mirror lines are connected to bonding pads, supported by large spacers on the electrode chip. An array size of 42 × 21 has been chosen for this architecture, enabling the operation and actuation of all 882 mirrors with the custom 64 high-voltage channels electronics.

In the second architecture the row-column separation is implemented purely on the electrode chip. This has the advantage that the design of the mirror layer is independent of the actuation scheme and no handle layer bar is required. The electrode chip is conceived such that line-electrodes are etched in the device layer (rows) and, perpendicularly, line-electrodes in the handle layer (columns); the mask layout is illustrated in Fig. 4.20 (a). The device layer electrode is structured such that the electrode surface underneath one mirror consists of about 60% of device electrode and 40% of handle electrode; a detailed view of the electrode layout is given in Fig. 4.20 (b). Note that the device layer electrode fills the part where the mirror is most sensitive in the ON-position. This is useful, as the device layer electrodes (rows) are used for holding the mirrors in the ON-position and the handle layer electrodes are reset to zero. The latter is necessary, as the handle layer electrodes in column $j$ serve as landing pad for the mirrors in column $j+1$ (see Fig. 4.20 (b)). This is taken into account in the row-column actuation scheme in Fig. 3.5, p. 57.[20]

### Assembly

Several layout aspects are related to the assembly concept for the large array architecture. The leading requirement implied by the assembly concept is that the mirror layer must be completely released from the mirror chip handle layer in order to avoid any mechanical constraints on the mirror layer.

The mirror layer consists of the 200 × 100 micromirrors, mirror frames and suspension and, specific for the assembly, alignment and bonding structures in the periphery. The mirror layer is separated by two means and in two steps from handle chip. A continuous large trench separates the mirror layer from the surrounding device layer. The trench is designed as quadruple-slit (see also Sec. 4.4.1 and in particular Fig. 4.16) in order to prevent jamming of the mirror layer after release: According to the built-in pretensions and the structuring of the SOI wafer, the bending of the silicon layer stack can change drastically after release and thus, the trench width between the relaxed mirror layer and the bent surrounding SOI-structure may be reduced by about 1–2$\mu$m.

Release slits in the periphery of the array and backside openings (handle layer etch) for the mirror release make sure that the mirror layer is completely released (detached) from the chip backside (handle layer) during final release etch of the chip (see Ch. 5). Note that not the complete handle layer on the backside of the mirror array is etched away but just rectangular openings, somewhat smaller than the mirrors themselves, leaving a grid that protects the mirror layer during further processing and handling.

In order to prevent the mirror layer to fall out of the handle chip after the release is complete, polysilicon latches are implemented in the periphery of the mirror array. Fig. 4.21 depicts the layout of the polysilicon latches: they are spanned between two attachment sites on the device layer of the handle chip over a bar of the mirror layer. Thus, after the release, the mirror layer is completely detached but restrained in the movement: in-plane by the device layer frame of the handle chip and in the vertical direction by the polysilicon latches on one side and the handle layer of the handle chip on the other side. The clearances are about $\pm 8\mu$m in-plane and $\pm 3\mu$m out-of-plane. The out-of-plane tilt-clearance of the mirror layer is given with $\arcsin(2 \cdot 10^{-2}/(6 \cdot 10^{-6})) \approx 0.3$mrad. This implies that the assembly

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[20] Though a column electrode 0 (left of first column), with voltage set to 0V, must be added, serving as a landing pad for the mirrors in column 1.

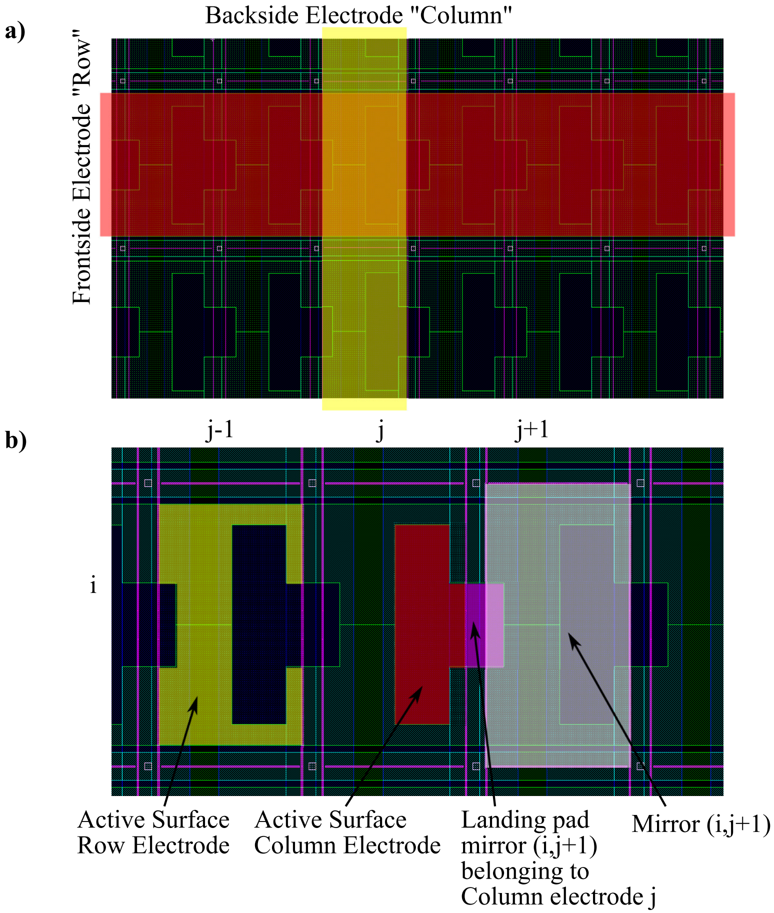

Figure 4.20: (a) Row-column architecture implemented purely on the electrode chip. The electrode rows are etched into the device layer and the columns into the handle layer. (b) Windows are etched into the electrode lines in the device layer such that the handle layer electrodes are not completely shielded.

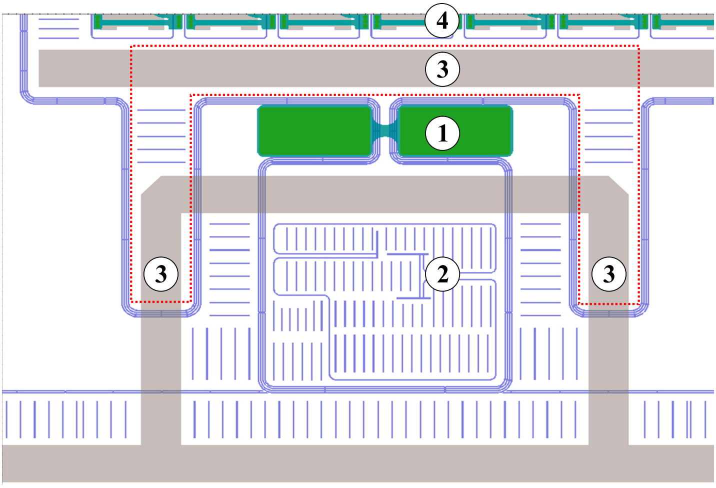

Figure 4.21: Layout features specific for the assembly. 1. Polysilicon latch 2. Alignment marks 3. Protection wall, prevents debris from polysilicon latch glowing to be scattered on the mirrors on the array edge 4. Edge of the mirror array

setup must be able to achieve a parallelism between the handle chip and the electrode chip better than 0.3 mrad[21].

The polysilicon latches are fused after assembly of the mirror layer and the electrode chip. For preventing that the debris created during this process spills out in the sensible mirror array area, a wall, implemented on the electrode chip, encloses the area around the latches (depicted in Fig. 4.21). Within the same area the alignment features for aligning the electrode chip and mirror layer are located. They consist of two shifted, rectangular 2$\mu$m wide beams in the mirror layer and of a counterpart on the electrode chip. When aligned, the bars form a seamless rectangular corner; in conjunction with a 10x microscope this system allows alignment within 2$\mu$m. As the mirror layer and handle chip obstruct the line of sight between microscope and electrode chip during assembly, a window in the handle chip and a clearing around the alignment bars in the mirror layer are etched.

### Chip holder

In order to accommodate for the assembly of the very fragile mirror chip, dedicated chip holders were designed and fabricated. The chip holder is a part of the assembly setup that is presented in Sec. 5.2.4. For each mirror array size a dedicated chip holder was designed.

Fig. 4.22 shows the chip holder concept and layout. The silicon chip holder provides a fixture for the mirror chip for holding it upside down during assembly. As with mechanical clamping solutions the risk of destroying the very fragile mirror layer is very high, vacuum clamping is used instead. In order to avoid that vacuum suction destroys the released mirrors, the two vacuum slits of the chip holder are placed such that they overlay with handling zones of the backside of the mirror handle chip. The handling zone is 400$\mu$m wide and the length corresponds to about one side of the mirror array. Allowing a tolerance of ±150$\mu$m for posing the mirror chip on the chip holder, the vacuum slits on the chip holder are 100$\mu$m wide and the length corresponds to one side of the considered mirror array minus

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[21] parallelism is always a concern in chip assembly techniques. However, in conjunction with a compliant chip holder fixture, a slight parallelism error is auto-compensated by pressing the two chips together with considerable force. This is applicable for chip architectures that are designed for sustaining relatively large pressures during chip-to-chip bonding. In our case the applied pressure during assembly must be minimized due to the very fragile structures. In a future development one might consider to implement a chip holder or handle chip architecture which would provide a very compliant fixture and would enable auto-compensating of parallelism errors with very little pressure.

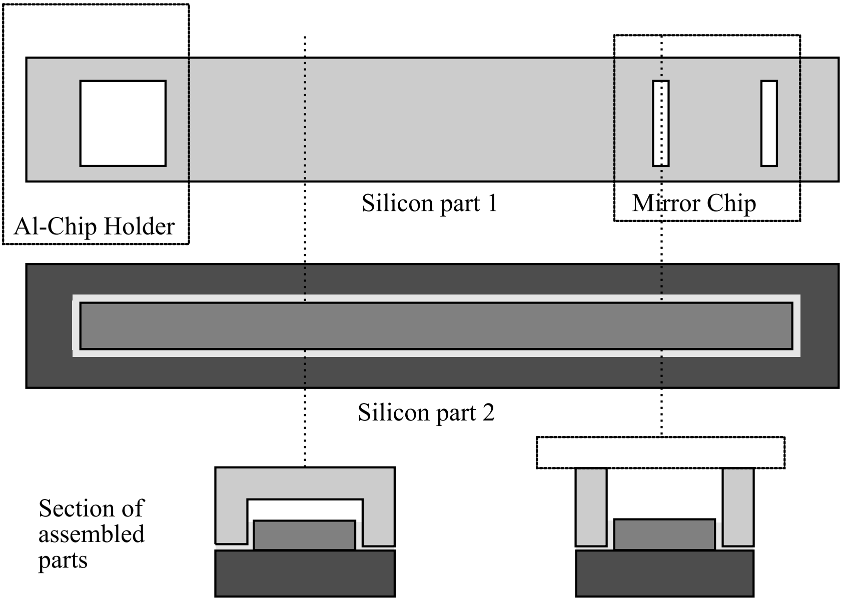

Figure 4.22: Chip holder concept and layout

the alignment tolerance of ±150$\mu$m. A buried channel connects the vacuum slits with a larger opening for vacuum connection to a machined aluminum workpiece (part of the alignment setup, described in Sec. 5.2.4). The chip holder is designed such that the alignment structures of the mirror chip is not obstructed: for small arrays, windows allow seeing through the chip holder. The chip holders for large arrays are kept less wide than the mirror chip such that the alignment features on the chip edges are visible.

The chip holder is manufactured from two assembled silicon parts. The individual parts are microfabricated based on a SOI wafer, using a front- and backside deep reactive ion etching step and a subsequent hydrofluoric acid release step. Fig. 4.22 depicts schematically the chip holder concept and the mask layout exemplary for the 200 × 100 mirror array chip holder. The two vacuum slits are each 2mm long and thus, assuming ideal conditions, provide a clamping force of about $2 \cdot 10^5\mathrm{Pa} \times 10^{-4}\mathrm{m} \times 2 \cdot 10^-2\mathrm{m} = 4 \cdot 10^{-1}\mathrm{N}$. The mass of the 200x100 mirror array chip is about $4 \cdot 10^{-4}$ and therefore the clamping force is sufficient to hold the mirror chip upside down.

# Chapter 5

# Fabrication

## 5.1 Process Flow

The overall fabrication process includes the following steps:

- Processing of the mirror chips
- Processing of the electrode chips
- Assembly of the mirror chip and electrode chip
- Packaging of the assembled micromirror device

Below the main steps of the mirror and electrode chip fabrication sequence are summarized. The fabrication process for MIRA1 and MIRA2 generation are identical, unless otherwise noted. Evident steps as for instance photolithography, resist stripping, etc., are omitted here.

### 5.1.1 Mirror Chip

Fig 5.1 shows the fabrication process of the mirror chip. The device layer of a silicon-on-insulator (SOI) wafer is structured into horizontal mirrors and supporting frame by deep reactive ion etching (DRIE). At the same time the trenches for the dice free release (see Sec.2.2) are etched. A combination of thermal oxidation and chemical vapor deposited (CVD) is used to refill the trenches between the mirrors and the frame. Note that this oxide layer is also used as sacrificial layer between the silicon device layer and the polysilicon layer. Reactive ion etching (RIE) is used afterward to open the $SiO_2$ where the suspension is attached to the mirrors and the frame. A polysilicon layer is then deposited by CVD and doped. Then the suspension and the landing posts are etched into the polysilicon layer—this can be done by either DRIE or RIE. In a final DRIE step the backside openings of the mirror and the dice free chip release trenches are etched into the handle layer. First the mirrors and then the whole chips are released in a dry HF vapor etch step (see Sec.2.2). The mirror chips are now ready for assembly with the electrode chip.

### 5.1.2 Electrode Chip

Fig. 5.2 shows the fabrication process of the electrode chip. The device layer of a SOI wafer is patterned using a self-aligned delay mask process [27]. In the first step a thermal silicon dioxide is grown. In the first photolithography and subsequent RIE step the spacer mask is coarsely defined in the oxide mask. In the second photolithography and RIE step the precise form of the spacer is defined in the oxide mask and at the same time the electrodes, connection pads and connecting lines are patterned into photoresist. Then by time controlled deep reactive ion etching the first couples of micrometers are etched. This step defines the height of the electrodes and connecting lines. After oxygen plasma resist strip the remaining thickness of the device layer is etched. In that way the electrode and connecting lines pattern is transferred to the bottom of the device layer, while the spacers, protected by a silicon dioxide mask, still have the initial height of the device layer. In order to minimize sources for short-circuit, an thermal oxidation step of 200nm is carried out to remove possible silicon residues originating from the delay mask DRIE. In MIRA1 (small array architecture) the wafer is diced in a final step to obtain the individual electrode chips. In MIRA2 the frontside processing is followed by a backside DRIE and a HF release step, similar to the mirror chip fabrication[1].

The last fabrication step is the assembly of the electrode and the mirror chip (Fig. 5.2 (d)). This process step differs for the small and the large array generation and is described hereafter.

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[1] The dice-free release step is required to account for the many different chip sizes in the second MMA generation.

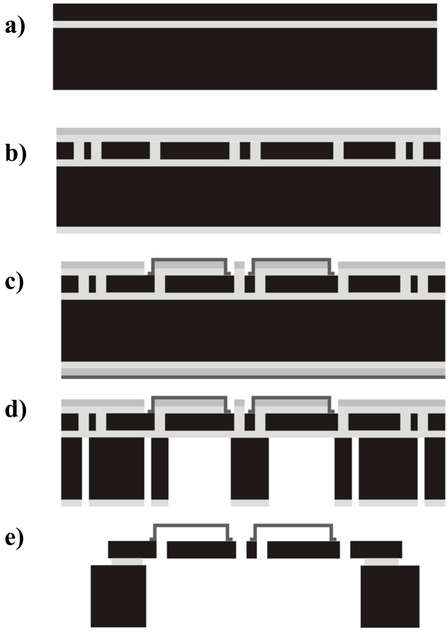

Figure 5.1: Mirror chip fabrication sequence. As starting substrates a SOI wafer with a 10$\mu$m-thick device layer is utilized (a). In a first step the mirrors, frames and alignment structures (clip-system) is etched into the device layer using DRIE (b). Then the trenches are refilled using a combination of thermal oxidation and APCVD $SiO_2$ (c). The oxide layer is opened at the attachment sites for the polysilicon structures and a polysilicon layer, using LPCVD, is deposited and doped. Then the polysilicon layer is structured using DRIE yielding the cantilevers and stopper beams (d). A backside DRIE is carried out providing openings for the mirrors and trenches for later chip release (e). In a final step the mirrors are released and the chips are singulated by etching the buried oxide layer with HF vapor (e). The chips are now ready for assembly with the electrode chip.

Figure 5.2: Electrode chip fabrication process sequence. As starting substrate a SOI wafer with a 50$\mu$m-thick device layer (35$\mu$m for MIRA2) is utilized (a). In a two-level DRIE process (delay mask process [27]) the electrodes (lower level) and spacers are etched into the device layer. In a first step the patterns of the lower level are etched utilizing a resist mask(b); at this time the height of the electrodes is defined through timed-etching. Then the resist mask is removed and the pattern is transferred to the bottom of the device layer, such that the trenches between the electrodes are completely etched and provide electrical insulation. The spacer structures are protected during the two etch steps with an oxide mask, so that the resulting spacers have the height of the initial thickness of the device layer. After completion of the delay mask process the chips are singulated either by dicing (MIRA1) or a dice-free release process, involving an additional DRIE of the backside and HF vapor release (MIRA2).

### 5.1.3 Assembly of MIRA1 Chips

The assembly of small array architecture chips consists of three steps:

1. Applying a thin glue film on the spacers of the electrode chip
2. Bring into contact the two chips and push the mirror chip into the spring-loaded end-stop position, whereas the chip is guided laterally through on-chip guiding structures
3. Post-bake of the chips for glue hardening

The assembly is carried using simple tweezers for initial assembly and spring-loaded prober needles for pushing the mirror chip into the end-stops.

### 5.1.4 Assembly of MIRA2 Chips

Assembly of the MIRA2 chips was carried out using a custom built assembly setup (see Sec.5.2.4), installed under a white-light interferometer (Veeco Wyko NT1100, see Sec. 2.3.3). The assembly of large array architecture chips consists of the following steps:

1. Applying a thin glue film on the lateral spacers of the electrode chip
2. Posing the electrode chip on the vacuum chuck (hotplate) and the mirror chip on the dedicated vacuum gripper
3. Adjust parallelism of the two chips, using the interferometer as feedback
4. Bring the two chips into proximity, use the vertical scanning interferometer as feedback
5. Align the two chips with respect to the in-plane degrees of freedom
6. Bring into contact the two chips, feedback with interferometer
7. Release mirror chip gripper from mirror handle frame and post-bake the glue at 100° during one hour using the hotplate
8. Remove assembled device from hot-plate and remove mirror chip handle frame

## 5.2 Fabrication Details

The fabrication was carried out at the IMT Cleanroom. The cleanroom was equipped with all major MEMS processing technology and besides research activities it has the resources for small series production. Given that fact, most of the equipment (in particular the DRIE and RIE machines) are operated by technical staff that are experts in their respective field and guarantee the continuity of process knowledge.

This section gives an in-depth discussion of selected key elements of the fabrication process. A summary of the process parameters is given in the Appendix.

### 5.2.1 Micromirror

**Gap Refill** It could only be determined with certainty that the trench is completely and hermetically filled at the very end of the process when the device was finally released. I.e. even though when a trench appeared to be completely filled in a cross-sectional SEM analysis, the polysilicon could still find its way in hidden voids and very shallow trenches leaving residues after final release etch of the trench oxide. This made the optimization of the trench refill difficult.

The process base-line was to use technologies that were available at IMT cleanroom: thermal oxidation, APCVD or PECVD of SiO2. The most conformal oxide deposition technique is the thermal growth of SiO2 from bulk silicon. One precondition for the fill with thermal oxide is that the trench width is the same everywhere. Even though by design/mask layout this condition is met, the gap width still varies after the device layer DRIE due to process variations. There are variations from wafer to wafer and variations within one wafer; the variations from wafer to wafer can be accounted for by measuring the effective gap width after DRIE for each wafer and adapting the amount of thermal oxidation. By design a nominal effective gap after photolithography and DRIE was assumed to be the designed gap width plus 400nm. It turned out that this assumed value was lower than the real value. Fig. 5.3 (a) shows a double gap which nominally should have been filled after an oxidation of 1.8$\mu$m; clearly the gap is not completely filled leaving a thin open trench. A second oxidation step of additionally 0.5$\mu$m thermal oxide was necessary to completely fill the gap, as shown in Fig. 5.3 (b)—a slight overfill accounts for gap width variations across the wafer. Even though the thermal growth of oxide with an overfill was able to close the gaps throughout the wafer completely it has serious drawbacks that are related to the growth mechanism of the thermal oxide. The first drawback is that the thermal oxide continues to grow in the trenches, though at slower rate, when the trench is completely filled. This exerts a huge compressive stress on the device layer, as the oxide cannot expand, being confined in the trenches. The effect is a large wafer bow and even worse, voids and shallow trenches can be formed, as the middle bar in the double slits is pushed upwards under the huge pressure[2]. This effect can clearly be seen in Figure 5.3 (b) where the middle bar is pushed up by about one micrometer. Note also the shallow trench right and left of the middle bar. Partially this shallow trench is related to the fact that the middle bar is pushed upwards; the main cause is also a direct consequence of the growth mechanism[3]: unlike in a deposition process (e.g. PECVD SiO2) the thermal SiO2 requires bulk silicon in order to grow, i.e. it grows at the Si/SiO2 interface pushing the SiO2 outwards. A simple geometrical reflection leads easily to the conclusion that the shallow trench at the interface between the oxide originating from the middle bar and the oxide originating from the other trench border will never be filled up by further growing thermal oxide. Another consequence is partial plastic deformation of the mirror layer; this is unveiled in Sec. 6.1.1.

As consequence an additional oxide layer using a deposition technique is required in order to fill up completely the remaining voids and shallow trenches to a maximum extend. PECVD and APCVD SiO2 have been tried which both showed acceptable results. Fig. 5.3 (c) shows the trench from (b) with an additional 1$\mu$m thick APCVD SiO2 layer. Due to charging of the oxide in the SEM the image is not very clear but one can still guess that the additional APCVD SiO2 layer at least partially filled up the shallow trenches. Unfortunately it still leaves a certain topology and, as it was revealed after polysilicon deposition, some of the voids where not completely closed. Apparently the only way to completely fill voids and cancel out topography, i.e. planarizing the substrate, was to use oxide in a liquid phase: driven by capillary force a liquid would naturally find its way into small dips and holes leveling everything out. Technologically there are two options: spin-on glass (SOG), which is spin-coated on the substrate in liquid phase and solidified subsequently at elevated temperatures. An experiment carried out with a solution of pure SiO2 from Emulsitone[4] revealed that the spin-on

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[2] This effect could almost be compared to the clash of tectonic plates and the subsequent formation of mountains.

[3] For more detailed information on this topic refer to Sec. 2.2.

[4] http://www.emulsitone.com/

SiO2 layer started to crack and become brittle when exposing to very high temperatures, which are required for the subsequent polysilicon deposition and doping steps.

The second way of filling the voids with a liquid phase oxide is to deposit a highly doped oxide and carry out a reflow step. This technique was explored for the large array architecture (MIRA2). Oxide doped with 4% boron and 4% phosphor (so called BPSG for Boron-Phosphor Silicate Glass) starts to become viscous and beginns to reflow at temperatures as low as 700°C. A 1$\mu$m thick BPSG layer with 4% boron and 4% phosphor content has been deposited (at the CMI of the EPFL[5]) on trenches that have been prefilled with thermal oxidation; the second option was to deposit a 2$\mu$m-thick BPSG layer without prior oxidation of the trenches. Subsequently the BPSG layer has been reflown at 1050°C during one hour. The result is shown in Figure 5.4. In the trenches without thermal oxide, enclosed air or gas formation within the BPSG caused the BPSG to bend upwards and form bubbles at the surface (a)[6]; this was not observed for the trenches that were prefilled with thermal oxide: here the reflown BPSG layer not only filled up voids and shallow trenches but also planarized the topography remaining from the thermal oxide gap refill (b). Whereas the property of BPSG to reflow at elevated temperature is a desirable effect for the trench filling, it represents a limitation on subsequent high-temperature steps. In Fig. 5.5 (a) a zoom-in of a deposited, annealed and structured polysilicon feature is given; the polysilicon structures show serious deterioriation at certain parts, originating from the underlying layer. It was believed that this effect was partially related to the effect observed in Fig. 5.4, the formation of BPSG bubbles, and caused by the high anneal temperature of the polysilicon layer (1050°C). Lowering the anneal temperature to 900° seemed to alleviate this effect (Fig. 5.5 (a))—though the lower anneal temperature is less effective in

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[5] http://cmi.epfl.ch/

[6] The bubble has a diameter of about 5$\mu$m, the bubble sidewall thickness is in the range of 100nm at the thinnest location. The cause for this bubble formation is probably gas that has been trapped during the deposition process of the BPSG layer. In the subsequent reflow process an overpressure in the encapsulated trench void caused bubbling of the liquified BPSG (this effect is very comparable to the traditional glass blowing technique!). It is clear that this bubbling occurs only in the presence of a pressure difference between the enclosed gas in the trench void and the surrounding atmosphere during the reflow process. In the considered BPSG trench refill experiment the deposition of the BPSG was an LTO LPCVD at 200 Torr; the reflow process was carried under N2 atmosphere at a pressure slightly below 200 Torr. Of course one could adjust the pressures in the two steps in order to avoid this effect or even make use of it by reversing the pressure difference, such that the BPSG is pushed into the trenches.

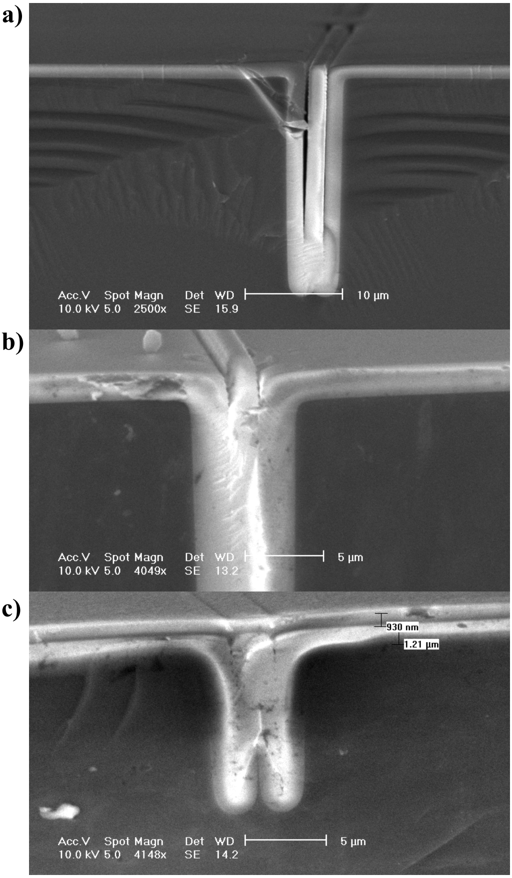

Figure 5.3: Trench fill baseline process. (a) shows a partially filled double-slit trench after incomplete oxidation; the trench is, expect for a dip at the top surface, completely filled after a second oxidation step (b); a 1$\mu$m-thick APCVD $SiO_2$ layer is added to ensure complete fill and partial planarization of the topology that is present after oxidation (c).

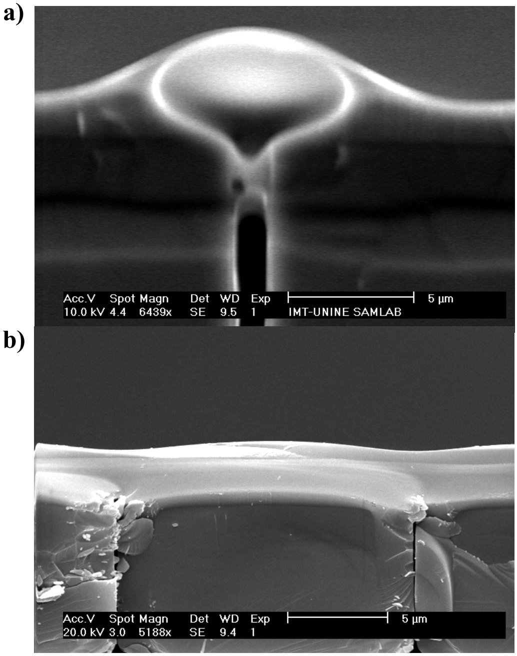

Figure 5.4: Trench refill using BPSG and reflow. In (a) no pre-fill with thermal oxide was utilized; the trapped gas in the cavity expanded during reflow and caused bubbles in the BPSG layer, located over the trenches (this effect can be considered as blowing glass at the micron-scale). With thermal oxide prefill the reflowed BPSG revealed a good trench refill and a fairly good planarization (b).

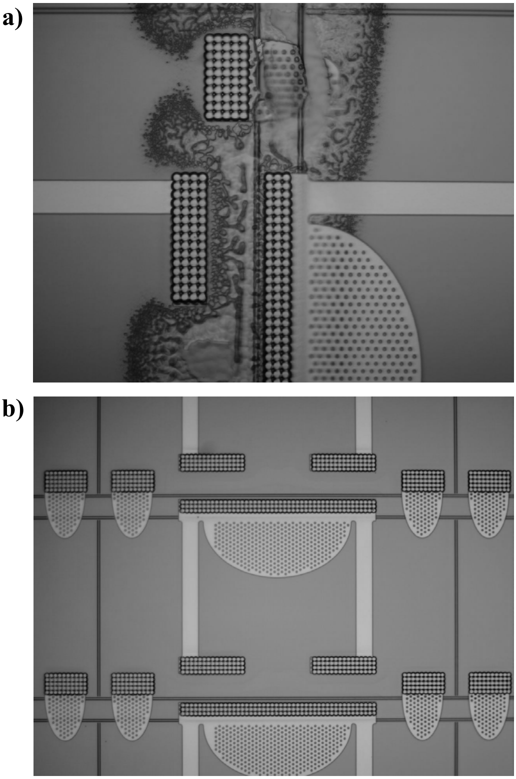

Figure 5.5: BPSG filled trenches after polysilicon deposition, annealing and structuring. Annealing (and doping) of polysilicon at 1050° caused the underlying BPSG layer to reflow; further gas formation and/or gas expansion in the trenches was believed to cause deterioration of the polysilicon layer (a). Reducing the anneal temperature seemed to alleviate this issue (b).

terms of stress relieve in the polysilicon layer

Another issue that was related to the use of BPSG were the formation of phosphorous and boric acids during the final HF vapor release step. Removal of these residues implies a device release in (liquid) BHF, which implies a process redesign and is subject for future work (see also Sec. 5.3.3).

In summary the most reliable trench refilling technique, that worked well for MIRA1 fabrication, was the combination of thermal oxidation and low doped APCVD oxide, as exhibited in Fig. 5.3. Even though the BPSG reflow technique showed the best results regarding the trench fill (in combination with a thermal oxide pre-fill) and topology reduction (planarization), it was not compatible with the subsequent processing steps.

**Polysilicon layer—structure preservation** Even though the polysilicon layer was only 600nm thick, its structuring—meaning: the complete removal of the polysilicon where it shouldn't be—was not trivial. In fact, the topology created by the gap-filling process provides a lot of cavities for the polysilicon: the very high aspect ratio in the hyperbolic cone-shaped indents above the trenches (see Fig. 5.3 (b)) yielded an effective polysilicon thickness twice or more than the nominal thickness. Therefore the etch time during the RIE process was doubled and more to clean out these cone-dips. Unfortunately this overetch not only reduced the design-dimensions of the polysilicon structures but also transformed the stopper-beams located on the mirror to nano-tips: Fig. 5.6 (a) shows a SEM of a mirror stopper beam after RIE overetching. The radius of the tip (that was designed to be a rectangular shaped end with a width of 2m) is probably below 10nm. It appears that the underetching of this rectangular shaped stopper beam end was highly anisotropic. This effect that happened only for the very small structures (no effect seen for the larger stopper beam located on the frame) is a reproducible result, but not fully understood. Either way it is not acceptable for operation as this tips break of easily when they touch the landing pad on the electrode chip, or worse, they get stuck. The design was changed for the second generation of MMA avoiding the small feature size and possible edge effects. A near-notch free DRIE recipe has been chosen, which showed a better structure preservation, even when heavily overetching: Fig. 5.6 (b).

**Wafer bow and stress: keeping the balance** An issue that one should take into particular consideration when designing a microfabrication process is the wafer bow. Whenever adding (and sometimes even when taking away) material to the wafer one induces stress and causes the wafer to warp. This

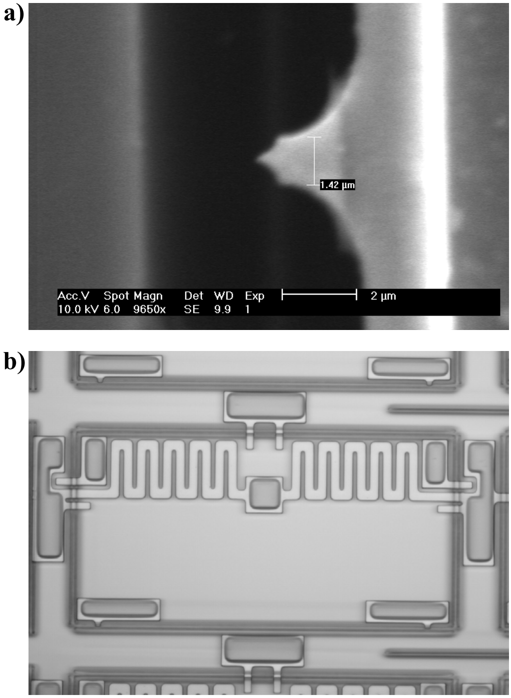

Figure 5.6: Polysilicon etching. A heavy overetch is required to remove the polysilicon in the dips that remain from the trench fill process. A RIE etch revealed strong anisotropic overetch (a), transforming the landing beams into nanotips—which is a highly undesirable effect, seen the function of the landing beam as mechanical stopper. A DRIE process, even though not conceived for etching very thin layers, has been employed that proved to be very efficient for structure preservation even when largely overetching (b). Note that the different stopper beams in this design have the same lateral dimension (4$\mu$m) as in (a).

wafer bow/warp is a real yield-killer; many issues during processing can be related to too much stress in the wafer/material stack. A typical issue that occurred also in the present mirror chip fabrication was the failure of the automatic handling tools due to a very large bow of the wafers. This caused the loss of a few wafers but even more serious, it made the handle layer (or backside) etching impossible in some cases. In fact the bow was such that the electrostatic chuck of the DRIE machine couldn't no longer clamp the wafer, causing a large helium leakage and failure of the etching. A root cause analysis revealed that the gap filling with thermal oxide is to blame. In theory if a silicon wafer is thermally oxidized it won't bow as the thermal oxide induces equal compressive stress of the front and backside of the wafer: the stress on the front and the backside balance each other. In our case however the compressive stress exerted by the oxide layer on the front side was much higher than the stress exerted by the same layer on the backside—caused by the trench filling on the front side. As already mentioned before, the thermal oxide in the trench pushes the trenches apart[7], the pressure created in the trenches yields a much larger compressive stress in the device layer than by the thermal oxide on an even surface. To account for this disequilibrium two measures were taken: the compressive stress on the backside was increased by depositing a compressive PECVD SiO2 layer; this approach didn't prove very efficient, as the PECVD parameters normally are tuned to deliver the least (compressive) stressed layers and the development of a highly compressive stressed PECVD SiO2 coating would have been somewhat against common sense. The other tactic was to reduce the compressive stress on the topside by etching away some of the thermal SiO2 until the wafer bow was in an acceptable range of below 150$\mu$m. This approach worked out, with the drawback that the polysilicon structures on the frontside were partly underetched and therefore particularly vulnerable, as the wafer is placed upside down on the chuck for the backside (or handle) DRIE. A resist layer was applied on the frontside before processing the backside in order to protect the polysilicon structures to a maximum extend. In conclusion it is possible to balance out the stresses and reduce the wafer bow to a great extend. However it comes at the cost of a longer and riskier process flow. As always it would be more clever to avoid the problem from the beginning than trying to solve it afterwards, i.e. avoiding the very large compressive stress on the frontside using another gap fill process. This is discussed in Sec. 5.3.3

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[7] A good analogon is the way formerly large granite blocks were cleaved: first holes were drilled and then filled with wood plugs, which were wetted subsequently. The water causing the wood to expand and exert enough pressure to split the massive granite block.

### 5.2.2 Electrode

**Self-aligned delay mask process** Even though the self-aligned delay mask process is established technology, the particular geometry of the electrode chip—particularly the small array electrodes—required process development. The difficulty was the imbalance of critical dimension and surface to be etched between the two layers or etch steps. The upper layer consist of the spacers that cover only a small percentage of the surface, i.e. a large percentage of the surface is to be etched. The lower layer consist of the electrodes, connecting lines and bonding pads filling out a large surface but with small feature size and gaps. Furthermore the lower level must be etched to a target height of 5$\mu$m, which is small compared to the total etch depth of 50$\mu$m. This has two main implications. The first is related to the etch non-uniformity across the wafer. The etch non-uniformity is about 10% to 15% etch speed variation accross the wafer. Given the target height of 5$\mu$m, about 45$\mu$m of silicon must be etched, yielding in a height variation of total 7$\mu$m at the lower level. Thus, the nominal height must be targeted in a zone on the wafer which is in the middle range of etch speed in order to avoid regions where the lower level is completely etched away. However, this is relevant only for the yield of the fabrication process, i.e. the number of usable electrode chips per wafer. In our case the small array chips are meant for research, therefore hand-picking the chips from the good zones on the wafer and discarding the rest is acceptable—particularly, as there was a great number of electrodes per wafer for the small arrays. When going towards development of a prototype or even series fabrication yield is a primary concern; therefore the design and process has been adapted for the large arrays, where the usable wafer surface is of primary concern seen the few number of chips that fit on one wafer. Here, due to the different assembly concept and the fact that the mirror lands on the handle substrate and not on the lower level, the spacer height is reduced to 35$\mu$m, the lower level still being 5$\mu$m. Therefore only 30$\mu$m of silicon have to be etched resulting in a smaller absolute height variation.

Fig. 5.7 (a) shows strongly overetched connection lines that connect the electrodes of a 5x5 array to the peripheral bonding pads. A closer look unveils that the overetching is even stronger at the sites where large open surfaces are neighboring: such as at the intersection between two electrodes and at the place where the connection line leaves the electrode array. An additional effect that caused partial vanishing of the thin connection lines is showed in Fig. 5.7 (b): it can be described best as tapered edges. It

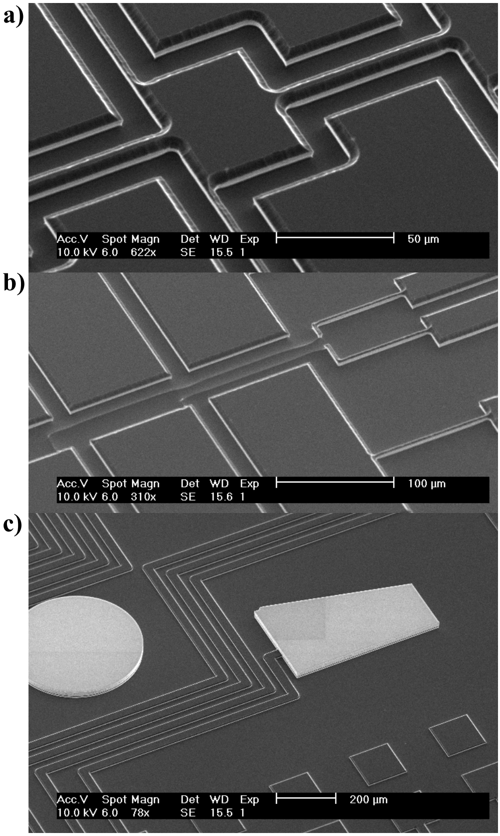

Figure 5.7: Delay mask etching of small array electrodes (MIRA1). Overetching of the bottom layer (electrodes and connecting lines) (a) was believed to originate from tapered etches (b) and mismatch between large surfaces to be etched and small trenches between electrodes. The tapered etches probably originated from RIE etching of the oxide mask, that was used to protect the spacers. Utilizing BHF etching of the oxide mask, an improved DRIE process and admitting somewhat higher electrodes (less etching) could resolve the above issues (c). Note that the white structures are the spacer and guiding structures utilized for subsequent self-aligning chip assembly. The height of the spacers is $50\mu$m and the height of the electrodes around $10\mu$m

is evident that these tapered edges are transferred inwards during the pattern is etched downwards, i.e. a line of initial rectangular section ends in a line with triangular section—this causes a thinning of the line and thus an even faster overetching. The cause for this effect was that here RIE was used for structuring the oxide mask, in order to reduce undercut and thus dimensional loss that is associated with a wet oxide-etch process. A precise dimensional control was required for the counterpart of the clip-spring assembly system. As the selectivity of the RIE oxide-etch towards silicon is not as high as in the case of BHF, some of the silicon was pre-etched during the first and second oxide-etch step, which caused slight beveling of the edges. This problem was solved by using BHF for the oxide structuring and allowing a certain dimensional loss of the spacer structures (and hence a less-than-optimal counterpart of the clip-springs). This dimensional loss was accounted for in the design of the large array electrodes; in the case of the large array the underetching of the oxide mask was also less pronounced as here a 300nm thick oxide layer was sufficient for the reduced etch depth.

Finally, using BHF for structuring the oxide mask, a somewhat higher target value for the lower level height and improved DRIE process yielded in usable electrodes for the small array MMAs. Fig. 5.7 (c) shows a section of an small array electrode chip with the spacers and guiding structures at the top level and connection lines and bonding pads in the lower level.

**Small pillars—from square to elliptical cross-section** Learning from the challenges from the small array electrode geometry, the design of the large array electrodes was adapted such that the structure and gap widths over the array where homogenized to a maximum extend - this is true for the lower level. The introduction of very thin pillars with very high aspect ratios on the upper level combined with rather small gaps on the lower level increased the process complexity again. In a first design iteration, a square section of $5\text{x}5\mu\text{m}^2$ has been chosen for the pillars; Figure 5.8 (a) shows a successful example of these pillars. One can see that the pillars tend to get thinner towards the base, which is related to the large etched surface surrounding the pillar.

In a second design iteration the pillars where all designed to have an elliptical cross-section, with half-axis length of $3.5\mu$m and $7\mu$m. This change, together with an improved process, yielded in very reliable pillar: even after processing the backside, where the etched pillars laid upside down on the wafer chuck, no broken pillar was observed! Recall that on one 200x100 electrode chip, an impressive number of 60’000 pillars are present. Figure 5.8

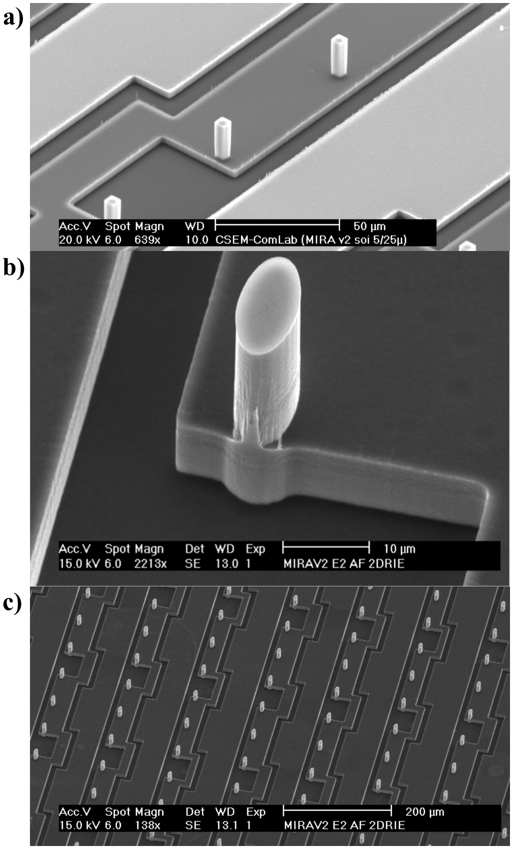

Figure 5.8: Large array electrodes (MIRA2). Unlike in the MIRA1 design the spacers are distributed over the array; the spacers are small pillars located between the line electrodes. (a) First generation of pillars having a square section; for improved stability, the second generation of pillars were changed to have an elliptic cross-section (b) and proved to be extremely rugged: in several large arrays (60’000 pillars!) no broken pillars have been found after fabrication; (c) shows a section of a fabricated 100×200 electrode.

(b) shows a single second generation pillar and (c) exhibits a section of a $200\times100$ array electrode.

### 5.2.3 Assembly of Small Arrays

The alignment procedure was conceived such that the only active displacement of the mirror chip is in positive y-direction. The x-translation and the z-axis rotation are self-aligning through the in-plane guide structures (see Sec. 4.4.2, Fig. 4.18, p. 104). The assembly procedure was carried out in a prober station, featuring prober needles, each mounted on a spring-loaded, manual xyz-translational stage for fine positioning. The prober station is equipped with an optical microscope for observing chip alignment.

The electrode chip was placed on the vacuum chuck of the prober station. The mirror chip was placed upside down within the pre-alignment region of the electrode chip. This operation was done using tweezers; the alignment precision with a calm hand (zero caffeine content) was sufficient to place the electrode in the target zone of 200x200$\mu$m$^2$. Then the mirror chip was pushed in the +y-direction with the aid of a prober-needle and the alignment structures, as presented in Sec. 4.4.2 guided the chip smoothly to the target position. The snap-in of the clip springs in the target position could clearly be sensed and seen. Once the mirror chip was in the target position it couldn't be moved either forward or backwards without willingly destroying the chips. Sideways (parallel to the x-axis) the chip could be moved against the force of the clip spring within the alignment tolerances of about 5$\mu$m; as this could be done in the +x and -x direction equally, one can assume that the alignment precision in this case was better than the designed +/-5$\mu$m. It turned out however that the clip springs hold the mirror chip in position only under very moderate accelerations and thus the clip-spring system alone proved not to be reliable for permanent joining of the two chips—the reduced spring force results from a dimensional loss of the stopper structures during electrode fabrication, which yielded a lower compression of the clip-springs in the target position.

For permanent fixation a thin layer of glue was applied to the electrode spacers before assembly. The glue film was deposited using a stamp procedure, i.e. pushing the electrode chip upside down onto a few-microns-thin glue layer prepared on a glass slide. The increased friction due to the glue film during alignment hindered the mirror chip to be properly centered through the clip springs in the target position, such that the alignment error in that case was +/-5$\mu$m (compared to +/-2$\mu$m without using glue).

Curing was carried out in a convection oven during one hour at 100°C and yielded a strong and reliable bond between the two chips.

### 5.2.4 Assembly of Large Arrays

#### Assembly setup

In order to perform the assembly steps for the large array as described in Section 5.1.4 a dedicated assembly setup has been realized. The specifications of this assembly setup is summarized in Table 5.1. The setup has been conceived such that it can be installed on the motorized table of a Veeco Wyko NT1100 (see Sec.2.3.3), imposing a limit on the weight, the height and the lateral dimension of the setup. The assembly setup is mounted on a base plate which can be clamped with three screws to the motorized stage of the Wyko NT1100. It is composed of four functional blocks: the first block contains the three translational stages, the second block is a detachable chip holder and the third block contains the three rotational stages. The latter includes a hot-plate and vacuum chuck for the second chip. A detachable gold coated silicon wafer mounted on a pivotable post acts as heat shield that can be turned over the hot plate and protect the Wyko optics during heating operation.

**Translational block** The translational block consists of a XYZ-stage equipped with piezo-stepper motors from NewFocus[8] and an interface to the chip holder. The piezo-motors allow displacements steps of 30nm around all three axis and are controlled by RS232-type interface. The chip holder interface consists of two mounting pillars, onto which the chip holder is plugged and fixed with two wormdrive screws. This system allows easy mounting and dismounting of the chip holder and provides reasonable pre-alignment. The translational block is mounted on sliding rails, allowing coarse displacement for safe chip holder loading.

**Chip holder** The chip interface consists of a microfabricated silicon chip holder which is fixed with a spring clamp to a machined aluminum part. The spring clamp allows easy mounting and dismounting of the silicon chip holder. The silicon chip holder is made from two DRIE-etched silicon parts that are fabricated from a SOI wafer, singularized and glued together. It contains vacuum slits for clamping the mirror chip and a buried vacuum

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[8] NewFocus 9065-XYZ-PPP, http://www.newfocus.com

channel[9]. The vacuum channel is connected to the aluminum part and from there via a rubber hose to an external vacuum source. Note that in order to match the vacuum slits with the mirror chip, a dedicated chip holder has been fabricated for each mirror chip layout.

**Rotational block** The rotational block consists of a manual rotational stage with a 360° coarse travel range and a fine travel screw allowing a rotational resolution in the range of arcseconds. On top a dual-axis goniometer is mounted, equipped with differential screws allowing a tip/tilt resolution of some arcseconds. The hotplate, serving as chip chuck, mounted on the goniometer is dimensioned such that the axes of rotation are centered within the chip center. The copper hotplate is thermally and electrically isolated against the goniometer, which allows heating up to 400°C—this is the temperature required for eutectic bonding. A simple vacuum hole serves as clamp mechanism for the electrode chip, laser-cut thin metal films serve as pre-alignment forms to center and roughly align the chip on the hotplate.

A Visual C++ interface has been developed for easy controlling of the translational displacement of the mirror chip relative to the electrode chip. As feedback on the lateral position serves the camera of the Wyko NT1100 white light interferometer. Relative tilt can be adjusted making use of the interferometer, where the interference fringes give a direct feedback on the parallelity of the chips relative to the optics reference mirror. The instrument's VSI mode[10] can be used to determine the vertical gap between the two chips.

### Assembly procedure

Glueing with Epotek H20 silver-glue[11] has been chosen as joining technology for the first run of large array assembly. We chose to bond the mirror membrane only on its border and assume that the membrane is clamped in operation electrostatically against the pillars. By bonding the membrane only on the border, we minimize the risk of whatsoever glue-induced issues. The glue is deposited with the aid of a prober tip on the edges of the lateral alignment mark spacers. For maximum bond strength the glue is deposited on all the lateral spacers, which particularly for the 100x200 mirror array is a time consuming operation. It is evident that for future fabrication runs

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[9] The layout is presented in Sec. 4.4.3

[10] See Section 2.3.2

[11] http://www.epotek.com/

| | |
|---|---|
| **Aligner** | |
| X translation | Motorized, travel: 110mm coarse, 13mm fine, resolution <30nm |
| YZ translation | Motorized, fine travel 13mm, resolution <30nm |
| XY tilt | Manual, range 5/10, resolution a few arcsec |
| Z rotation | Manual, coarse range 360, fine range |
| Control | Joystick, RS232 and Ethernet interface |
| Feedback | Optical and interferometric via external optical profiler |
| **Hotplate** | |
| Chip clamping | Vacuum |
| Temperature | RT–400C |
| Electrical | Grounded |
| **Chip Holder** | |
| Chip clamping | Vacuum |
| Electrical | Isolated, HV up to 400V can be applied |
| **Overall** | |
| Platform size | $150\times195$mm$^2$ |
| Weight | 3kg |

Table 5.1: Alignment Stage Specification

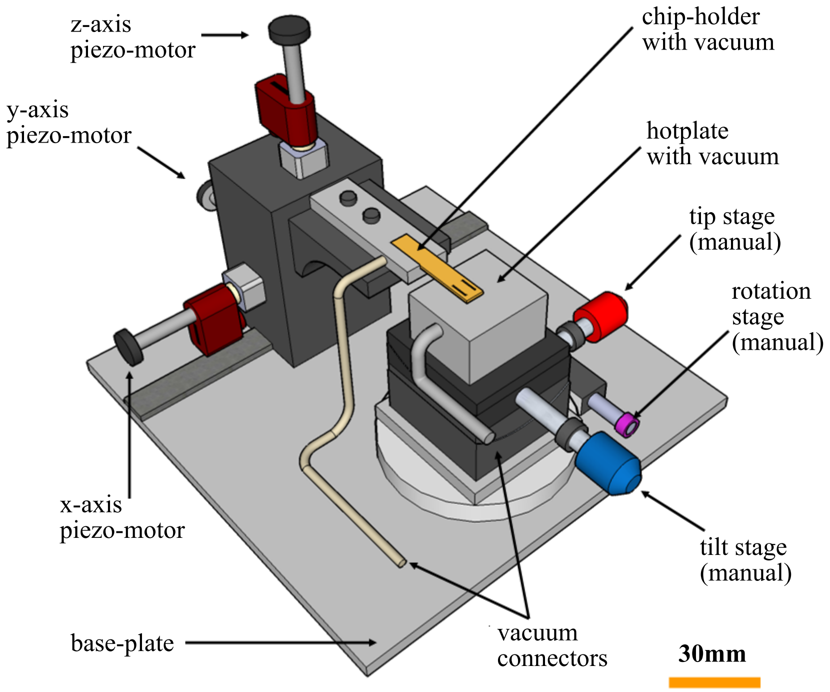

Figure 5.9: Schematic drawing of the custom assembly setup. The setup consists of a base plate, serving as an interface to the motorized stage of the Veeco Wyko NT1100, onto which the two main components, the electrode chip holder assembly and the mirror chip holder assembly, are mounted. The electrode chip holder assembly consists of a hot-plate, with an integrated vacuum feed for clamping the electrode chip, that is mounted onto a tip-tilt goniometer; the latter is mounted on a rotational stage. The mirror chip holder assembly consists of the silicon chip holder itself that is mounted to a detachable aluminum part; the latter being mounted on a motorized XYZ translational stage. The translational stage is mounted on sliding rail, allowing coarse displacement of the chip holder assembly for chip loading and unloading.

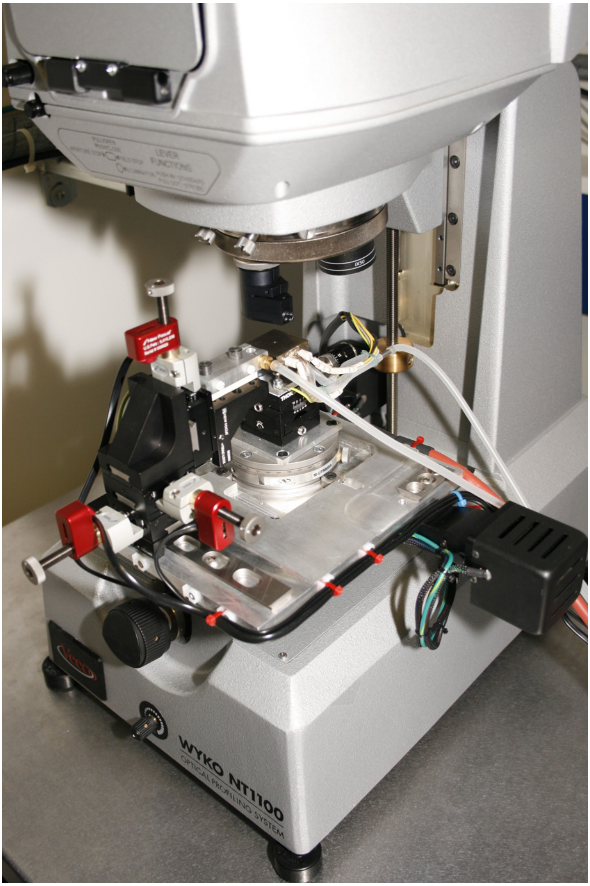

Figure 5.10: The custom assembly stage mounted on the motorized stage of the Veeco Wyko NT1100. This setup allows feedback on in-plane and out-of-plane alignment thanks to interferometric measurement.

a more operator- and throughput-friendly glue dispensing process must be developed.

The glue-processed electrode chip is placed on the hotplate chuck, centered with the aid of a stencil mask. The alignment of the chip relative to the vacuum slits on the silicon chip holder is crucial: the mirror chip must be positioned such that the backside frame covers the vacuum slits, else the vacuum may suck-in the mirror membrane[12]. The alignment tolerance here was +/-100$\mu$m perpendicular to the vacuum slits. Engaging the vacuum, the mirror chip is clamped to the silicon chip holder and the latter to the aluminum part and the assembly can safely be mounted on the translational stage.

With the aid of the optical feedback of the Wyko the mirror chip is now aligned relative to the electrode chip using the alignment marks on the mirror chip and the electrode chip (see Fig. 5.12). Parallelism of the two chips is achieved by canceling out all interference fringes individually on the two chips, i.e. making the two chips parallel to the reference mirror of the Michelson objective of the Wyko (5x obective with a 0.5x zoom lense for the largest field of view). The vertical scanning interferometry (VSI) mode of the Wyko has been used to check the resulting parallelism.

Once properly aligned the chips where brought into contact using a very slow z-translation speed—in proximity the z-stage was displaced in single step mode; one step being about 30nm, this procedure allowed a very soft landing of the mirror chip on the electrode chip. The silicon chip holder proved to be sufficiently flexible to account for the slight parallelism error during the landing operation. The moment of contact between the mirror and the electrode could be detected very precisely by the simple observation of the interference fringes on the mirror membrane and the membrane frame: once contact was established the fringes on the mirror membrane remained static, whereas the fringes on the membrane frame continued to move when still lowering the mirror chip.

After the optics of the Wyko were protected with the heat-shield the glue was cured at 100°C (hotplate temperature). In the first experiment the chip holder remained in place during the curing process: it showed that this caused a post-alignment displacement of the mirror membrane relative

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[12] At a later stage in the assembly process it could be observed that the micromirrors where sucked against the handle layer grid of the mirror chip even though the vacuum slits were well aligned with respect to the handle frame, indicating a leakage between the chip holder and the mirror handle frame. But this effect proved to be reversible, as the mirrors moved back to the idle position once the vacuum suction was cut.

to the electrode chip. This can be explained by a differential expansion of the hotplate chuck and the mirror chip holder and as the two elements are mechanically decoupled, this can yield in a relative in-plane displacement of the hotplate chuck and mirror chip holder. In a second experiment the mirror chip holder was removed before heating. Even though a slight misalignment was introduced during the chip holder detach operation, the alignment error introduced during glue-curing was much smaller in this case.

It is questionable if with a joining technology that requires high temperature and high pressure, as for instance eutectic bonding, the micron alignment-precision can be reached with this setup. Another possible approach would be to utilize electrostatic clamping of the mirror layer frame to the electrode columns by applying a high bias voltage between the two—even though this would be a very experimental approach, it would not require any external mechanical pressure to be applied (and hence no misalignment induced due to differential lateral thermal expansion).

**Detachment of the mirror handle frame: unleashing the ties** The final step consists of detaching the mirror handle frame from the assembly. At the moment of the assembly the mirror membrane is attached to the mirror handle frame by polysilicon latches. The assembly concept has foreseen to unleash these ties by burning the latches with electrical current. Experiments on not yet assembled mirror chips have showed that the polysilicon latches can glowed almost debris-free at moderate currents. However it turned out that this burning operation was not required for detaching the mirror handling frame—the latches ruptured either during the assembly process or after assembly under moderate shocks. The remarkable fact is that the latches held the mirror membrane reliably in place during handling of the mirror chip before assembly—no accidentally detached mirror membrane were observed among the mirror chips. Even though it was not the intention[13], the polysilicon latches were dimensioned such that they sustain the mass of the mirror layer only and not the mirror layer bonded to the electrode chip. To detach the mirror handle frame it was therefore sufficient to turn the assembled device upside down; this was achieved with the detached vacuum chip holder.

Fig. 5.13 shows a successfully assembled transferred 64x32 mirror layer and the detached mirror handle frame. Fig. 5.12 shows the alignment marks of an assembled and bonded chip, indicating that the alignment accuracy is around 4$\mu$m.

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[13] Blessed are the ignorant!

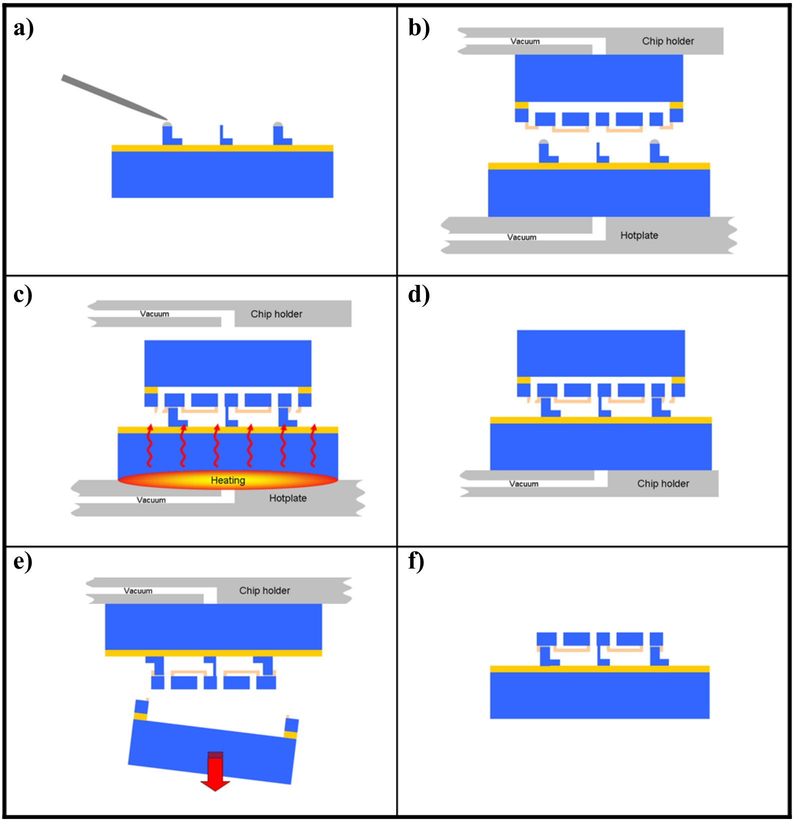

Figure 5.11: Assembly procedure for large arrays. (a) Dispense silver glue on the lateral spacer elements (b) Alignment between the two chips (c) Bring the two chips into contact, remove chip holder and cure the glue. The polysilicon latches break when the two chips are brought into contact. (d) The assembled MMA is picked up with the chip holder. (e) The mirror handle frame is removed by turning the MMA upside down. (f) The released and assembled device is ready for packaging.

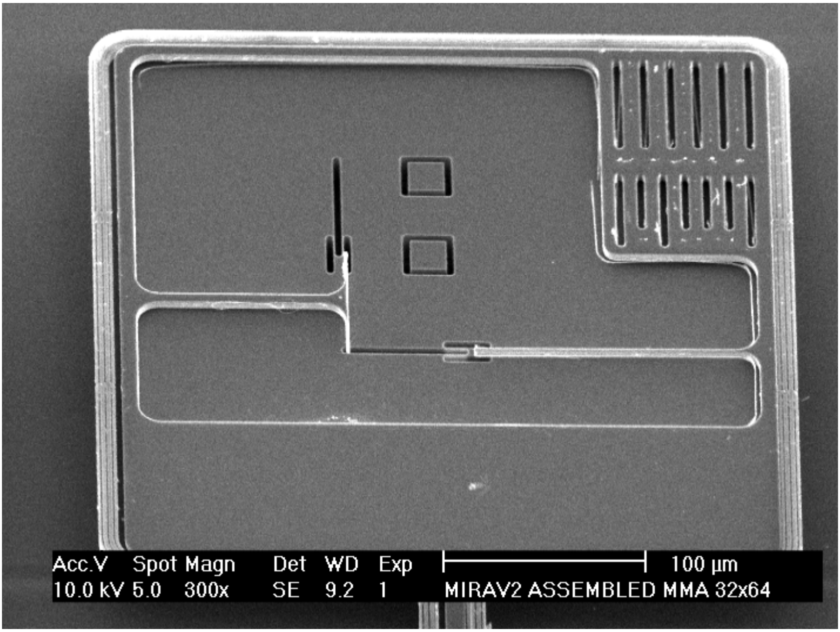

Figure 5.12: Alignment marks after assembly and glue curing. The alignment bars are 2$\mu$m wide, here indicating an alignment error of 4$\mu$m and 1$\mu$m for the x and y axis, respectively.

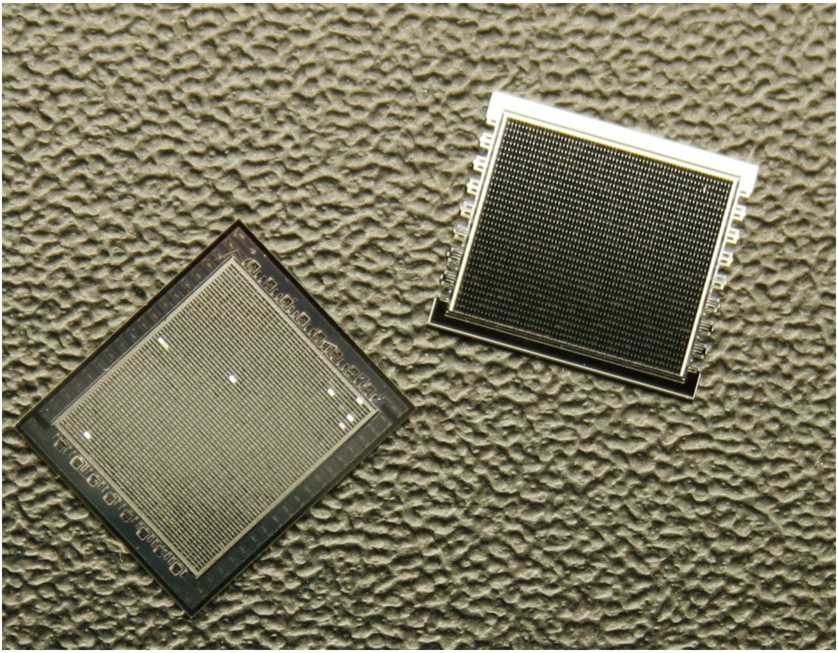

Figure 5.13: Assembled 64x32 mirror array. The mirror layer was transferred without mirror loss to the electrode chip and the mirror handle frame was detached (left).

### 5.2.5 Packaging

The small arrays have been packaged in 84-lead ceramic Pin Grid Array (PGA84) housing from Kyocera[14]. The base material of the ceramic PGAs from Kyocera is $Al_2O_2$ with a coefficient of thermal expansion (CTE) of $7.1{\cdot}10^-6$/K and thus, somewhat higher than the CTE of silicon. If this difference would turn out to be an issue for cryogenic operation, other ceramic substrates are available from Kyocera: for instance AlN with CTE of $4.7{\cdot}10^-6$/K[15]. The assembled micromirror array chip has been glued using conductive silver-glue H20 from Epotek[16] onto the PGA. After a curing step of one hour at 100°C the bond pads of the electrode were wire-bonded to the bond pads of the package. The wire-bond technology used was aluminum wire and ultrasonic bonding; this technology has the advantage that one can bond directly on silicon pads, if contact resistance is not of concern. An interface PCB has been manufactured for easy interfacing (see Fig.5.14 and 5.17). It contains a grid zip socket from 3M[17], which serves as a zero-force receptacle for the PGA84 package and enables easy and safe device swap. As the pin receptacles of the grid zip connector are spring loaded it provides a compliant interface between the PCB and the ceramic chip package. This is crucial for cryogenic testing as the FR4 base material of the PCB has a much higher CTE than Al2O3. The interconnections from the grid zip array are routed to two standard flat cable 50pin connectors which provide the interface to external control electronics (see Fig. 5.14).

The large array devices from MIRA2 do not fit into a standard PGA package. The development of a custom ceramic package solution is subject of future work within the MIRA project.

### 5.2.6 Electronics

In Fig.5.14 the custom driver electronic board interfacing the chip holder PCB with ribbon cables; the schematic of the driver electronic is given in the Appendix. The core elements are two high voltage sample and hold arrays HV257 from Supertex[18], each with 32 channels. The HV257 are fed each from a 12bit digital-to-analog converter AD5340 from Analog Devices[19].

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[14] http://global.kyocera.com

[15] http://global.kyocera.com/prdct/semicon/material/index.html

[16] http://www.epotek.com/

[17] 3M Textool Burn-In Grid ZIP Sockets, http://www.3m.com

[18] http://www.supertex.com/

[19] http://www.analog.com

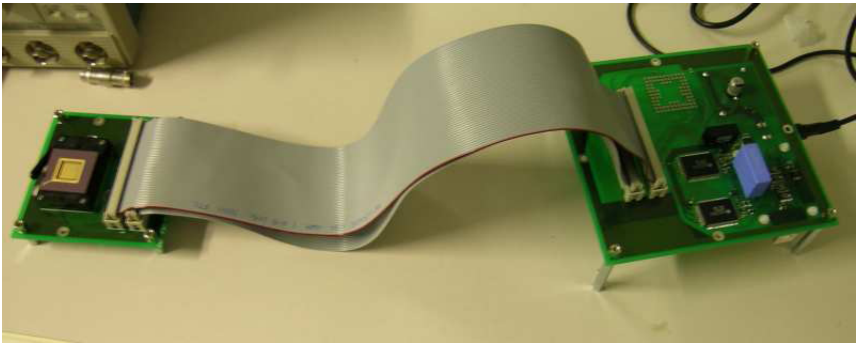

Figure 5.14: Electronic assembly: The chip interface PCB (on the left) is connected through ribbon cables to the driving electronics (on the right). The driving electronics provide 64 high voltage (up to 200V) channels that can be controlled from a PC with a custom C++ program through a USB interface.

The high voltage supply for the HV257 is provided with an on-board DC-DC converter from HiTek Power[20], providing 200V output voltage from a 12V power supply. The output channels are fed to two 50-pin connectors allowing easy interfacing to the chip holder PCB via ribbon cables; an on-board mounted grid zip socket can alternatively used for direct interfacing of the packaged MMA.

The DACs and the high voltage amplifier arrays are controlled through on-board mounted commercially available USB module QuickUSB from Bitewise Systems[21]. The QuickUSB module provides on board-side a vast number of parallel and serial I/O ports; the module can be programmed on PC side, allowing to configure the ports and send and receive data. A C++ program has been written, providing a user-interface for setting arbitrary patterns to a 5×5 mirror array.

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[20] GMA Series, http://www.hitekpower.com/

[21] http://www.quickusb.com/

## 5.3 Results

### 5.3.1 Small Arrays

Fig. 5.15 shows a scanning electron microscope (SEM) image of a fabricated 5×5 micromirror array, exhibiting suspension- and mirror-side. The polysilicon suspension structures are almost completely obscured by the mirror itself, limiting potential stray light from bent suspension beams to a minimum. Further, note that the fill-factor is, due to the fact that only a one-dimensional frame is used, very high (around 98%) along the long side of the mirrors and still relatively high in the perpendicular direction (around 85%). In Fig. 5.16 a close-up micrograph of a single mirror and corresponding electrode is given. Note that in the MIRA1 design the landing beam of the mirror (marked with a pink spot) lands, in the ON-state, on a corresponding landing pad (marked with a pink square) on the electrode, the landing pad having the same elevation as the electrode. The stopper beams are part of the uniform tilt-angle concept and provide, together with the landing beams, a geometrically well defined position in the ON-state. In Fig. 5.17 a completely assembled, packaged and wire-bonded chip is shown.

Fabrication yielded in over 95% of functional mirrors and less than 5% of the mirrors had a broken suspension or have been torn off completely. The critical step, i.e. where damage to the suspension can occur, is the release step and before all, the assembly. Since the suspension extends out of the mirror plane, it is quite sensitive to mechanical contact, for instance if the mirror chip is laid upside down on a surface other than the electrode chip. Fortunately it showed that there is no systematic weak spot within the polysilicon suspension; when breaking of the suspension occured (during above mentionned steps) it did so at random locations accross the suspension beam, as suggested in Fig. 5.18.

In a preliminary brute-force reliability test, the mirrors of (not yet assembled) 5×5 array where forced to tilt 90°, see Fig. 5.19. Vacuum suction underneath the mirror array forced the mirrors to operate in "shutter-mode" and even after several cycles no broken mirror suspension was detected. This indicates that the polysilicon spring suspension is mechanically viable and indeed designed to operate well below the fracture limit.

The effective spacing between the mirror and the electrode of the assembled devices is an important parameter for device characterization, as it is the determining factor of the tilt-angle. The spacing between mirror and electrode $d_a$ is determined by the electrode height $h_e$, the electrode spacer

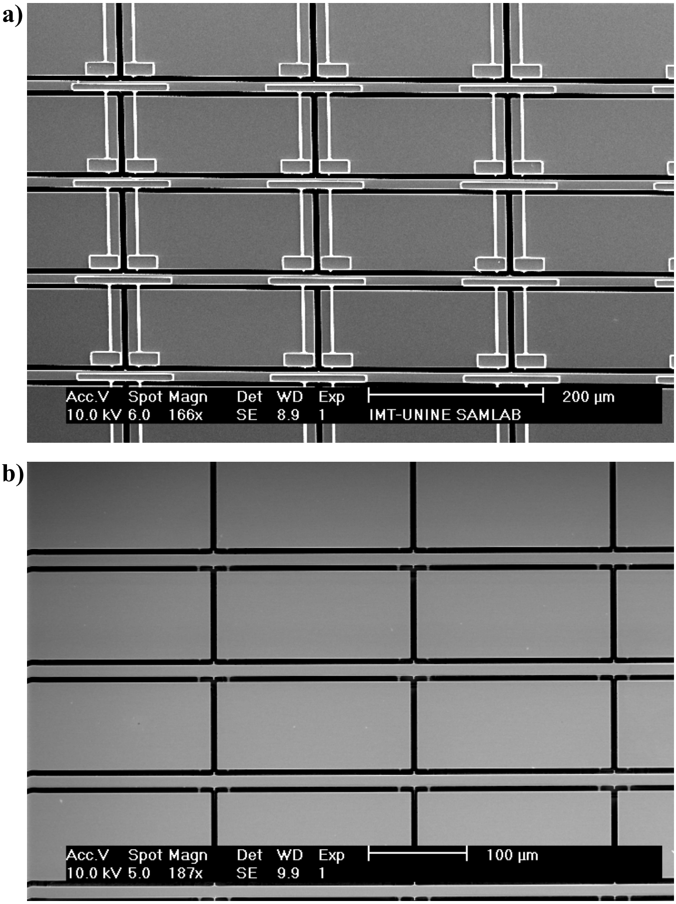

Figure 5.15: SEM micrograph of a fabricated 5×5 micro-mirror array, showing the suspension side (a) and the mirror side (b). Note that the suspension beams are hidden by the mirror itself, reducing potential stray light.

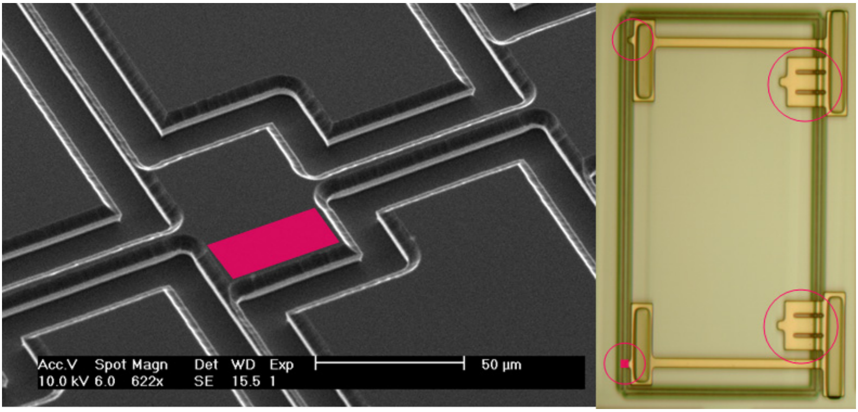

Figure 5.16: Suspension side view of a fabricated micromirror with stopper beams and the electrode counterpart. The stopper beams, located on the frame (encircled, on the right part of the micromirror), are conceived to provide a uniform tilt-angle. The landing beams (encircled, on the left part of the micromirror) land on landing pads (highlighted in the figure) located on the electrode chip, situated at the edges of the electrode. The landing and stopper beam provide a tilt-angle that by concept is independent of process variations (thickness and lateral dimensions of the polysilicon structures).

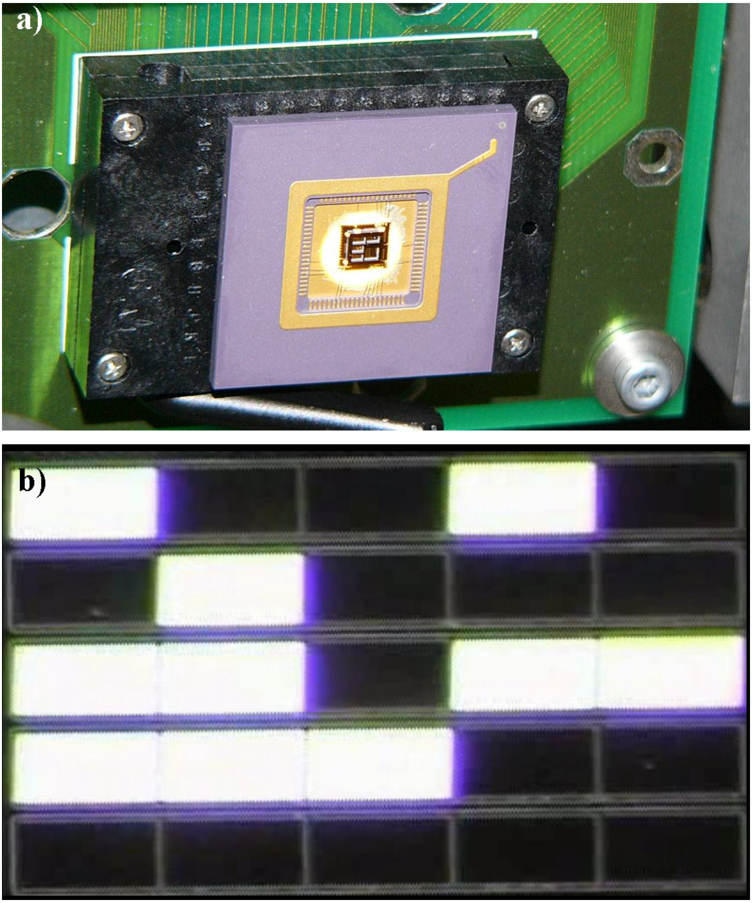

Figure 5.17: Assembled and packaged chip mounted on the grid zip connector (a), the latter providing an interface to the custom control electronic board (see also Fig. 5.14) (b) actuation test of a 5×5 micromirror using the control electronics to create random ON-OFF patterns.

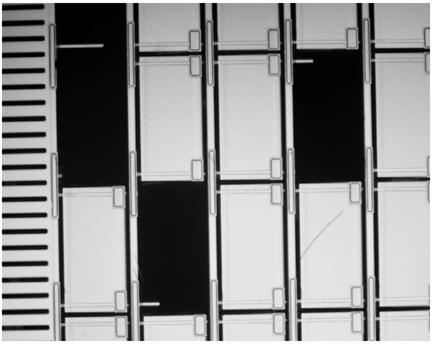

Figure 5.18: Mirrors that broke during handling and assembly. No systematic weak point could be identified.

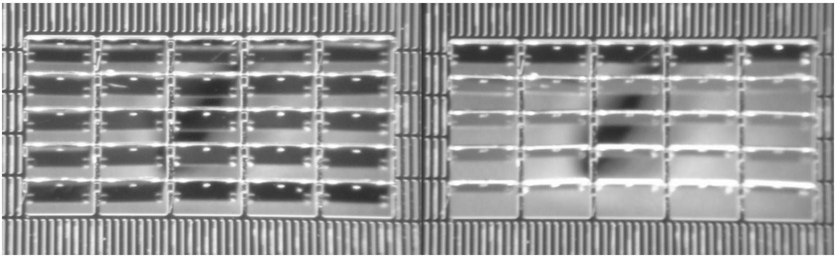

Figure 5.19: MMA operated in shutter mode: Brute force mechanical stress testing of the polysilicon spring suspension; by vacuum suction a near 90° deflection of the mirrors was obtained (which is four times more than in normal operation). No broken suspension occurred, indicating that the maximum stress in the cantilevers is well below the fracture limit in normal operation.

height $h_s$, the thickness of the glue-interface $t_g$ (between spacer and mirror chip) and the mirror thickness $t_m$ and given by $h_a = h_s + t_g - h_e - t_m$. The spacer height was 48±1$\mu$m for all measured electrodes, the electrode height was between 4$\mu$m and 15$\mu$m, the glue thickness between 1$\mu$m and 3$\mu$m and the mirror thickness was 9±1$\mu$m. The quite uniform values over different devices from different wafers is not surprising as they represent the initial thicknesses of the device layer of the mirror and electrode starting substrates (minus the thickness that was used for thermal oxidation in the case of the mirror wafer). The very large spread of the electrode thickness resulted from process variations that are inherent to the delay mask process (non-uniform etch speed across the array) and further from the attempts to avoid over-etching of the very fine connection lines on the electrode chip (see Sec. 5.2.2). Accordingly, the good electrode chips feature a electrode height rather in the upper end of the above indicated height range and consequently most of the assembled devices have electrode-mirror spacings that are below the design value of 35$\mu$m (see Sec. 4.3). Thus, most of the device exhibit tilt-angles somewhat lower than 20°, as will be shown in Sec. 6.2.1.

Note that the uniformities of the electrode chip topology within one chip was in any case much better: here the variation of the spacer height was less than 10nm (which represents the measurement error of the optical profilometer) and the variation of the electrode height was less than 100nm.

The variation of the electrode height was the main motivation for changing the device architecture in MIRA2 to that effect that the mirror lands on the electrode handle layer (and not on a landing pad at the same height-level as the electrodes).

### 5.3.2 Large Arrays

Fig. 5.20 shows a section of the suspension side of a fabricated 200×100 mirror array. Visible is a part of the mirror array (mirror size 100×200$\mu$m$^2$) and, highlighted with a frame (a), an alignment pad and a polysilicon latch; the alignment pad is utilized during assembly of the mirror chip to the electrode chip (see also Fig.5.12) and the polysilicon latch is utilized to prevent the mirror layer from falling out of the handle frame. The border between the mirror layer and the mirror handle frame is the large, curved trench. In inset b) a close-up of one micromirror is shown, exhibiting the changed geometry of the landing and stopper beams (compare with MIRA1 geometry in Fig.5.16). In inset c) a close-up of the corresponding electrode is shown. Note that the (single) landing beam (marked with pink) lands on the substrate of the electrode chip (denoted with a pink square) rather than on an elevated landing pad. This removes the dependence of the tilt-angle on the height of the electrode layer.

The position of the supporting columns on the frame after assembly is indicated yellow spots. Note that the clearance in the x-direction is about $10\mu$m on either side and, more critical, $4\mu$m in the y-direction, hence the necessity of a high-accuracy assembly procedure.

In Fig. 5.21 two fully assembled large MMAs are shown: a 64×32 array (a) and a 200×100 array (b). It can be considered as an achievement that fully released and structured $9\mu$m-thin and up to $22\times25$mm$^2$-large mirror layers could be successfully transferred onto an array of micro-pillars without mirror loss. However, it was found that the concept of uniform spacing using the glue-joining method failed at this point. It turned out that a non-uniform glue distribution on the electrode chip induced a large deformation of the mirror layer. The measured peak-to-valley deformation is about $17\mu$m, which is about half of the nominal spacing between mirror and electrode, and therefore not acceptable. The non-uniform glue distribution on the pads on the edges of the chip and the stickiness of the glue prevented correct settlement of the mirror layer on the electrode spacer columns. Ironically it was the very high compliance of the mirror layer, which by concept should have allowed a conformal attachment to the electrode chip, that finally allowed the very large deformation and consequently large spacing non-uniformity.

Note that the measured uniformity of the electrode spacer height (large spacers at the edge and the micro-columns) was excellent: within the largest array (200×100) the height was $34.8\pm0.1$ $\mu$m. For comparison the height of the electrodes was $3.8\pm0.4$ on the same array.

Potentially, a bonding solution in which an interlayer is used that is not “sticky” in the beginning and activated only when the mirror layer is correctly settled on the electrode spacer columns, should indeed yield an uniform spacing. Such a joining method could be soldering (e.g. AuSn) or eutectic bonding (e.g. AuSi).

Besides the mirror layer deformation the MIRA2 devices suffered from a large amount of polysilicon residues; this problem was believed to be resolved (or at least minimized) for the latest MIRA1 fabrication run but reappeared due to changed trench widths and device designs (imposed by the large array architecture). The issue of polysilicon residues is further discussed in the next section. The abundant appearance of polysilicon residues on the first run of MIRA2 prevented the devices from correct operation.

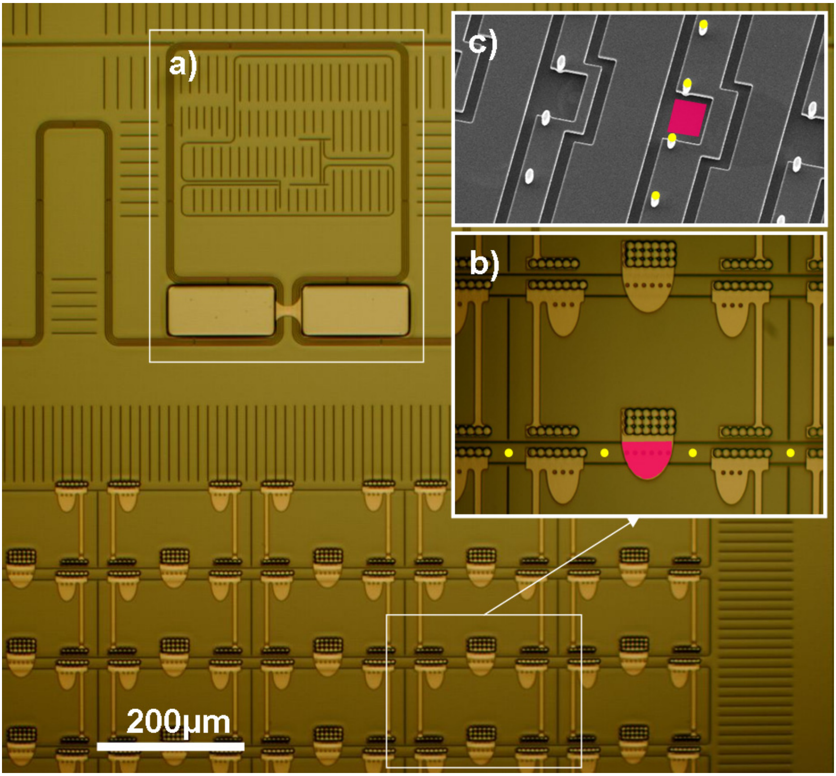

Figure 5.20: MIRA2 large array architecture fabrication results.

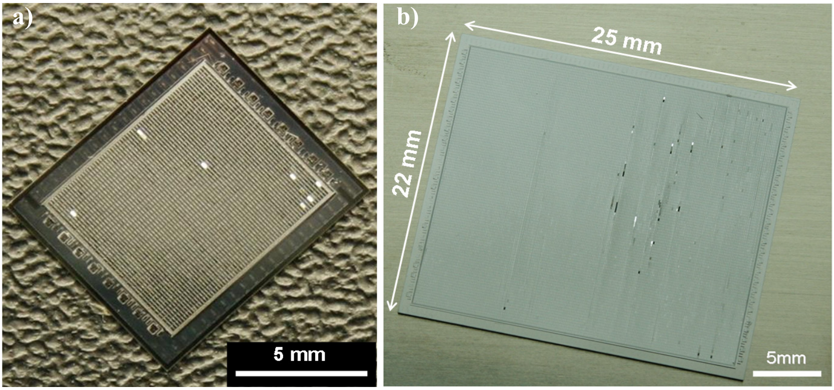

Figure 5.21: Assembled MIRA2 devices. (a) 64×32 array and (b) 200×100 array

### 5.3.3 Issues

The main issue of the present fabrication process (particularly for the MIRA2 generation) was the presence of polysilicon residues (we also refer to it as poly-hairs) in the final device. Fig. 5.22 shows two different forms of manifestations of polysilicon residues: either as loose hairs trailing around in the trenches or connected to the polysilicon suspension structures in the trench between mirror and frame.

The cause and what already had been done for its prevention was already extensively discussed in Sec. 5.2.1; therefore we focus here on its impact and give a short outlook on how to solve this problem for good.

The poly-hairs caused the following issues:

- Polyhairs on the mirror surface degrades the optical quality and adds straylight
- Polyhairs on the suspension side may cause electrical shortcuts between the mirror and the electrode
- Polyhairs between the mirrors can cause mechanical shortcuts leading to mechanical coupling of mirrors and in worst case complete blocking of mirrors.
- Polyhairs on the frame can cause problems during assembly

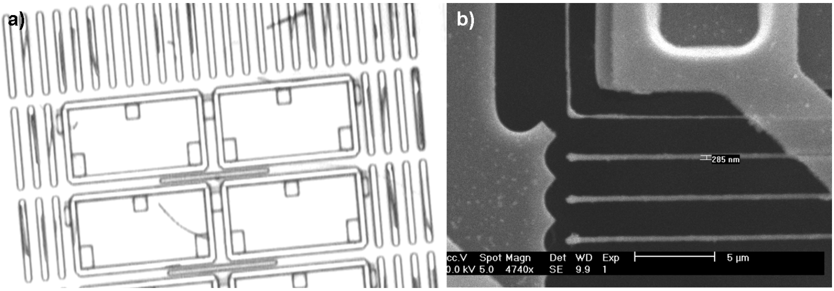

Figure 5.22: Poly-hairs revealed

The best approach to completely avoid the polysilicon residues would be to conceive a process where no trench refill is required; this could be a similar process as utilized for the fabrication of NASA's microshutter array [29], where the surface micromachined suspension structures are patterned first and then the device layer is etched from the backside. An improved filling process based on reflow, BHF release and critical point drying, which completely removed the poly-hair issue, has been shown by Canonica [8].

# Chapter 6

# Characterization

In this chapter the fabricated and packaged devices are characterized in terms of their optical and electromechanical properties at room and cryogenic temperatures. Full characterization was carried out for MIRA1 devices, i.e. 5 × 5 micromirror arrays. The actual device performance is compared, where applicable, against the design performance and the fulfillment of the requirements and potential performance of later MIRA generations is discussed. The chapter concludes with the presentation of a MOS demonstrator setup using a MIRA1 5 × 5 micromirror array for object selection.

## 6.1 Optical Characterization

### 6.1.1 Surface Quality of Individual Mirrors

The surface deformation was measured using phase-shift interferometry; the measurements were carried out with a Veeco Wyko NT1100 optical profiler and confirmed with the characterization bench at LAM (see Sec. 2.3). From the surface deformation map the peak-to-valley deformation (PTV) was extracted utilizing the following procedure: first a rim of $5\mu$m around the mirror under test (MUT) was excluded (edge exclusion)—this in order to rule out any edge effects. Then the residual tilt of the mirror was removed by a plane-fit. After filtering out measurement artifacts and outliers, e.g. from dust particles or the like, the peak-to-valley deformation is defined as

$$PTV \equiv z_{max} - z_{min} \tag{6.1}$$

Table 6.1: Surface quality measurements of individual mirrors: peak-to-valley deformation.

| | Mean PTV [nm] | Variance [nm] |
|---|---|---|
| Uncoated mirror nominal gap | 12.4 | 7.8 |
| Uncoated mirror large gap | 3.8 | 2.2 |
| Cr/Au coated single side | 35 | 4.1 |
| Cr/Au coated double side | 19.8 | 2.5 |
| Uncoated large mirrors | 16.4 | 6.8 |

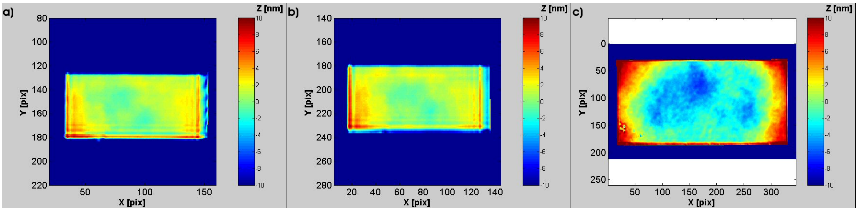

Figure 6.1: Surface quality of uncoated mirrors. The topographic images were obtained with a custom made phase shift interferometric setup at LAM. (a)-(b) showing a $100\times200\mu m^2$ sized micromirror in its OFF and ON state. Clearly, there is no added deformation due to actuation of the micromirror. (c) exhibits the surface quality of a $250\times500\mu m^2$ large micromirror.

The surface quality of uncoated MIRA1 mirrors was measured in the OFF and the ON state. The $100\mu m\times200\mu m^2$ sized mirrors showed a peak-to-valley deformation between 3nm and 13nm, depending on the mirror design and the fabrication run. The mirrors show exactly the same deformation in OFF position as well in ON position—the mirrors remain flat when operated, see Fig.6.1. Larger mirrors of $250\mu m\times500\mu m^2$, which may be used for larger plate scales, showed a PTV of 15nm, still satisfying the requirement on optical flatness. Tab. 6.1 summarizes the measured PTV data; for the uncoated mirrors two types of mirror design are distinguished: one with a large gap between the individual mirrors (and frame) and one with a small (nominal) gap. Note that the mirrors with the nominal gap show a significantly higher deformation; the cause is discussed further below.

Using a reflective layer increases the mirror deformation. A 50nm gold layer, with a 10nm chrome adhesion layer, is deposited on the micromirrors, providing reflectivity in the near and mid-infrared range. The peak-to-valley deformation increases to about 35nm when coating only the topside of the mirror. This value is in good agreement with the predicted values in Sec. 4.2.1—from Tab. 4.4, p. 68, we have a calculated peak-to-valley deformation of 33nm. Additionally coating the backside of the mirror with the identical layers decreases the peak-to-valley deformation to below 20nm (Fig. 6.3). Note that the curvature of the mirror changed from concave to convex. In theory, a perfectly balanced sandwich coating would yield the initial deformation of the uncoated mirror; however in our case the backside of the mirror is partially shadowed by the suspension beams leading to a geometric asymmetry between the front- and backside coating and thus inducing this residual deformation.

Interestingly almost all mirror, except for the large gap mirror design, show a concave deformation shape in uncoated state; recalling the list of surface deformation causes in Sec. 4.2.1, p. 62 we can rule out initial non-uniformities of the mirror substrate. As possible causes remain the deformation due to a stressed silicon-polysilicon interface and plastic deformation during fabrication (including SOI substrate fabrication). Reconsidering the simulated deformation due to a stressed polysilicon-silicon interface, also in Sec. 4.2.1, we note that even for an exorbitantly high compressive stress of the polysilicon layer of 300MPa, the resulting deformation of the mirror is much smaller (and of other shape) than what show the actual measurements. Therefore one must conclude that the deformation results from a partial plastic deformation of the single-crystalline silicon mirrors.

There is strong evidence that this plastic deformation occurs during the thermal oxidation of the mirror wafer for trench refill: Consider Fig. 6.2, showing a PSI measurement of a portion of the suspension side of two mirrors, one belonging to the high-deformation design (nominal gap width, Design A) and the other to the low deformation design (large gap width, Design B). Mirror of Design A shows a remarkable, hill-type deformation all around the mirror within 10$\mu$m of the mirror edge, whereas the mirror of Design B is perfectly flat. Observation of the mirror wafer during fabrication indicated that this hill-type deformation, even visible with a normal microscope, occurs during thermal oxidation of the mirror wafer. The oxide, growing in the trenches, literally squeezes the mirrors in between; in conjunction with the resulting high pressure, plastic deformation occurs even at the moderate temperatures [63].

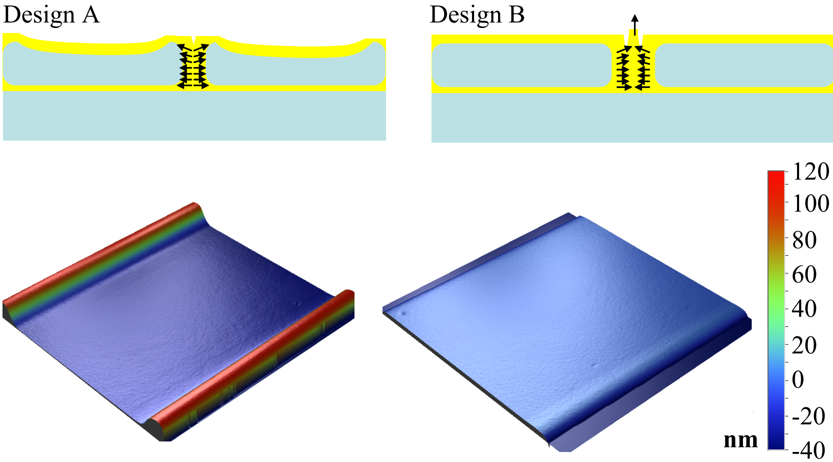

Figure 6.2: Plastic deformation of micromirrors due to thermal oxidation during trench refill. PSI micrographs of the suspension side of different mirror designs exhibit hill formation on mirror edges. The magnitude of the deformation changes drastically in function of the width of the trenches that separate the mirrors: Design A, featuring nominal trench width, shows a deformation of approximate 150nm at the edge, whereas Design B, having large trenches, shows a deformation of a few nanometers only. The explanation for the difference is schematically depicted in the upper part of the figure: whereas the trench design in B allows for some lateral expansion of the growing oxide, in Design A the large pressure exerted by the oxide growth must be fully absorbed by the mirror edges, which, in combination with high temperatures (1050°), leads to plastic deformation.

The difference between Design A and Design B is that the latter features a triple trench gap where a remaining airgap buffers the lateral expansion of the thermal oxide. This and the squeeze-effect in Design A is schematically depicted in 6.2. We conclude that with a proper design or, even better, by avoiding the thermal oxidation step where a device concept that avoids refilling the trenches, i.e. thermal oxidation of the mirror wafer, we could reduce the PTV of the uncoated mirrors to a very low value of 2-3nm.

The RMS roughness was measured on completely processed micromirrors, also using the Veeco Wyko's PSI mode and a 100x magnification; these measurements indicate that the RMS roughness is below 1nm over a field of $10\times10\mu\text{m}^2$. Using the backside of the device layer as mirror surface yields this almost flawless surface, as the device layer backside remains protected by the buried oxide layer throughout the whole fabrication process and is exposed only in the very last step.

### 6.1.2 Optical Quality of the Array

The optical quality of the overall array includes the mirror layer deformation and the position of the individual mirrors in the unactuated (or OFF) position—as is after fabrication and packaging. Even though at present there is no hard requirement on the OFF-position, information on the actual OFF-tilt-angle might be relevant for future optical system layout. The mirror layer deformation is the deviation of the mirror frame grid from a planar surface. The deformation can be either a global deformation of the electrode-chip/mirror-chip assembly, a deformation of the mirror layer relative to the electrode chip or a combination of the two. The first case yields in a non-uniform spacing between mirror and electrode and hence a non-uniform tilt-angle over the array. When a uniform spacing is assured by the device architecture, which should be the case for large arrays, the tilt-angle measured against the (local) mirror frame plane is indeed constant across the array—however if a global deformation is present, the tilt-angle relative to an external reference plane is no longer constant[1]. Therefore all types of chip deformations are performance-relevant and must be carefully examined.

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[1] In the case where the focal plane of the telescope is not planar in principle also the MMA should follow the curved shape of the focal plane. In practice, this is not easily achievable; another solution in that case would be to vary the tilt-angle over the array—this could be implemented using the stopper beam system. Such an approach is discussed in the very last chapter.

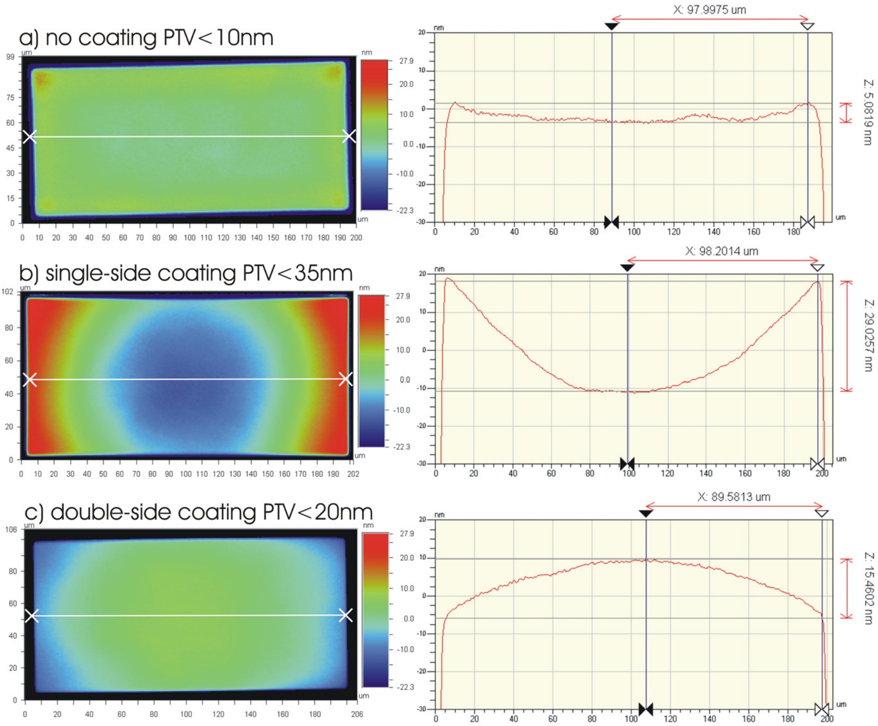

Figure 6.3: Topographic images and cross-sections obtained from a Veeco/Wyko NT1100 showing the influence of the reflective coating on the surface quality of $100 \times 200 \mu m^2$ micromirrors. All micromirrors in the OFF position. A reflective coating on the optical side of the mirror increases the peak-to-valley deformation from below 10nm (uncoated (a)) to about 35nm (b); adding the same coating on the backside of the mirror decreases the peak-to-valley deformation to below 20nm (c). Note that this backside coating also changed the sign of the curvature of the mirror. The reflective coating consists of a 10nm chrome adhesion layer and a 50nm gold reflective layer.

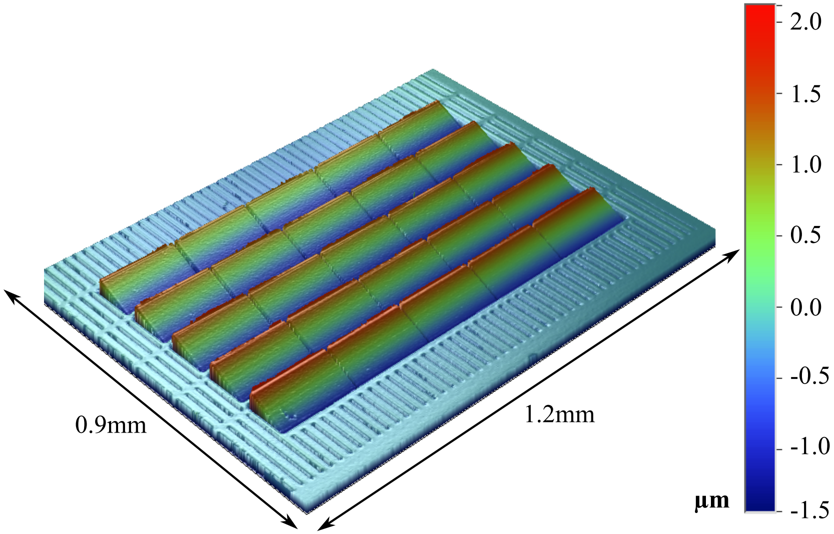

Figure 6.4: Surface quality of the array: pre-tilt of the mirrors. After fabrication and assembly the mirrors show a slight negative pre-tilt (opposed to the actuation direction). Here the tilt-magnitude is around 1° for most of the mirrors. The pre-tilt value varies between -0°.5 and -2° across mirrors from different devices.

### Mirror Pretilt

Fig. 6.4 shows a 3D-view of a VSI image of a 5×5 mirror array. Clearly, the mirrors are not coplanar with the device layer but show a slight tilt of around -1°. The tilt-direction is opposite the nominal ON position; i.e. the mirrors have a negative pre-tilt around the nominal rotation axis. The pre-tilt varies between -0°.5 and -2° across different mirrors and devices.

The cause for this pretilt in the OFF position is the intrinsic stress and its gradient along the thickness within the polysilicon suspension beams—gravitational effects can clearly be excluded, as shown in the modeling section (Sec. 4.2.2, p. 71) and confirmed by measurement: first, the center of gravity of the mirror moves out-of-plane opposite the gravitational field and, second, the pre-tilt magnitude and direction does not change when the mirror chip is put upside down[2]. Given the bending direction of the beams we conclude

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[2] The upside-down measurement was carried out on the mirror chip before it was as-

that the stress gradient within the polysilicon layer points toward the silicon (mirror) layer.

A negative pretilt is in principle favorable for the row-column actuation scheme, as it decreases the OFF-tilt-angle (that by definition is non-zero) and thus, increases the ON-OFF tilt-angle without increasing the spacing between mirror and electrode. An ideal case would be when the negative pretilt completely cancels out the effect of the hold-voltage for the mirrors in the OFF state[3]; for that a negative pretilt of around -3° would be required. The technique to make use of a vertical stress gradient in a suspension beam is known for instance from HELMBRECHT [23]—although here the stress gradient was achieved using a stack of materials with different intrinsic stresses[4].

### Mirror Layer Deformation

Fig. 6.5 (a) shows a PSI measurement of an unassembled mirror chip (suspension side up). We note two important facts: first, the chip is very flat (some tens of nanometers over a distance of a few millimeters) where the device layer is not released from the thick handle layer. Second, the device layer (the mirror layer) has a considerable bow where it is released from the handle layer—the crucial point being that although it is released it is still clamped on four sides by the solid handle layer frame. In this case the PTV of the mirror layer (not of the individual mirrors!) is about 200nm over an area of barely 0.5 × 0.5mm$^2$. PSI measurement on an assembled 5×5 array mirror layer showed a deformation of the frame of about 260nm (Fig. 6.5 (b)); the dominant deformation occurs along the direction of the frame bars.

Assuming the underlying electrode layer to be planar, the frame deformation would result in a variation of the spacing between mirror and electrode layer of the same magnitude and thus, in a tilt-angle variation of about 10arcmin. If the deformation of mirror layer corresponds to the deformation of the electrode layer, i.e. the spacing between the two layers is assumed to be constant, the resulting deviation of the tilt-angle relative to an external plane would be equal to the maximum slope variation of the mirror layer; here that would be about 3arcmin. Thus, the measured deformation of the

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sembled to the electrode chip.

[3] Recall Sec. 4.2.2, p. 77

[4] Considering the cryogenic operation environment of the MMA one could make use of a layer stack with materials having different CTEs, such that the pretilt is achieved through cooling the device to operation temperature. The drawback of such solution would be that the device must be tuned for a certain operation temperature, i.e. the performance would be temperature dependent.

mirror layer results in case in a tilt-angle uniformity error, the magnitude depends on the deformation of the underlying electrode and the spacing uniformity between the two.

The measurement of the bow of an unassembled MIRA1 electrode is depicted in Fig. 6.6. The radius of the bow is about 15m; projected on a surface of a 5×5 array the resulting spacing uniformity error is around 40nm and the slope error below half of an arcminute. The slope error will only be important over larger surfaces: the measured radius of curvature of a fabricated MIRA2 electrode of 200×100 array is in the same order of magnitude and the resulting peak-to-valley slope error is about 9arcmin. Note that for both electrodes the exposed $SiO_2$ of the SOI layer was removed before the measurement; however the BOX is still present between the handle layer and the electrodes, landing pads and connecting lines. The only practical way of reducing the electrode bow would be to utilize substrates with thicker handle layers[5].

Packaging of MIRA1 increased drastically chip deformation. The bow of the electrode after packaging was measured to be about 1m, correspondingly resulting in about 8arcmin in slope error or about 200nm spacing uniformity error over a 5×5 array. The packaging method utilized for the MIRA1 devices however, was not optimized for minimizing packaging induced deformations. The utilized ceramic chip carrier was not quantified in terms of flatness, the layer of glue that is used to join the chip to the ceramic carrier even less. Further, there is a CTE difference of $4{\cdot}10^{-}6/K$ between the carrier material and silicon that causes additional deformation during the gluing process. Note that, given the CTE difference between chip and ceramic package, the chip deformation is expected to be worse in cryogenic environment. Utilizing the MMAs in future systems, a decent mounting and packaging method needs to be established (e.g. utilizing compliant interfaces and materials with matched CTE) in order to avoid these additional deformations.

Further contribution to spacing uniformity errors and thus, tilt-angle uniformity errors originate from spacer and landing pad height variations within a chip; these were characterized in Sec. 5.3. The impact of the different spacing uniformity error contributions, electrode bow and other effects on the total tilt-angle uniformity error budget will be discussed in Sec.6.4

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[5] Reducing the burried oxide thickness would also reduce the bow; however the 2$\mu$m-thick BOX is required for providing sufficient electrical isolation between substrate and electrodes.

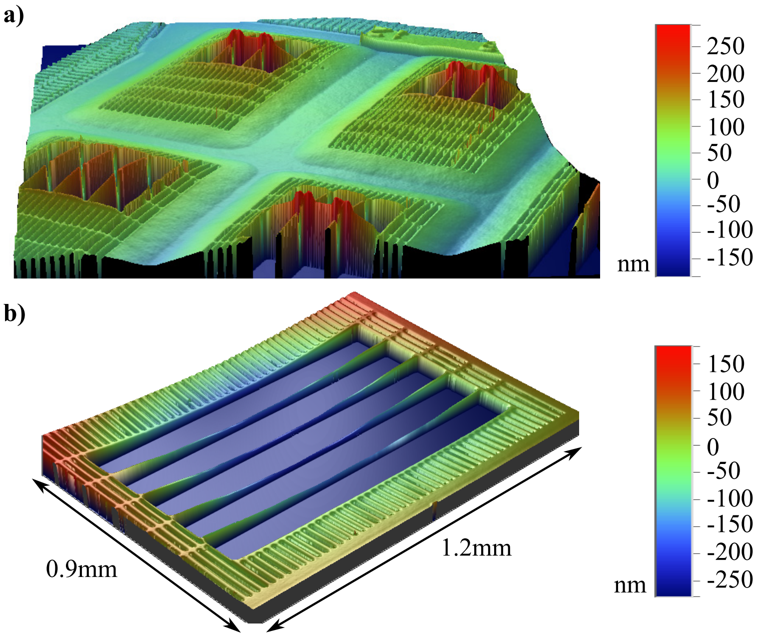

Figure 6.5: Mirror layer deformation. (a) PSI measurement of the mirror layer deformation of a unassembled MIRA1 chip. Note that the deformation is minimum for places where the device layer is still attached to the handle layer of the mirror chip. The deformation of the released portions of the device layer is induced by the four-side clamping through the handle layer. (b) Mirror layer deformation of a assembled and packaged 5×5 mirror array. The mirrors itself are filtered out, as the PSI measurement method yields erroneous position information for non-continuous surfaces. The PTV deformation over the 5×5 array is about 260nm; the main deformation occurs along the direction of the frames.

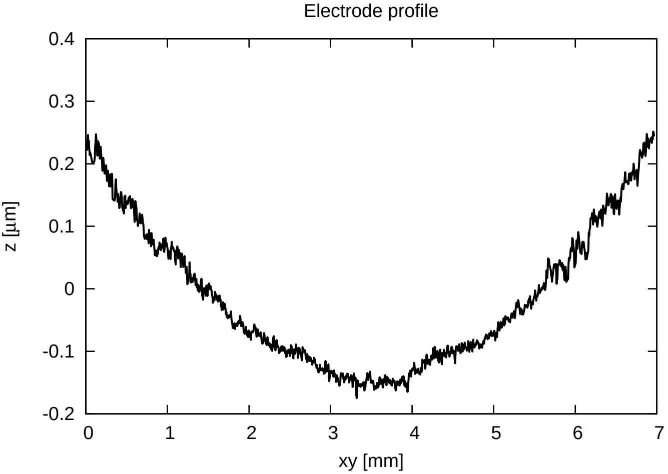

Figure 6.6: Section of a VSI measurement on the backside of an electrode chip. The curvature of the electrode chip is about 15m. In angular terms, the maximum deviation from a planar surface is about one arcminute (over a surface of 5×5mm$^2$).

## 6.2 Electromechanical Characterization

In this section the relevant characterization on the mechanical and electromechanical performance is given and discussed.

### 6.2.1 Tilt-Angle versus Voltage Characteristics

#### Method

The measurement of the tilt-angle versus voltage hysteresis is carried out using the vertical scanning interferometry mode (VSI) of a Veeco/Wyko NT1100 optical profilometer. The 50× objective was used in order to get the highest available NA, under ideal conditions allowing detecting slopes up to 24°; with a 0.5× zoom lens a field of view of $250 \times 190$ $\mu$m was obtained. The arrangement in pairs of mirrors, in some zones of the chip, with and without stopper beams (or mirrors with different stopper beam length) allowed measurements of both mirrors at once by placing the FOV center between the two[6].

First the pull-in voltage $V_a$ of the mirror under test (MUT) is determined manually, driving the mirror with a Keithley Sourcemeter. The tip/tilt stage of the Wyko is adjusted such that the optical reference plane is bisecting roughly the mirror layer plane (defined by the mirror frame) and the plane defined by the MUT in ON-state. This is necessary to equalize the resolution/contrast of the fringes on the device frame and the MUT. A VSI scan of the tilted MUT and the surrounding frame is performed and the acquired topographical data is used as template for Veeco's pattern recognition software SureVision. As reference surface for the tilt-angle calculation the frame that surrounds the mirror is utilized. Note that the frame surface is rather small and furthermore, the frame itself can be subject to local slopes, see Fig. 6.5 in the previous section.

The actual measurement sequence is controlled through a Matlab script. A voltage sequence from 2V to $1.2 \cdot V_a$ and from $1.2 \cdot V_a$ down to 2V in 2V-steps was applied to the MUT. At each voltage step a VSI scan is performed, followed by an automated pattern recognition and analysis of SureVision. The values that are extracted for each voltage step are the mean height, tilt-angle orientation and tilt-angle magnitude relative to the mirror frame reference plane. For each characterized mirror the local spacing between mirror and electrode/landing pad has been measured. This measurement

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[6] The drawback is that only half of each mirror surface is available for tilt-angle calculation which may degrade the measurement accuracy.

has been carried out using VSI through the gap between mirror and frame with a 50× objective and a 2× zoom lens.

Note that the present measurement method yields the following limitations:

1. The automated measurements of the pull-in voltage underlies a discretization error of 2V.
2. Only the local tilt-angle, i.e. the tilt-angle relative to the local slope of the frame that surrounds the mirror is measured. This must be taken in account when comparing the absolute value of different measured mirrors.

A more adapted method for assessing the tilt-angle uniformity over an array, rather than characterizing individual mirror behavior, would be utilizing an interferometric setup, such as the bench installed at LAM[7] and monitor the tilt-angle in ON-state only. Orienting the MMA such that the tilted mirrors are coplanar with an external reference plane (and consequently only low local slopes are present), one could use a low magnification (low NA) and large field of view in order to compare the tilt-angle of all mirrors within an array against the common external reference plane. Such an experience should be carried out on future generations of large array devices.

### Results

As already depicted in Sec. 5.3.1 the actual spacing between mirror and electrode landing pad varied strongly from device to device (and also within a device). As a consequence the resulting tilt-angle varies strongly from device to device. Nonetheless, using the measurements of the effective spacing, the tilt-angle characteristics can be correlated with the modeled performance.

Fig. 6.7 shows an exemplary measurement of a complete tilt-angle versus voltage hysteresis. The measurement was carried out on two mirrors with medium length cantilevers: one with and one without stopper beams. In the first, analog phase, the tilt-angle increases steadily, nicely exhibiting the quadratic dependence on the voltage. At 83V the mirrors make a sudden jump from 6° to 20°; this is the pull-in or snap-in of the mirror and we refer to it as the transition to the ON position; the corresponding voltage is $V_a^+$ and the resulting tilt-angle (after pull-in) is denoted as $\alpha_a^+$ for the mirror

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[7] See Sec. 2.3.3, p. 36

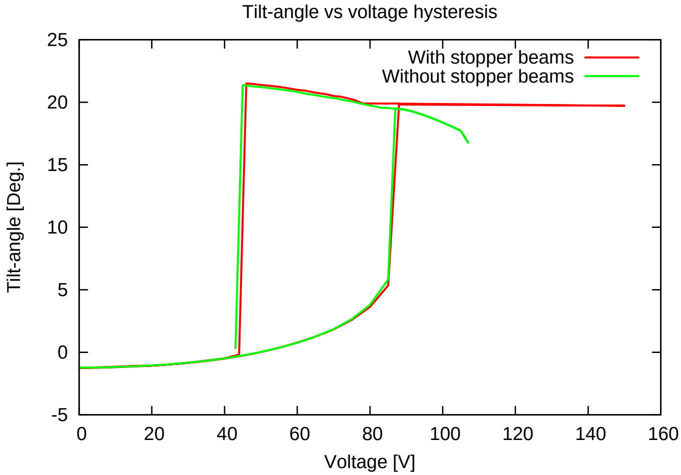

Figure 6.7: Exemplary tilt-angle versus voltage hysteresis

without stopper beams and $\alpha_{\mathrm{ON}}$ for mirror with stopper beams, following the conventions from Sec. 4.2.2 (depicted in Fig. 4.9).

From this point on the mirror without stopper beams and the mirror with stopper beam follow different paths. The tilt-angle of the mirror without stopper beams continues to follow a quadratic dependence on the voltage—but at this time the sign is inversed, i.e. for increasing voltage the tilt-angle decreases quadratically. On the other hand the mirror with stopper beams stays in position after pull-in—even when almost doubling the actuation voltage. This is clearly the effect of the stopper beams: the mirror is hold in position by the stopper beams (recall Figure 3.2 in Sec. 3.2, p. 47).

When lowering the voltage departing from $V_a^+$ the mirror continues to stay in position until a certain point, from which on it starts to follow the quadratic behavior of the mirror without stopper beam—this is the point where the mirror detaches from the stopper beam located on the frame, corresponding to the voltage $V_s$[8]. When further lowering the voltage to

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[8] For reason of clarity the curve of the mirror without stopper beam is not plotted left of the pull-in point; however the shape of the curves clearly suggest that the point where the mirror detaches from the stopper beam is located where the graph of the stopper-beam-less mirror crosses the flat zone of the graph of the mirror with stopper beams. This is exactly what the modeling would suggest, assuming that the two mirrors are identical (except for the presence of stopper beams), and discussed further below.

$V_r^+$ the tilt-angle of the mirrors reaches the maximum tilt-angle ($\alpha_r^+$) after which the mirror makes a sudden drop back to the OFF position—this is the snap-back of the mirror.

The measured performance parameters for this and other mirror designs are summarized in Tab. 6.2, where always a mirror with and without stopper beam was measured for a given design/device. The performance parameters where introduced in Sec. 4.2.2 and 4.2.2; recall for instance Fig. 4.9, p. 84.

The most critical geometrical parameters for the device performance are the cantilever length $l_c$, the stopper beam length $l_s$ and the spacing between the electrode and the mirror $d_a$. In Fig. 6.8 the tilt-angle versus voltage hysteresis of two different mirror designs is given: one with a long (a) and one with a short (b) cantilever suspension, having a cantilever offset $o_c$ of $10\mu$m and $30\mu$m, respectively. Even though the basic behavior of the mirrors (with stopper beams) is the same, the two mirror designs vary strikingly in the magnitude of their tuning range $\alpha_r^+ - \alpha_a^+$ in the ON-state[9]; compare with the modeled dependence of this range on $o_s$ in Fig. 4.13 (a).

Consider the stopper beam like behavior of the mirror without stopper beam for the long cantilever suspension: as predicted in the modeling section, the cantilever suspension itself acts as stopper beam for this design, setting a lower limit for the tilt-angle at pull-in $\alpha_a^+$. Measurements on experimental mirror designs, where the cantilever beams are not behind the mirror but located laterally (and consequently do not interfere with the mirror movement), showed that mirrors with $o_c = 10\mu$m indeed collapse into the second pull-in, yielding a zero tilt-angle.

The impact of the stopper beam length on the device performance is depicted in Fig. 6.9; here the tilt-angle versus voltage hysteresis of mirrors with nominal and long stopper beams are plotted. We note that the mirror with the long stopper beam has, as expected, a higher (stable) tilt-angle $\alpha_{\mathrm{ON}}$ in the ON-state. It is remarkable that the variation of the tilt-angle in the flat zone $\Delta\alpha_{\mathrm{ON}}$ is about the same for the two stopper beam lengths—one would expect the variation to be larger for the longer stopper beam, due to its reduced stiffness.

All characterized mirrors show the exact same behavior with respect to the stopper beam functionality, i.e.:

- The stopper beams stop the mirror at a tilt-angle that is higher than the pull-in tilt-angle of the same mirror design without stopper beams.

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[9] Referring to the mirror without stopper beams; see Fig. 4.9, p. 84 for the definition of the tuning range.

Table 6.2: Measured device performance. Compare with modeled design performance parameters in Tab. 4.13, p. 93. For the mirrors with ID 7,8,9 (baseline design) simulated values based on an adapted FEM, taking into account actual geometrical values, are given.

| | Geom. Param. | | | Performance Param. | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| ID[1] | $l_c$[2] [$\mu$m] | $l_s$[2] [$\mu$m] | $d_a$[3] [$\mu$m] | $V_a$ [V] | $Vr$ [°] | $Vs$ [V] | $\alpha_a^+$ [°] | $\alpha_r^+$ [V] | $\alpha_{\text{ON}}$ [°] | $\Delta\alpha_{\text{ON}}$[4] [’] |
| 1 | 85 | 23 | 34 | 83 | 42 | 78 | - | 23 | 19.9 | 1.5 |
| 2 | 85 | - | 34 | 83 | 42 | - | 19.5 | 23 | - | - |
| 3 | 75 | 24 | 29 | 62 | 32 | 52 | - | 19.3 | 17.8 | 3 |
| 4 | 75 | - | 29 | 60 | 30 | - | 17.4 | 19.1 | - | - |
| 5 | 95 | 21 | 31 | 64 | 28 | 36 | - | 20.5 | 17.9 | 1.2 |
| 6 | 95 | - | 31 | 60 | 26 | - | 15.8 | 20.4 | - | - |
| 7 | 95 | 27 | 25.5 | 58 | 34 | 56 | - | 17.1 | 14.2 | 1.8 |
| *S*[5] | *95* | *27* | *25.5* | *64* | *40* | | | *16.6* | *14.1* | |
| 8 | 95 | 29 | 25.5 | 58 | 28 | 54 | - | 16.8 | 14.6 | 1.8 |
| *S*[5] | *95* | *29* | *25.5* | *64* | *40* | | | *16.6* | *14.5* | |
| 9 | 95 | - | 25.5 | 58 | 30 | - | 13.5 | 17.1 | - | - |
| *S*[5] | *95* | - | *25.5* | *62* | *40* | | *13.3* | *16.6* | | |

[1] Mirror identifier

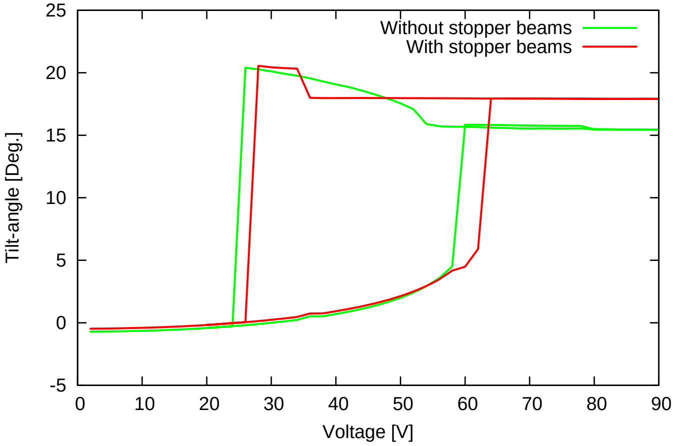
[2] Design value

[3] Measured value

[4] Tilt-angle variation within stopper angle regime, i.e. for $V_s < V < V_a$

[5] Adapted FEM simulation for this particular chip; the adapted values were $d_a = 25.5\mu$m, $d_p = 3\mu$m and $e = -5\mu$m

a) Long cantilever suspension



b) Short cantilever suspension

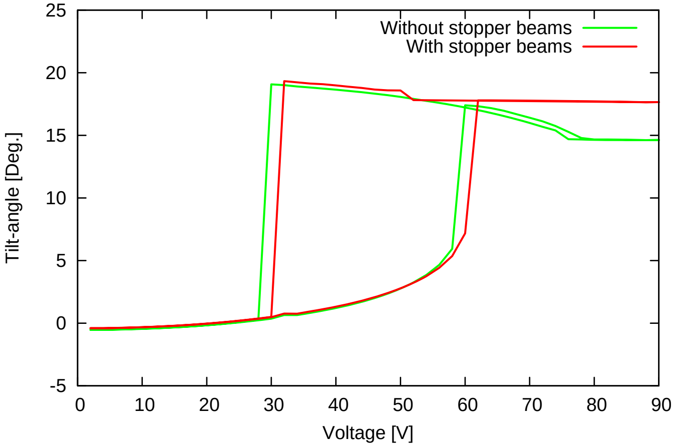


Figure 6.8: Tilt-angle versus voltage for two different cantilever length. a) Long cantilever suspension $l_c = 95\mu\text{m}$, $o_c = 10\mu\text{m}$. b) Short cantilever suspension $l_c = 75\mu\text{m}$, $o_c = 30\mu\text{m}$

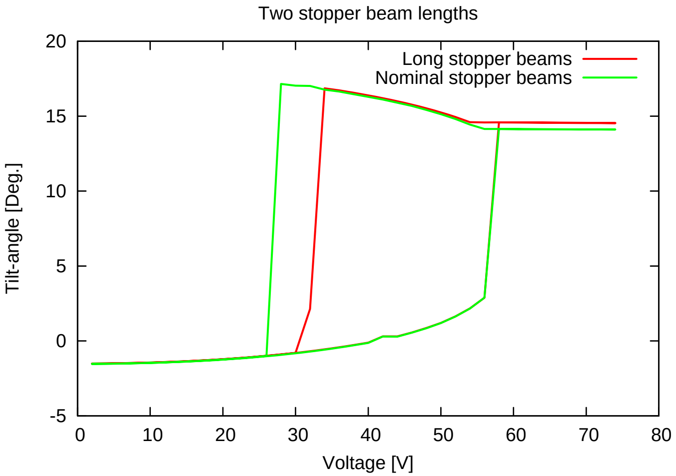


Figure 6.9: Tilt-angle versus voltage for two different stopper beam lengths.

- There is a voltage range left and right of the pull-in point (in the ON-state) where the tilt-angle is stabilized (flat zone in the tilt-angle versus voltage hysteresis)

Further, we have seen, that

- the tuning range, i.e the range between minimum and maximum tilt-angle wherein the stopper beam can be set, depends on the cantilever attachment offset $o_s$ and
- the length of the stopper beam defines the (stable) ON-tilt-angle

which is in accordance with the modeling and confirms the device concept.

There are two effects that were not foreseen by modeling. The first, possibly related to the stopper-beam behavior of the mirror without stopper beams, is a hysteresis of the mirror within the ON state, visible in Fig. 6.8 (in graph (b) right of the pull-in point). This behavior was noticed for several mirrors without stopper beams. In order to exclude an apparent hysteresis induced by a drift of the measurement system, the measurement of such a suspicious zone was repeated multiple times—and the “hysteresis within the hysteresis” was found to be perfectly repeatable. The hysteresis within the hysteresis is plotted in Fig. 6.10: the plot starts with the pull-in state. The

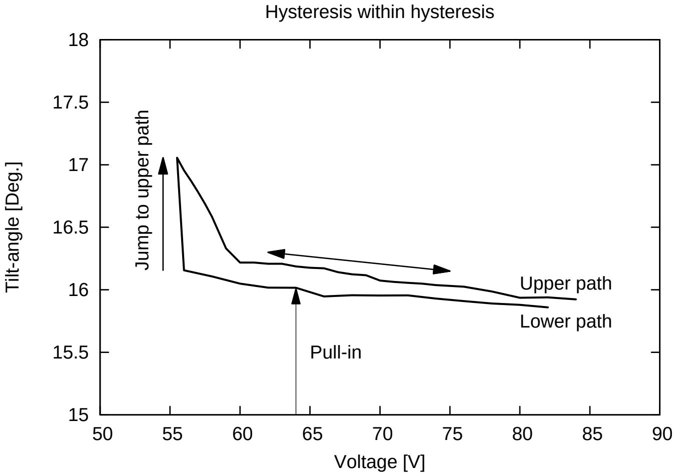


Figure 6.10: Hysteresis behavior of mirror without stopper beams.

tilt-angle versus voltage curve follows a "lower" path, until the voltage is decreased below a certain value: here the tilt-angle increases in a sudden step of about one degree. From then on the tilt-angle follows an "upper" path. This schema is reproducible, i.e. after the OFF-ON transition the tilt-angle follows the lower path and jumps to the upper path at about ten volts below the pull-in voltage; once it is on the upper path it stays there until the mirror is switched OFF and ON again. Note that the jump from the lower to the upper part is sharp, i.e. even when decreasing the voltage steps to below 0.1V no intermediate tilt-angle values could be produced (similar to the OFF-ON transition). It is conceivable that this hysteresis represents the switching of the bent cantilever from one into another bending state (snap-through), for instance from an S-shape into a C-shape. However, as in the nominal design the stopper beam prevents the mirror from reaching this state, this effect is, though interesting, not performance relevant.

The second effect is the appearance of an erratic transition between the (left) end of the flat zone and the quadratic zone, i.e. the state $V_s^m$ where the mirror detaches from the stopper beam. Whereas, for instance, for the mirrors in Figs. 6.7 and 6.8 (b) this transition is continuous, the mirror in Fig. 6.8 makes a "jump" when it detaches from the stopper beam. However, in contrast to the sudden transition in the case of the mirror without

Table 6.3: Difference between design and actual dimensional parameters and their impact on the actual performance.

| Parameter | Design | Actual | Impact | | | | |
|---|---|---|---|---|---|---|---|
| | | | $V_a$ | $\alpha_a^+$ | $\alpha_{\mathrm{ON}}$[1] | $\alpha_r^+$ | $f_r$ |
| $d_a$ | $35\mu$m | 25 to $34\mu$m | $\downarrow$ | $\downarrow$ | $\rightarrow$ | $\downarrow$ | $\rightarrow$ |
| $d_p$ | $2\mu$m | $3\mu$m | $\rightarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\rightarrow$ |
| $o_e$ | $-10\mu$m | -10 to -$5\mu$m | $\rightarrow$ | $\downarrow$ | $\rightarrow$ | $\rightarrow$ | $\rightarrow$ |
| $t_p$ | $0.6\mu$m | $< 0.6\mu$m[2] | $\downarrow$ | $\rightarrow$ | $\rightarrow$ | $\rightarrow$ | $\downarrow$ |
| $E$ | 169GPa | <169GPa[2] | $\downarrow$ | $\rightarrow$ | $\rightarrow$ | $\rightarrow$ | $\downarrow$ |

[1] The relative position of $\alpha_{\mathrm{ON}}$ within the tuning range $\{\alpha_a^+, \alpha_r^+\}$ is considered

[2] No direct measurement of the polysilicon thickness nor its Young modulus was carried out. However resonance frequency measurement and actuation voltage $V_a$ matched to actual height, showed that either of the two must be lower than the design value.

stopper beams, this transition is not reproducible. When increasing the voltage again, the tilt-angle follows the inverse quadratic behavior of the unobstructed mirror until it settles again in the flat zone (where the stopper beams stabilize the mirror). Therefore we might conclude that $V_s$ in these cases somewhat underestimates the "real" $V_s$; we introduce therefore the value $V_s^*$ that represents the voltage where the characteristics of the mirror without stopper beam would intersect the characteristics of the mirror with stopper beam (depicted in Fig. 6.9)[10]. This value can be considered as the safe lower limit for the hold voltage $V_h$ of the row-column actuation scheme. One can assume that this somewhat smaller $V_s^m$ is attributable to partial sticking of the mirror to the stopper beams[11]. However, this has no impact on the device performance, as long as $V_h$ is set within the range $\{V_s^*, V_a\}$.

### Discussion

Comparing the measured performance parameters of the micromirrors with the modeling in Sec. 4.3, Tab. 4.5, p. 97, Fig. 4.12, p. 92 and 4.13, p. 93 we

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[10] Note that by device concept we have $V_s = V_s^*$.

[11] Note that this case is different (different geometry and different actuator behavior at this state) from the OFF-ON transition, where it was showed that no tendency to systematic sticking is present (see Sec. 6.2.4).

note that *qualitatively* the mirrors behave as expected and required—but not *quantitatively*. The reason for the quantitative mismatch is mostly related to a difference between design and actual values of geometrical parameters:

- Reduced spacing between mirror and electrode $d_a$ yielding lower tilt-angles and actuation voltages; the actual spacing $d_a$ was between $25\mu$m and $34\mu$m versus a design value of $35\mu$m; the reason for the reduced spacing is that the electrode and landing pad height was larger than projected (see 5.3.1).

- Increased vertical spacing between mirror and cantilever $d_p$, yielding lower values of $\alpha_{\mathrm{ON}}$ relative to the ON-tilt-angle tuning range $\{\alpha_a^+, \alpha_r^+\}$; the actual spacing $d_p$ was around $3\mu$m versus a design value of $2\mu$m; the increased spacing results from an additional oxide layer that was deposited on the $2\mu$-thick thermal oxide for improved gap filling (see 5.2.1).

- Shifted barycenter of the electrode representing the electrode offset $o_e$ and yielding a lower $\alpha_a+$ (resulting in an increased ON-tilt-angle range); the actual equivalent $e_o$ was between $-5\mu$m and $-10\mu$m versus a design value of $-10\mu$m; this mismatch was caused mainly by alignment errors between mirror and electrode chip.

- Either lower thickness or lower Young modulus of the polysilicon layer causing lower actuation voltages; see Sec. 6.2.3.

Above considerations are depicted in Tab. 6.3. The explicit comparison between modeled and measured performance is presented for the baseline design (mirrors with ID 7 through 9). A FEM simulation has been carried out with adapted geometrical parameters; the following (adapted) values where used: $d_a = 25.5\ \mu$m, $d_p = 3\mu$m and $o_e = -7\mu$m. The resulting performance values are presented in Tab. 6.2, denoted with the ID *S*. We note that, using the adapted geometrical parameters, the measured and simulated values are in good agreement. The parameter $o_e$ has in principle no impact, as it mainly influences $\alpha_a^+$ which in the case for $o_c = 10\mu$m is limited by distance between the mirror and polysilicon layer $d_p$ (the minimum tilt-angle is limited by the point where the mirror touches the cantilever suspension).

It is noteworthy that without any knowledge of the actual length of the landing $l_l$ and stopper beam $l_s$ the measured ON-tilt-angles for the two different stopper beam lengths are in almost perfect agreement with the modeling; this confirms that $\alpha_{ON}$ depends only on $l_s - l_l$ and not on the absolute values (within certain limits) and thus, makes the ON-tilt-angle immune against whatsoever process variations of the polysilicon structural layer (assuming that the variation within the surface of one mirror is zero).

Beside setting the ON-tilt-angle, the main purpose of the stopper is to provide feed-forward uniformity of the tilt-angle over large arrays, given a uniform spacing $d_a$ between mirror and electrode layer. Though the latter precondition was not yet fulfilled with the characterized devices, we can still provide an estimation of the ability of the stopper beams to suppress process variation within the structural polysilicon layer. In the modeling section we calculated, assuming worst-case process variations, an edge-to-edge actuation voltage variation across a $200 \times 100$ mirror array of 10V; we can extract from the measured device performance the tilt-angle variation in the ON-state over this voltage range—these values are given (for a range of 12V, providing some margin) in Tab. 6.2, in the column denoted with $\Delta\alpha_{\mathrm{ON}}$. Typical values are around two arcminutes, the largest variation within a range of 12V that was measured is 3arcmin—by modeling and indirect measurement we can therefore conclude that the tilt-angle uniformity (assuming uniform $d_a$) for large arrays will be around 3arcmin.

In summary we conclude that

1. we have a tuning range for the ON tilt-angle; for certain designs this tuning range can be up to 5°;
2. within this range the ON tilt-angle can be set by properly choosing the length of the stopper (and landing) beams;
3. the stopper beam stabilizes the ON tilt-angle over a certain voltage range within a few arcminutes and has the potential to stabilize the tilt-angle against process variations even across large arrays;
4. this behavior was correctly predicted by modeling;
5. a better dimensional control during fabrication of the devices, in particular of $d_a$ is required to validate above points for large arrays;
6. there are certain side-effects that are not fully studied but are not performance relevant.

### 6.2.2 Crosstalk

There are two different crosstalk situations

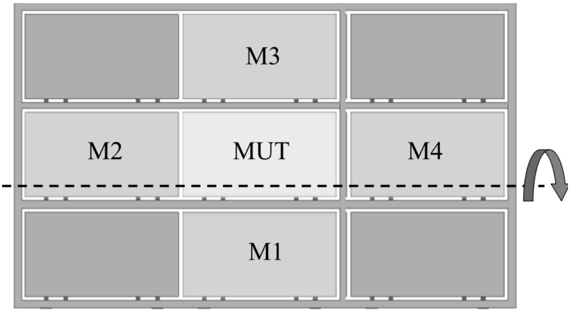

Figure 6.11: Crosstalk measurement geometry

1. The influence of the actuation state of surrounding mirrors on the mirror under test (MUT) in the OFF position
2. The influence of the actuation state of surrounding mirrors on the MUT in the ON position

We define the crosstalk as follows: tilt-angle change due to OFF-ON passage of a neighboring mirror expressed in arcminutes. The crosstalk may depend on the mirror configuration; each mirror (except the ones at the array edge) has four neighbors and the different neighbors are expected to exert a different influence on the MUT (Figure 6.11). We consider the influence of neighbors 1,2 and 3 according to Figure 6.11; neighbor 4 is symmetric to neighbor 2 and therefore has the same influence. The crosstalk measurement was done according to the following procedure for each of the three neighbors (here for neighbor 1):

1. Measurement of MUT with $V_i = 0$ for all $i \in \{\text{MUT}, 1, 2, 3\}$
2. Measurement of MUT with $V_1 = V_a$, $V_i = 0$ for all $\in \{\text{MUT}, 2, 3\}$
3. Measurement of MUT with $V_{\text{MUT}} = V_a$, $V_i = 0$ for all $i \in \{1, 2, 3\}$
4. Measurement of MUT with $V_j = V_a$ for all $j \in \{\text{MUT}, 1\}$, $V_i = 0$ for all $i \in \{2, 3\}$

The experience has been done for mirror with stopper beam and a mirror without stopper beam as MUT. The resulting values have to be considered carefully as the measurement error is in the same order of magnitude as the detected cross-talk. The only noticeable effect on the MUT has the mirror in position 1 when the MUT is in the ON position. From a geometrical point of view this was expected as here the mirror is in the closest position to a neighboring electrode. The induced change of tilt-angle was measured to be 0.5 arcmin.

There was no significant difference between the mirror with and without stopper beam. That is somewhat more astonishing, as the mirror with stopper beams was expected to be less susceptible to crosstalk.

### 6.2.3 Step Response

The measurement of the step response of a micromirror provides directly the minimum time that is required for switching the mirror from the OFF to the ON state. This value is important for the total reconfiguration time of the array. Further, from the ringing behavior that occurs for fast transitions, we can extract the resonance frequency of the mirror (which might be relevant for future mechanical stability considerations).

The dynamic mode of a Veeco/Wyko N1100 (DMEMS) (see Sec. 2.3) was utilized to record the step response of a mirror with medium length cantilever suspension ($o_c = 20\mu$m). A periodic rectangular signal with a duty cycle of 50% and a frequency of 100Hz was applied. Two cases were considered: in the first case the amplitude was chosen such that the mirror was cycled outside the pull-in (45V) and in the second experiment the amplitude was set to the pull-in voltage of the mirror (60V). In the first case the mirror movement was recorded in $1^\circ$ phase steps over one period, in the second case a step of $0^\circ.5$ was chosen to comply with the expected steep transition in pull-in regime.

Fig. 6.12 (a) shows the mirror movement inside the analog regime. Plotted is the tilt-angle magnitude evaluated around the nominal tilt-axis. The rising edge of the voltage step occurs at $0\mu$s and the falling edge at $5000\mu$s. The Fourier transform exhibits the first resonance at around 2kHz. Also a second and a third peak at around 3kHz and 4kHz, respectively, are discernible. The simulated first resonance frequency for this design was 2500KHz, indicating a reduction of stiffness of about 27%. The measured pull-in voltage was 78V, versus a modeled voltage (using the actual spacing) of 98V, which in first approximation agrees well with the measured reduced stiffness value. As the cantilever width of fabricated devices is close to the design value of $3\mu$m, we attribute the reduced stiffness to either a lower thickness $t_p$ and/or lower Young's modulus $E$ of the polysilicon layer. In either case, the absolute value of cantilever stiffness is not performance relevant, as long as the resulting actuation voltage is below the specified 100V.

In Fig. 6.12 (b) the step response for a mirror with and one without stopper beams for the pull-in case is plotted; as comparison the corresponding portion of the step response outside pull-in regime is given. Again the rising edge of the voltage step occurs at 0$\mu$s. Even though one can expect this behavior, the difference between the step response for the analog and the pull-in regime is striking. Whereas the mirror in analog mode oscillates for 5000$\mu$s (1/e decay at about 2000$\mu$s), the mirror in pull-in mode is stabilized (within one arcminute!) already after 800$\mu$s in the ON position. We note that the behavior in terms of ringing and switching-speed of the mirror with and the one without stopper beams is identical. The resulting switching speed of 800$\mu$s is well within the requirements and, even more important, can be achieved with a simple voltage step. No complex voltage pulse is required to avoid ringing during ON-switching[12].

### 6.2.4 Reliability

Even though reliability considerations are a main focus in more advanced development phases, some potential issues shall be addressed already at this stage—conceptual no-go's must be excluded in a very early phase. In the potential applications of the present development there are at least the following three subjects of concern: shock-resistivity (for space-based instruments), sticking of mirrors after long exposure times and life-time. The shock-resistivity is strongly dependent on the larger mechanical and dynamical context and cannot be addressed in simple experiments; this is clearly a subject for future characterization. Sticking is a known issue in the MEMS-world. Even though conceptually the risk of sticking is reduced to a maximum extend by minimizing the contact surface, the application in a MOS demands very long ON times of the mirrors; this can be up to an hour and beyond and potentially increases the risks of sticking. A preliminary experiment is presented hereafter that has the goal to establish a relation between ON-time and risk of sticking. Further, a preliminary investigation on effects related to repeated cycling is presented.

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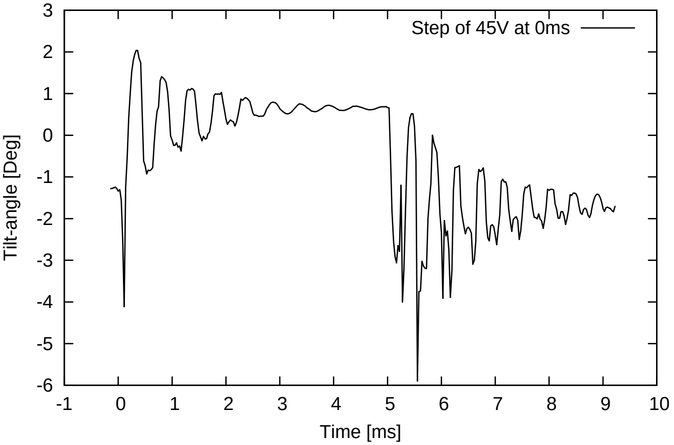
[12] However, ringing is still present when switching from ON to OFF; this must be considered when reconfiguring individual lines within the array utilizing the row-column actuation scheme.

a) Step response analog range



b) Step response pull-in

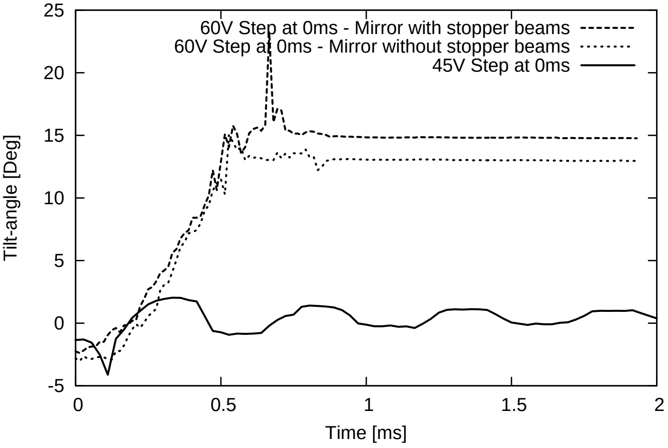


Figure 6.12: Step response. (a) Analog range, voltage step of 45V applied at t=0$\mu$s and reset at t=5000$\mu$s b) Pull-in, voltage step of 60V applied at t=0$\mu$s

Table 6.4: Sticking behavior of the micromirrors in function of ON-time; three different situations were examined: first the mirror is held in the ON-position close to the release voltage, second the hold voltage was set to the pull-in voltage and third, the mirror was held in ON-position at a voltage 50% higher than the pull-in voltage.

| | Mirror 1[a] | | | Mirror 2[b] | | |
|---|---|---|---|---|---|---|
| ON-time | $V_a$ | $V_r$ 1[c] | $V_r$ 2[d] | $V_a$ | $V_r$ 1[c] | $V_r$ 2[d] |
| 0 | 59 | 31 | 31 | 59 | 32 | 32 |
| 1 | 59 | 31 | 31 | 59 | 32 | 32 |
| 2 | 59 | 31 | 31 | 59 | 32 | 32 |
| 3 | 59 | 31 | 31 | 59 | 32 | 32 |
| 5 | 59 | 31 | 31 | 59 | 32 | 32 |
| 10 | 59 | 31 | 31 | 59 | 32 | 32 |
| 30 | 59 | 31 | 30 | 59 | 32 | 32 |
| 90 | 59 | 30 | 30 | 59 | 32 | 31 |

[a] With stopper beams

[b] Without stopper beams

[c] Hold voltage equals pull-in voltage

[d] Hold voltage equals 1.5× pull-in voltage

### Sticking

Some cases of sticking of mirrors was observed throughout functional testing of MIRA1 devices. Certain suspension designs seemed to be more concerned than others but within a class of mirror design the sticking that has been observed appeared to be completely at random. Some mirrors on some chips seemed to be more susceptible to sticking than others. The sticking mechanisms are well researched; a summary is given in Sec. 2.1.3. Clearly the more compliant the spring design is, the higher the tendency to get stuck; we can define the following simple condition for sticking to occur:

$$F_s > F_r \tag{6.2}$$

The restoring force $F_r$ is solely dependent on the geometrical spring dimensions and the bend state in ON position, i.e.

$$F_r = f(k_r, \alpha) \propto k_r \cdot \alpha \tag{6.3}$$

The sticking force $F_S$ is somewhat more complicated to express as there are many contributors and dependencies; we assume now that we have a given surface state, atmosphere and contact surface. For the intended application of the MMAs the ON-time may be significant; we must therefore investigate if there is a relationship between ON-time $t_c$ and increased risk of sticking; further it may be relevant for the driving scheme (hold voltage), if there is an influence from the force $F_\perp$ with which the landing beams push on the landing pads during the ON-state: We pose therefore

$$F_s = f(F_\perp, t_c) \propto F_\perp, t_c \tag{6.4}$$

and examine this hypothesis in the following experiment.

As measure for the sticking force we characterize the voltage $V_{OFF}$ at which the mirror snaps back to the OFF position, i.e. releases itself from the ON position. In the case we have no sticking force, this voltage is given with

$$F_r = F_e \qquad \text{with} \qquad F_e \propto V_{OFF}^2$$

If we add the sticking force we have as condition for the OFF-ON transition

$$F_r = F_e(V_s) + F_s$$

and therefore

$$F_s = F_r - F_e(V_s) \Rightarrow F_s \propto -V_s^2$$

We examine the following three mirror positions within the ON state:

1. Near the snap-back voltage
2. At pull-in voltage
3. 20% above pull-in voltage

The contact force increases from position 1 through 3. In the proposed row-column actuation scheme the hold-voltage would be situated between position 1 and 2. The contact duration, i.e. ON-time was varied from one minute to 90 minutes, which is a typical range for integration times in a telescope. For each position/contact-duration data point the following procedure was carried out:

1. Determination of pull-in and snap-back voltage
2. Moving the mirror to the corresponding position
3. Wait xx minutes
4. Lower the voltage in steps of one volt until the mirror snaps back for determining the voltage $V_r$
5. If the mirror does not snap back at 0V try to release mirror with a voltage pulse of $2V_a$

The results for two mirrors, one with and one without stopper beams, are shown in Tab. 6.4. There is no apparent systematic relation for the mirrors to stick under either long exposure (ON) times or high hold forces, and thus, we conclude that above assumption in Eq. 6.4 does not hold true, i.e.

$$F_s \neq f(F_\perp, t_c) \tag{6.5}$$

The sticking that was observed for some mirrors is therefore to be considered to be related to another factor, such as localized contamination (condensed humidity or solvents from the gluing process). Note that stuck mirrors could be released by applying a voltage pulse that was two times higher than the actuation voltage.

### Life Time

The life-time requirement of one million cycles is rather low for a MEMS mirror. Moreover, as the device is intended to be operated in vacuum, cyclic fatigue failure of the polysilicon beams is not of concern—see Sec. 2.1.3. A potential issue due to repeated cycling could be wear and related particle generation of the landing and stopper beams that at each switching cycle hit the electrode substrate and mirror, respectively.

In order to study such effects a lifetime experience for several mirrors with stopper beams was carried out. First, the complete hysteresis was measured; then $10^6$ OFF-ON cycles were performed, using a rectangular voltage signal and the complete hysteresis was measured again. The same procedure was carried out for a neighboring mirror, except at this time the amplitude of the actuation voltage signal was adapted such that the mirror did not switch to the ON state. As control for both experiments the hysteresis of another neighboring mirror that was not cycled was recorded in order to exclude drift effects of the measurement system.

The hysteresis of a mirror before and after 1M cycles is plotted in Fig. 6.13. There are several effects visible:

1. The characteristics before pull-in were not altered
2. The pull-in voltage remained the same
3. The ON-tilt-angle slightly increased
4. Increased sticking tendency

The first and second point indicates that no drifting of the measurement system occurred (also confirmed by the control measurement), that the mechanical properties of the cantilever suspension and the electrical properties of the actuator were not altered during cycling. The third and fourth effect however, indicate that something *did* happen during cycling. The ON-tilt-angle (after pull-in) is primarily defined through the geometrical parameters of the landing and stopper beams and secondarily through the applied voltage in ON-state. The change of the ON-tilt-angle between before and after cycling is about 9arcmin.

From the characterization made in Sec. 6.2.1 we know that the tilt-angle variation in ON-state (flat zone) due to a difference in applied voltage is maximum three arcminutes for a $\Delta V$ of more than 10V; to explain the 9arcmin difference, the effective electrical potential that sees the mirror in the ON-state should be several tens of volts different after and before cycling; such a large difference must have been seen in the characteristics before pull-in. As this was not the case, we rule out electrical effects as cause for the changed tilt-angle in ON-state.

Thus, we must attribute this change to an altered geometry of the landing beam (and landing pad) and/or stopper beam. For all tested mirrors the tilt-angle magnitude in ON-state *increased*; recalling the mirror architecture, an increase of the tilt-angle in ON-state (for a given air-gap height $h_a$) can only be achieved by either shortening the landing beam or elongating the stopper beam. The measured 9arcmin tilt-angle difference before and after cycling corresponds to a shortening of the landing beam (or elongating the stopper beam) of about 600nm. Even though it is not unheard of that localized oxide growth mechanism in stressed structures exist, it is far more probable that the landing beams shortens by that amount that the stopper beam elongates. Given the very fragile, only a few microns wide, geometry of the landing beam one can easily imagine that parts of it break off due to repeated OFF-ON cycles. If this is the cause, one can easily imagine more

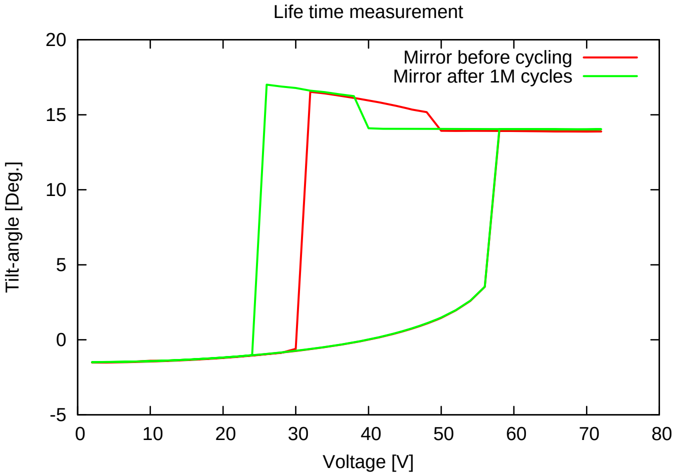


Figure 6.13: Life-time measurement. The hysteresis of a mirror with stopper beams was measured before and after 1M OFF-ON cycles

adapted design of landing beams—this has already been implemented in the MIRA2 design[13]. Another cause, not forcedly related to the stopper beam geometry, might be wear due to static friction or temporary stiction [51]. Such a cause could be alleviated by applying a wear-resistant coating to the landing beam and onto the landing pad, for instance using atomic layer deposited (ALD) $Al_2O_3$ [37].

A changed landing/stopper beam geometry in conjunction with particle generation might also be the cause for the forth effect, the increased susceptibility to sticking. However, for a conclusive statement on the cause of the life-time effects a thorough analysis (e.g. SEM) of the concerned structures before and after cycling must be carried out—this should be subject of future work. For now we state that with the MIRA1 design we see a change of the ON-tilt-angle over life-time (only accounting for the number of cycles and for no other, for instance environmental, effects) in the order of ten arcminutes.

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[13] See for instance Fig. 5.20, p. 5.20.

## 6.3 Cryogenic Characterization

### 6.3.1 Preliminary Characterization at 120K

In order to study potential effects on the mechanics of the device a preliminary cryogenic characterization has been carried out in an environmental SEM (ESEM) from Phillips. The cryogenic chamber installed in the SEM, normally used for examination of biological samples, allows cooling down to approximative 120K. As the temperature sensor in this setup is not directly attached to the sample, the sample temperature is estimated to be about 10K higher. Several unpackaged chips, some with gold coating on front and on backside of the mirror and a fully packaged chip were examined. The parts that are most susceptible to cause problems in cryogenic environment are:

- Gold coating on the silicon mirrors
- Aluminum wire-bonds on the silicon bond pads
- Silver-glue interface electrode chip/mirror chip and electrode chip - ceramic package
- Polysilicon-silicon interface

All these parts/interfaces could be observed at room temperature, during cooling and under cryogenic conditions. No noticeable effect has taken place: no delamination of layers, wrinkling or detachment. Mechanically, the only visible effect was an increased parasitic tilting of a mirror where incidentally gold has been deposited on the suspension beams (see Fig. 6.14). The polysilicon-gold beams thus acts as bimetal beams. The bimetal effect is also clearly visible in the case of the gold-coated mirrors, as the main cryogenic characterization showed (see next section). One effect that occurred during cryogenic testing was of electrical nature. In Fig. 6.14 a mirror array at room temperature and at about 130K is shown. The white zones that appear on the mirrors at cryogenic temperatures indicate increased charging—however, it will be shown in the next section that the actuator properties of the micromirrors are not affected by the cold temperatures.

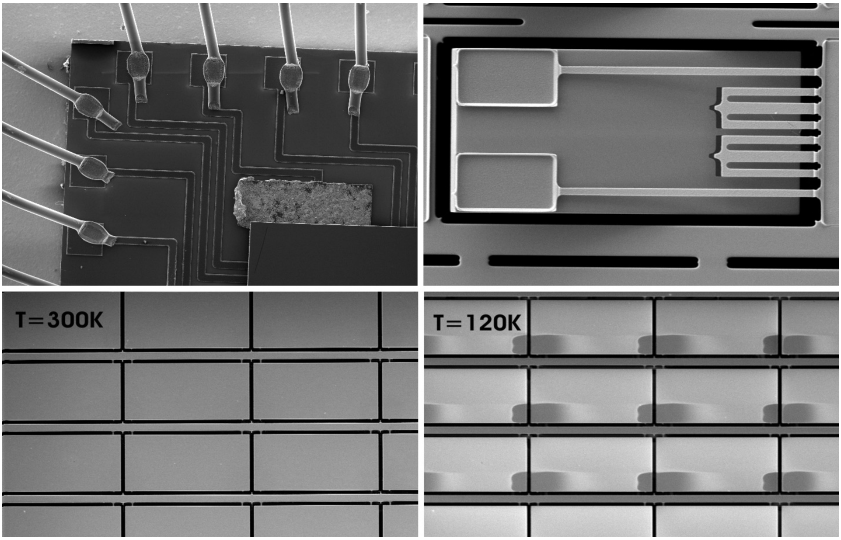

Figure 6.14: Critical parts observed in cryo SEM and charging effect.

## 6.3.2 Characterization at 90K

### Setup and Method

Cryogenic characterization was carried out in a custom built cryogenic chamber installed on the interferometric setup at LAM (see Section 2.3.3). The cryo-chamber is equipped with a turbo-pump and can be evacuated down to $10^{-6}$ mbar. The cryogenic generator allows to cool down the sample down to 60K. The chamber is equipped with an internal screen insulating radiatively the sample from the chamber[14]. Control of the environment is obtained by means of temperature sensors and local heaters.

The chamber has a glass window that allows observing and measuring the sample chip during cryogenic testing. The micro-mirror device is illuminated and imagined by a CCD camera on the outside; the micro-mirror device is rotated such that the light of the tilted mirrors (ON state) is sent to the CCD camera. The presence of a glass window at the entrance of the chamber is an issue for getting fringes with a high contrast. Two elements have to be

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[14] The sample still "sees" 300K through the observation window and thus, steady cooling of the sample is required to maintain the desired cryogenic temperature.

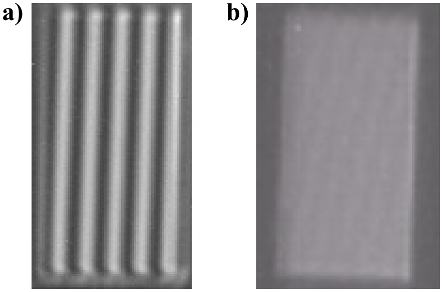

Figure 6.15: Degradation of the fringe contrast due to a dispersive media in one of the optical path of the interferometric setup. The image shows interference fringes on a micro-mirror; (a) without and (b) with a dispersive media in the object branch of the Michelson interferometer.

corrected:

1. The path difference between the interferometer arms (sample arm and reference mirror arm)
2. The dispersion of the glass medium

The first point can be overcome by moving the reference mirror in order to balance the path difference induced by the index difference between the window material and air. The dispersion of the glass medium is a more serious effect to handle. In principle there are only two ways of completely avoid the contrast reduction due to the dispersion effect: either place a perfectly identical piece of glass, ideally cut from the same glass substrate as the object glass, in the reference beam or work with a light source having an infinitesimal narrow bandwidth. As no identical glass plate was available for the present setup, the only way to improve contrast is to use a very narrow filter for the light source. The narrowest filter available within the setup was 10nm, which yielded a degraded but still acceptable fringe contrast. Fig. 6.15 shows the effect on the fringe contrast due to the insertion of a dispersive media into the object light path and finite source bandwidth. The reduced fringe contrast decreases the signal to noise ratio, as will be seen in Fig. 6.16 (e), but does not decrease validity of the mirror deformation measurement.

The PGA84 housing containing the sample chip is mounted via a spring loaded grid zip connector on a specially conceived printed circuit board (PCB). Large copper surfaces on the PCB facilitate cooling down the system; renouncing the solder-stop layer eases outgassing of the PCB FR4 base material during evacuation of the chamber. The PCB itself is mounted via a fix-point-plane-plane attachment system to a solid aluminum block, the latter being interconnected to the cryo-generator. Thick copper wires between the PCB and the aluminum block further enhance thermal transport between the sample chip and the cryostat. Teflon-isolated electrical wires allow to interconnect up to 27 electrical connections through a Deutsch connector to the outside environment. On the outside environment the wires are connected to the custom drive electronics. Temperature sensors are connected to the aluminum block and to the grid zip connector adjacent to the sample chip. The chamber has a glass window that allows observing and measuring the sample chip during cryogenic testing. The micromirror device is illuminated and imagined by a CCD camera on the outside; the micromirror device is rotated such that the light of the tilted mirrors (ON state) is sent to the CCD camera.

### Results

The cryogenic chamber was cooled down until thermal equilibrium was reached. This yielded a temperature of 64K measured at the aluminum block and 86K measured adjacent to the sample chip. From experience the actual temperature on the chip was estimated to be about 5K higher than on the adjacent temperature sensor. The pressure in the chamber was at $10^{-6}$mbar. In order to avoid vibrations originating from the cryogenic pump, cooling was halted during the interferometric measurements, taking seven minutes in total. The temperature raise during this period was less than 1K.

The chip could successfully be actuated before, during and after cryogenic testing. Single mirrors were actuated, as well lines as of micromirrors, implementing the long slit mode. Fig. 6.16 (b-c) shows the transition from OFF to the ON state of a line of micromirrors in cryogenic environment. This proves that the micromirror device remains functional below 100K. The actuation voltage for the mirror to snap from the OFF to the ON position was identical before, during and after cryogenic testing, indicating that there is no mechanical degradation of the different material interfaces, confirming the preliminary observations in the cryogenic SEM. The pull-in occurring at the same voltage in warm and cold environment is a strong indication that the electrical properties of the actuator were not been altered in cryogenic environment, at least as far as relevant for static operation.

Figure 6.16 (d) shows the surface quality measured of one gold-coated

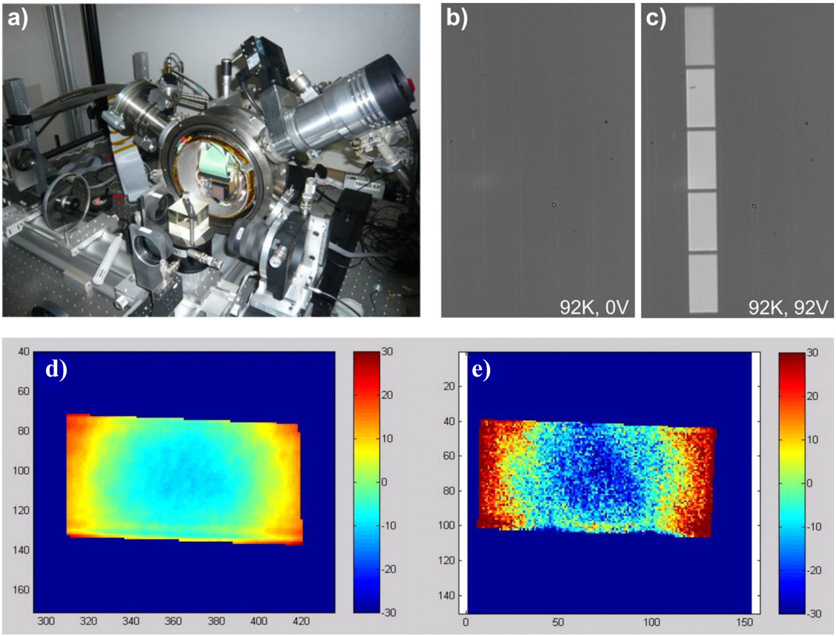

Figure 6.16: Cryogenic setup (a), functional characterization (b-c) and interferometric measurement (d-e) of mirror quality at cryogenic temperatures. (a) Cryogenic chamber installed on an interferometric setup. On the picture the chamber cover is removed, showing the packaged micromirror array mounted on a dedicated printed circuit board in the chamber. (b-c) Functional testing of the micromirror array. One line of micromirrors, initially in the off-state (b) is switched into the ON state (c). (d) Surface quality measurement at room temperature, exhibiting a PTV of 36nm and (e) the same mirror at 92K, the PTV being increased to about 50nm. Note that the decreased signal to noise ratio in (e) originates from the reduced fringe contrast due to the window in front of the cryogenic chamber.

micromirror in the cryogenic setup, at room temperature and before closing the chamber. The peak-to-valley deformation here was 36nm, which corresponds to the measurements made before outside the cryogenic chamber (see Sec. 6.1.1). Fig. 6.16 (e) shows the measurement made after closing the chamber and cooling down below 100K. The deformation shape of the mirror remains identical compared to room temperature. As expected, due the CTE mismatch between the silicon substrate and the gold-coating, the peak-to-valley deformation increases to 50nm. The lower signal-to-noise ratio in this measurement has been induced by the presence of the window at the entrance of the cryogenic chamber (see above).

The measured value of the peak-to-valley deformation at 100K is in good agreement with the estimated value in Sec. 4.2.1, where a value of 52nm was found. This deformation of 50nm is within the requirement of $\lambda/20$ at $\lambda = 1\mu$m. For lower temperatures however, according Sec. 4.2.1, a thicker substrate or a titanium (instead of chromium) adhesion layer for the gold coating has to be used.

## 6.4 Discussion

In this section the results of the characterization are discussed with respect to the main requirements that were deduced in Sec. 3.1.2. The resulting performance for the characterized small arrays and the projected performance for future generations of large arrays is summarized and compared against the specified values in Tab. 6.6.

### 6.4.1 Tilt-Angle Uniformity

The tilt-angle uniformity, or, more precise, the open loop tilt-angle uniformity is a crucial performance parameter for the use of the MMA as reflective slit mask in a multiobject spectrometer. It determines the required oversizing of the pupil for a given f-number; or, the other way round, the maximum allowable oversizing determines the requirement on the tilt-angle uniformity. Due to mass considerations (for space applications) and reduced contrast, the pupil oversizing should be kept to a minimum.

Note that in the discussion below the terms “tilt-angle uniformity” and “tilt-angle uniformity error” are interchangeable. Further, the tilt-angle uniformity error is indicated as peak-to-valley value, for instance, a tilt-angle uniformity of 10arcmin over the array means that the maximum deviation between any two mirrors within the array is 10arcmin.

We distinguish three main contributions to the tilt-angle uniformity error over the array:

1. Actuator related variations
2. Variations of the spacing between electrode and mirror
3. Global array deformation

Actuator related tilt-angle variations include the performance of the stopper beam locking system, crosstalk and life-time effects. The uniformity with respect to the air-gap height reflects tilt-angle variations that origin from variations of the spacing between mirror layer and electrode layer. Finally the global array deformation includes the tilt-angle variation that is due to variations of the local slope of the MMA device, i.e. deviation of the micromirror array from a plane. Hereafter we summarize the measured data of the individual contributions and estimate the bottom-up tilt-angle uniformity budget for future 200×100 MIRA generations; further, the ultimate performance limit for the individual contributions is discussed. The bottom-up tilt-angle uniformity budgets are summarized in Tab. 6.5.

The performance of the stopper beam locking system in terms of providing uniform tilt-angle was discussed in Sec. 6.2.1. We summarize that, excluding defects as broken stopper beams or cantilevers, a tilt-angle uniformity of three arcminutes seems to be a realistic value for 200×100 large arrays.

The inter-mirror crosstalk was measured to be around 0.5 arcmin for MIRA1 devices and is assumed that this value cannot considerably be reduced in future designs, before all given its very low magnitude. More important is the last actuator related contribution: with nine arcminutes, the drift over lifetime is certainly the most significant share of the uniformity budget. One could think of adapted driving signals, which reduces the impact/shock when switching the mirror from OFF to ON, more adapted stopper beam geometry or the application of wear-resistant coatings. However, as the causes for the tilt-angle change over life-time are not yet completely understood, it is difficult to make a forecast on the impact of these measures.

The contributions of the air-gap variation, i.e. tilt-angle uniformity error due to a non-uniformity of the spacing between mirror and electrode layer depend on the respective architecture; MIRA1 that was not conceived such that the mirror layer follows the electrode layer and MIRA2 were the mirror layer is supposed to follow the electrode layer. For the MIRA1 architecture the following contributions sum-up to the total spacing uniformity:

- Variation of the landing pad height 100nm
- Variation of the spacer height 10nm
- Deformation of the mirror layer 260nm
- Bow of the electrode chip 40nm

The measured values were evaluated over a surface corresponding to the 5×5 array of the MIRA1 generation; given their stochastical nature, contributions one to three are added by their squares, whereas the bow of the electrode chip is added linearly as it has a preferential shape. The total spacing variation error is 320nm and the corresponding tilt-angle uniformity error 11.7 arcmin.

By design the MIRA2 architecture should yield devices were the mirror layer follows the electrode layer, ensured by intermediate spacer columns and a mirror layer that is completely detached from the handle layer of the mirror chip. Unfortunately the first fabrication and assembly run of MIRA2 chips showed that the utilized joining method is not suited to pose the mirror layer uniformly on the electrode columns and yielded an unacceptably high mirror layer deformation. Assuming that for future MIRA large array generations a more adapted fabrication method will be found, the spacing uniformity error is given with the height variation of the spacer columns only. Measurements on fabricated MIRA2 electrodes show that the height variation over a 200×100 array is about 200nm. This, assuming that the mirror lands on the electrode handle layer[15], would result in uniformity error of 7.3 nm. As this value assumes a perfectly uniform joining/interface between the mirror layer and spacer columns it can be considered as ultimate performance limit in terms of air-gap contribution.

The last contribution to the tilt-angle uniformity error budget is the global deformation of the MMA relative to an external plane. This is only relevant for the MIRA2 (and future) design generation where the mirror layer follows the topology of the electrode layer. A measurement on a fabricated MIRA2 electrode showed that the radius of the chip-bow is about 15m and the corresponding maximum slope deviation from a fitted plane is 9arcmin. From MIRA1 characterization it was found that the packaging induced bow is even larger than the intrinsic bow of the electrode—however, here the packaging was not optimized for minimizing deformation. Thus, assuming an

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[15] As designed for MIRA2. If in a future generation the mirror lands on a landing pad similar to the MIRA1 design, one must add 0.8$\mu$m for the variation of the landing pad height across the array.

ideal packaging, we can consider the intrinsic electrode chip bow as ultimate performance limit for the global deformation type contribution[16].

### 6.4.2 Tilt-Angle, Actuation and Voltage

The OFF-ON tilt-angle is considered together with the requirement on the actuation voltage and the resonance frequency, which are concurrent requirements. Disregarding the implications of the row-column actuation scheme, which are considered further below, the OFF-ON tilt-angle of 20° at an actuation voltage below 100V and with a resonance frequency of larger than 1kHz could be reached.

However, the spacing between mirror layer and electrode layer and consequently the absolute tilt-angle seemed to be hardly controllable in MIRA1 architecture; this was mainly due to the bad height control of the landing pad relative to the spacer height. Conceptually this could be overcome with the MIRA2 design, where the mirror lands on the electrode handle layer and therefore the spacing is uniquely given by thicknesses of the electrode and mirror device layer. Therefore, the control of the absolute tilt-angle depends on how well the absolute device layer thicknesses of the SOI wafers are characterized. In order to face variations of the latter, one could think of implementing arrays with different stopper beam lengths on one wafer—in that way, within a certain magnitude of thickness variation of the device layer, one could always produce arrays with the desired absolute tilt-angle.

### 6.4.3 Mirror Quality

The mirror quality was found to be within the requirements ($\lambda/20$ for $\lambda > 1\mu$m) at room temperature and cryogenic environment; the peak to valley deformation of gold-coated $100\times200\mu\text{m}^2$-sized mirrors was 35nm and 50nm at 300K and 90K, respectively, and the surface roughness was below 1nm RMS.

### 6.4.4 Operating Environment

It could be shown that the implemented device design is suitable for operation in cryogenic environment below 100K. Most important aspects were

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[16] Utilizing thicker electrode handle layer might be useful to further decrease the intrinsic bow of the electrode chip. Other methods, such as compensation layers on the electrode chip backside, are also conceivable, but it will be very challenging to compensate the bow with such methods for cryogenic operation.

Table 6.5: Open-loop tilt-angle uniformity. Measured and projected contributors to tilt-angle non-uniformity for MIRA1, MIRA2 and future large array devices. Where not otherwise indicated, the projected values are based on actual topographical and tilt-angle measurements on MIRA1 and MIRA2 devices. The indicated values are given in arcminutes and read like follows: an uniformity error of one arcminute signifies that the maximum deviation between any two mirrors across the array is one arcminute; following this specification, the total uniformity error is the linear sum of all contributions (and not the sum of squares).

| | Direct Measurement | | Projected |
|---|---|---|---|
| | MIRA1 | MIRA2 | Performance |
| | 5×5 | 200×100 | 200×100 |
| Actuator Variation | 3 | - | 3 |
| Crosstalk | 0.5 | - | 0.5 |
| Lifetime | 9 | - | (9) |
| Air-gap height | 11.7 | 7.3[a] | 7.3 |
| Electrode bow | 0[b] | 9 | 9 |
| Packaging[b] | 0[b] | - | 0[c] |
| Total Uniformity Error | 24.4 | - | 19.8[d] |

[a] Based on measured spacer height variation

[b] Included in the air-gap height variation

[c] Assuming a dedicated packaging approach

[d] Excluding possible lifetime effects; as the characterization of lifetime effects in MIRA1 is to be considered as preliminary, no projected values are given for this contribution

that the mirror quality stayed within the specified $\lambda/20$, that the mirrors could be switched and no device deterioration was observed. Given the very low CTE value of silicon at these temperatures (see also inset in Fig. 4.3, 69), it is expected that from a structural point of view the device can also be operated at 30K (for wavelengths between 5$\mu$m and 28$\mu$m); for operation at 30K one should possibly switch to 15$\mu$m-thick mirrors, sandwich coating or different adhesion layer (see Sec. 4.2.1). One should be careful concerning the electrical properties of the utilized semiconductor materials, especially the not-so highly doped polysilicon, at that temperature. However, in principle it should be feasible, as for instance the micro-shutter array for the JWST NIRSPEC *is* already qualified for operation at 30K (see Sec. 1.4).

### 6.4.5 System Simplicity

The requirement on system simplicity implies that above key performance characteristics, such as absolute tilt-angle and above all, tilt-angle uniformity must be reached within the specified environment without making use of a monitoring and feed-back system and integrated electronics. This is a necessity as otherwise the system, with its millions of mirrors and cryogenic operation environment, could hardly be handled, technologically and economically spoken.

The stopper beam system and the row-column-actuation scheme are the two central concepts that potentially enable operating the device in feed-forward mode and still satisfying the stringent requirements on tilt-angle uniformity. The stopper beam concept has been successfully demonstrated and a stable tilt-angle of less than 3arcmin variation over a voltage range exceeding 10V could be shown. Even though the RCA scheme could, by the lack of corresponding MIRA2 devices, not directly be demonstrated, the major pre-condition, the stopper beam system providing a “flat” voltage range for setting the hold voltage could been shown. The RCA scheme has the potential to control $m \times n$ micromirrors with only $n + m$ signals, and in principle, only two voltage levels, enabling low-complexity driving electronics even for a very large number of micromirrors.

Whereas it was not intended by concept, the negative pre-tilt of the micromirrors (due to a stress gradient in the polysilicon layer) has potentially a positive effect on the RCA; as the pre-tilt adds a negative offset only to the mirrors in OFF-state, it compensates partially for the positive OFF-angle due to the non-zero hold voltage $V_h$ that is applied to all mirrors in the RCA scheme.

It has showed that mirrors can be switched, without any feed-back nor feed-forward compensation, within 800$\mu$s from the OFF- to the stable ON-state, easily satisfying the requirement on switching speed (5ms). Switching to a state within the OFF-range will require some more consideration in a future implementation of the driving scheme as, due to very high quality factors in vacuum environment, large overshoots and long ringing (as already measured in ambient air) is to be expected. However, this is only of some note at the very first step of the RCA when a common voltage (below the actuation voltage) is applied to all mirrors, presenting a certain risk that mirrors switch accidentally in to the ON-state. This can certainly be avoided with a soft start approach. A conceptually interesting approach would be to find a way to latch the mirrors also in the OFF-state, providing maximum operation safety.

### 6.4.6 Summary

In summary, many key requirements of a MMA suited for the use in future multiobject spectrographs were shown. There remain two elements, that need to be demonstrated in future developments:

- Large Arrays with uniform spacing
- Line-Column Actuation

In the next section a demonstration of the object selection capabilities of a 5×5 mirror array of the MIRA1 generation is presented.

## 6.5 System Integration: MOS Demonstration

For demonstration of the object selection capability of the fabricated micromirror arrays a characterization bench at LAM has been utilized. This optical bench has been developed during the prestudies for the JWST and dedicated to the operational characterization of MOEMS-based slit masks, MMA as well as MSA [60]. Several parameters can be addressed with this modular characterization bench, as the size of the source, its location with respect to the micro-elements, the wavelength, and the input and output pupil size. Three groups of elements are considered (Fig. 6.17 (a)):

- Sources: a large variety of optical sources, point or extended source, laser or white light are used. Two arms define sources by a hole or a

Table 6.6: Comparison of actual MMA performance against required performance. Note that all performance parameters are valid within the specified temperature range and operation environment

| | Specification | MIRA1[a] | MIRA2[a] | MIRAX[b] |
|---|---|---|---|---|
| Tilt-angle OFF-ON | $\geq 20°$ | OK | - | OK |
| Tilt-angle uniform.[c] | Goal: <10' | <25' | - | <20' |
| Mirror Flatness[d] | $\lambda/20$, $\lambda > 1\mu$m | OK | - | OK |
| Surface Roughness[c] | $\leq$1nm RMS | OK | - | OK |
| Mirror Size | $100\times200\mu$m$^2$ | OK | OK | OK |
| Array Size | 200×100 | 5×5 | OK | OK |
| Fill Factor | $\geq$95% [e] | OK | OK | OK |
| Resonance frequency | $\geq$1kHz | OK | - | OK |
| Actuation Voltage | $\leq$100V | OK | - | OK |
| Operating Environment | $10^{-6}$mbar | OK | - | OK |
| Operating Temperature | $\leq$100K[d] | OK | - | OK |

[a] Measured performance

[b] Projected performance

[c] Maximum tilt-angle deviation of any two mirrors within the array in ON-state with respect to an external reference plane including drift over life-time.

[d] Gold coated mirrors

[e] Along the long slit direction

group of holes with the proper diameter in order to simulate a typical astronomical field of view. Number of sources, relative location in the field of view, magnitude, wavelength and spectra could be chosen independently on the two arms. The sources are focused on the MMA. Fine tuning stages permit to locate very precisely the sources on the MMA. This way the objects of interest as well as the spoiler sources can be generated.

- Component environment: injection and collection of the light to and from the optical MEMS device with the possibility to configure independently the input and output pupils. According to the optical design of JWST different instruments as well as future instruments for ELTs, the optical aperture in the focal plane of the telescope could be tuned from F/6 to F/50. The output pupil of the characterization bench simulates the size of the grating inside the spectrograph. Oversizing of the output pupil is limited in a space instrument. In order to obtain high resolution images of the micro-mirrors, also F/2 output pupil can be used.

- Detectors: a high dynamical range CCD for device imaging and contrast measurement, and a conventional CCD for pupil imaging.

The setup was configured to demonstrate the object selection capabilities of MMA1 generation micromirrors. Two distinct objects are set in the field of view and a 5×5 array is used to select either one or the other object. Here the long slit mode is used, i.e. all five mirrors in a line of the 5×5 micromirror array are tilted at the same time, as illustrated in Fig. 6.17 (b). Note that the fill-factor along the slit is very high, i.e. 97%. First, both objects are selected, that is the mirror lines where the objects are located are tilted. Then only either the right or the left object is selected. Fig. 6.18 shows the series of images as seen by the CCD camera (spectrograph).

In order to measure the contrast, all mirrors of the array were set to the ON-position and then in OFF-position. After removing the background light for each measurement, the total flux is integrated on each micro-mirror surface in both positions. The ratio between these two values is said to be the contrast.

This procedure has been applied for a 5×5 MEMS mirror array of the MIRA1 generation and values between 200 and 300 have been measured. These values do not meet yet the contrast requirement, but are still promising as the cause for the rather low values and a measure for its alleviation are identified.

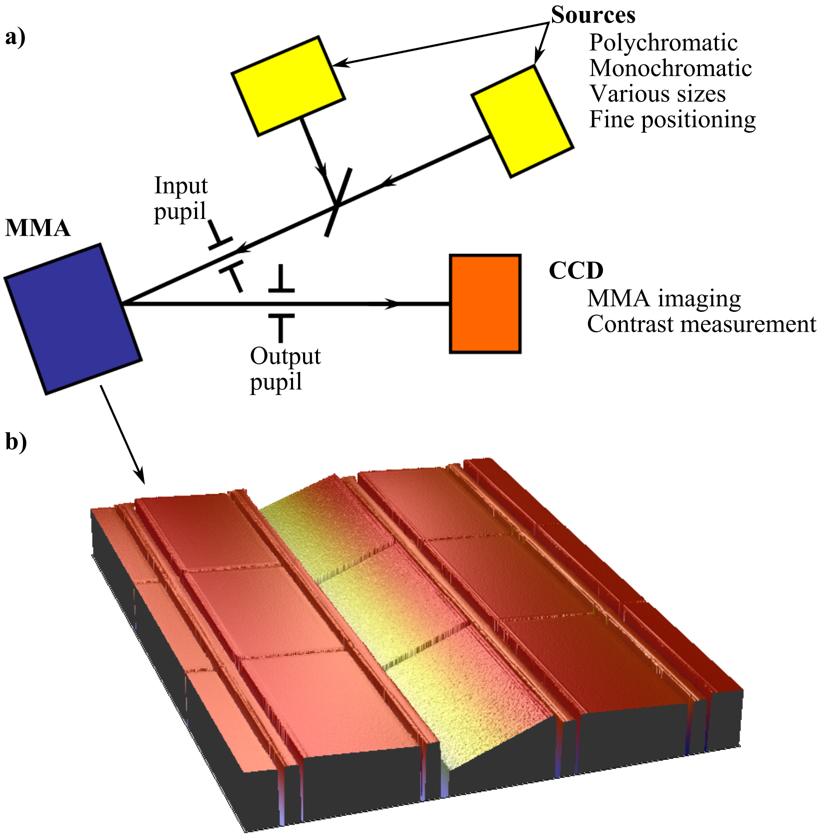

Figure 6.17: (a) Object selection setup. (b) Long slit mode of a 5×5 array; the object that falls on the tilted line is selected and sent to the spectrograph. The long slit mode is commonly used in astronomical spectrographs for background subtraction.

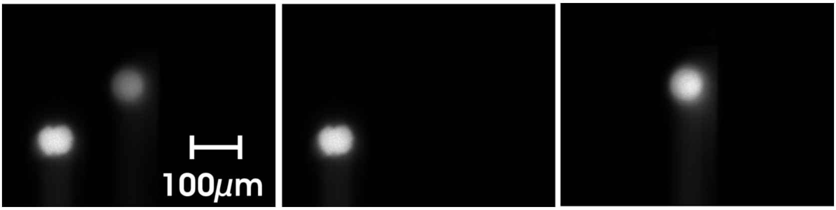

Figure 6.18: CCD images corresponding to the image plane of the spectrometer. In the first image, two objects are present in the field of view, in the second and third image one out of two object is selected, blocking completely the light of the other object. The projected object has a diameter of 50$\mu$m which corresponds to the size of a typical astronomical object in the focal plane of a telescope.

The main contribution to the stray-light, causing the low contrast value, is originating from the rounded edges of mirrors and frame. This is indicated in Fig. 6.19, showing a section of a full-field illuminated MMA with all mirrors in the OFF position and a cross-section SEM of a mirror and frame edge. The rounded edges originate from the oxidation process that was utilized to fill the trenches during processing. A process avoiding thermal oxidation would alleviate the rounded edges and lead, potentially, to higher contrast values.

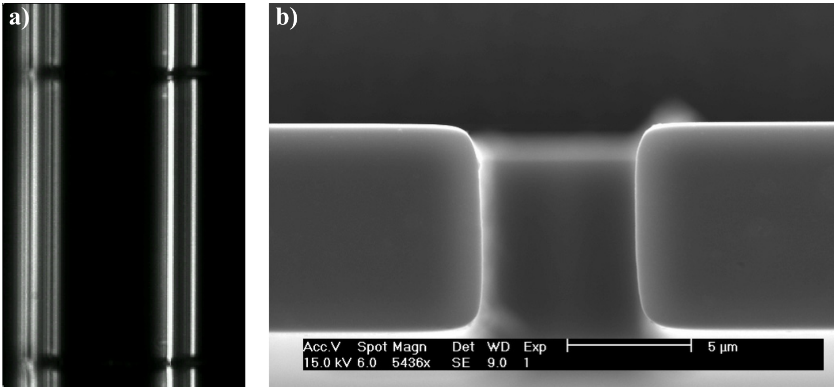

Figure 6.19: Stray light due to rounded mirror edges. (a) Section of a full-field illuminated MMA with all mirrors in the OFF position is shown (same setup as in Fig. 6.17. The very bright lines indicate the location of the mirror and frame edges (one line of mirrors is shown). (b) Cross-section SEM of two adjacent mirrors, exhibiting the rounded edges originating from a thermal oxidation step during fabrication. For future development the thermal oxidation step should be avoided, in order to yield sharp edges, which would strongly reduce stray-light and consequently increase the contrast.

# Chapter 7

# Summary and Perspectives

Photons are very precious in astronomy and therefore optimum instruments and sub-components matching the science case are a necessity for scientific progress. Missions and projects devoted to study the dark energy and dark matter distribution and evolution, i.e. the formation and evolution of the Universe, must use different observational probes. One major probe is the study of the Baryonic Acoustic Oscillations (BAO), based on low-resolution spectroscopic observations of a very large number of high-red-shift galaxies, covering a large fraction of the whole sky. In order to optimize the Signal-to-Noise Ratio (SNR) value, the high precision spectra measurements are obtained via multi-object spectroscopy. Multi-object spectroscopy (MOS) with multi-slits is the best approach to eliminate the problem of spectral confusion, to optimize the quality and the SNR of the spectra, to reach fainter limiting fluxes and to maximize the scientific return both in cosmology and in legacy science.

MEMS arrays where identified by the major global astronomical and space societies as high-potential candidates for the use as reconfigurable object selection masks in future MOS: they are lightweight, remote-configurable, versatile and can be operated in cold environment. Within the scope of this thesis the corner stones for a new class of micromirror arrays (MMA) for the use in future MOS has been laid: the MIRA project. The conceptual and technological basis has been elaborated that is required to yield MMA satisfying the very challenging requirements imposed by the application in astronomical MOS. The main requirements where: large tilt-angles of $\geq 20°$, feed-forward tilt-angle uniformity, large micromirrors of $100 \times 200\mu\text{m}^2$ with a surface quality better than $\lambda/20$, operation in cryogenic environment and large array size.

A device concept matching these stringent requirements has been presented. The device concept includes a two-chip architecture required to accommodate the large tilt-angle of $\geq 20°$ for the $100 \times 200\mu\text{m}^2$-large micromirrors (and provide the potential for implementing even larger mirrors according to the needs of the considered instrument). The micromirrors are made from $10\mu$m-thick bulk single crystalline silicon to provide maximum flatness. A central element of the device concept is a system of landing and stopper beams that, together with a cantilever beam suspension, is aimed to provide feed-forward tilt-angle uniformity, suppressing process variations of the actuator and suspension elements. Further, a device architecture, based on intermediate supporting columns, for large arrays have been conceived, potentially providing uniform spacing between mirror and electrode chip. A fabrication process, based on bulk-micromachining for the micromirrors, trench refill and polysilicon surface micromachining for the cantilever suspension and stopper beams has been developed for the mirror chip. The electrode chip was fabricated using a delay mask process, yielding spacer elements with uniform height and electrodes and wiring in the same silicon layer. An assembly scheme for small arrays, allowing passive aligning with an accuracy of $\pm 5\mu$m, based on guiding structures and clip-system, has been developed and demonstrated.

Fabrication yielded functional small array architecture devices; arrays of $5\times5$ micromirrors were been used for optical and electromechanical characterization and proof of device concept. The micromirrors showed to have an excellent surface quality, with a maximum peak-to-valley deformation of less than 10nm for uncoated mirrors, 35nm for gold-coated mirrors at room temperature and 50nm for gold-coated mirrors at cryogenic temperatures (100K)—thus, fulfilling the requirements of $\leq \lambda/20$ for $\lambda \geq 1\mu$m. Electromechanical characterization confirmed the device concept and modeling. Micromirror devices yielding a tilt-angle of 20° at an actuation voltage below 90V and a resonance frequency of 2kHz where shown. The tilt-angle in ON-state was stable within 3arcmin over a voltage range of more than 10V, demonstrating the stopper and landing beam concept, which was conceived for suppressing process variations and consequently providing uniform tilt-angle.

Successful operation of the micromirror array *in vacuo* and cryogenic environment at temperatures below 100K was demonstrated, validating the all-silicon device concept, conceived for cryogenic compatibility. A demonstration of the object selection capabilities of the fabricated micromirrors on a MOS-demonstrator-bench at LAM has been carried out. First contrast measurements showed that the contrast is rather low (between 200 and 300); the reason was believed to be attributable to rounded mirror edges, originating from a thermal oxidation step during fabrication.

Avoiding the oxidation step in future development will yield sharper edges and potentially much better contrast values. Other subjects that need to be tackled in future work are an adapted assembly process for providing spacing uniformity in large arrays, improved fill-process for avoiding polysilicon residues (or adapting the process such that no trench-refill is required) and demonstration of the row-column-addressing scheme. The direct proof of tilt-angle uniformity on large arrays is also subject to future work.

A central element and achievement of the present thesis was the concept and implementation of the stopper beam concept. The thorough analysis and engineering of the stopper beam concept and uniform spacing approach promoted fundamental understanding of the potential and limits of a pure feed-forward based tilt-angle uniformity. Feed-forward tilt-angle uniformity and stability of the tilt-angle and the corresponding row-column addressing scheme are central elements for the success of a MIRA-based MMA in future large-scale MOS, seen the very large number of mirror elements that will be needed to handle. Based on measurements and theoretical considerations a feed-forward tilt-angle uniformity of better than 20arcmin was predicted for future generations of 100×200 mirror arrays. In a MOS this would be an acceptable value for an F-number of the incoming beam of F/10 and a pupil oversizing of 20%. The tilt-angle uniformity could potentiall be further improved if fabrication substrates with a very low total thickness variation (TTV) are employed.

Besides providing uniform tilt-angle, it has been showed that the stopper beam system can also be used to tune the ON-tilt-angle (in the design phase!) over a range of 5° around the nominal ON-tilt-angle by varying the length of the stopper beam, without the need to alter the actuation voltage! This could be used to intentionally vary tilt-angle within one array of from array to array within one wafer. The stopper beam system, feed-forward tilt-angle uniformity, large tilt-angles and large, flat mirrors could be prove to be useful also for applications beyond astronomical instrumentation.

A very good indication for the success of the present work is the fact that the MIRA project is being continued. At the time of print it is Michael

Canonica who is continuing the present work within the frame of his Ph.D thesis. He already showed an improved fabrication process, resolving the poly-hair issue [8] and is working on a new generation of MIRA, based on a wafer-level assembly process, which potentially provides the required spacing uniformity for large mirror arrays (to be published). On the other hand, the partner institute LAM, Marseille, and the Italian astronomical institute, Brera and Bologna, are currently working on a prestudy for a MMA-based MOS demonstrator to be installed on the Italian 3.6m Galileo telescope on the Canary islands[1]. So, with a little luck—or not too much of bad luck!—in a few years first spectra with a MIRA-based MOS will be recorded.□

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# Acknowledgments

I would like to acknowledge all the people who contributed, directly and indirectly, to the realization of this work. First of all I would like to express my gratitude to Prof. Nico de Rooij who gave me the opportunity to work in his group and carry out my Ph.D work in an outstanding environment.

I sincerely acknowledge Wilfried Noell and Frederic Zamkotsian who guided and supported me as supervisors and co-directors through the highs and lows of my time as Ph.D student—anybody who ventured doing a Ph.D knows how precious a good support is (especially during the lows!). Frederic's dedication to astronomy and his commitment to the promotion of MEMS for astronomy is unique and without his initiative, this thesis would not have been materialized.

I'm grateful to Michael Canonica, my successor, for having supported me during our common time at IMT and even beyond. Michael, I wish you all the best for your Ph.D and successful continuation of MIRA—though I don't think you need luck, given the outstanding work you are doing!

Also in the context of the MIRA-project I would like to acknowledge the work of the students who did their semester or master work under my supervision and contributed to this thesis: Pradyumna Ayyalasomayajula, Andreas Hugi and Zhao Yazhou. Further, I would like to thank the colleagues of Frederic Zamkotsian—Rudy Barette, Emmanuel Grassi and Patrick Lanzoni—for their valuable assistance during interferometric and cryogenic characterization at LAM.

I thank the—present and former—members of the OMEMS group, namely Roland Bitterli, Nicolas Golay, Thomas Overstolz, Yves Pétremand, Stefan Weber and Michael Zickar for their support and fruitful discussions (technical and non-technical!). Thank you Michi for showing me the ropes in the clean-room and beyond!

My acknowledgments to the excellent work of the current and former

SAMLAB staff[2]: Pierre-Andre “Clairon” Clerc, Edith Millote, Giovanni “La Vanne” Bergonzi, Sylvain Jeanneret, Gianni Mondin, Nicole Hegelbach, Sylviane Pochon, Jose Vaquera, Stephan Ischer, Massoud Dadras, Mireille Leboeuf, Claudio ”Forza Italia“ Novelli and Karine Frossard—*un grand merci a vous tous pour votre support et les bons relations, au-delà des discussions techniques!*

Special thanks to Martial Racine, the former administrator of the IMT, with whom I shared some unforgettable moments during the preparation of the 30-year-IMT celebrations—*Martial, on n’a pas droit d’erreur!*.

And not to forget Reinhard Völkl from Suss Micro-Optics who would never cease to push me finishing my thesis—thank you Reinhard, also for helping me understanding the culture of my new employer. At this place I also acknowledge Jürgen Huber, my current superior, for having a lot of understanding for my situation during the writing of my thesis.

There is not only work in life, as they say! I express my sincere gratitude to my big Family, Ali, Karolin, Stöff, Seraina, Alfred, Lili, Andrea, Monica, Mouldi and Phippu (my little sister’s fiancé—*Hopp YB!*). Thanks also to Cathy, the sister of my girlfriend (and thus, a potential future family member), for supporting (in every sense of the word) me during the sometimes cumbersome process of thesis-writing.

Good friends are the backbone of every man: thank you for sharing all the fun (and holding together in difficult times): Ändu, Basil, Felix, Fredy, Jérome *le Genevois*, Moni, Pädi, Sile, Stu, Tobi, Urs, Vine, Xa, Xändi, and—in memoriam—Gregy.

In the end, I even express my gratitude to a thief—to Michèle who has stolen my heart! Besides, she read my thesis—*nota bene* as a non-physicist—from the first to the last word, which I would consider as a major achievement and a sincere commitment to our relationship! Needless to say that

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# Appendix

Table 7.1: Process Parameters for the micromirror chip fabrication

| # | Step | Equipment | Parameters |
|---|---|---|---|
| 1 | Substrate | SOI Wafer | Device L. 10$\mu$m,<br>Handle L. 350$\mu$m |
| 2 | Cleaning | | $H_2O_2SO_4$+$H_2O_2$ 95°C,<br>BHF |
| 3 | Photolitho Device L. | | S1318 1.1$\mu$m[a] |
| 4 | DRIE Device | STS | 10$\mu$m |
| 5 | Resist Strip | Oxygen Plasma | 30min |
| 6 | Cleaning | | $H_2O_2SO_4$+$H_2O_2$ 95°C,<br>BHF |
| 7 | Thermal wet oxidation | | 2$\mu$m |
| 8 | APCVD SiO2 | | 1$\mu$m |
| 9 | Photolitho SiO2 | AZ4562 5.6$\mu$m[a] | |
| 10 | RIE SiO2 | Alcatel | 3$\mu$m |
| 11 | LPCVD Polysilicon | | 0.6$\mu$m |
| 12 | p-doped APCVD SiO2 | | 300nm |
| 13 | Diffusion in $N_2$ | | 1050°C 1h |
| 14 | Photolitho Poly | | AZ1518 2.1[a]$\mu$m |
| 15 | DRIE Poly | | 1.2$\mu$m |
| 16 | Resist Strip | Oxygen Plasma | 30min |
| 17 | BS protection | | AZ1518 2.1 |
| 18 | Partial FS SiO2 removal | | BHF 12min 1$\mu$m |
| 19 | Resist Strip | Oxygen Plasma | 30min |
| 21 | FS protection | | AZ1518 2.1 |
| 22 | Photolitho Handle | AZ4562 8$\mu$m[a] | |
| 23 | BS SiO2 etch | | BHF 20min 2$\mu$m |
| 24 | DRIE Handle L. | STS | 350$\mu$m |
| 25 | Resist Strip | Oxygen Plasma | 30min |
| 26 | HF vapor release | Idonus | 40°C 2h |

[a] See Table 7.2

Table 7.2: Photolitho parameters. For all processes a HMDS surface pretreatment before resist spin has been carried out. The parameters were: Dehydration 15’,150°C;HMDS 5’,150°C,80 Torr. A postbake was carried out for all process at 85° during 2h. These parameters can be considered as starting values; the actual values varied in function of environmental parameters, feature dimensions, substrate reflectivity, etc.

| # | Name | Spin | Prebake | Exposure | Development |
|---|---|---|---|---|---|
| 1 | S1318 1.1$\mu$m | 5500RPM, 40” | 1’,110°C | 30mJ | AZ400:DI 1:4, 45s |
| 2 | AZ1518 2.1$\mu$m | 4000RPM, 40” | 1’,100°C | 40mJ | AZ400:DI 1:4, 60s |
| 3 | AZ4562 5.6$\mu$m | 5500RPM, 40” | 10’,95°C | 120mJ | AZ400:DI 1:3, 90s |
| 4 | AZ456 8$\mu$m | 2500RPM, 40” | 10’,95°C | 120mJ | AZ400:DI 1:3, 120s |

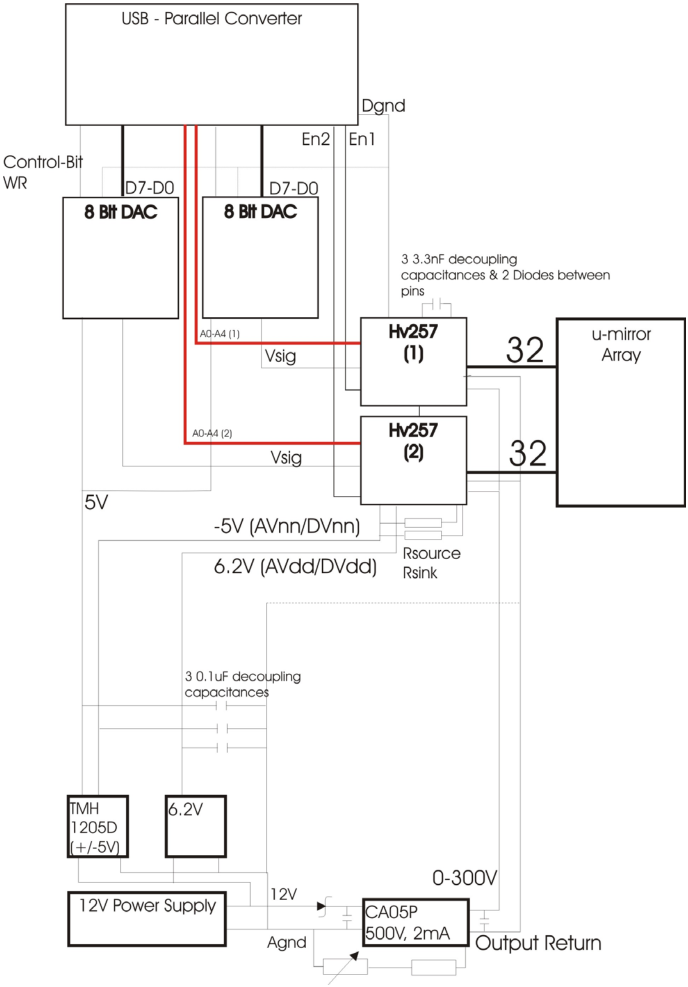

Figure 7.1: Schematic of driving electronics