Published in IEEE International Conference on Electronics, Circuits and Systems, 147-150, 1998
which should be used for any reference to this work

An 8-bit Low-Power ADC Array for CMOS Image Sensors

Steve Tanner, Alexandre Heubi, Michael Ansorge, and Fausto Pellandini

Institute of Microtechnology, University of Neuchâtel, Breguet 2, CH-2000 Neuchâtel, Switzerland
Phone: +41 32 718 34 30, Fax: +41 32 718 34 02, E-Mail: steve.tanner@imt.unine.ch

***Abstract* — The paper presents an original analog-to-digital converter (ADC) array meeting the constraining requirements in resolution, speed, size, and low power consumption of high-performance low-cost video cameras. The converter array is based on ADC cells relying on a cyclic redundant signed digit (RSD) algorithm supporting comparators with extended tolerance. A prototype ADC array composed of 32 converters was integrated in a 1µm CMOS process and tested. It is featuring an 8 bit resolution for an active area of 2.1 mm2, and a power consumption of 4 mW at a sampling rate of 4.2 MS/s, with a voltage supply of 2.6 V. Typical DNL and INL values of -0.5/+ 0.2 and ± 0.4 LSB, respectively, were measured for each ADC cell. Moreover, an overall SNR of 45 dB can be achieved with a digital off-chip offset compensation.**

I. INTRODUCTION

In many domains, especially in the emerging field of battery-powered multimedia devices, a steadily increasing demand for high-performance low-power and low-cost video cameras is observed, motivated by a variety of promising application potentialities.

The image acquisition is nowadays commonly performed by solid-state image sensors, which are most often integrated on dedicated process-specific circuits (e.g. CCDs), separately from subsequent AD converters and electronics. Besides higher packaging costs, this solution requires fast analog signal multiplexing and off-chip interconnection, implying in turn an increased power consumption, and a reduced noise immunity. Usually, the sensors are connected to a single *fast* ADC (Fig. 1.a), such as a pipelined ADC [1], or other kinds of ADCs [2, 3], contributing again to an increased power consumption. In addition, few of them are featuring a sufficiently small silicon area [4].

The discussed limitations can be alleviated using more recent low-power CMOS-compatible image sensors [5, 6], which can be integrated jointly to the AD converters. In particular, it is then possible to take fully advantage of the inherently parallel structure of image sensors, by using an array of slower but power optimised ADCs, as represented in Fig. 1b. However, one is then faced to potential matching difficulties: any offset, gain, or timing mismatch *between* the multiple ADC channels results in fixed-pattern effects reducing the overall absolute resolution of the conversion [7].

Compared to formerly published structures suffering from limitations in area, speed, or power consumption, e.g. [8], the key motivation of this paper is to show that ADC arrays can meet the requirements of low-power video applications in terms of achieved resolution, speed/area factor, and power consumption.

A prototype of an 8-bit ADC array consisting of 32 converters is presented, relying on a cyclic AD converter chosen for its performance in power consumption, small area, and sufficing speed [9]. The input multiplexing scheme is optimized accordingly. The prototype is featuring an overall resolution of 8-bit, an equivalent sampling rate of 2 MegaSamples/sec per mm2, and a power consumption resulting in an energy of less than 1 nJ per sample (1MS/s per mW), which is one of the lowest figures reported to date [3].

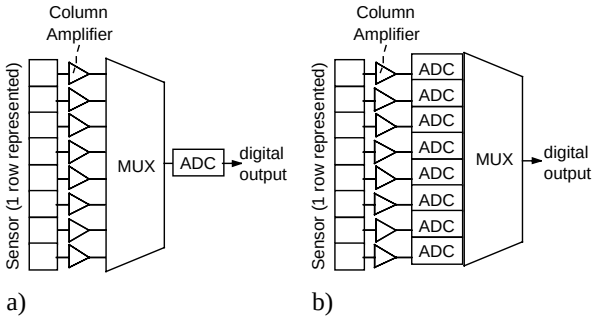

Fig. 1: a) Single ADC and b) Multiple ADC configuration.

The paper is organised as follows. Section II describes the constituent cyclic AD converter, whereas the ADC array architecture is discussed in Section III. Section IV is then presenting experimental results. The conclusions are finally drawn in Section V.

II. CYCLIC RSD AD CONVERTER

A. Algorithm and implementation

The selected AD converter, fully described in [10], is based on the cyclic RSD (Redundant Signed Digit) algorithm depicted in Fig. 2. Cyclic converters are known to require a very accurate comparison, with a tolerated inaccuracy smaller than half an LSB. This constraint can advantageously be alleviated using an RSD conversion scheme relying on two simple comparators, whose tolerated inaccuracy can reach up to half the reference voltage *Vref*, regardless of the number of bits. The inaccuracy of the comparison is then digitally compensated during the progress of the conversion cycle, by transforming the redundant digital result into a two's complement representation.

An efficient switched capacitor implementation of the algorithm, as proposed in [9], is used. The input signal is sampled at the very beginning of the conver-

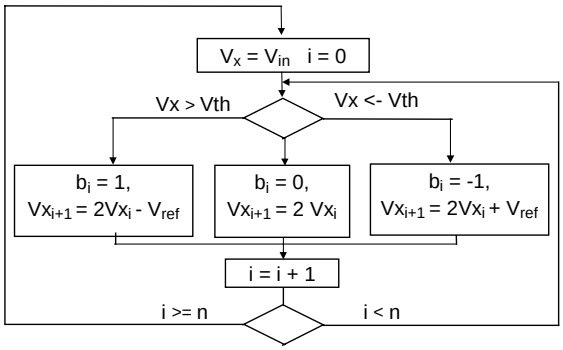

Fig. 2: Cyclic RSD conversion algorithm.

sion process, so that no sample & hold device is required. The large tolerance comparators are realised using simple strobed cross-coupled inverters. This implementation offers the next advantages [9]:

- offset of the analog devices and switch charge injection only result in a digital offset; the response linearity is in particular not affected;
- saturation of the active devices doesn't occur for low level input signals (no distortion), and causes a saturation of the digital response only.

B. Low-power techniques

To achieve a low power consumption, several techniques were jointly applied. The first consisted in using two-stage Miller OTAs, that are well suited for low-voltage operation. The corresponding differential p-MOS input transistors are working in weak inversion to get a higher DC gain and a lower offset. Second, capacitor values of 1 pF were selected as a good trade-off between matching requirements and power consumption. Third, the local logic (generation of switch signals, RSD to 2's complement conversion) was carefully reduced to the minimum number of components.

C. Resolution

The overall resolution of an ADC array is limited by the mismatch between the channels, and by the accuracy of the ADC itself. The response of the RSD conversion considered at the *i*th iteration is given by:

$$Vx_i = (2+\varepsilon)\cdot Vx_{i-1} + B_i \cdot (1+\beta)\cdot V_{ref} + V_{off} \qquad (1)$$

where Vx_i, V_{ref}, and V_{off} represent the actual signal voltage, the reference voltage, and the offset voltage, respectively. The ternary output bit (-1, 0, 1) is given by B_i, whereas ε and β denote error factors connected to voltage doubling and reference subtraction.

$$\varepsilon = \left(\frac{a}{a+3}\right)\cdot\left(\frac{C1}{C2}+\frac{a+1}{a}\right)-2 \qquad (2)$$

The ADC design described in this paper has a doubling error given by (2), where a is the OTA DC gain, $C1$ and $C2$ corresponding to the capacitors used for voltage doubling. According to [10], the maximum absolute DNL (Differential Non-Linearity) amounts to:

$$MaxDNL \cong |\varepsilon| \cdot 2^{n-3} \qquad (3)$$

where n indicates the number of bits resolved. According to (2) and (3), $MaxDNL \cong 0.2$ LSB for an 8 bit converter, for a maximum capacitor mismatch of $e = 0.4\,\%$ (double-poly CMOS process), and a DC gain of a = 66 dB. The INL (Integral Non-Linearity) depends in turn on the way the mismatch occurs, i.e. whether it is compensating the error induced by the finite gain of the OTA, or not. Fig. 3 shows the DNL and INL simulated under worst case conditions.

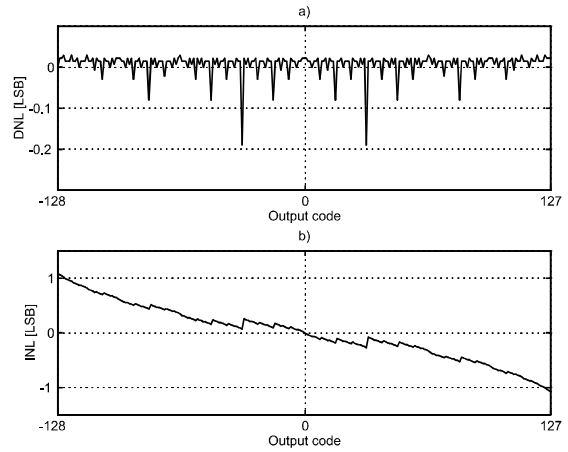

Fig. 3: a) DNL and b) INL for the RSD cyclic converter, with e = 0.4 % , and a = 66 dB .

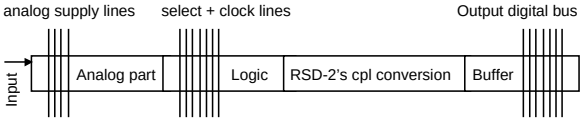

Fig. 4: Floorplan of the basic RSD converter cell.

D. Layout implementation

The pitch of the converter was selected to satisfy two contradictory constraints: on one side it should be as small as possible to stack many devices in a limited area, whereas on the other side it should remain large enough to preserve the square shape of the capacitors (better matching conditions). The layout is organised so that analog and digital parts are clearly separated to improve noise immunity. All supply and clock lines are drawn perpendicularly to the ADC cell to simplify interconnections and minimize area. Analog crosstalk between adjacent ADC cells is reduced by means of diffusion guard rings placed into the substrate wherever possible. Most important for CMOS sensor applications, the ADC has to be protected from light by a second metal layer to avoid charge generation and collection in the active areas; conversion inaccuracy and power consumption would otherwise increase. Fig. 4 shows the designed floorplan of the RSD converter, with a size of 980 x 60 μm2.

III. ARRAY ARCHITECTURE

A. Structural and operational organisation

The interconnection between the image sensor and the ADC array is supported by an M lines-wide analog bus, so as to take full advantage of the inherently parallel structure of image sensors, while disposing of

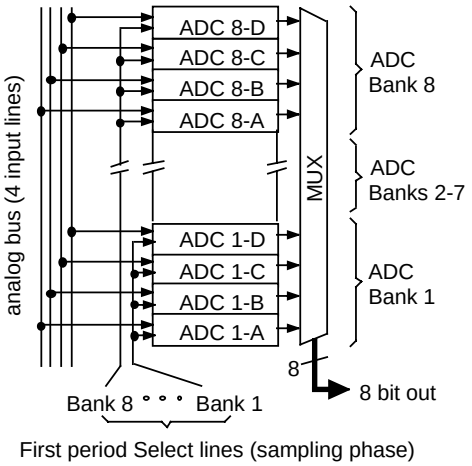

Fig. 5: ADC array architecture.

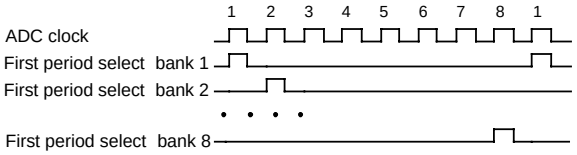

Fig. 6: Timing diagram of the select lines.

a certain flexibility in the organisation of the ADC array. The pitch of the ADC cell can this way be fixed independently of the pixel pitch of the image sensor.

Clearly, during each operational clock period of the ADC array, M pixel signals are conveyed to a bank of M converters for simultaneous signal sampling. From the n clock periods needed by the RSD converters to perform an n-bit conversion, only the first one devoted to signal sampling requires a connection to the analog bus. The remaining $(n-1)$ periods are then processed internally, so that the analog bus can be released to let other converter banks perform signal acquisitions. Globally, the ADC array is thus organised as a time-interleaved parallel ADC structure, composed of n banks of M converters each.

Fig. 5 shows the architecture retained for the designed prototype circuit, with $n=8$ and $M=4$, resulting in a total of 32 converters. The n ADC banks are steered by selection lines controlling the sampling phase occurring at the beginning of the conversion cycles (cf Fig. 5). The corresponding timing diagram is given in Fig. 6. The ADC array is connected to an experimental 128 x 8 pixel CMOS image sensor implemented on the same chip.

The proposed architecture is offering a high level of flexibility, the parameter M providing an easy way for adjusting the overall sampling rate. Moreover, the constituent ADCs are operating at an M times lower clock rate, which is beneficial for low-power design.

B. Input and output data multiplexing scheme

As shown in Fig. 7, the column lines of the sensor are grouped into sets of four signals, which are successively connected to the analog bus under the control of an input addressing shift register (SR). Similary, the 8

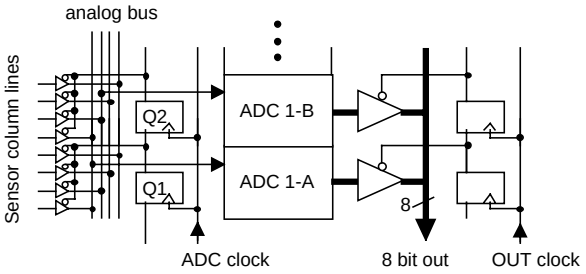

Fig. 7: Input and output multiplexing.

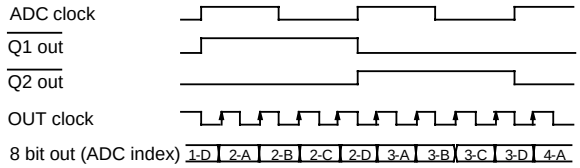

Fig. 8: Input and output timing diagram.

bit-parallel output data produced by the ADCs are read out through a time-multiplexed digital bus, controlled by an output addressing SR. Whereas the input SR is operating at the same rate than the ADC cells (cf *ADC clock* signal), the output SR is running four times faster (cf *OUT clock* signal) to keep track of the information flow. Fig. 8 shows the timing diagram of the output multiplexing.

C. Resolution limitations for ADC arrays

Two types of resolutions are considered for ADC arrays, namely the resolution of the constituent ADC cell, and the overall resolution achieved by interpreting the array as a single converter. The ADC cell resolution is limited by the quantisation error, and by the limited linearity. The average error power between the best fit line $a \cdot x + b$ and the measured transfer function of the ADC cell can be expressed as in [11]:

$$E_p = \langle\, \delta^2 \,\rangle, \quad \text{with} \quad \delta(x) = \hat{x} - (a \cdot x + b) \tag{4}$$

in which $\hat{x}$ is the quantised level of x, and a and b are error minimization terms corresponding to the best fit of the converter gain and offset. In case several converters are used in an array configuration, the best fit line of the *i*th converter will be specified by parameters a_i and b_i. Ideally, all converters should satisfy $a_i = a_0$ and $b_i = b_0$, $\forall i$. Hence, if we assume that a_i and b_i are equally distributed random Gaussian variables with variances σ_a^2 and σ_b^2, the SNR corresponding to a sinusoidal input signal is given by [11]:

$$SNR = -10 \cdot \log_{10}\left(\sigma_a^2 + 2 \cdot \sigma_b^2 \,/\, \alpha^2\right) \tag{5}$$

where α is the amplitude of the sinusoidal input.

TABLE I
EXPERIMENTAL RESULTS (Vdd = ±1.3 V, 25 °C)

General data	
Overall sampling rate:	4.2 MHz
Active area (1 µm CMOS tech.):	2.1 mm2
Power consumption:	4 mW
Input signal range:	±(Vdd – Vsat)
Single RSD ADC cell	
Typical SNR (*improvable*):	45 dB
Typical DNL (8 bit):	- 0.5 / + 0.2 LSB
Typical INL (8 bit)*:	± 0.4 LSB
Input-referred noise:	< 0.5 LSB
ADC Array	
Inter-channel gain variance:	0.1% (0.25 LSB)
Equivalent SNR (5):	60 dB
Inter-channel offset variance:	0.6% (1.5 LSB)
Equivalent SNR (5):	42 dB
ENB (effective number of bit):	6.7 bit
With digital offset correction:	7.2 bit

* referred to the best-fit line

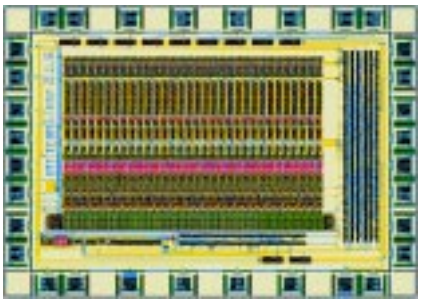

Fig. 9: Layout of the ADC array chip.

IV. EXPERIMENTAL RESULTS

A prototype chip consisting of an array of 32 8-bit RSD converters, including a 128x8 Active Pixel Sensor, exposure logic, and input/output multiplexing, was fabricated in the ALP1LV 1-µm CMOS process of EM-Microelectronic Marin, Switzerland. The chip layout is shown in Fig. 9. The bias and reference voltages used for the ADC array and the sensor column amplifiers were generated off-chip. A synopsis of the experimental results is provided in Table I.

The 32 constituent converters are working at a sampling frequency of 128 kS/s, corresponding to an overall sampling rate of 4.2 MS/s. The core of the ADC array (incl. input/output multiplexing) features a power consumption of ca. 4 mW for a supply voltage of ±1.3V. The prototype circuit is working properly from ±1.2V to ±1.6V. All constituent ADC cells are achieving an 8 bit resolution. The intrinsic ADC noise is higher than expected, but can clearly be reduced in future designs by proper shielding. The overall resolution of the ADC array is then limited by the offset variance (corresp. SNR of 42 dB), the gain variance having a small effect (equiv. SNR of 60 dB). Fig. 10 provides the superposition of the 32 ADC error functions (incl. saturation domains) after digital offset compensation. The image sensor characteristics are not reported here.

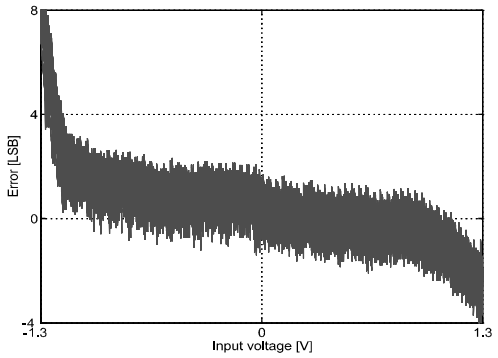

Fig. 10: Superposed error functions of the 32 ADC cells for a rail-to-rail analog input voltage.

V. CONCLUSION

An original ADC array meeting the requirements of battery-powered video cameras regarding resolution, speed, area, and power consumption, was presented. The concept was tested with a prototype circuit composed of an array of 32 8-bit cyclic RSD ADC cells, that features one of the lowest power consumption figures reported today, cf Table I. The overall resolution is mainly limited by the inter-channel offset, which can easily be compensated digitally, resulting in an overall resolution of 7.2 ENB (effective number of bit).

Acknowledgements

The fruitful collaboration with the project partners, and the financial support provided by the Swiss Priority Program MINAST (Grant 5.04) and the Swiss National Program MICROSWISS (Grant TR-IT-005), are acknowledged.

References

[1] T. Cho and P. Gray, "A 10-bit, 20 MS/s, 35 mW pipelined A/D converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 499-502, May 1994.

[2] K. Kusumoto, A. Matsuzawa, and K. Murata, "A 10-b 20-MHz 30 mW Pipelined Interpolating CMOS ADC," *IEEE JSSC*, Vol. 28, No. 12, pp. 1200-1206, Dec. 1993.

[3] M. Yotsuyanagi, et. al., "A 2 V, 10 b, 20 MSamples/s, Mixed-Mode Subranging CMOS A/D Converter," *IEEE JSSC*, Vol. 30, No. 12, pp. 1533-1537, Dec. 1995.

[4] B. Nauta, and A. Venes, "A 70-MS/s 110 mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE JSSC*, Vol. 30, No. 12, pp. 1302-1308, Dec. 1995.

[5] D. Renshaw, et. al., "ASIC Image Sensors", *Proc. IEEE Int. Symp. on Circuits and Systems*, 1990, pp. 7.3.1-7.3.4.

[6] R. H. Nixon, S. E. Kennedy, C. O. Staller, and E. R. Fossum, "128 x 128 CMOS photodiode-type active pixel sensor with on-chip timing, control and signal-chain electronics," *Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE*, Vol. 2415, pp. 117-123, 1995.

[7] C. S. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-µm CMOS," *IEEE JSSC*, Vol. 28, No. 4, pp. 447-454, April 1993.

[8] Z. Zhou, B. Pain, and E. R. Fossum, "CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-to-Digital Converter," *IEEE Trans. on Electron Devices*, Vol. 44, No. 10, pp. 1759-1763, Oct. 1997.

[9] A. Heubi, P. Balsiger and F. Pellandini, "Micro Power 13 bits Cyclic RSD A/D Converter ," *Proc. of ISLPED'96*, pp. 253-257, Aug. 12-14, 1996, Monterey CA, USA.

[10] B. Ginetti, P. Jespers, and A. Vandemeulebroecke, "A CMOS 13-bit Cyclic A/D Converter," *IEEE JSSC*, Vol. 27, No. 7, pp. 957-965, July 1992.

[11] W. Black and D. Hodges, "Time interleaved converter Arrays", *IEEE JSSC*, Vol. 15, No. 6, pp. 1022-1029, Dec. 1980.