

A novel low noise hydrogenated amorphous silicon pixel detector

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Abstract

First results on particle detection using a novel silicon pixel detector are presented. The sensor consists of an array of 48 square pixels with 380 μm pitch based on a n-i-p hydrogenated amorphous silicon (a-Si:H) film deposited on top of a VLSI chip. The deposition was performed by VHF-PECVD, which enables high rate deposition up to 2 nm/s. Direct particle detection using beta particles from ^{63}Ni and ^{90}Sr sources was performed.

1. Introduction

Vertical integration of light sensors by deposition of a hydrogenated amorphous silicon (a-Si:H) layer on a readout chip has recently gained a lot of attention [1–3]. This so-called thin-film on ASIC (TFA) or thin-film on CMOS (TFC) technology offers high integration level of the detecting device and the readout electronics. In combination with a scintillator, it has an interesting potential for high sensitivity and low level light detection. Therefore it has become an attractive solution for radiation detectors in particle physics and X-ray imaging applications.

Although a previous work has demonstrated that direct particle detection in a-Si:H films is possible [4], detection of minimum ionizing particles (MIP) was not yet proved. The total charge deposited by a MIP in the a-Si:H film is proportional to the film thickness. Due to the technical difficulty of depositing a thick a-Si:H film layer (up to 50 μm), the detector signal for a MIP above the noise is limited.

A radiation sensor for charged particles based on a-Si:H has recently been proposed [5]. In order to study

the electrical properties and detection characteristics of thick a-Si:H films, n-i-p structures have been deposited on glass substrates and above CMOS chips. Preliminary results on charge collection efficiency and speed with a 660 nm laser in 13 and 30 μm thick samples are described in [6,7]. In this paper we present results on direct particle detection from nickel (^{63}Ni) and strontium (^{90}Sr) sources.

2. Silicon pixel detector

The sensor, shown in Fig. 1, is a VLSI readout chip implemented in 0.25 μm CMOS technology combined with a 30 μm thick a-Si:H n-i-p film deposited on top. It consists of an array of 8×6 square pixels with a pitch of 380 μm . Octagonal metal pads, 150 μm wide, make the contact with the a-Si:H pixels. The chip is a 48 channel amplifier and shaper with a total size of $4 \times 4 \text{ mm}^2$. The preamplifier stage is a charge amplifier with an active feedback [8]. The shaper stage provides CR-RC shaping of the detected pulses with a peaking time of about 120 ns. The circuit was optimized to detect a 600 e^- signal with 30 e^- rms noise, for a pixel capacitance below 0.5 pF and a detector leakage current of up to 10 pA per channel. It is sensitive to negative and positive charges, with a dynamic range from 12 484 to 62 422 e^- and 2497 to 12 484 e^- , respectively.

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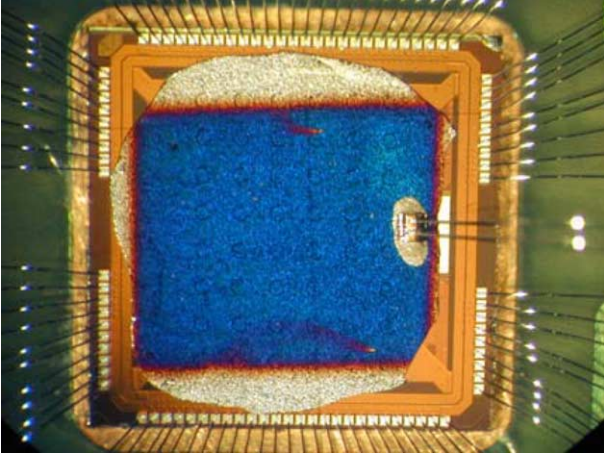


Fig. 1. Photograph of a 30 μm thick sensor. The a-Si:H n-i-p film was deposited on top of the $4 \times 4 \text{ mm}^2$ chip. The reverse bias was applied to the ITO layer via bonding wires.

2.1. Fabrication of the n-i-p diode

The a-Si:H n-i-p structures were deposited on the readout CMOS chip using the very high frequency (VHF) plasma enhanced chemical vapor deposition (PECVD) technique. This technique enables deposition of thick a-Si:H films on a small chip with low defect densities [5]. The deposition was performed at a rate of 15.6 \AA/s and a frequency of 70 MHz, using hydrogen dilution of silane. The relatively low temperature of this process (200 $^\circ\text{C}$) is compatible with post processing on finished electronic wafers. The main technological problem is to achieve uniform deposition of thick a-Si:H film on a small chip.

A cross-section of the a-Si:H film is shown in Fig. 2. The film consists of three layers: a top p-type layer of about 34 nm, a $32.6 \mu\text{m}$ intrinsic i-type layer and a 34 nm n-type layer, that makes the contact with the chip pads. In order to avoid the patterning of the bottom

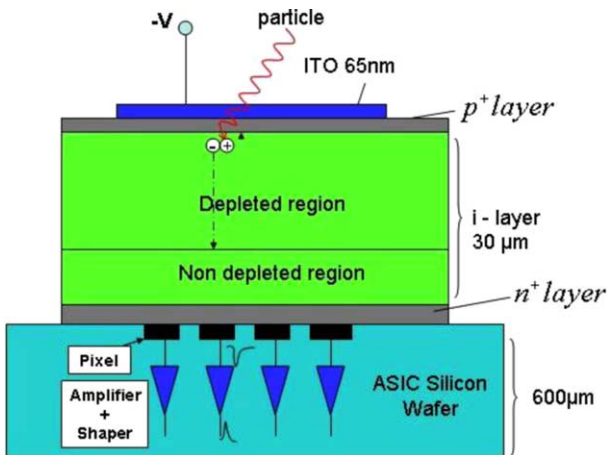


Fig. 2. Cross-section of a 30 μm thick a-Si:H n-i-p film deposited on top of the chip.

layer deposited on the ASIC, a low conductive n-doped layer was developed. An indium tin oxide (ITO) electrode was used for the top contact. The ITO layer has a thickness of about 650 nm and it was deposited by thermal evaporation assisted by an electron gun.

3. Measurement results

A negative voltage was applied to the ITO layer, depleting the n-i-p diode and increasing the detecting region from the p-i interface down towards the i-n interface. The charge deposited in the depleted region was directly sensed on the chip amplifier. An amplifier gain of 0.054 mV/e^- was measured using a test injection capacitance, for an amplifier feedback current of about 7 nA. The electronic noise from the ASIC alone together with the printed circuit board was measured to be 30 e^- per channel. This measurement was performed using a digital oscilloscope.

At a reverse bias of -70 V applied to the n-i-p diode, the measured leakage current was 4.5 nA per pixel. The noise distribution is shown in Fig. 3. A system noise of 4.5 mV rms, corresponding to 82 e^- was obtained from a Gaussian fit. This noise increase is mainly due to the unexpectedly high detector leakage current that forces an increase of the amplifier feedback current.

The sensitivity to charged particles has been measured with low energy electrons from the ^{63}Ni source where electrons are totally absorbed in the i-layer and with minimum ionizing electrons from ^{90}Sr . The measurements were performed in self-trigger mode, with a trigger level at about five sigma above the noise level. Fig. 4 shows the superposition of two oscilloscope traces from two separated beta particles from the ^{90}Sr source, for a reverse bias of -70 V and a threshold of 20 mV (370 e^-). The peaking time is about 130 ns and the signal amplitude varies with the beta electron energy.

The spectrum of beta particles obtained with the ^{63}Ni source is shown in Fig. 5. The peak corresponds to 700 e^- . The high detector leakage current prevented precise

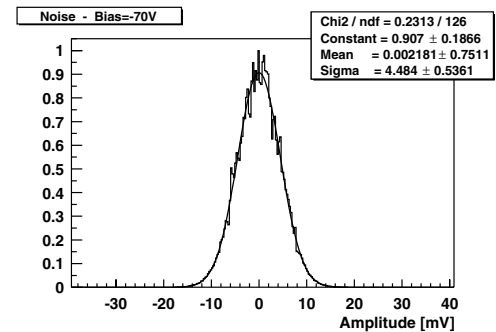


Fig. 3. Noise distribution of one pixel at a reverse bias voltage of -70 V . A Gaussian fit gives a noise of 4.5 mV rms, corresponding to 82 e^- .

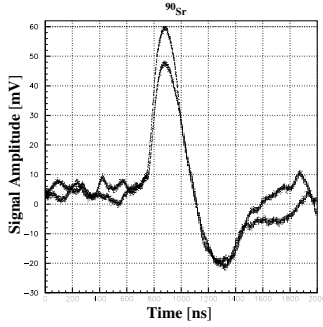


Fig. 4. Examples of a signal measured on one pixel following the absorption of beta particles from the ^{90}Sr source. The peak amplitudes correspond to 865 and 1100 e^- .

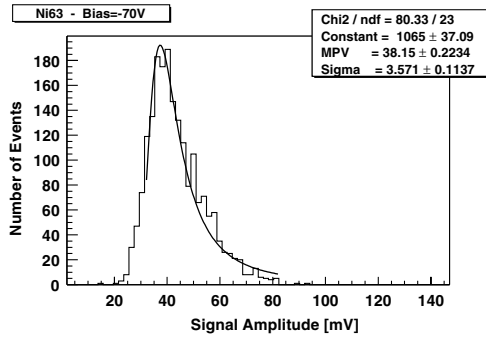


Fig. 5. Spectrum of beta particles obtained with the ^{63}Ni source, for an applied reverse bias of -70 V. The energy loss follows the Landau distribution with a peak at about 700 e^- (38 mV).

measurements and full depletion of the a-Si:H film, limiting the reverse bias voltage to -70 V. In this preliminary analysis a scan of the detector bias voltage

showed that even at -70 V, a full depletion of the a-Si:H diode was not yet achieved.

4. Conclusions

A novel silicon pixel detector based on a 30 μm thick n-i-p a-Si:H film deposited on top of a VLSI chip has been developed. The deposition of the a-Si:H film was performed by VHF-PECVD. The noise was measured to be 82 e^- rms at a reverse bias of -70 V and a detector leakage current of 4.5 nA per pixel. Charge sensitivity measurements, in a partially depleted sample, showed that electrons from ^{63}Ni and ^{90}Sr sources can be detected with a shaping time of 130 ns. The ASIC was optimized for a detector leakage current up to 10 pA and a higher value was measured in the sensor, limiting the applied reverse bias. Due to that a full depletion of the n-i-p diode could not be achieved. Although a spectrum from a ^{63}Ni source was measured, the detection of a MIP was not yet proven.

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