

Micro Power 14-bit RSD A/D Converter

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Micro power converters are required for power sensitive, battery-operated devices. Keeping this goal in mind IMT developed a 13-bit RSD cyclic converter. However, inaccuracies (capacitor mismatch, operation amplifier...) resulted in a relative precision behaviour. The implementation of a correction algorithm in a 2 μm CMOS technology is presented. It requires 1 mm^2 and simulations show that power consumption is less than 10 μW at 1.25 V. Consequently a fully linear 13-bit A/D converter featuring about 60 μW power consumption at 16 kHz and ± 1.25 V is feasible and will soon be realized as MPW.

1 Introduction

Progress in low power micro-electronics technologies and digital signal processing has opened the way to numerous digital portable applications. Targeted low power A/D converters are thus required to improve the overall power consumption and consequently the battery life.

In previous work, a Redundant Signed Digit (RSD) algorithmic converter was developed at IMT [Heub96]. It features 13 bits of dynamic range and its power consumption at ± 1.25 V and 16 kHz is less than 50 μW . Nevertheless, due to capacitor mismatch and 'low' gain operational amplifier the maximum SNR is only of about 60 dB. This 'relative precision' (error proportional to input signal) is well suited for audio appli-

however a drawback for applications such as instrumentation.

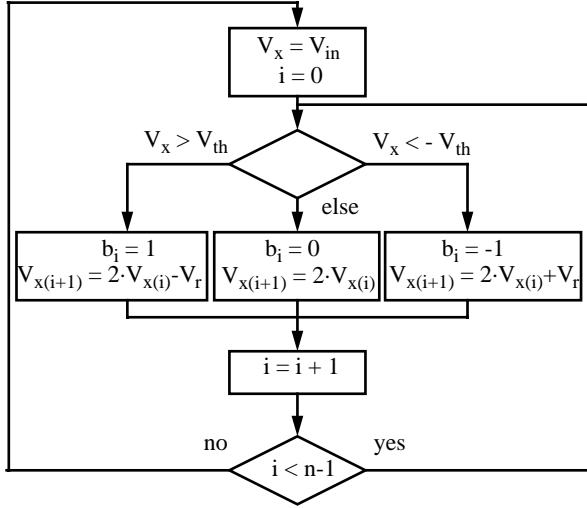
The non-linearity or lower SNR results from imprecise doubling operations. Consequently each bit b_i computed by the RSD converter has a $(2+\epsilon)^{-i}$ weight, while in an ideal case the weight would have been 2^{-i} . A simple base translation can thus be performed to obtain the correct word and achieve a linear characteristic over the whole input range.

This paper focuses on the implementation of the above correction in a low voltage 2 μm CMOS technology. Section 2 describes the relative precision RSD converter as developed by A. Heubi. Section 3 presents the base translation algorithm and its implementation. Finally, considered further works are presented in section 4 while section 5 concludes the discussion.

2 13-bit "Relative precision" RSD Converter

The Redundant Signed Digit (RSD) converter, whose algorithm is given in figure 1, was first published in [Gin92].

The original feature is to compare to both a negative and positive value. The advantage is that the very accurate comparator required by traditional algorithmic conversion (precision better than 1/2 LSB) can be replaced by two very simple comparators in which inaccuracies can reach half the reference voltage V_r regardless of the number of bits.



V_{in} : input voltage V_r : reference voltage
 $V_{x(i)}$: intermediate voltage b_i : output bits
 V_{th} : threshold voltage n : number of bits

FIGURE 1. Cyclic RSD converter algorithm

With the RSD-algorithm, if a “relative precision” (output error proportional to input signal) can be tolerated, it is not necessary to compensate the capacitor mismatch, nor to have very high gain operational amplifier and finally the reference does not have to be very accurate. The result of these imperfections only affect the maximum achievable signal-to-noise ratio as one can see in the simulation presented in figure 2. The latter shows the capacitor mismatch effect on the signal to noise ratio for a 1 kHz sinusoidal input signal and a sampling frequency of 16 kHz.

The use of RSD-algorithm has some other advantages listed below:

- active element offset gives only a digital offset (can be easily compensated if needed)
- switch charge injection has the same effect
- active element saturation causes digital saturation (no distortion for low level input signals)

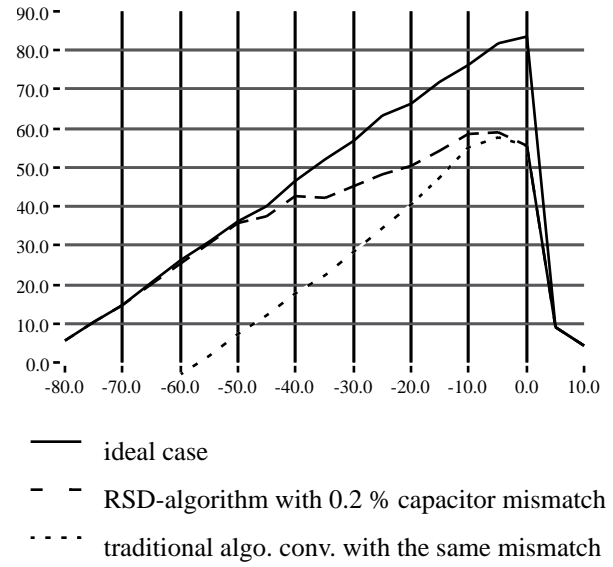


FIGURE 2. Signal-to-noise ratio as a function of the input signal level for 14 bits

- capacitors non-linearity only limits the maximal signal-to-noise ratio
- the quality of the reference has the same effect

The operations of the algorithm are performed with switched capacitors. The input signal is sampled at the beginning of the conversion cycle and thus no sample & hold is required. The large tolerance comparators are realized by simple strobed cross-coupled inverters. Finally, the RDS output is converted into a two’s complement representation.

The circuit was implemented by A. Heubi in the ALP2 LV double metal, double poly, 2 μ m CMOS technology from EM Microelectronic-Marin SA in Switzerland. The analog part is full custom layout while the digital part is realised using CSEL_LIB, a low power standard cell library developed at the CSEM SA, Neuchâtel, Switzerland. Additional components have been added to the test circuit (figure 3), particularly a D/A with the same relative precision as the A/D. The circuit is thoroughly presented in [Heu96].

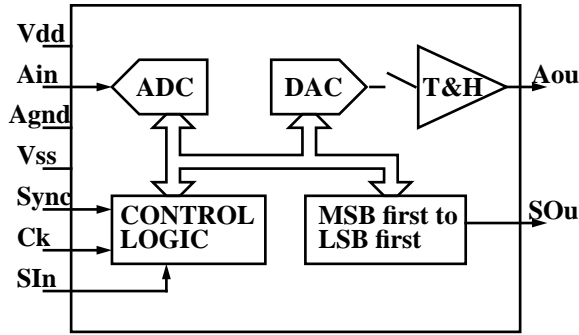


FIGURE 3. Bloc diagramm of the A/D and D/A chip

The whole circuit has an area of 4 mm^2 ($\approx 5900 \text{ sq-mil}$) including pads and the core an area of about 0.8 mm^2 . The analog part of the A/D is only $0,06 \text{ mm}^2$ including the polarization circuit.

Two signals “ck” and “sync” are used to control the sampling frequency and the number of bits (up to 15 bits word length supported by internal register). Thanks to the serial ports, the number of pins can be limited to 9.

The circuit has been tested on a PC based environment equipped with a data acquisition card from National Instruments (AT-MIO-16E-1) driven with the LabVIEW software.

The measured power consumption at $\pm 1.2 \text{ V}$ power supply and 16 kHz sampling frequency was:

- $13 \mu\text{A}$ for the A/D converter ($31 \mu\text{W}$)
- $32 \mu\text{A}$ for the D/A converter and the track & hold circuit ($75 \mu\text{W}$)
- $7 \mu\text{A}$ for the logic part ($17 \mu\text{W}$)
- $125 \mu\text{W}$ total power dissipation
- $< 1 \mu\text{A}$ in stand-by mode

The signal-to-noise ratios were measured with a 1 kHz sinusoidal input sampled at 16 kHz and $\pm 1.2 \text{ V}$ power supply. The input was generated by the 12 bits D/A converter of the acquisition card, with 64 kHz sam-

pling rate and variable reference voltage to reach the dynamic range.

The measurements (figure 4) of the Total Harmonic Distortion (THD) as well as THD + noise shows a saturation at about 60 dB SNR for large input levels and a linear behaviour for low input levels. This fits the simulations presented in figure 2.

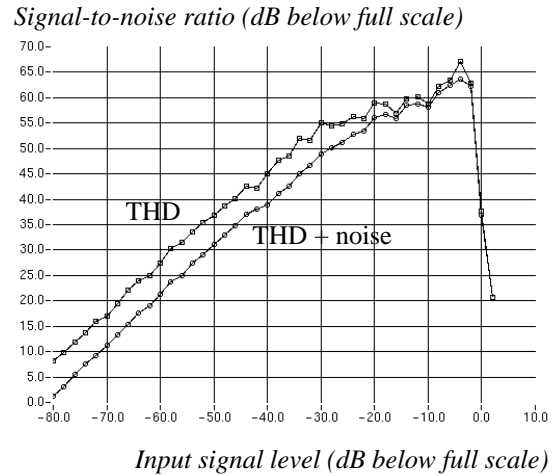


FIGURE 4. Signal to noise ratio versus input signal level

Finally figure5 shows the AD converter’s frequency response to a 1 kHz sinusoidal signal at -25 dB below full scale.

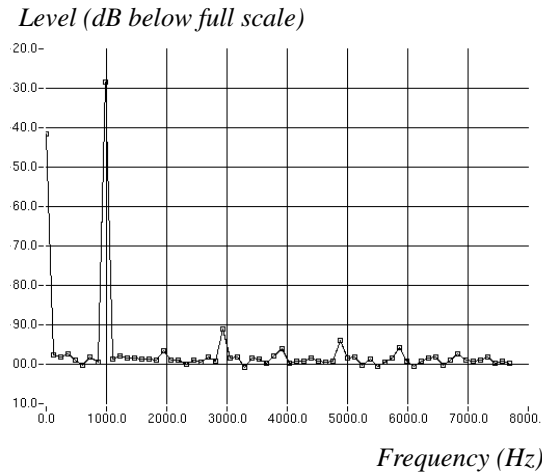


FIGURE 5. Frequency response to a 1 kHz input signal at -25 dB below full scale

It should be noticed that the measurements of this section give worst case results due to the limitation of the sinusoidal source (12 bits DAC).

The circuit works at up to 36 kHz at ± 1 V and 57 kHz at ± 2.5 V. A PSRR of 53 dB was measured when modulating the positive power supply with a 1 kHz sine.

3 Improvements

The A/D converter presented in the former paragraph has a dynamic of 13-14 bits and a maximum signal to noise ratio of 60 dB. It is thus well suited for applications requiring high dynamic range and where relative precision is sufficient. This is typically the case in audio applications where masking effects take place [Schr79]. Nevertheless, the 60 dB SNR is a drawback which should be improved to enlarge the possible use of the RSD converter.

The capacitor mismatch and ‘not so high’ gain amplifier affect the doubling factor. As a result, each computed bit b_i does not have a 2^{-i} weight (ideal case) but rather a $(2+e)^{-i}$ weight. It is thus necessary to perform a ‘base translation’ to transform the ‘base $2+e$ ’ word into a ‘base 2’ word. This means that each bit b_i computed by the RSD converter must be multiplied by $(2+e)^{-i}$. To simplify the implementation, the first and second term of the corresponding Taylor development (equation 3.1) are used.

$$(2+e)^{-i} = 2^{-i} + (i \cdot e) / 2^{(i+1)} \quad (3.1)$$

This is easily performed by the algorithm given in figure 6 where register 1 is initialized to $e/2$ and register 2 to one. Register 3 can be initialized to zero or, even better, to the proper value to ensure offset compensation.

The offset is easily measured by using a 0V input signal. Once this value is known, the doubling error e is obtained in two clock cycles [Lee93].

To obtain 14 correct bits at the output, all the computations must be performed on 18 decimal bit using a two’s complement repre-

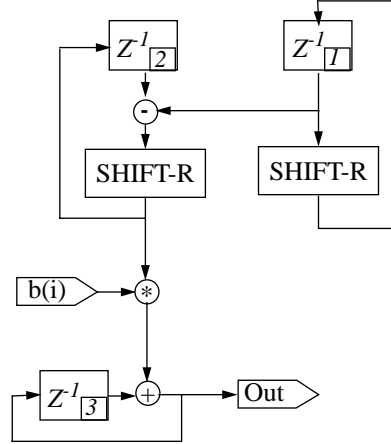


FIGURE 6. Flow graph of base translation

sentation. As a consequence, register 3 is 19 bits long while register 2 needs one extra bit to code the initial value 1.0. Since the maximum doubling error can reasonably be assumed smaller than 1%, register 1 is made of only 12 bit and is sign extended to properly perform the subtraction. The 19 bits computed by the adder are rounded and result in the 14 bit output.

The above configuration leads to an average absolute error of 0.4 LSB. The maximum error is 1 LSB with a probability of 0.05%.

The algorithm has been implemented (up to layout) in the ALP2 LV double metal, double poly, 2 μ m CMOS technology using the low power standard cell library CSEL_LIB from CSEM. It uses 191 standard cells (or 3267 transistors) resulting in a 1.15 mm² area. The simulated power consumption, at 1.25V and with a RSD cyclic converter delivering 14 bits at 16 kHz, is 8.5 μ W.

4 Further work

The above numbers are promising since the correction of the non-linearity consumes less than 10 μ W. Nevertheless, the hardware necessary to store the initialization values has not been considered yet. To determine the best solution, the calibration strategy must first be defined. Indeed, to keep the

power consumption as low as possible, the final implementation will differ based on whether the calibration is performed a single time (at the foundry, during the functional test) or at any time (during normal utilization). In order to decide which of those two strategies is best, some data regarding the sensitivity of the doubling error towards external parameters (such as temperature) should be collected. A MPW integration, with all the hardware necessary to easily measure, store and modify the initialization values, is thus foreseen in 1997.

5 Conclusion

The 13-bit ‘relative precision’ RSD cyclic ADC which has been developed at IMT is very well suited for audio applications where masking effects tolerate a 60 SNR only. Nevertheless, applications such as instrumentation demand that the non linearity and offset are corrected.

Since the non linearity results in a doubling error a simple ‘base translation’ can be computed. The offset is then subtracted and the correct converted output obtained.

The implementation of the corresponding algorithm in a low voltage 2 μm technology resulted in a area of 1.15mm² and a power consumption, for a 16 kHz converter, of 8.5 μW . This number does not consider the necessary hardware to store the initialization value.

Once the calibration strategy is defined, a MPW will be realized and thoroughly tested. The expected result is a 13-bit linear ADC consuming about 60 μW at 16 kHz sampling frequency and ± 1.25 power supply.

6 References

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Patent pending for relative precision cyclic RSD ADC:

Registration number: 95 10 174

Title: “Dispositif de traitement numérique d’un signal analogique devant être restitué sous forme analogique”

Registered at: “Institut National de la Propriété Industrielle”, Paris, France

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