

## Micro Power High-Resolution A/D Converter

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### Abstract

Due to their low number of biased components, algorithmic A/D converters are often used in low power implementations. This paper describes an algorithm developed at the Institute of Microtechnology (IMT) which allows extending performances of cyclic RSD converters, without greatly impairing its benefits (reduced silicon area, low consumption). To achieve a Total Harmonic Distortion + Noise (THD+N) of 14 bits as well as a Dynamic Range (DR) of 16 bits, this algorithm combines oversampling, filtering, pre- and post-processing. Results of such converter are discussed and widely presented.

### 1. Introduction

Nowadays an increasing number of consumer electronic products are targeted to be portable. However, this portability feature has two major constraints: a reduced size and weight and a supply independence using batteries. These cells have to power the whole product, therefore to extend the functioning duration a low power consumption of each component is mandatory. On the digital side, thanks to technology improvements and design tuning [6], many progresses in the reduction of the current consumption have been accomplished. However, on the analog side, and in particular in A/D and D/A converter, the power consumption still

needs to be reduced and here the technology betterment are not so helpful. Medium resolution micro power A/D and D/A converters have already been developed [1]. However, due to technological limitations (capacitor mismatch, finite gain...) their resolution and dynamic cannot be easily further increased. Overcoming these limitations, a new algorithm, which combines low power and high resolution, has been developed to fulfil the needs of portable instrumentation applications [5], (diving computers, embedded measurement systems, etc), which typically require devices having a 16-bit dynamic range.

This paper presents in Chapter 2 the targeted A/D performances. Chapter 3 explains the basis of the conversion principle and the limitation due to noise. The method used to overcome the noise problem is specifically presented in Chapter 4. Chapter 5 gives the whole conversion algorithm. Chapter 6 exposes some post processing improvements. Whereas integration results are given in Chapter 7. Finally, Chapter 8 draws the conclusions.

### 2. Problem Statement

The objective of this project is to extend the capabilities of micro power A/D, the final aim is design an A/D converter having a THD+N [4] of 84dB (14 bits) featuring a dynamic range of 16 bits. These

specifications correspond to a non-absolute converter (error dependant on the input), that features a linear transfer function. To be audio compliant, the targeted bandwidth is 25kHz, resulting in a sampling rate of 50kHz. Since consumer portable applications are aimed, the device should consume no more than 150 $\mu$ W and be as small as possible.

### 3. Principle of Conversion

For medium (10-14 bits) resolution, the use of cyclic algorithm converters seems particularly interesting in terms of power consumption. Thanks to their multi-pass approach, these converters use only a small number of biased elements, and hence consume less current. Unfortunately, the direct implementation of such A/D requires high precision comparators [2] (inaccuracy smaller than half LSB), which leads to large bias currents. To overcome this accuracy limit a comparators'offset tolerant algorithm called Redundant Signed Digit (RSD) [3] can be used. Such a RSD converter has been implemented, under the code name Adam [1] and the chips featured a 13-bit dynamic range, a power consumption of 48  $\mu$ W at 16 kHz with a 2.5 V voltage supply, and a THD+N of about 63 dB. The latter is due to circuit non-idealities and cannot be improved by simply increasing the number of cycles. These non-idealities can be classified as follows: The systematic ones (e.g. offset, saturation, matching accuracy, ...) which impair mainly the Total Harmonic Distortion (THD)[4] and are similar at each conversion and secondly the non-systematic (noise on switched capacitors, noise on resistor, ..) which obviously impair the Signal to Noise Ratio (SNR)[4]. Due to their repetitiveness, errors due to the systematic imperfections can be modelled and correct thereafter though a suitable digital processing. On the contrary, the non-systematic errors cannot be compensated later on, so they have to

be minimised following two approach: increase the bias current, which is not the best way to keep a low power consumption, or use algorithm based on the statistical properties of the noise.

## 4. Algorithmic Noise Reduction

### 4.1 The Method

In order to reduce the noise effect, some algorithm improvements can be done. The most common way to implement these is to use the non-correlated property of the noise. To exploit this, different option can be taken and one of them is the input sample integration. The principle is to oversample the input signal and to sum all the analog samples before digitised them. This addition performs noise shaping through filter and decimation. Furthermore, when implemented in complement of an n-clock converter, the main advantage of executing this summation in analog rather than in digital, is to greatly reduce the number of clock events needed to complete the conversion. Table 1 shows the amount of clock cycles needed, for both (analog & digital) integration techniques, to perform the whole conversion, (assuming an internal n=12 clock cycles A/D).

# int. "m"	1	2	4	8	16	32
analog	12	13	15	19	25	43
digital	12	24	48	96	192	384

Table 1: Effect of the Number of integration with a n=12 ADC converter

Since there are technical limitations on the clock speed, the input integration seems more appropriate for ADC realizations.

### 4.2 The Effect

The noise can be considered as equally spread over the whole spectrum of the sampled signal. An "o" factor oversampling allows to extend this spectrum which then lowers the noise on the useful bandwidth (0 to Fc). Afterwards, the summation of the samples performs a

natural filtering and decimation function, which leads to noise reduction. Since this system is aimed to be implemented, coupled with an n-cycle converter, an integration of m-samples leads to an oversampling “o” and decimating “d” factors equals to “m+n”. This noise reduction is better than in the case of a digital output integration, where these factors are lower [5] (i.e. “o=d=m”). The improvements in SNR that can be obtained using this method are summarised in Table 2.

Integration Factor m	2	4	8	16	32	128
Gain using Input integration. [dB]	3.3	5.9	8.6	10.9	13.1	17.8

Table 2: Gain in SNR for a n=12 cyclic converter

However, in this method, to guarantee proper conversion the accumulated value must remain within the input range of the following A/D. As a consequence, the overall system input Dynamic Range is reduced by “m” compared to original one of the n-cycle converter. This is a major drawback.

### 4.3 Distortion in the Bandwidth

The filtering effects of the input integration not only affect the noise but also modify the useful bandwidth (0 to  $F_c$ ). The Figure 1 shows the distortion that is applied on the sampled signal.

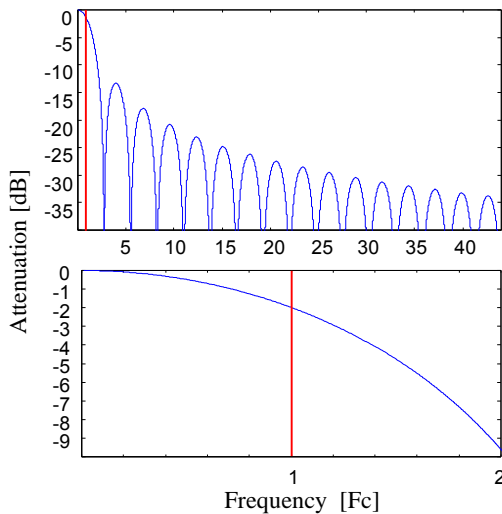


Figure 1: Input integration filter shape for m=32 and n=12

The shape of this filter, due to the summing, is a function of the number of integrations. However, the bandwidth on which this function is applied is proportional of the oversampling “o” factor. Since “m” is different than “o” in the input integration, it is not possible to create a unique output correction, which is valid for all “m” values. Nevertheless, for a given “m”, a specific filter can be applied at the output to reduce the deformation. A specific case is discussed in chapter 6.

## 5. IMT Conversion algorithm

To extend the precision while keeping a “full” input dynamic range and maintaining a reasonable output sampling frequency the conversion system uses a multi-stage technique as shown in Figure 2. The first stage is an input integrator, which is coupled with a coarse converter. This method allows both calculating the firsts MSB’s and avoiding the supply saturation problem in the integrator. After a given number of accumulation-subtraction steps, the residue is fed to a second converter that computes the remaining bits.

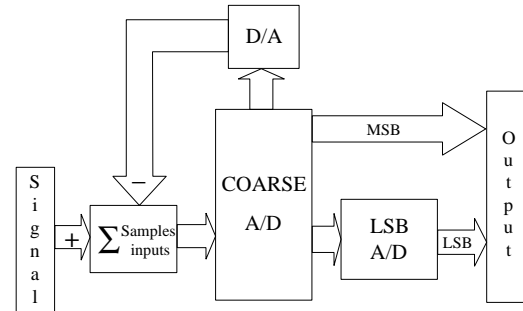


Figure 2: Principle of mixed converter using a feedback structure

Having in mind the power consumption and area requirements a new algorithm, which implements such a multi-stage converter has been developed. Its flow graph is given in Figure 3. In this algorithm, the coarse quantifier, which calculates the MSB’s, works similarly to a cyclic converter. However, instead of doubling the sample values at each loop,

the circuit performs an accumulation of the input samples (i.e.  $N$  loops are replaced by  $2^N$  accumulations). This has two main benefits: firstly since an input integration is performed, the noise level is lowered and secondly, the mismatch effect is virtually eliminated since a feed-only scheme is used instead of a recycling one. The consequence is that the numerical systematic error correction algorithm is not required anymore. Therefore, this results again in smaller size and power consumption. The second converter is implemented as a standard RSD A/D [1],[3].

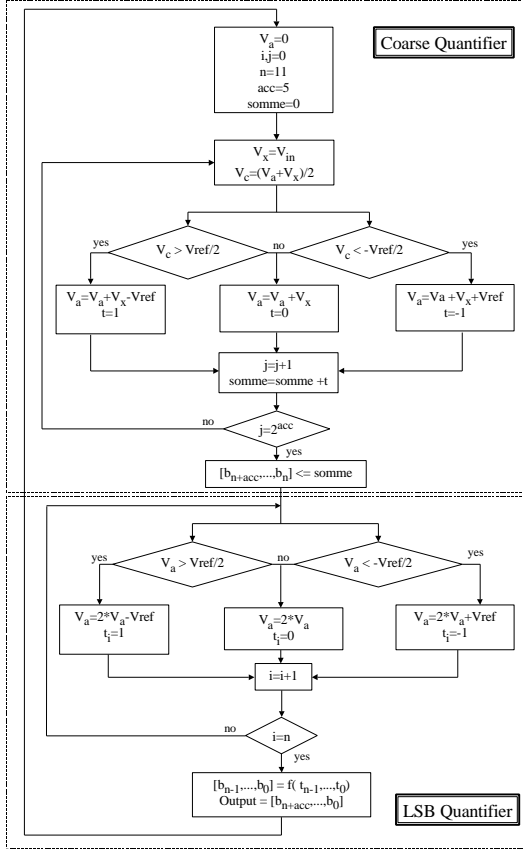


Figure 3: IMT algorithm

A close look at both the input integration and RSD part shows that some of the functions/steps are equivalent. This is a significant advantage since the circuit realisation can be simplified and only a single A/D is used. The latter is a modified RSD that can be transformed into the integration stage by simply changing the

control signals and configuration settings. The obvious advantage of using a single hardware for both functions is to reduce the overall chip size as well as the power consumption. Furthermore, by using the same hardware, the transmission of residue ( $V_a$ ) is no more required. So the LSB conversion is done on almost the best-amplified value possible, which helps to extend the overall system precision.

## 6. Output Distortion Correction

Since the new converter algorithm implements an input integration, a modification of the useful bandwidth (0 to  $F_c$ ) is effective. To reduce this distortion, a digital compensation could be applied at the output though filtering. Keeping in mind the low power, small area requirements of the targeted circuit, the following filter can be used.

$$H(z) = \frac{1}{(1-a) + az^{-1}}$$

Furthermore, in order to lower the needs of multiplier,  $\alpha$  is been taken as a negative power of two. (e.g.:  $n=12, m=32, \alpha=0.25$ )

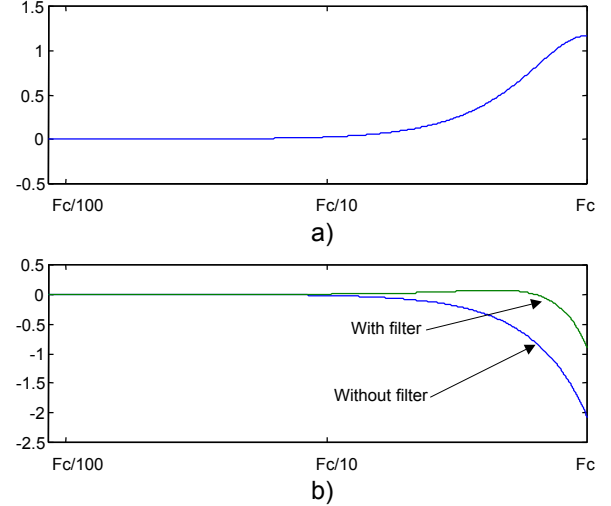


Figure 4: a) response of the filter  
b) effect on the A/D output

This filter allows extending the bandpass by a factor two, dividing the end-of-band attenuation by more than two, whereas it only inserts a small ripple of less than 0.1 dB.

## 7. Chip Implementation

To demonstrate the robustness of the proposed algorithm a first chip has been realised in a  $1\mu\text{m}$ , 2 metals, 2 poly technology, under the code name Sono [5]. However, the tests feature performances below those expected (THD+N=75 dB, THD=80 dB, SNR=82 dB, Power=130 $\mu\text{W}$  @fs = 22kHz & 2.5V). A new chip (SonoII) targeted to get better results, has been designed and is about to be manufactured. On the analog side, several issues have been reconsidered and on the digital side, thanks to a technology change (0.5 $\mu\text{m}$ , 3 metals, 2 poly) more output processing has been included, without greatly impairing the size (0.7mm<sup>2</sup>).

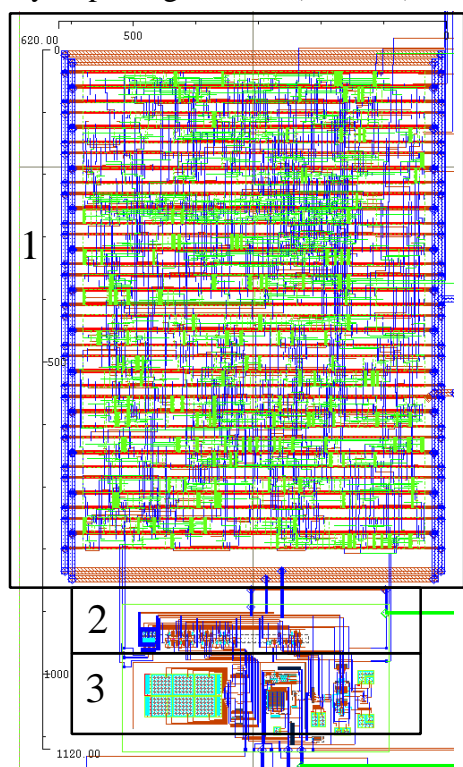


Figure 5: SonoII-Chip Snapshot

In the chip snapshot of the Figure 5, three sections can be identified. The upper section {1}, done in standard digital cells, contains most of digital circuitry (the ternary-binary decoding, the control sequences, output processing). Because it has to deal with different voltage level, complementary clock creation and delays,

the second section {2}, which is also digital, is only constituted of hand-made logical cells. This technique permits to reach a more accurate characterisation than while using standard cells. The last section {3} is made of size- and position-optimised analog components (transistors, capacitors, etc). Furthermore, due to its particular sensitivity to noise, this part possesses multiple shields: One is protecting from the part {1} which is clock at 2MHz (@fs=48kHz) and a second from all glitches which are produced by the switches of part {2}.

## 8. Conclusion

This paper presents a new conversion concept that uses a multistage approach. A cyclic RSD algorithm combined with noise-shaping technology has shown to be a good candidate for lowest power ADC design. The first design, which has been integrated, has shown on silicon good performance in terms of dynamic range (16 bit) and SNR (82 dB) besides a very low power consumption (130  $\mu\text{W}$ ) and smallest chip area (0.5 mm<sup>2</sup>). However, in order to improve these performances, a second design, which included more output processing, is about to be realised.

## References

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