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INSTITUT DE MICROTECHNIQUE

Design of Low Phase Noise Low Power CMOS Phase Locked Loops

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ACCEPTÉ SUR PROPOSITION DU JURY

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IMPRIMATUR POUR LA THESE

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Abstract

Phase locked loop (PLL) is one of the most critical devices in modern electronic systems. PLLs are widely used as clock generator or frequency synthesis in communication systems, computers, radio and other electronic applications. Phase noise represents the phase variations of a PLL output signal and is the most important characteristic of PLLs because it reflects the stability of PLL systems. Low power consumption is always desired for any electronic products today. CMOS technology is the most common process to make integrated-circuits. In this thesis, we focus on the design of low phase noise and low power CMOS PLL integrated circuits. Understanding phase noise generation mechanism in PLLs is the basis for low phase noise design. Therefore, phase noise contributed by each components in PLLs are studied at first. Voltage controlled oscillator (VCO) is a critical component and the main noise contributor in a PLL. A detailed phase noise analysis for LC-tank based VCO and ring oscillator VCO, which are the most implemented VCO types, is performed. Then, the techniques for designing low phase noise and low power VCO and PLL are studied.

Two PLL prototype chips are designed and fabricated in CMOS technology to demonstrate the design techniques for low phase noise and low power PLL. The first PLL is applied as clock generator in a LVDS transmitter and implemented into the AMS 0.35 μm CMOS process technology. A novel low noise charge-pump is implemented in this PLL to achieve low phase jitter together with a VCO based on fully differential ring oscillator, a PFD based on dynamic logic circuit, and a passive loop filter. The measurement results of the PLL chip exhibit excellent phase jitter-power consumption product and wide lock range. The second PLL chip is used in an atomic clock system to provide a reference frequency of 1.5 GHz. The test chip is implemented into

the UMC 0.18 μm process technology. A PMOS-only differential VCO based on LC-tank oscillator is implemented to achieve low phase noise. The VCO has a very low fine tuning gain to minimize phase noise and a high coarse tuning gain to compensate the frequency offset due to process variations.

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Chapter 1

Introduction

A phase-locked loop (PLL) is an electronic feedback system that generates a signal, the phase of which is locked to the phase of an input reference signal. PLLs are widely used in radio, telecommunication, computer and other electronic systems. The important applications of PLLs include:

- Clock generation. Most of the electronic systems (including processors) operate at hundreds of megahertz. Typically, the clocks of these systems are generated by PLLs, which multiply a lower frequency reference clock (usually < 100 MHz and generated by crystal oscillators) up to the required operating frequency. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just a few tenths of megahertz.
- Frequency synthesis. In telecommunication systems, such as wireless communication and satellite communication systems, PLLs are used to generate the radio frequency (RF) signals required for both up-conversion and down-conversion in transceivers.
- Clock recovery. Some data streams, especially high-speed serial data streams (such as the raw data stream from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL.
- Deskewing. If a clock is sent in parallel with data for data sampling, the clock must be received and amplified before it can drive flip-flops which sample the data. There will be a finite, and process, voltage, and

temperature dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is using a deskew PLL on the receiver side, so that the clock at each sampling flip-flop is phase-matched to the received clock.

In this thesis work, we focus on the design of CMOS integrated PLLs for clock generation and frequency synthesis. Two prototypes of CMOS PLLs are designed and integrated. The first one is used as an clock generator in a high speed Low Voltage Differential Signalling (LVDS) transmitter; the second one is employed as an frequency synthesizer in an atomic clock system.

1.1 Motivation and Research Objectives

Due to their crucial role in a widely variety of modern applications, such as high speed digital systems and wireless communications, PLLs have been the subject of extensive research in recent years. The most critical performance specifications for an PLL are phase noise and power consumption.

In high speed serial data applications, the clock is usually generated by multiplying the references clock with a PLL. The phase noise of the PLL is directly related to the clock jitter, which is a discrete quantity and means the phase noise at the crossing time. Jitter causes errors when the timing of a signal transition fluctuates horizontally across the sampling point. Large jitter reduces the signal-to-noise ratio (SNR) and results in high bit-error-ratio (BER). In communication systems, the local oscillator (LO) is typically implemented as a PLL. The phase noise of the LO limits the ability to detect a weak signal in the presence of a signal in an adjacent channel. Therefore, PLL designs are mostly focused on achieving low phase noise.

Power consumption is always an important specification for all electronic devices and products. Low power consumption is environment-friendly. The use of portable electronic products has been rapidly increased in the last few years, low power consumption becomes even more important for portable electronic products in order to have a long battery life. When PLLs are embedded in low power systems, they must be designed for low power consumption.

Complementary Metal-Oxide Semiconductor (CMOS) is a major and the cheapest technology for integrated circuits. It is commonly used in microprocessors, microcontrollers, static RAM, and other digital circuits. CMOS tech-

nology is also used for a wide variety of analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. It is always desired to integrate the whole system on one chip, referred as System-On-Chip (SOC,) which includes both digital and analog parts in order to optimise cost and power consumption.

Motivated by the above trends, the main goal of this thesis is to study and practice measures for designing low phase noise, low power PLLs in CMOS technology.

This thesis work is based on two research projects. The first project was to design a LVDS transmitter for Camera Link communication interface embedded in a CMOS camera system. The core of the LVDS transmitter is a PLL that generates a clock with a 7 times frequency of the input reference clock. The PLL has to be designed for low jitter, wide lock range , low power consumption and small area. According to these requirements, a CMOS PLL based on ring oscillator was designed. The prototype PLL was integrated with AMS $0.35 - \mu m$ mixed-signal CMOS process.

The second project was to design a 1.5 GHz frequency synthesizer for an atomic clock system. The project requires to design a PLL with very low phase noise (< 90 dBc/Hz at 10 kHz), ultra high frequency resolution (< 1 Hz), and low power consumption (< 15 mW). A Σ-Δ PLL with LC VCO was designed for achieving the specifications. LC VCO has lower phase noise than the VCOs based on ring oscillator. Σ-Δ frequency divider allows high frequency resolution. The prototype PLL was integrated with UMC $0.18 - \mu m$ RF CMOS process.

1.2 Organization of the thesis

Chapter 1 gives an introduction to this thesis. Chapter 2 presents an overview of the fundamental theory of PLL from system level. Chapter 3 focuses on circuit design technique of important PLL components, such as phase-frequency detector, charge pump, loop filter, and frequency divider. The most important and complicated component in a PLL is the VCO. Chapter 4 presents the two most used VCO types, LC-tank VCOs and ring oscillator VCOs. Chapter 5 investigates the phase noise theories for VCOs and PLLs. Chapter 6 studies the low phase noise and the low power design techniques for VCOs and PLLs. Chapter 7 presents the design and implementations of two prototype PLL chips. A summary of the results presented in this thesis as well as sug-

gestions for future work are offered in Chapter 8.

Chapter 2

PLL Fundamental

The phase-locked loop (PLL) is the most important technique for the generation of clock and frequency signals. It allows the generation of variable output frequency with the same stability than a crystal oscillator by means of feedback. More precisely, a PLL synchronizes the output phase and frequency of a controllable oscillator to match the output phase and frequency of a reference oscillator. Ideally, the steady-state condition will show a zero difference in phase and frequency between the controlled oscillator output and the reference output. In this chapter, we will introduce the working principles of PLL, PLL transfer function and stability analysis, PLL order and type, the difference between Integer-N PLL and fractional-N PLL, and the PLL modelling for system-level simulation.

2.1 PLL working principles

The schematic block diagram of a PLL is shown in Figure 2.1. It consists of four basic functional blocks:

1. Voltage-controlled oscillator (VCO). The output frequency of this devices is a monotonic increasing function of its input voltage.
2. Phase detector (PD). The PD compares a periodic input signal (reference signal, normally a sine or square wave) with the frequency divider output signal. The PD output voltage is proportional to the phase difference between the two signals.

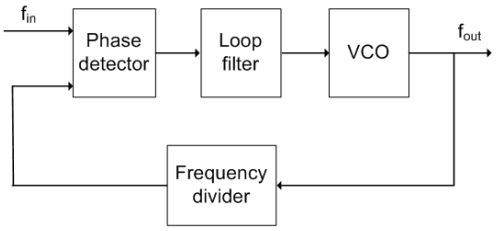


Figure 2.1: An basic block diagram of PLL.

3. Loop filter (LF). This is a lowpass filter that smoothes the PD output signal and applies it to the VCO input.
4. Frequency divider (FD). The output of the frequency divider is a signal with a frequency equal to the VCO output frequency divided by a division factor N.

The PLL is a servo-controlled system. If its loop gain is high enough and the loop is stable, the system will reach a stable condition where two PD inputs have the same phase and thus the same frequency (the angular frequency is the derivative of the phase with respect to time). In this condition, the output frequency equals the input frequency multiplied by N.

$$f_{out} = N \cdot f_{in} \tag{2.1}$$

When the frequency division factor N is modified, the output frequency will be modified accordingly. If the reference signal is a very stable one, the output frequency will become very stable as well.

2.2 PLL transfer functions and stability analysis

The block diagram of a PLL for Laplace transform in phase domain is shown in Figure 2.2, where K_d is the gain of the PD, F(s) is the transferfunction of the loop filter, and K_v is the gain of the VCO. Thus, the feed forward transfer function in the phase domain can be expressed as:

$$G(s) = \frac{K_d K_v F(s)}{s} \tag{2.2}$$

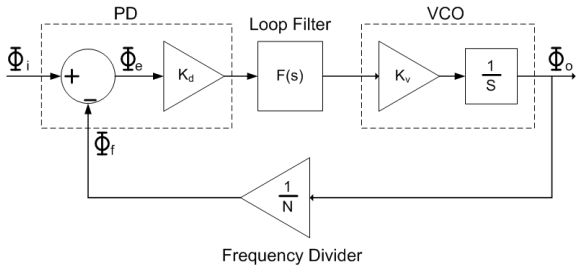


Figure 2.2: PLL phase domain block diagram in Laplace transformation.

The feedback transfer function is:

$$H(s) = \frac{1}{N} \tag{2.3}$$

The closed-loop transfer function is:

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{G(s)}{1 + H(s)G(s)} = \frac{\frac{K_d K_v F(s)}{s}}{1 + \frac{K_d K_v F(s)}{Ns}} \tag{2.4}$$

The PLL phase error response is also of interest. The phase error is defined as:

$$\Phi_e(s) = \Phi_i(s) - \Phi_f(s) = \frac{1}{1 + G(s)H(s)}\Phi_i(s) \tag{2.5}$$

The closed-loop stability analysis can be made by analyzing the open-loop frequency response G(s). For this purpose the open-loop gain amplitude and phase gain calculation are needed. From feedback control system theory, we know that a system is unstable if the phase shift ϕ_0 at the frequency where the open-loop gain has unitary amplitude, f_0, equals π (180 degrees).

The open-loop gain G(s) is the product of three factors:

1. Constant factor $\frac{K_d K_v}{N}$.
2. Lowpass function F(s).
3. Integrator transfer function $\frac{1}{s}$

The loop filter frequency response can be written as:

$$F(f) = \frac{\sum_{k=0}^{m} A_k (j2\pi f^k)}{\sum_{k=0}^{n} B_k (j2\pi f^k)} \tag{2.6}$$

Its low pass characteristic means that F(f) has to satisfy the conditions:

$$\lim_{f \to 0} |F(j2\pi f)| > 0 \tag{2.7}$$

and

$$\lim_{f \to \infty} |F(j2\pi f)| \leq |F(j2\pi f)|_{f=0} \tag{2.8}$$

Therefore, we can obtain the following conclusions:

$$A_0 \neq 0 \tag{2.9}$$

$$n \geq m \tag{2.10}$$

At zero frequency, the open-loop gain is infinite because the loop filter term is finite and the integrator frequency response becomes infinite. At infinite frequency, the open-loop gain is zero because the loop filter term is finite and the integrator term is zero. So the amplitude of the open-loop gain ranges from infinity (at zero) to zero (at very high frequencies). Thus there is at least one frequency value that makes the open-loop gain to have unitary amplitude. The phase of the open-loop gain is the sum of the phases of the previous listed three terms. The constant factor's phase is zero, the loop filter phase is a delay variable with frequency, and the integrator phase is a constant $-\frac{\pi}{2}$ over frequency. Therefore, the phase of the loop filter determines the phase margin of the PLL loop. A zero-order loop filter has less than a $-\frac{\pi}{2}$ phase shift, so the total open-loop phase shift is less than π and the loop is always stable. High-order filters are not unconditionally stable. Bode and Nyquist diagrams are normally used to check the phase margin.

2.3 PLL order and type

The PLL order is defined by the number of poles of the closed-loop transfer function. From the closed-loop transfer function (2.4), we see that the PLL order equals the loop filter order plus one.

Another PLL classification is based on the value of the steady state phase error. This error depends on the number of integrator in the loop. According to classical control theory, the number of integrator determines the type of the system. This means that the type of a PLL equals the number of poles of its open-loop gain located at the origin. From the open-loop gain equation (2.2),

we can find that the open-loop gain has at least one pole given by the integrator factor $\frac{1}{s}$ due to the inherent integration property of VCO. The loop filter can have at most one additional pole and can't have more, because circuit theory tells us that one network with two coincident poles on the imaginary axis of variables (including zero) is unstable. Summarizing, the open-loop transfer function of PLL can have one or two poles depending on whether the loop filter DC gain is finite or infinite. The number of poles of the open-loop transfer function is the type of the PLL (1 or 2).

Various inputs can be applied to a PLL system. Typically, these include step, velocity, and acceleration. The response of type 1 and 2 PLL systems will be examined with the various inputs. As expressed in equation (2.5), $\Phi_e(s)$ represents the phase error that exist in the phase detector between the incoming reference signal $\Phi_i(s)$ and the feedback $\Phi_f(s) = \Phi_o(s)/N$. In evaluating a system, $\Phi_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum or satisfactory. The transient response is a function of loop stability. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. According to the final value theorem, we have:

$$\lim_{t\to 0}(\Phi_e(t)) = \lim_{s\to 0}(s\Phi_e(s)) \tag{2.11}$$

The input signal $\Phi_i(s)$ is characterized as follows:

$$Step : \Phi_i(s) = \frac{C_p}{s} \tag{2.12}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by a radians:

$$Step\,velocity : \Phi_i(s) = \frac{C_v}{s^2} \tag{2.13}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency step to the system:

$$Step\,acceleration : \Phi_i(s) = \frac{2C_a}{s^3} \tag{2.14}$$

where C_a is the magnitude of the frequency rate of change in radians per square of second. This means a time variant frequency input.

A first order PLL means that the loop has no filter. This is the simplest case of a PLL. The first order PLL is rarely realized in practice. Therefore, we will not discuss it in the following.

Step	0
Step velocity	Constant
Step acceleration	Constantly increasing

Table 2.1: Steady state phase errors of a type-I second-order PLL for various input types.

2.3.1 Type-I second-order PLL

Assuming a first-order low-pass loop filter with a transfer function as:

$$F(s) = \frac{1}{1 + \frac{s}{\omega_1}} \tag{2.15}$$

the open-loop transfer function of a type-I second-order PLL is obtained:

$$G(s)H(s) = \frac{1}{N}\frac{K_v K_d}{s}\frac{\omega_1}{s+\omega_1} = \frac{K}{s(s+\omega_1)} \tag{2.16}$$

where $K = \frac{K_v K_d \omega_1}{N}$.

The final value of phase error for a type-I second-order PLL with a step phase input is found by using equations (2.5) (2.11) and (2.12):

$$\Phi_e(s) = (\frac{1}{1 + \frac{K}{s(s+a)}})(\frac{C_p}{s}) = \frac{(s+a)C_p}{s^2 + as + K} \tag{2.17}$$

$$\Phi_e(t=\infty) = \lim_{s\to 0}(s\frac{(s+a)C_p}{s^2 + as + K}) = 0 \tag{2.18}$$

Thus, the final value of the phase error is zero when a step phase input is applied.

Similarly, applying step velocity and step acceleration inputs into a type-I second-order system and utilizing the final value theorem. Table 2.1 shows the respective steady state phase errors.

The closed-loop transfer function of a type-I second-order PLL can be written as:

$$H(s)|_{cl} = \frac{G(s)}{1 + G(s)H(s)} = \frac{K_d K_v \omega_1}{s^2 + \omega_1 s + \frac{K_d K_v \omega_1}{N}} \tag{2.19}$$

The denominator of the closed-loop transfer function can be rewritten in a familiar form used in control theory, $s^2 + \xi\omega_n s + \omega_n^2$, where ξ is the damping factor and ω_n is the natural frequency. So, we have:

$$H(s) = \frac{\omega_n^2 N}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.20}$$

where

$$\omega_n = \sqrt{\frac{\omega_1 K_d K_v}{N}} \tag{2.21}$$

$$\xi = \frac{1}{2}\sqrt{\frac{\omega_1 N}{K_d K_v}} \tag{2.22}$$

The two poles of the closed-loop system are given by:

$$s_{1,2} = (-\xi \pm \sqrt{\xi^2 - 1})\omega_n \tag{2.23}$$

According to control theory, if $\xi > 1$, both poles are real, the system is overdamped, and the transient response contains two exponentials with time constant $\frac{1}{s_1}$ and $\frac{1}{s_2}$; on the other hand, if $\xi < 1$, the poles are complex and the response to an input frequency step $\Phi_i = \Delta\Phi u(t)$ is equal to [1]

$$\Phi_o(t) = (1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} sin(\omega_n\sqrt{1-\xi^2}t + \theta))\Delta\Phi u(t) \tag{2.24}$$

where $\Phi_o(t)$ denotes the change in the output phase and:

$$\theta = sin^{-1}\sqrt{1-\xi^2} \tag{2.25}$$

The step response contains a sinusoidal component with a frequency $\omega_n\sqrt{1-\xi^2}$ that decays with a time constant $(\xi\omega_n)^{-1}$. Since the frequency and phase are related by a linear operator, $\omega = \frac{d\Phi}{dt}$, the system exhibits the same response if a frequency step is applied to the input and the output frequency is observed.

The settling speed of PLL is of great concern in most applications. Equation (2.24) indicates that the exponential decay determines how fast the output approaches its final value, implying that $\xi\omega_n$ must be maximized. For the type-I second-order PLL studied here, equations (2.21) and (2.22) yield:

$$\xi\omega_n = \frac{1}{2}\omega_1 \tag{2.26}$$

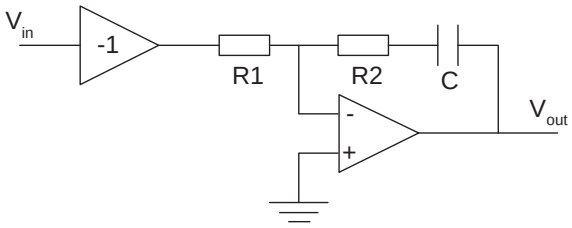


Figure 2.3: A first-order active loop filter.

This result reveals a critical trade-off between the settling speed and the ripple on the VCO control input: the lower ω_1, the greater the suppression of the high-frequency components produced by the phase-detector, but the longer the settling time.

2.3.2 Type-II second-order PLL

To implementing a type-II PLL, we need a filter transfer function with a pole at zero frequency. This means that the ideal DC gain of this filter is infinity. This kind of filter has to be an active filter. If an active filter as shown in Figure 2.3 is used as loop filter, a type-II second-order PLL can be obtained.

The transfer function of this active filter has a pole at zero frequency:

$$F(s) = \frac{1 + sR_2C}{sR_1C} \tag{2.27}$$

The open-loop transfer function of a PLL with this loop filter is expressed as:

$$G(s)H(s) = \frac{1}{N}\frac{K_vK_d}{s}\frac{1 + sR_2C}{sR_1C} = \frac{K(s + \omega_2)}{s^2} \tag{2.28}$$

where $K = \frac{K_vK_dR_2}{NR_1}$, and $\omega_2 = \frac{1}{R_2C}$.

By exploiting the final value theorem, the steady state phase errors of this type 2 second order PLL for various inputs can be analyzed and listed in Table 2.2.

The closed-loop transfer function of this type-II second-order PLL is:

$$H(s)|_{cl} = \frac{G(s)}{1 + G(S)H(S)} = \frac{\frac{K_dK_v}{R_1C}(1 + sR_2C)}{s^2 + \frac{K_dK_vR_2}{NR_1}s + \frac{K_dK_v}{NR_1C}} \tag{2.29}$$

Step	0
Step velocity	0
Step acceleration	Constant

Table 2.2: Steady state phase errors of a type-II second-order PLL for various input types.

This equation can be converted to a familiar form in the control theory:

$$H(s)|_{cl} = \frac{N\omega_n^2(1+\frac{2\xi}{\omega_n}s)}{s^2+2\xi\omega_n s+\omega_n^2} \tag{2.30}$$

where ξ is the damping factor and ω_n is the natural frequency:

$$\xi = \frac{R_2 C}{2}\sqrt{\frac{K_d K_v}{N R_1 C}} \tag{2.31}$$

$$\omega_n = \sqrt{\frac{K_d K_v}{N R_1 C}} \tag{2.32}$$

The natural angular frequency determines the switching the rise and fall time responses, and the damping factor determines the phase margin.

The Bode plot is often used to analyze system stability. For this type-II second-order PLL, the damping factor and natural frequency can be related to the open-loop Bode plot by the following equations [2]:

$$\phi_{PM} = arctan(2\xi\sqrt{2\xi^2+\sqrt{4\xi^4+1}}) \tag{2.33}$$

$$f_{unit\_gain} = \frac{\omega_n}{2\pi}\sqrt{2\xi^2+\sqrt{4\xi^4+1}} \tag{2.34}$$

These equations allow design trade-offs to be evaluated between time response and stability margins. If a PLL is desired to track reference frequency without zero phase error, a type-II PLL is required.

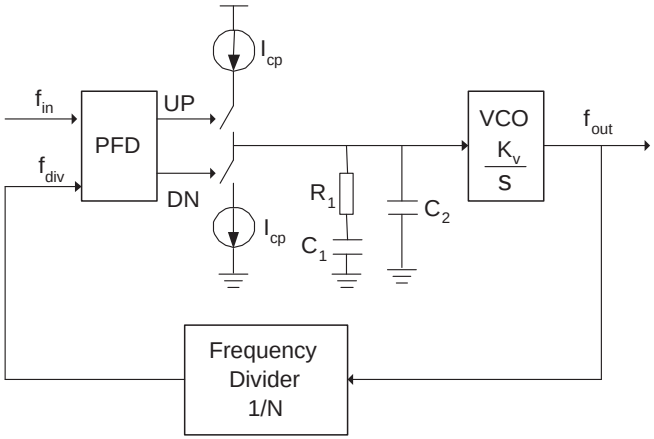


Figure 2.4: A typical charge-pump PLL.

2.3.3 Charge-pump PLL

Charge-pump based PLLs are used in most of the PLL systems. A typical charge-pump PLL, consisting of a phase-frequency detector (PFD), a charge-pump, a second order passive loop filter, a VCO and a frequency divider, is shown in Figure 2.4.

The charge-pump PLL offers several advantages. Using PFD, the PLL is able to lock to any frequency, regardless of how far it is initially in frequency. Simple passive loop filters can be used in charge-pump PLLs to implement a type-II PLL with zero static phase error. The charge-pump PLL also provides flexible design trade-offs by decoupling various design parameters such as loop bandwidth, damping factor, and lock range.

The phase detector can be implemented with various circuits. Possible implementations include mixer, XOR gate, JK flip-flop. However, it can be proved that the PLLs, that have such phase detector implementations, do have some limitations [3] [4]. With passive loop filters, these PLLs can not lock to the correct frequency if the target frequency is too far away from the initial frequency of the VCO. Also, even if the PLLs are in lock, they can fall out of lock if the VCO signals change more than a certain amount in frequency. Even when the PLLs are in lock, there are steady state phase errors. The one

solution for these problems is using active filters. Although active filters do fix the problems, they require opamps that add cost and noise.

The phase-frequency detector (PFD) does a much better job dealing with a large error in frequency. It is typically accompanied with a charge pump. The PFD converts the phase error presented to it into a voltage, which in turn is converted by the charge-pump into a correction current. A charge-pump PLL always includes a PFD and a charge-pump.

The PFD is a sequential logic circuit that generates three states responding to the rising edges of the two inputs as shown in Figure 2.5. The PFD has actually four states, but the fourth state is simply a reset state. Three conditions are possible for phase error:

1. Positive. f_{in} leads f_{div}. UP is a rectangular waveform whose width equals the time distance between the f_{in} and f_{div} rising edges. DN is a very short pulse.
2. Negative. f_{div} leads f_{in}. DN is a rectangular waveform whose width equals the time distance between the f_{in} and f_{div} rising edges. UP is a very short pulse.
3. Zero. f_{in} is synchronous with f_{div}. Both UP and DN are very short pulses.

Figure 2.6 shows an example of PFD waveforms.

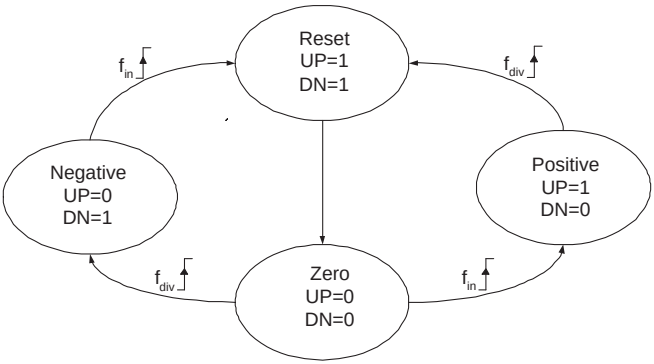


Figure 2.5: State diagram of tristate PFDs.

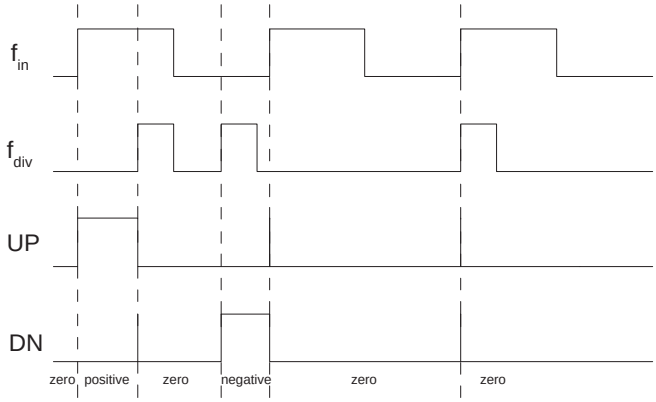


Figure 2.6: An example of PFD waveforms.

As shown in Figure 2.4, a charge-pump can be symbolized by a three-position electronic switch that is controlled by the PFD outputs. When the PFD is in positive state, a current I_{cp} flows out of the charge-pump and charge the loop filter. When the PFD is in negative state, a current I_{cp} flows in the PFD and discharges the loop filter. When the PFD is in zero state, there is no current flows in or out of the charge-pump, therefore, the loop filter voltage keeps constant.

The loop filter in a charge-pump PLL can be either passive or active, however, in most cases, passive filters are preferred because they don't need opamps that increase power consumption and add noise.

Because of the sampling nature of PFD, the charge-pump PLL is a time-varying system. An exact analysis of charge-pump PLL involves complicated discrete-time z-domain models [5] [6]. However, if the loop bandwidth is much smaller than the reference signal frequency, the state of the PLL changes by only a very small amount on each cycle of the reference signal. In such cases, the detailed behaviour within a single cycle is of less concern than the average behaviour over many cycles. By applying an average analysis, the time-varying operation can be bypassed and the PLL can be approximately analyzed by a continuous-time model.

The PFD and charge-pump together have an average transfer gain over

one reference cycle:

$$K_d = \frac{I_{out}}{\Delta\Phi} = \frac{I_{cp}}{2\pi} \tag{2.35}$$

where $\Delta\Phi = \Phi_{in} - \Phi_{div}$ is the phase difference between the input reference signal and the output signal of the frequency divider, I_{cp} is the charge pump current, and I_{out} is the average current that charges or discharges the loop filter over a reference input cycle.

Now the open-loop transfer function of the charge-pump PLL is:

$$H(s)|_{cl} = \frac{K_d Z_{lf}(s)\frac{K_v}{s}}{1 + K_d Z_{lf}(s)\frac{K_v}{s}\frac{1}{N}} \tag{2.36}$$

where $Z_{lf}(s)$ is the impedance of the loop filter. A second-order passive loop filter as shown in Figure 2.4 is commonly used in charge-pump PLLs. The resistor R_1 adds a zero in the PLL transfer function in order to stabilize the PLL system. The capacitor C_2 is used to suppress the frequency jumps caused by the switching operations of the PFD and charge-pump. Normally, C_2 is chosen to be about one-tenth of the value of C_1, so in the first consideration, we can ignore C_2 and get a second order transfer function of the PLL:

$$H(s)|_{cl} = \frac{\frac{I_{cp}}{2\pi}\frac{K_v}{s}(R_1 + \frac{1}{sC_1})}{1 + \frac{I_{cp}}{2\pi}\frac{K_v}{s}(R_1 + \frac{1}{sC_1})\frac{1}{N}} = \frac{N\omega_n^2(\frac{2\,xi}{\omega_n}s + 1)}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{2.37}$$

where ω_n is the nature frequency given by:

$$\omega_n = \sqrt{\frac{I_{cp}K_v C_1}{2\pi N C_1}} \tag{2.38}$$

and ξ is the damping factor given by:

$$\xi = \frac{R_1}{2}\sqrt{\frac{I_{cp}K_v C_1}{2\pi N}} \tag{2.39}$$

The transfer function (2.37) looks exactly the same as the transfer function (2.30) for a type-II second-order PLL as we discussed before. Therefore, the equations (2.33) (2.34) for the phase margin and the unit-gain frequency of type-II second-order PLLs are also valid for second-order charge-pump PLLs, and can be used for PLL loop stability analysis.

The complete loop transfer function of the practical charge-pump PLLs has to include the capacitor C_2 in the loop filter. Now the open-loop and closed-loop transfer functions are third order and can be written as:

$$H(s)|_{ol} = \frac{\Phi_f}{\Phi_i} = \frac{K_v K_d (1 + sC_1 R_)}{s^2 N(C_1 + C_2)(1 + sC_s R_1)} \tag{2.40}$$

$$H(s)|_{cl} = \frac{\Phi_o}{\Phi_i} = \frac{N K_v K_d (1 + sC_1 R_)}{s^2 N(C_1 + C_2)(1 + sC_s R) + K_v K_d (1 + sC_1 R_1)} \tag{2.41}$$

where $K_d = \frac{I_{cp}}{2\pi}$ is the gain of the PFD and charge-pump, and $C_s = \frac{C_1 C_2}{C_1 + C_2}$. C_2 adds an extra pole at $\frac{1}{R_1 C_s}$ in the open-loop transfer function, and degrades the phase margin. Figure 2.7 shows the Bode plot of the open-loop gain and the phase. At very low frequency range, there is a magnitude slope of -40 dB/dec and the phase shift is -180 degrees. After the zero, the slope becomes -20 dB/dec and the phase goes back towards 90 degrees. After the high-frequency pole , the slope is again -40 dB/dec and the phase approaches 180 degree. The dashed lines in the graph show the response of the system if the capacitor C_2 is not included. For optimal stability (maximum phase margin in the system), the unity gain point should be at the geometric mean of the zero and the high-frequency pole since this is the location where the phase shift is furthest away from 180 degrees. If the zero and the high-frequency pole are relatively far away from each other, then, up to the unity gain point, the loop parameters are nearly the same whether or not the high frequency pole is included. Normally, C_2 is about one-tenth of C_1, the effect of C_2 can be neglected.

The continuous time analysis of charge-pump PLL is valid only if the loop bandwidth is much smaller than the reference frequency. The minimum ratio between the input reference frequency and the natural frequency for a stable PLL loop is given by [8]:

$$\frac{\omega_i}{\omega_n} \geq 2\pi\xi \tag{2.42}$$

So, for instance, if $\xi = 0.707$, this ratio must be greater than 4.4. A safe ratio often quoted as the rule of thumb for charge-pump PLL design is 10:1.

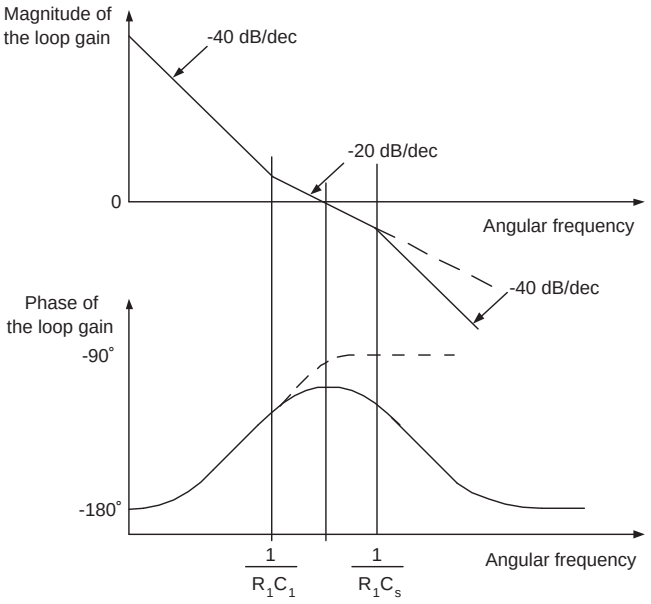


Figure 2.7: Open-loop magnitude and phase response of the third-order charge-pump PLLs.

2.4 Integer-N PLL and fractional-N PLL

A typical charge-pump integer-N PLL is shown in Figure 2.8. The phase-frequency detector (PFD) compares the phase and frequency of the input signal and the feedback signal and generates the UP and DN signals according to the phase difference. The charge pump charges the loop filter when UP signal is active and discharges the loop filter when DN signal is active. The voltage controlled oscillator (VCO) generates the output signal, whose frequency depends on its input control signal. The frequency divider divides the frequency of the output signal by an integer N. Through the feedback, the loop forces the phase of the feedback signal to track the phase of the input signal. Thus, the

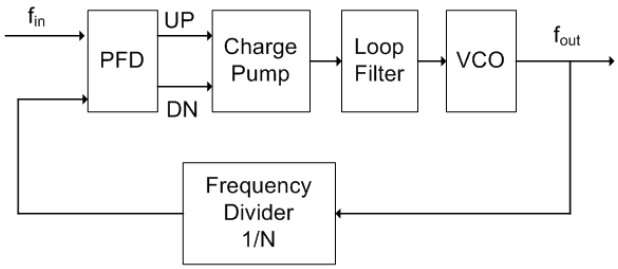


Figure 2.8: Block diagram of an integer-N PLL.

output frequency, which is a multiple of the feedback signal, is given by:

$$f_{out} = N f_{in} \tag{2.43}$$

The phase transfer function of the closed-loop can be written as:

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_\phi Z(s) \frac{K_{vco}}{s}}{1 + \frac{1}{N} K_\phi Z(s) \frac{K_{vco}}{s}} \tag{2.44}$$

where $K_\phi = \frac{I_{cp}}{2\pi}$ is the gain of the PFD and the charge pump, I_{cp} is the charge pump current, Z(s) is the impedance of the loop filter, and K_{vco} is the gain of the VCO.

In an integer-N PLL, the output frequency is an exact integer multiple of the input reference frequency. In an fractional-N PLL, the output frequency can be a non-integer multiple of the input frequency. In the cases when the required output frequencies are not integer multiple of the input frequencies, fractional-N PLLs have to be used instead of integer-N PLLs. In other cases, such as in wireless applications, PLLs are often used as frequency synthesizer, and their output frequencies are programmable. If integer-N PLLs are used for these cases, the minimum frequency step has to equal to the input reference frequency. Therefore, in order to get a small frequency step, the reference frequency must be small. A small reference frequency means a small PLL loop bandwidth, a long locking time and weak suppression of the VCO noise. However, all these problems can be removed with a fractional-N PLL, which allows the minimum frequency step to be a fraction of the reference frequency.

Fractional-N PLLs are usually implemented by dynamically changing the division ratio of the frequency divider between two or more integers. As an example, if the division ratio toggles between 8 and 9, and the divider always divides by 8 for 12 cycles and by 9 for 4 cycles, then the average division ratio will be:

$$\overline{N} = \frac{8 \times 12 + 9 \times 4}{16} = 8.25$$

However, toggling the divider ratio between two values in a repeating manner generates spurious components at integer multiples of the repetition rate of the time sequence. In the spectrum of the VCO output signals, the spurious frequencies are in the sides of the centre frequency. Such spurious components can be reduced by using Σ-Δ modulator (SDM) to generate pseudo random signal to control the divider ratio.

2.4.1 Σ-Δ fractional-N PLL

The Σ-Δ fractional-N PLL compensates the fractional spur in the digital domain. The digital noise-shaping Σ-Δ modulator is used to randomize the instantaneous loop divider ratio. Figure 2.9 shows the concept of Σ-Δ fractional-N PLLs. A digital SDM is used to control the frequency division ration in the PLL. The instantaneous division ratio is the sum of a base integer, N_B, and the integer output of the SDM, $n_Q(t)$, so the average fractional division ratio is:

$$N = N_B + \overline{n_Q(t)} \tag{2.45}$$

where $\overline{n_Q(t)}$ is the average output of SDM,

2.5 Modelling and system-level simulation of PLL

In a top-down PLL design flow, before transistor level circuit design, a system level simulation is necessary to determine the important design parameters, such as the loop bandwidth, the charge pump current and the VCO gain, according to design specifications, such as phase noise and lock time. However, simulations of PLLs, especially fractional-N PLLs used as frequency synthesizer in wireless communication, is particularly challenging for a variety of reasons. First, the high output frequency of the PLL (often in the GHz range) imposes a high simulation sample frequency for the simulator. Unfortunately, the overall PLL dynamics have a bandwidth that is typically three to four orders of magnitude lower in frequency than the output frequency (often 100

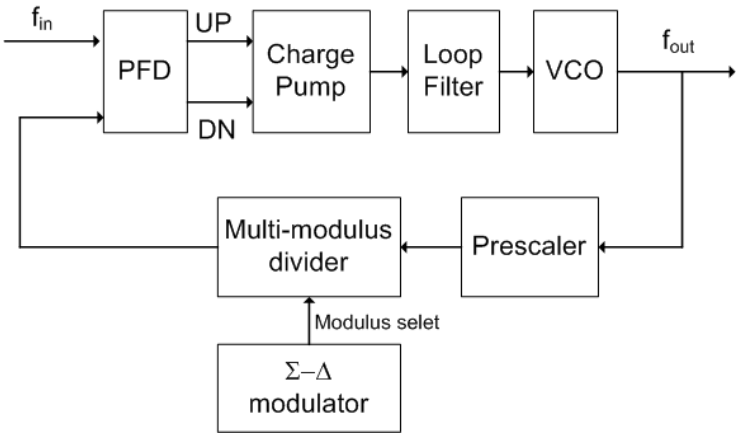


Figure 2.9: Block diagram of an Σ-Δ fractional-N PLL.

kHz to 1 MHz bandwidth compared to a GHz output frequency). Thus, it takes a long time for simulators to compute the dynamic response of the system since many samples are required for simulation. For noise simulation, the fractional-N PLL adds the additional constraint that its behaviour is non-periodic in steady-state due to dithering action of the division factor, which prevents the use of methods developed for periodic steady-state conditions as used in Cadence SpectreRF simulator [18]. Some simulation approaches are proposed in [19] [20] [21] [23] to try to make accurate and efficient system-level simulation. They are briefly summarized here:

1. Matlab and Simulink based simulation. [19] and [21] present the simulation methods using Matlab and Simulink.
2. C++ based simulation. [20] introduces a custom C++ simulator for the behaviour simulation of PLL systems with uniform time steps based on an area conservation principle to minimize the adverse effects of signal quantization.
3. Verilog-A based simulation. [23] describes the simulation method with Verilog-A behavioral model. Instead of modelling the system in terms of voltage and currents, a phase-domain model based on the phase of the signal is developed. The high frequency variations associated with

the voltage-domain model are not present in phase domain models, so the simulations are considerably faster.

2.6 Summary

In this chapter, we introduced basic PLL working principles, transfer function and stability analysis. We presented the PLL order and type from the point of view of the classical control theory. We introduced charge-pump based PLL, which is a type-II PLL and mostly used in integrated PLL designs. A simple introduction and comparison for two most important PLL types, integer-N and fractional-N PLLs, are presented. At the end, we briefly introduced the modelling and system level simulation.

In the next chapter, we will present the basic PLL building block from the point of view of circuit design.

Chapter 3

PLL Building Blocks

In this chapter, we will present the building blocks for charge-pump PLLs. These blocks are phase frequency detector, charge pump, loop filter and frequency detector. The implementations of them in circuit and schematic level will be described. Voltage-controlled oscillator is the most important and complicated block, and will be presented in the next chapter.

3.1 Phase-Frequency Detector

A phase-frequency detector (PFD) compares the two input signals, the output of the frequency divider and the input reference signal, and generates the output signals that corresponds to the phase difference between the two input signals. PFDs are usually implemented with digital circuits.

A conventional tristate PFD circuit is shown in Figure 3.1. If the phase of the reference input F_{ref} is ahead of the phase of the feedback input F_{back}, then the circuit generates an UP signal that will speed up the VCO. Conversely, if the reference phase is lagging behind the feedback phase, a DN signal is generated and the VCO will slow down. If REF and DIV are in phase, the PFD generates synchronized, narrow, coincident pulses on both UP and DN, that are needed for eliminating the deadzone effect. Deadzone phenomenon [1] is a non-ideality of the PFD and can be explained as the following: when the phase difference of REF and DIV is very small, the circuit generates very narrow pulses on UP or DN. However, owing to the finite rise-time and fall-time resulting from the capacitance seen at these nodes, the pulses may not

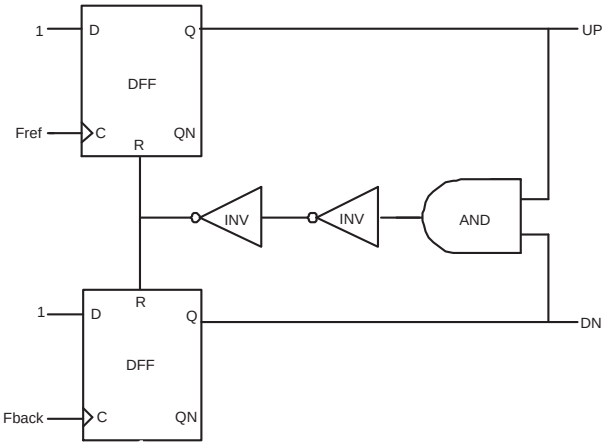


Figure 3.1: A conventional tristate PFD.

be wide enough to reach a logical high level and fail to turn on the charge pump switches. In other words, if the input phase difference Δf falls below a certain value ϕ_0, then the output voltage of the PFD is no longer effective to the charge pump, as shown in Figure 3.2. Deadzone phenomenon is highly undesirable, because it allows the VCO to accumulate random phase errors without corrective feedback as soon as the PFD input phase error is lower than ϕ_0. Deadzone can be eliminated by generating coincident pulses on UP and DN, which is a result of the delayed reset signal path made by two inverters as shown in Figure 3.1. For $|\Delta\phi|$=0, the coincident UP and DN pulses turn on the charge pump, but the net output current of the charge pump is zero. For an infinitesimal increment in the phase difference of the PFD input, the net output current of the charge pump is proportional to the phase difference. The two most widely used PFD types are the static logic PFD (SPFD) [9] and the dynamic logic PFD (DPFD) [10]. Figure 3.3 shows the schematic of a SPFD, and Figure 3.4 shows the schematic of a DPFD. The DPFD exhibits some advantages in comparison to SPFD:

1. Fewer transistors, thus smaller area.
2. Lower power consumption.

3. Higher maximal operating frequency.

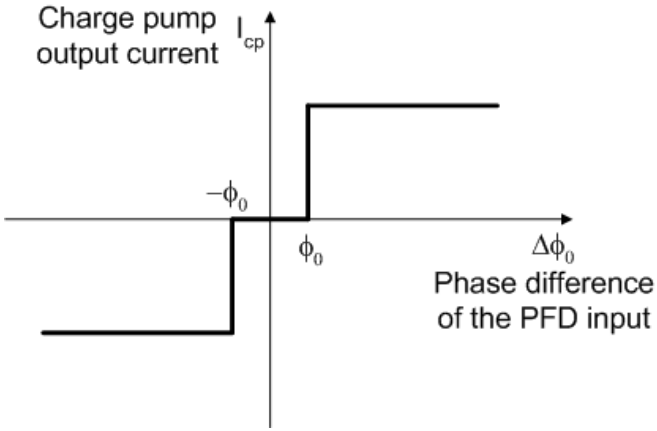


Figure 3.2: Deadzone of the PFD.

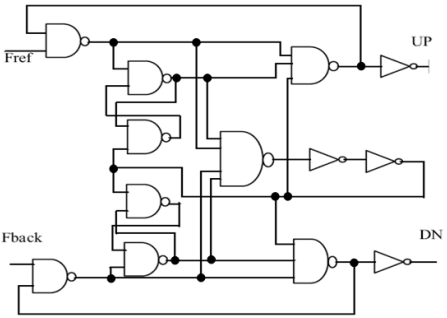


Figure 3.3: Schematic of a static logic PFD.

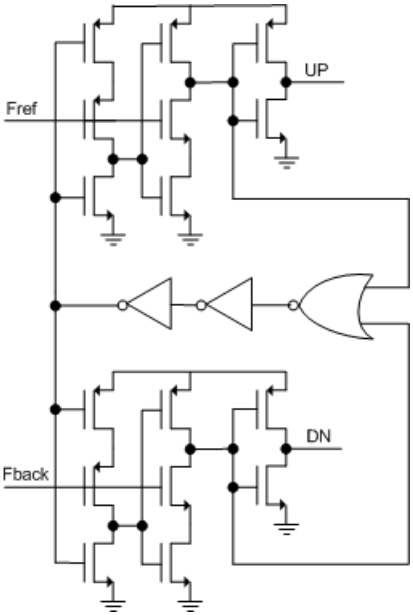


Figure 3.4: Schematic of a dynamic logic PFD.

3.2 Charge Pump

The charge pump (CP) is responsible for charging or discharging the loop filter, and consequently adjusting the control voltage of the VCO. Any noise generated by the CP will directly contribute to the VCO phase noise, therefore, charge pumps must be very carefully designed to minimize the phase noise. A basic CP circuit is shown in Figure 3.5. There exist some non-ideal effects that impair the performance of this basic circuit:

1. Current mismatch. Ideally, the currents I_{up} and I_{dn} should be exactly equal. However, due to the finite output impedance, I_{up} and I_{dn} are only equal for a certain output voltage, and for other output voltages, they are not.
2. Charge sharing. The capacitors at the nodes 'a' and 'b' consist of the

parasitic source/drain capacitances of MOSFET transistor. When the switching transistors MN2 and MP2 are open, the charges on the nodes 'a' and 'b' move towards V_{DD} and V_{SS} respectively. When the switches close, instantaneously, some of the charge stored on these parasitic capacitors will be transferred to the loop filter, and cause voltage spikes on the VCO control line.

3. Clock feedthrough. When UP and DN signals change their logic levels, due to the parasitic gate-drain capacitance of MN2 and MP2, some charges are coupled to the loop filter, and cause spikes on the VCO control voltage.
4. Switching time mismatch. When the PLL is in lock, he PFD generates the coincident narrow UP and DN pulses in each reference input period for eliminating deadzone. However, the switching time mismatch between the UP and DN signals causes also spikes on the VCO control voltage.
5. Leakage current. This is a common nonideal phenomenon in submicro CMOS technology. The output leakage current in the charge pump cause also spikes on the VCO control voltage.

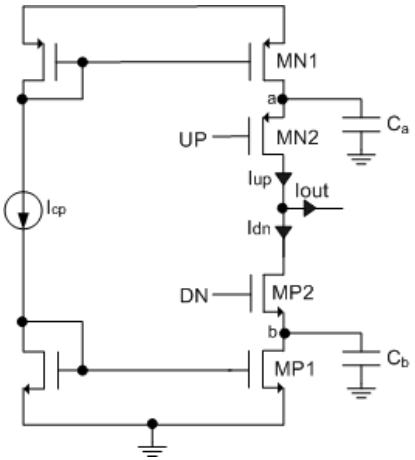


Figure 3.5: Schematic of a basic charge pump circuit.

When a PLL is in locking state, all those nonideal effects mentioned above contribute to the VCO phase error. The analytic expression of the total phase error ϕ_{err} [11] [12] can be expressed as:

$$\phi_{err} = 2\pi\Big(\frac{I_{leak}}{I_{cp}} + \frac{\Delta I}{I_{cp}} \cdot \frac{T_{on}}{T_{ref}} + \frac{\Delta T_{sw} \cdot T_{on}}{T_{ref}^2} + \frac{\Delta Q}{T_{ref} \cdot I_{cp}} \cdot \frac{T_{on}}{T_{ref}}\Big) \tag{3.1}$$

where I_{cp} is the charge pump current, I_{leak} is the leakage current, ΔT_{sw} is the switching time mismatch, ΔI is the mismatch current, T_{on} is the charge pump turn-on time, ΔQ is the total charge injected to the charge pump output due to charge sharing and clock feedthrough, and T_{ref} is the reference clock period. The resulting reference spurs for a typical third-order PLL can be approximated by [12]:

$$P_r = 20\log\Big(\frac{N \cdot f_{bw} \cdot \phi_{err}}{\sqrt{2} f_{ref}}\Big) - 20\log\Big(\frac{f_{ref}}{f_{pl}}\Big) \tag{3.2}$$

where N is the division ratio of the frequency divider, f_{bw} is the loop bandwidth, and f_{pl} is the pole frequency of the loop filter.

From the above discussion, we summarize some design principles for achieving low phase noise:

1. Increasing the charge pump current reduces the phase reference spurs, but the cost is more power consumption.
2. Reducing the charge pump turn-on time reduces the reference spurs, however, the minimum turn-on time is required for eliminating dead-zone phenomenon.

More circuit design techniques for low-phase noise, low-power charge pump design will be discussed in Chapter 6.

3.3 Loop Filter

Normally, VCOs are controlled by a voltage and not a current. Thus, in a charge-pump PLL, the function of the loop filter is to convert the output current of the charge pump into the VCO control voltage. In addition, low-pass filtering is needed since it is not desirable to feed pulses into the VCO. The most important characteristics of a PLL, such as loop bandwidth, settling time, and phase noise are highly dependent on loop filter design. Basically,

the loop filter can be realized either with pure passive elements or with an operational amplifier to form an active loop filter. Passive filters are generally recommended over active filters for reason of cost, simplicity, and in-band phase noise.

3.3.1 Passive loop filter

Most passive loop filters are second-order or third-order, as shown in Figure 3.6. Higher order filters often become unrealistic because the required capacitor values become too small relative to the VCO input capacitance and they become unnecessarily complex. The transimpedance of the second-order passive loop filter is given by:

$$Z(s) = \frac{1 + sC_1R_1}{s(C_1 + C_2)(1 + sC_tR_1)} \tag{3.3}$$

where $C_t = \frac{C_1C_2}{C_1+C_2}$.

By adding a series resistor, followed by a shunt capacitor, the simple second-order passive filter becomes a third-order passive filter. The additional pole is useful to reduce noise and spurs in high frequency band. This is especially important in fractional-N PLL to suppress out-of-band fractional spurs. The transimpedance of the third-order passive loop filter is given by:

$$Z(s) = \frac{1 + sT_1}{sC_t(1 + ST_2)(1 + sT_3)} \tag{3.4}$$

where $T_1 = C_1R_1$, $C_t = C_1 + C_2 + C_3$, $T_2 = \frac{R_1C_1C_2}{C_t}$, and $T_3 \approx R_3C_3$. The approximation is valid as log as $C_1 >> C_2, C_3$, and $\frac{C_2}{C_3} >> 1 - \frac{T_3}{T_1}$. Detailed analysis shows that $T_1 >> (T_2 + T_3)$ is required for stability [13].

3.3.2 Active loop filter

An active loop filter is usually employed in cases where the VCO requires a higher tuning voltage than the charge pump can operate. The presence of the opamp has the added advantage that the output voltage of the charge pump is constant. Thus, the charge pump no longer has to operate near the rails-to-rail voltages, and the current mismatch can be minimized. Active components always introduce additional noise that contributes to the PLL in-band phase noise. In order to attenuate the added opamp noise, it is recommended to use

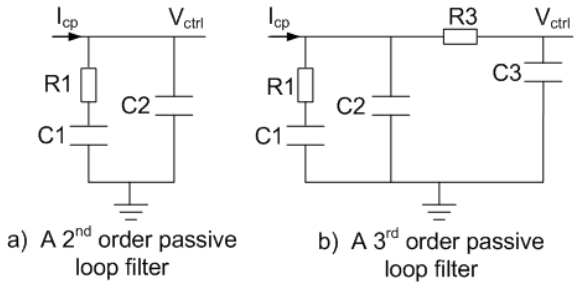


Figure 3.6: Passive loop filter.

an active filter of third or higher order, even if it is not required for spur suppression. A third-order active loop filter is shown in Figure 3.7. The feedback path of the opamp provides second-order low-pass filter characteristics, and an additional pole is added at the opamp output. The filter transfer function is given by:

$$Z(s) = \frac{1 + sT_1}{sC_t(1 + ST_2)(1 + sT_3)} \tag{3.5}$$

where $T_1 = C_1R_1$, $C_t = C_1 + C_2$, $T_2 = \frac{R_1C_1C_2}{C_t}$, and $T_3 = R_3C_3$.

3.4 Frequency divider

Frequency dividers can be implemented with either CMOS rail-to-rail logic circuits or CMOS current mode logic (CML) circuits. At low frequencies, rail-to-rail logic is preferred for its simplicity and low static power dissipation, while, at high frequencies, CML is a better choice, as it can operate faster with lower power consumption because of the reduced output swing. These two circuit types are often combined to implement frequency dividers: the input stage of the frequency dividers are implemented with CML in order to reduce power consumption with high operating frequency; the other stages are implemented with rail-to-rail logic, which is pure digital circuit consisting of only standard logic cells. While the frequency dividers with constant division ratio are normally used for integer-N PLLs, multi-modulus dividers are necessary for fractional-N PLLs.

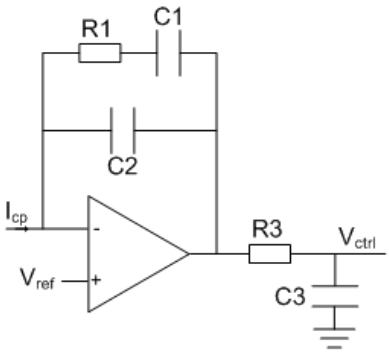


Figure 3.7: A third-order active loop filter.

3.4.1 Divide-by-2 circuit

The divide-by-2 circuit is a basic building block of the frequency divider. Figure 3.8 shows an efficient divider-by-2 structure known as Johnson counter. The structure consists of two cascaded D-latches within a negative feedback loop. The maximum operating frequency of this structure is determined by the propagation delay of each latch. D latches can be implemented either with rail-to-rail static logic when the operating frequency is low, or with CML when the operating frequency is high.

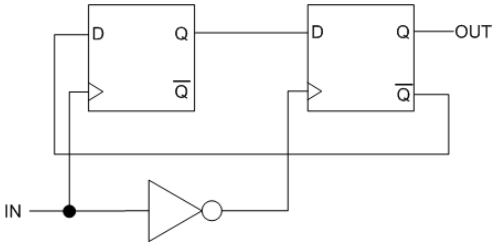


Figure 3.8: A divide-by-2 circuit implemented as a Johnson counter.

Figure 3.9 shows an usually implemented CMOS CML D-latch. When CLK is low, all current are passed through MN1, and MN2 is off. Thus, MN5 and MN6 are also off and do nothing. In this state, the circuit behaves as a differential pair, and the output follows the input. When CLK goes high, MN1 turns off, turning off MN3 and MN4. In this state, MN5 and MN6 turn on. These two transistors are connected in positive feedback, which latches the output value. Two CML D-latchs connected in negative feedback each other implement a divide-by-2 circuit, which can provide output signals with quadrature phases required in many frequency synthesizers.

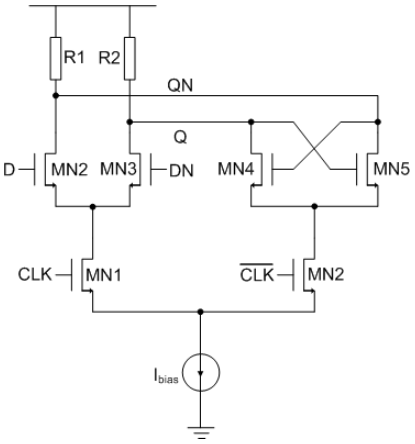


Figure 3.9: CML D-latch circuit.

High speed CMOS divide-by-2 circuits can also incorporate dynamic latches. Figure 3.10 shows two examples, In the circuit of Figure 3.10(a), the first two inverters operate as dynamic latches controlled by CLK and $\overline{CLK}$, and the third inverter provides the overall inversion required in the negative feedback loop. Figure **??**(b) is a divider based on the true single-phase clocking (TSPC) circuit [14] for achieving a high speed. The drawback of these two circuits is the lack of precise complementary quadrature outputs.

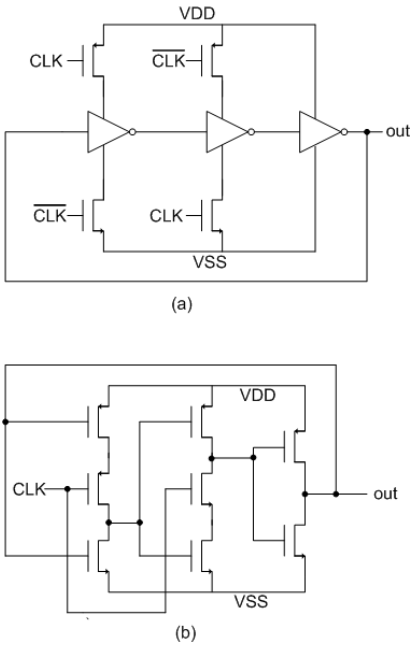


Figure 3.10: Dynamic CMOS dividers using (a) inverters, (b) TSPC .

3.4.2 Divide-by-3 circuit

Figure 3.11 shows a divide-by-3 circuit utilizing two flip-flops and an AND-gate. Both flip-flops are clocked to rising edge of the input clock. The logic function of this circuit can be expressed as:

$$Q_2(n+1) = \overline{Q_2(n)} \cdot \overline{Q_2(n-1)} \tag{3.6}$$

3.4.3 Multi-modulus dividers

Multi-modulus dividers divide the input frequency by one of the modulus according to the input control bits. A commonly used dual-modulus divider is a divide-by-2/3 circuit. Figure 3.12 shows a divide-by-2/3 circuit controlled

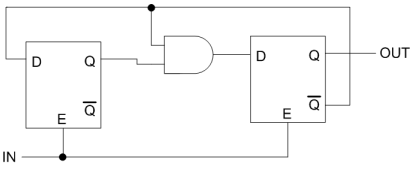


Figure 3.11: Divide-by-3 circuit and the timing diagram.

by bit CON. The circuit is configured as a divide-by-2 circuit when CON is high, and a divide-by-3 circuit when CON is low.

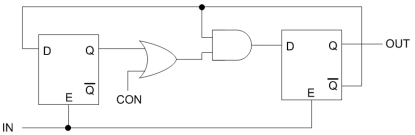


Figure 3.12: A divide-by-2/3 circuit using gating logic.

One method to implementing a multi-modulus divider is to cascade 2 or more dual-modulus dividers. Figure 3.13 depicts a programmable divider architecture with local feedback [15]. The modular structure consists of a chain of divide-by-2/3 cell. The circuit operates as follows. Once in a division period, the last cell on the chain generates the signal mod_{n-1}. This signal then propagates up the chain, being reclocked by each cell along the way. An active *mod* signal enables a cell to divide by 3 (once in a division cycle), provided that its programming input p is set to 1. Division by 3 adds one extra period of each cell's input signal to the period of the output signal. Hence, a chain of n divide-by-2/3 cells generates an output signal with a period of:

$$T_{out} = (2^n + 2^{n-1}p_{n-1} + 2^{n-2}p_{n-2} + ... + 2p_1 + p_0)xT_{in} \tag{3.7}$$

where T_{in} is the period of the input signal, and $p_0, ..., p_{n-1}$ are the binary programming bits of the divide-by-2/3 cells. The nth cell runs at a speed of 1/n of the first cell. Therefore, if each cell is implemented as a custom block, the current can be scaled accordingly to achieve low-power consumption. The divide-by-2/3 cell for this multi-modulus divider can be implemented as shown in Figure 3.14.

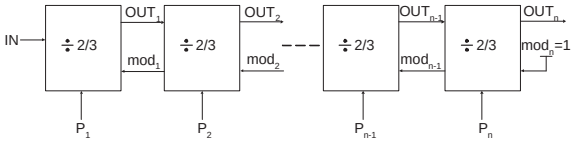


Figure 3.13: A programmable multi-modulus divider.

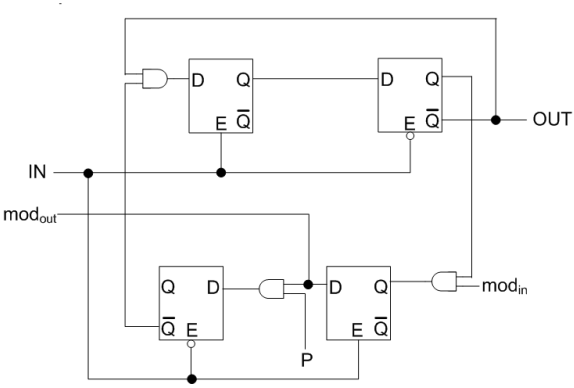


Figure 3.14: Logic implementation of a divide-by-2/3-cell.

Another approach to implementing a multi-modulus divider is based on phase-switching technique [16]. Figure 3.15 illustrates a divide-by-4/5 circuit using this approach. A divide-by-2 circuit is cascaded by a 4-phase divide-by-2 circuit, and a MUX circuit is followed to select the output from the 4 input signals with different phases.

3.5 Summary

In this chapter, we presented the circuit implementation of the PLL building blocks, such as PFD, charge pump, loop filter and frequency divider. We described their functions and circuit implementations, and analysed the non-idealities of the implemented circuits. The non-idealities of these blocks de-

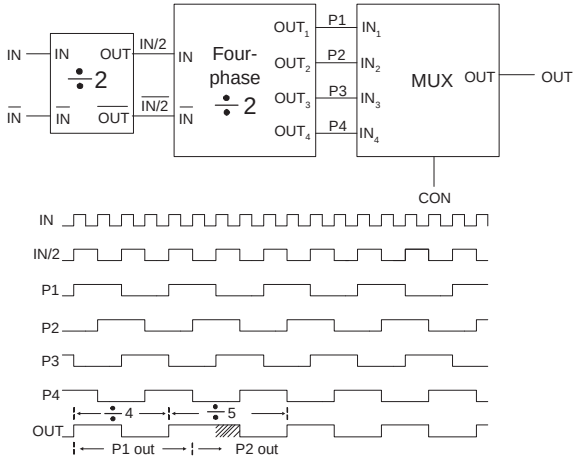


Figure 3.15: A divide-by-4/5 circuit using phase-switching approach.

teriorate phase noise of PLLs. In the next chapter, we will present the most critical block of PLLs: voltage-controlled oscillator.

Chapter 4

Voltage Controlled Oscillator

In the last chapter, we presented some PLL building blocks, such as PFD, charge pump, loop filter and frequency divider. In this chapter, we will present voltage-controlled oscillator (VCO), which is a key component in PLL systems. As shown in Figure 4.1, an ideal VCO is a circuit whose output frequency is a linear function of its input control voltage:

$$f_{out} = f_0 + K_{vco}V_c \tag{4.1}$$

where f_0 represents the output frequency corresponding to $V_c = 0$ and K_{vco} is the gain of the VCO. The achievable output frequency range, $f_2 - f_1$, is the tuning range of the VCO. The important performance parameters of VCO are:

- **Centre frequency** is the midrange value of the maximum and minimum frequency $\frac{f_1+f_2}{2}$.
- **Tuning range** The required tuning range is determined by two parameters: (1) the variation of the VCO centre frequency with process and temperature and (2) the frequency range necessary for the application.
- **Gain** K_{vco} should be designed to be large enough to fulfill the tuning range requirement. However, any noise on the input control voltage results in variation of the output phase and frequency. For a given noise amplitude, the noise in the output frequency is proportional to K_{vco}. Thus, to minimize the effect of noise in V_c, K_{vco} must be minimized, a constraint directly conflicts with the required tuning range.
- **Tuning linearity** The tuning characteristics of realistic VCOs usually exhibit nonlinearity, i.e., K_{vco} is not a constant. Such nonlinearity degrades

the settling behaviour of PLLs and leads to high sensitivity for some frequency region. For this reason, it is desired to minimize the variation of K_{vco} across the whole tuning range.

- **Output amplitude** It is desirable to achieve a large output oscillation amplitude, thus making the waveform less sensitive to noise. The amplitude trades with power dissipation, supply voltage, and even the tuning range in certain cases. Also, the amplitude may vary across the tuning range, an undesirable effect.
- **Output signal purity** Even with a noiseless input control voltage, the output waveform of a VCO is not perfectly periodic. The electronic noise of the devices in the VCO and supply noise lead to noise in the output phase and frequency.
- **Power dissipation** As with other analog circuits, oscillators suffer from trade-offs between speed, power dissipation, and noise.
- **Supply and common-mode rejection** Oscillators are quite sensitive to common-mode noise, especially if they are realized in single-ended structure. Even differential oscillators can exhibit supply sensitivity. It is often the case in today's mixed signal IC that VCOs are surrounded by noisy digital circuits, that introduce noise to the VCO through the substrate. For this reason, it is preferable to employ differential paths for both the oscillation signal and the input control signal.

The general requirements for a high-quality VCO include high spectral purity, linear voltage-to-frequency transfer characteristic, and good frequency stability to power supply and temperature variation. For VCOs applied in digital wireless applications, low power consumption and low fabrication cost are also important. In some applications, e.g. high speed digital interfaces, high and wide tuning range may be necessary. Two types of oscillators are widely implemented in today's CMOS PLL designs: the first is the ring oscillator based VCO, and the second is the LC oscillator based VCO. Each type has its advantages and drawbacks. LC VCOs have superior phase noise performance but normally need on-chip inductors, which occupy large silicon area. Ring VCOs are compact and easy to achieve wide tuning range, but usually exhibit higher phase noise than LC VCOs for the same power consumption.

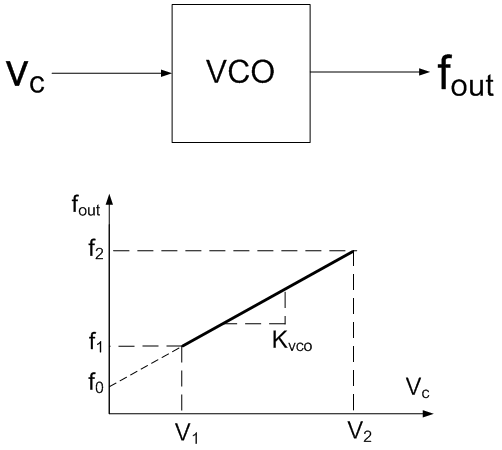


Figure 4.1: Functional model of a VCO.

4.1 Ring oscillator based VCO

A ring oscillator consists of a number of delay stages in a loop, which forms a unstable negative feedback circuit. Its period of oscillation is twice the sum of the delay of each delay cell in the ring. Figure 4.2 shows the linear model of a three-stage ring oscillator. The open-loop transfer function of this model is:

$$H_{j\omega} = (\frac{-g_m R}{1 + Rj\omega C})^3 \tag{4.2}$$

where g_m is the small signal gain of each delay stage, R and C are the load resistance and capacitance at the output of each delay stage. The circuit oscillates only if the frequency-dependent phase shift equals 180 degrees, i.e., if each stage contributes 60 degrees. The frequency at which this occurs is given by:

$$tan^{-1}\omega_{osc} RC = 60^o \tag{4.3}$$

and hence:

$$\omega_{osc} = \frac{\sqrt{3}}{RC} \tag{4.4}$$

The minimum voltage gain per stage must be such that the magnitude of the loop gain at ω_{osc} is equal to unity:

$$\frac{(g_m R)^3}{(1+(\omega_{osc} RC)^2)^{\frac{3}{2}}} \geq 1 \tag{4.5}$$

It follows from (**??** and (4.5) that:

$$g_m R \geq 2 \tag{4.6}$$

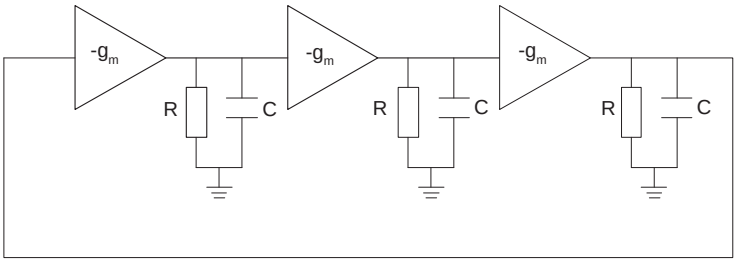


Figure 4.2: Linear model of a three-stage ring oscillator.

The minimum number of the stages for a ring oscillator is 3, because for 1 or 2-stage rings there are no enough phase shift for oscillation [1]. The oscillation frequency is usually controlled by varying the biasing current of the delay cell.

Ring oscillators are often used in high-speed digital circuits for clock generation. Several reasons justify this popularity: (a) a wide tuning range is easily obtained with a ring oscillator; (b) ring oscillators are compatible with digital CMOS technology and occupy substantially less area than LC oscillators; (3) the behaviour of ring oscillators across process, supply and temperature corners can be simulated with reasonable accuracy by standard MOS models, whereas the design of LC oscillators heavily relies on inductor and varactor models. However, because ring oscillators do not have high-Q tank for frequency selection, they have traditionally much larger phase noise than LC-tank based oscillators.

4.1.1 VCOs based on single-ended ring oscillator

Single-ended ring oscillators consist of single-ended delay buffers. Two most common single-ended delay buffers are current-starved inverter [25] and the shunt-capacitor inverter [26] as shown in Figure 4.3.

In the current-starved inverter, the control voltage V_{ctrl} modulates the turn-on resistances of the pull-down transistor MN1, and, through a current mirror, the pull-up transistor MP1. These variable resistances control the current available to charge or discharge the load capacitance. Large value of V_{ctrl} allows a large current to flow, producing a small resistance and a small delay.

In the shunt-capacitor inverter, the control voltage V_{ctrl} adjusts the resistance of a shunt transistor MN1, which connects a large load capacitance to the output of the inverter. The shunt transistor MN1 in essence controls the amount of effective load capacitance seen by the driving gate. Large values of V_{ctrl} decrease the resistance of MN1, so the effective capacitance at the logic gate output is large, producing a large delay.

The oscillation frequency of a single-ended ring oscillator can be expressed as [38]:

$$f_o = \frac{1}{2Nt_D} = \frac{1}{\eta N(t_r + t_f)} \approx \frac{\mu_{eff} W_{eff} C_{ox} \Delta V^2}{8\eta N L q_{max}} \tag{4.7}$$

where N is the number of the stage, t_D is the delay of each stage, t_r and t_f are the rise and fall time respectively, η is a proportional constant, $W_{eff} = W_n + W_p$ is the sum of the width of the PMOS and NMOS transistor, $\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p}$ is the effective mobility, $\Delta V = VDD/2 - V_T$ is the gate overdrive in the middle of transition, and q_{max} is the maximum charge in the output node.

4.1.2 VCOs based on differential ring oscillator

On today's mixed-signal ICs, almost all ring oscillators use differential delay stages because of their superior immunity to power supply disturbances and substrate noise. A conventional differential delay stage with the replica-biasing circuit is shown in Figure 4.4 [9] [52] . The oscillation frequency of a N-stage differential ring oscillator can be expressed as:

$$f_o = \frac{1}{2Nt_d} \approx \frac{I_{bias}}{2NC_L V_{sw}} \tag{4.8}$$

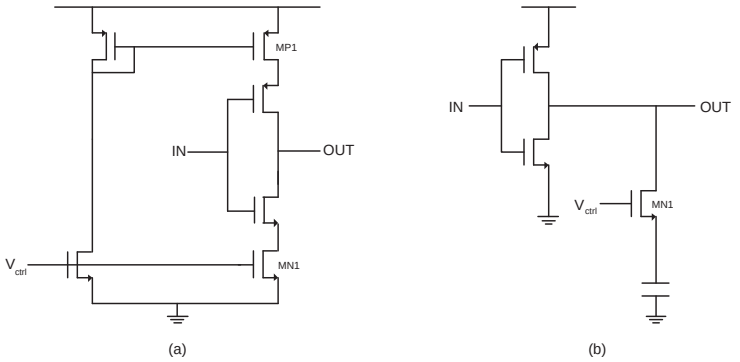


Figure 4.3: Two most common single-ended delay buffers: (a) Current-starved inverter, (b) Shunt capacitor inverter .

where V_{sw} is the output voltage swing. The oscillation frequency is controlled by current I_{ctrl}. The replica-biasing circuit consists of an opamp and the copy of the half delay buffer. Through negative feedback, the output swing is kept to a constant value $VDD - V_{ref}$ independent of the biasing current. The value of V_{ref} is chosen to ensure that the PMOS load transistors work in the triode region.

4.2 LC oscillator based VCO

LC oscillators have found wide usage in RF frequency synthesizers. LC oscillators offer a number of advantages over ring oscillators: (a) lower phase noise for a given frequency and power dissipation; (b) larger output voltage swing with peak levels that can exceed the supply voltage; (c) ability to operate at higher frequencies. However, LC VCOs require precise devices and circuit modelling because (a) the narrow tuning range calls for accurate prediction of the centre frequency; (b) the phase noise is greatly dependent on the quality of inductors and varactors; (c) they occupy a large area when on-chip inductors are used. The design of LC VCOs involves the following parameters: centre frequency, phase noise, tuning range, power dissipation, voltage headroom, start-up condition, output voltage swing, and drive ability. The most widely used LC oscillator in integrated circuits is the LC-tuned oscilla-

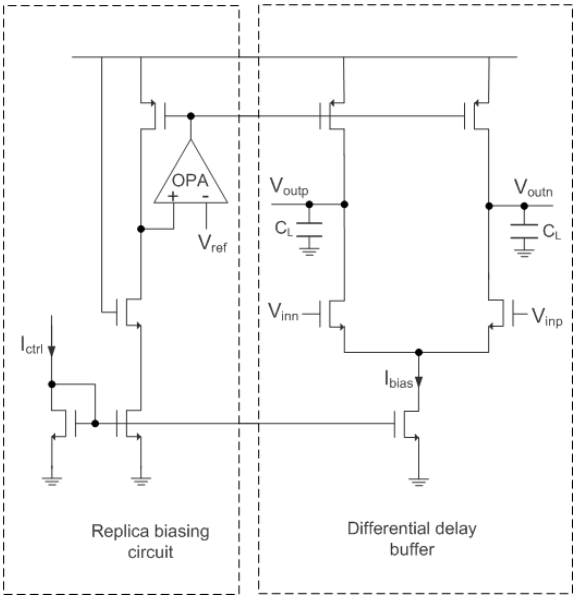


Figure 4.4: A differential delay buffer with the replica-biasing circuit.

tor. The concept of a LC-tuned oscillator is shown in Figure 4.5. R_p represents a total equivalent loss from the inductor and capacitor and the transistors. A negative resistance $-R_p$ provided by an active circuit compensates the loss of R_p so that the oscillation can be sustained. The frequency of oscillation is the resonance frequency of the tank:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{4.9}$$

A variable capacitor, or a varactor, can change its capacitance according to the voltage between its two nodes. Thus, the oscillation frequency of an LC oscillator can be tuned by changing the voltage of the varactor to realize a voltage-controlled oscillator (VCO). Three basic implementations of CMOS LC-tuned VCO are shown in Figure 4.6.

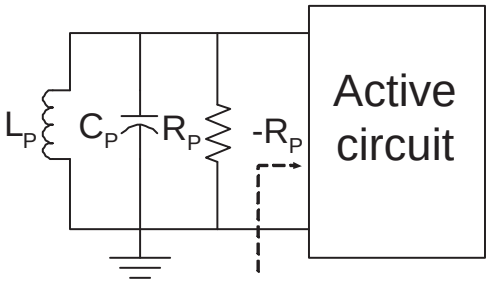


Figure 4.5: Basic model of LC-tuned oscillators.

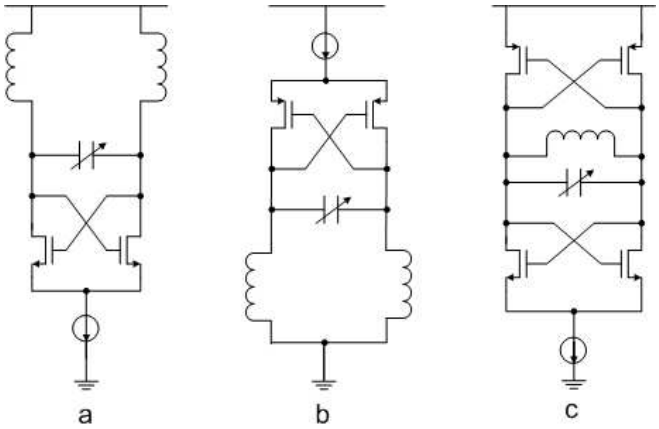


Figure 4.6: Various LC-tuned oscillator implementations: (a) NMOS-only LC VCO, (b) PMOS-only LC VCO, (c) Complementary LC VCO.

4.2.1 NMOS-only VCO

If the oscillator is voltage limited, the maximum voltage swing on each output node is twice the power supply voltage, which is well suited for low voltage design. If the oscillator is current limited, the output voltage per side is:

$$V_{out\_se} = \frac{R_p I_{bias}}{\pi} \tag{4.10}$$

where R_p is the equivalent parallel resistance of the LC tank, and the differential voltage is:

$$V_{out\_de} = \frac{2R_p I_{bias}}{\pi} \tag{4.11}$$

4.2.2 PMOS-only VCO

The output swing is the same as that of the NMOS-only VCO. PMOS transistors are about half as fast as NMOS transistors, so for the same transconductance per current, the double width is needed. PMOS transistors usually have lower flicker noise than NMOS transistors. Moreover, they are situated inside NWELL because most of actual process are of NWELL/P-substrate, so they are less impacted by substrate noise. Therefore, PMOS-only VCOs are more favorable for low phase noise design [29].

4.2.3 Complementary VCO

The negative resistance needed for the compensation of the tank loss is generated by both NMOS and PMOS transistors, thus enabling effectively to half the power consumption for the same negative resistance. The signal swing is limited to power supply voltage in voltage limited case. However, in current limited case, because the current is flowing through the full R_p in each direction, the output swing is twice as large as that in NMOS or PMOS-only VCOs:

$$V_{out\_de} = \frac{4R_p I_{bias}}{\pi} \tag{4.12}$$

4.3 Summary

In this chapter, we presented voltage-controlled oscillators (VCOs). Two types of VCO are mostly used in integrated PLL circuits: ring oscillator based VCO and LC oscillator based VCO. We described the operation principles and circuit implementations for the both VCOs. We analysed the advantages and disadvantages for each of them. In the next chapter, we will analyse the phase noise theory of VCOs and PLLs.

Chapter 5

Noise in VCOs and PLLs

In the previous chapters, we presented all building blocks in PLLs. In this chapter, we will analyse the phase noise mechanism of PLL. The main phase noise contributor in a PLL is the VCO. At first, we will introduce the phase noise theories for LC VCO and ring oscillator based VCO, and analyse VCO phase noise. Then we will analyse the phase noise contributions from the other blocks, such as PFD and charge pump.

5.1 Phase noise of LC VCOs

The output of an ideal sinusoidal oscillator can be expressed as:

$$V_{out} = Asin(\omega_o t + \phi) \tag{5.1}$$

where A is the amplitude, ω_0 is the oscillation frequency, and ϕ is an arbitrarily fixed phase reference. Therefore, the spectrum of an ideal oscillator is a pair of impulses at $\pm\omega_o$. In a practical oscillator, however, the output is more generally given by:

$$V_{out} = A(t)f(\omega_o t + \phi(t)) \tag{5.2}$$

where A(t) and $\phi(t)$ are now functions of time, and f is a periodic function with a period of 2π. As a consequence of the fluctuations represented by A(t) and $\phi(t)$, the output spectrum of a practical oscillator has sidebands close to the oscillation frequency ω_o. A signal's short-term instabilities are usually

characterized and measured in terms of the single side-band spectrum density. It has units of decibels below the carrier per hertz (dBc/Hz) and is defined as:

$$L_{tatal}(\Delta\omega) = 10log(\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}} \tag{5.3}$$

where $P_{sideband}(\omega_o + \Delta\omega, 1Hz)$ represents the single sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1Hz. The above definition includes the effect of both amplitude and phase fluctuations, A(t) and $\phi(t)$. However, in an oscillator, the amplitude noise is naturally rejected by the limiting action inherent in any real implementation. Therefore, in most applications, $L_{total}(\Delta\omega)$ is dominated by its phase portion, $L_{phase}(\Delta\omega)$, known as phase noise, which is simply denoted as $L(\Delta\omega)$. Various models of oscillator phase noise have been built and evaluated. Some most important models are: (a) Leeson's model, which is based on a linear time-invariant (LTI) system assumption; (b) Hajimiri's model, which treats the oscillator as a linear, time-varying system; (c) Samori's model, which treats an oscillator as a non-linear system.

5.1.1 Linear time-invariant model phase noise analysis

Oscillators are fundamentally nonlinear system. However, linear models are often used to describe oscillator behavior. A linear model can yield a start-up condition for oscillation because oscillation at start-up is a small signal. A LC oscillator can be modelled as a positive feedback system as shown in Figure 5.1. The oscillator is constructed using an amplifier (cross-coupled transistors) and a phase shift network (LC tank). The amplifier provides no phase shift. For a sustained oscillation, Barkhausen criterion requires that the loop gain is exactly unity and the phase shift around the loop is 360 degrees. This leads to the following equations:

$$g_m R = 1 \tag{5.4}$$

$$\omega_o^2 LC = 1 \tag{5.5}$$

Noise can come from two sources in this system: the resistor and the transconductor. Resistor noise is modelled by a white thermal noise current whose density is given by:

$$i_n^2 = \frac{4kT}{R} \tag{5.6}$$

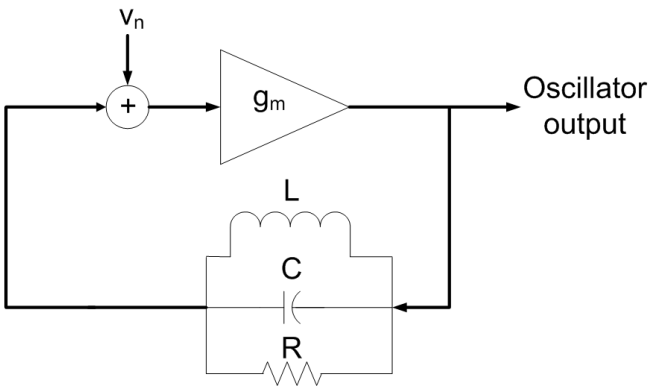


Figure 5.1: Feedback amplifier model of the LC oscillator.

Noise in the transconductor is also modelled as a white noise current whose density is given by:

$$i_n^2 = 4kTg_m\gamma \tag{5.7}$$

where γ is the noise figure of the transconductor.

The combined noise can be referred to the input of the transconductor as a white noise voltage given by:

$$v_n^2 = \frac{4kT\gamma}{g_m} + \frac{4kT}{g_m^2 R} \tag{5.8}$$

Substituting from (5.4), the input referred noise voltage at the transconductor input is given by:

$$v_n^2 = 4kTR(1+\gamma) = 4kTFR \tag{5.9}$$

where F = 1 + γ is the noise figure of the entire oscillator.

The tank impedance at a frequency $\Delta\omega$ away from the resonance frequency can be approximated by:

$$Z(\Delta\omega) = \frac{R}{1 + j2Q\frac{\Delta\omega}{\omega_o}} \tag{5.10}$$

where Q is the tank quality factor.

Using basic feedback theory, the closed-loop transfer function from the noise input to the oscillator output is given by:

$$|H(\Delta\omega)|^2 = (\frac{\omega_o}{2Q\Delta\omega})^2 \tag{5.11}$$

In noise analysis, it is customary to represent noise by a sine wave in a 1 Hz bandwidth. At the output of the oscillator, noise power at a frequency $\Delta\omega$ away from the carrier (i.e. oscillation fundamental tone) can be obtained using (5.9) and (5.11):

$$P_{n,out} = 4kTFR(\frac{\omega_o}{2Q\Delta\omega})^2 \tag{5.12}$$

The noise-to-carrier ratio is obtained by dividing the output noise by the carrier power:

$$L_{\Delta\omega} = \frac{4kTFR}{A_o^2}(\frac{\omega_o}{2Q\Delta\omega})^2 = \frac{kTFR}{A_o^2}(\frac{\omega_o}{Q})^2\frac{1}{\Delta\omega^2} \tag{5.13}$$

where A_o is the oscillation amplitude. This is the well-known Leeson's equation [28].

With the linear time-invariant model, no frequency translation of noise can occur. This means that low frequency noise, such as flicker noise, cannot create phase noise. Only the noise originating around the oscillation frequency can create phase noise. Moreover, it has to have an equivalent amount of amplitude noise because it is additive noise. In any LC oscillator, this not true. Some elements contribute pure phase noise and no amplitude noise.

5.1.2 Hajimiri's time-variant phase noise model

Hajimili has developed a time-variant oscillator model for phase noise analysis [30]. The model treats the oscillator as a linear but time-varying system and assumes that noise in an oscillator is a cyclostationary random process. Cyclostationarity means that the first and second-order statistics of the random process are periodic with a period T. Where T is the oscillation period. The model is built on the following assumptions:

1. White noise can be treated as uncorrelated random samples in time.
2. The response of the oscillator to a noise sample (current impulse) depends on the time that sample occurs with respect to the oscillation waveform such that:

- Noise that occurs at the peak of oscillation can only create amplitude noise.
- Noise that occurs at the zero-crossings of oscillation can only create phase noise.

Based on these assumptions, Hajimiri developed what is called an Impulse Sensitivity Function (ISF). It measures the sensitivity of the phase of the oscillator to a small perturbation current injected at a particular moment in time. The ISF has the same period T of the oscillator itself due to the cyclostationarity assumption. By using a Spice-like transition simulator, the ISF can be evaluated from each noise source in the oscillator to the output. An impulse of current, representing noise in a transistor channel or a resistor etc., is injected into the oscillator at one instant. The effect on the oscillator phase is evaluated after multiple cycles when the oscillator is back to its normal limit cycle. The position of the impulse is shifted with respect to the oscillation waveform and simulation is re-run to evaluate the ISF from a particular noise source at a different time point. Using a fairly tedious simulation procedure, the ISF of each noise source is constructed.

5.1.3 Samori's non-linear phase noise model

Samori [31] developed a non-linear system model for phase noise analysis of LC oscillators. From the phase noise expression (5.13), a large oscillation amplitude is required for minimizing the phase noise. However, a large oscillation amplitude leads to drive the cross-coupled transistors (transconductor) into a highly nonlinear regime. For a LC oscillator with a CMOS differential pair and a biasing current I_b, the oscillation voltage limit for driving the transistor pair into nonlinear region is:

$$V_o > \frac{2I_b}{\beta} \tag{5.14}$$

where $\beta = \mu_o C_{ox} \frac{W}{L}$.

A key property of nonlinear circuits is that they respond differently to AM and PM noise. For example, if an AM input is applied to a differential pair, whose output is clipped by the large voltage amplitude, the output voltage is not affected by this AM input. However, if an PM input is applied, the output voltage is affected by it. In the following, the relationship between the carrier-to-PM sideband ratio of the input and the carrier-to-PM ratio of the output is

investigated. Furthermore, it was proven that in any nonlinear circuits without any reactive elements, there is no AM to PM conversion. Therefore, in the following noise analysis. AM noise is omitted because it has no contribution to phase noise [33].

A noise at a fixed offset $\Delta\omega$ from the carrier as shown in Figure 5.2 can be decomposed into equal amounts of amplitude and phase modulation. Both forms of modulation have components at $\omega_+ = \Delta\omega$ and $\omega_- = -\Delta\omega$.

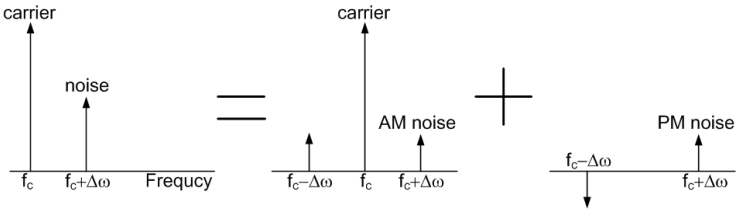


Figure 5.2: Single noise tone decomposed into AM and PM component.

Assuming the input of the transconductor consists of a carrier, $V_c = V_o cos(\omega_o t)$, and a lower sideband, $V_{lsb} = V_m cos((\omega_o - \omega_m)t + \phi$, located at $\omega_o - \omega_m$, if the transconductor characteristic is I = I(V) and the amplitude of V_{lsb} is much smaller than the amplitude of V_c, then the transconductor output is approximately given by:

$$I(V_c(t) + V_{lsb}(t)) \approx I(V_c(t)) + \frac{dI}{dV}|_{V_c(t)} V_{lsb}(t) \tag{5.15}$$

The derivative dI/dV is the transconductance g(V) = dI/dV, which, in the above equation, is evaluated in presence of the carrier only. For the case of a cross-coupled differential pair, the transconductance $g(V_c(t))$ is an even function of time with a fundamental component at $2\omega_c$ as shown in Figure 5.3. The corresponding Fourier series is given by:

$$g(V_c(t)) = g_0 + \sum_{n=1}^{\infty} (g_{2nI} cos(2n\omega_o t) + g_{2nQ} sin(2n\omega_o t)) \tag{5.16}$$

Because the transconductance is an even function, the quadrature terms g_{2nQ} are equal to zero.

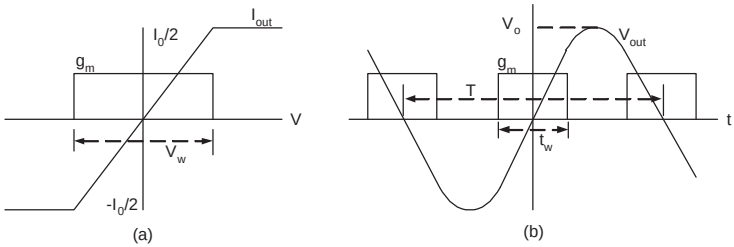


Figure 5.3: (a) Characteristic of a cross-coupled differential pair with transconductance. (b) Transconductance turns on at twice the carrier frequency and is an even function.

The amplitude of the fundamental of the output current is derived using (5.15). This term can be noted as $I_c(t)$. Since:

$$\frac{dI}{dt} = \frac{dI}{dV}\frac{dV}{dt} = g(V)\frac{dV}{dt} \tag{5.17}$$

$I_c(t)$ may be written as:

$$I_c(t) = I(V_c(t)) = \int g(V_c(t))\frac{dV_c}{dt}dt \tag{5.18}$$

This equation shows that mixing between the transconductance function and the derivative causes different terms of g(V) to fall at ω_o. For example, the second harmonic of g(V) mixes with the carrier to generate component at $3\omega_o$ and ω_o. For oscillators, only the terms at ω_o are of interest since the resonator attenuates any out-of-band tones. A final value of $I_c(t)$ is given below. The transconductance terms are combined and referred to the effective transconductance:

$$I_c(t) = (g_0 - \frac{g_{2I}}{2})V_o cos(\omega_o t) = g_{eff}V_o cos(\omega_o t) \tag{5.19}$$

The inter-modulation tones that result from the lower sideband, V_{lsb}, are described by the second term of (5.15). The resulting current tones that fall near the carrier are given by:

$$I_{m1} = g_0 V_m cos((\omega_o - \omega_m)t + \phi) + \frac{g_{2I}}{2}V_m cos((\omega_o + \omega_m)t - \phi) \tag{5.20}$$

If the lower sideband is part of a phase modulation pair, then the upper sideband, V_{usb} must be:

$$V_{usb}(t) = -V_m cos((\omega_o + \omega_m)t + \phi) \tag{5.21}$$

The resulting current tones from this sideband are:

$$I_{m2} = -g_0 V_m cos((\omega_o + \omega_m)t - \phi) - \frac{g_{2I}}{2} V_m cos((\omega_o - \omega_m)t + \phi) \quad (5.22)$$

The total output sidebands are:

$$\begin{aligned} I_{mt} \; = \; & -V_m(g_0 - \frac{g_{2I}}{2})(cos((\omega_o - \omega_m)t + \phi) - \\ & cos((\omega_o + \omega_m)t - \phi)) \end{aligned} \quad (5.23)$$

The output carrier-to-sideband ratio is easily calculated by using (5.19) and (5.23):

$$\frac{I_c}{I_{mt}} = \frac{(g_0 - \frac{g_{2I}}{2})V_o}{(g_0 - \frac{g_{2I}}{2})V_m} = \frac{V_o}{V_m} \quad (5.24)$$

This result proves that in a nonlinear element, the ratio of the carrier to the PM sidebands at the input is equal to the output. Based on this property, if the cross-coupled differential pair in a switched current oscillator is driven by an oscillation on which phase noise side band are superimposed, the output current carrier-to-noise ratio is the same as the carrier-to-noise ratio of the input. This fact greatly simplifies the phase noise analysis.

5.1.4 Phase noise analysis of LC oscillator based on Samori's model

Based on Samori's nonlinear phase noise model, Hagazi [33] made analysis of phase noise of CMOS cross-coupled LC oscillators with the noise sources coming from the tank resistance, the differential pair and the tail current respectively.

PHASE NOISE CAUSED BY THE THERMAL NOISE OF THE TANK RESISTANCE
The phase noise caused by resistor thermal noise in the resonator tank can be calculated by using the following principles:

- The resonator noise can be decomposed into a series of sinewave. Each sinewave noise can be decomposed into equal parts of PM and AM sidebands.
- Because there is no AM to PM conversion, only PM noise components cause the output phase noise.
- Using the conclusion of Samori's model that the ratio of the carrier to the PM sidebands at the input equals that at the output.

The calculated output phase noise is given by:

$$v_n = \frac{kT}{R}\frac{L\omega_o^2}{\Delta\omega} \tag{5.25}$$

$$L(\Delta\omega) = \frac{4kTR}{V_o^2}(\frac{\omega_o}{2Q\Delta\omega})^2 \tag{5.26}$$

PHASE NOISE CAUSED BY THE THERMAL NOISE OF THE DIFFERENTIAL PAIR Noise injected into the LC resonator only when the both transistors of the differential pair are active. If one transistor is off, it obviously contribute no noise, and neither does the other transistor that is on because it acts as a cascade transistor whose current is fixed by the tail current. As shown in Figure 5.3, when the differential pair is in active linear region, the transconductance of the differential current, the current that actually flows through the resonator, is $G_m = I_0/V_w$, which is half the transconductance of the individual devices. As oscillation occurs, the instantaneous transconductance toggles with time between G_m and 0. The phase noise caused by the thermal noise of the differential pair is given by:

$$i_n = v_n G_m(t) \tag{5.27}$$

where v_n is the input referred voltage noise and $G_m(t)$ is the transconductance of the differential pair. Since the transconductance is varying with time, the output noise appears as pulse of noise current with a pulse width equal to the duration when the differential pair is in the linear region. Figure 5.4 shows the process to calculate the noise generated by the switching differential pair. The noise pulse in the time domain is shown in Figure 5.4 (a). In the frequency domain, the noise envelope is the pulse shaped with a sin(x)/x envelope with the first null at $1/t_w$ where t_w is the pulse width in the time domain. An important characteristic is that the frequency domain pulses only appear at the even harmonics of the oscillation frequency. This mixing process causes noise folding to occur, allowing noise from many frequency locations to congregate at one point near the oscillation frequency. The frequency spectrum of the noise pulses is convolved with the white noise density, as shown in Figure 5.4 (c) and (d), to produce the output noise.

First, let us suppose that there is a noise just above the oscillation frequency (labelled '1' in Figure 5.4c), this convolves with the first two components of the noise pulse located at DC and $2\omega_o$, and produces a pair of

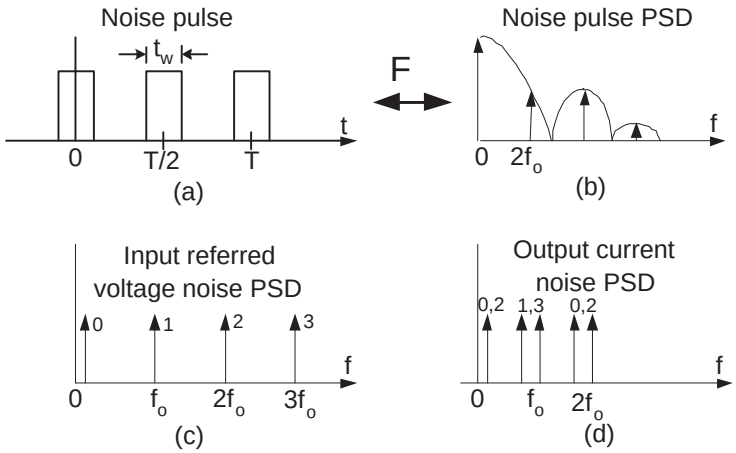


Figure 5.4: (a) Noise in the differential pair appears as noise pulse in the time domain, (b) (c) In the frequency domain, these pulses are the results of a convolution between a sin(x)/x function and the white noise PSD of the transistor, (d) The result of the convolution in the frequency domain shows only the noises at the oscillation frequency and the odd multiples are important.

sidebands around the carrier. Next, let us consider the noise near the second harmonic (labelled '2' in Figure 5.4c). This convolves with the first three components of the noise pulses (DC, $2\omega_o$, and $4\omega_o$) to produce phase noise sidebands, which are far away from the carrier. Finally, the noise at the third harmonic convolves with the second and third components of the noise pulses to again produce phase noise around the carrier. So it is clear that only the noise at the oscillation frequency and its odd multiples is important. Also, the noise is eventually band-limited by the sinc envelope. There are a number of ways to calculate the summation of the convolution terms as the sin(x)/x function decays. A simplified method is presented here: the sinc function of the noise pulses in the frequency domain is approximated as having impulses with constant amplitude up to $1/t_w$ and zero elsewhere. The DC component, g[0] is just the DC value of the time domain waveform:

$$g[0] = G_m \frac{t_w}{T/2} = 2G_m \frac{t_w}{T} \tag{5.28}$$

For $t_w << T$, we have:

$$\frac{V_w}{2} = V_o sin(\omega_o \frac{t_w}{2}) \approx V_o \omega_o \frac{t_w}{2} \Rightarrow \frac{t_w}{T} = \frac{V_w}{2\pi V_o} \tag{5.29}$$

Since all the non-zero terms are equal to g[0], the frequency domain function is fully described. Now, the gain from a noise located above the carrier to output noise can be calculated. The DC term mixes with the upper sideband of the voltage noise to produce an output noise current located at the upper sideband. This is shown in the following equation:

$$i_{n,usb} = v_{n,usb} g[0] = v_{n,sub} \frac{2I_0}{V_w} \frac{V_w}{2\pi V_o} = v_{n,usb} \frac{I_0}{V_o \pi} = \frac{v_{n,usb}}{2R} \tag{5.30}$$

Since each frequency term convolves with white noise, the final answer is simply the sum of the square of the frequency domain envelope times the white noise. Because all the frequency terms are equal, only the number is required. This is just the bandwidth divided by $2f_o$:

$$N_{fold} = \frac{1/t_w}{2f_o} = \frac{1}{2f_o t_w} \tag{5.31}$$

The final output noise power is obtained as

$$i_{on}^2 = \frac{v_n^2}{4R^2} N_{fold} N_{dev} \tag{5.32}$$

The equivalent voltage noise is set by the transconductance of the individual transistors:

$$v_n^2 = \frac{4kT\gamma}{g_m} \tag{5.33}$$

After substituting the value of the voltage noise, the folding term, and the number of transistors, the final output noise is calculated:

$$i_{on}^2 = 4kt\gamma \frac{I_0}{\pi V_o} \tag{5.34}$$

This equation shows that the output current noise density caused by the differential pair only depends on the amplitude and the bias current, and not on the transistor size.

The final phase noise due to the differential pair is calculated by scaling the output current noise by the loss of the tank and normalizing it by the amplitude of the fundamental:

$$L(\Delta\omega) = \frac{8kT\gamma I_0 R^2}{\pi V_o^3} (\frac{\omega_o^2}{2Q\Delta\omega}) \tag{5.35}$$

PHASE NOISE CAUSED BY THE THERMAL NOISE OF THE TAIL CURRENT The third noise source in differential LC oscillators is the biasing current. Any noise from biasing current is commutated and frequency translated by the differential pair as in a single balanced mixer, and injected into the LC tank. Let us assume that the oscillation amplitude is much larger than the transition region of the differential pair, in this case, the current flowing through the LC tank is more like a square wave than a sine wave, as show in Figure 5.5. In the frequency domain, the PSD of this square wave has components only at the oscillation frequency and its odd multiples. After the convolution between the tail current noise and the PSD of the square wave, only the noise located at the DC and the even harmonics will be translated into noise around the oscillation frequency.

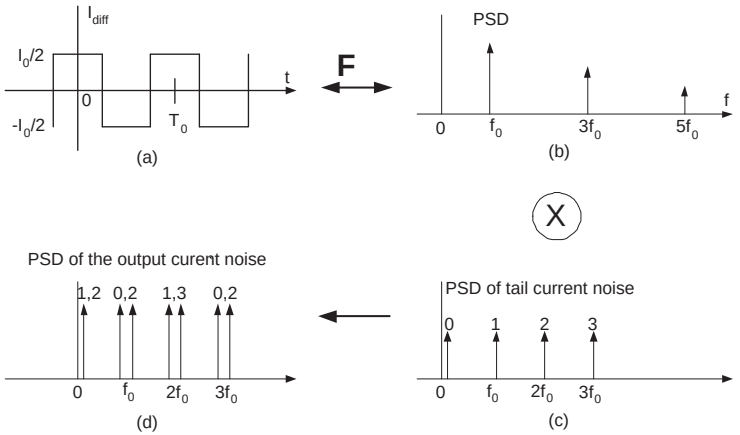


Figure 5.5: (a) (b) Output current of the differential pair and its PSD (c) PSD of the tail current noise, (d) The result of the convolution in the frequency domain shows that only the noises at DC and odd multiples are important.

For example, the noise at DC and the second harmonic of the oscillation frequency is modelled as:

$$i_{n,in} = i_{n0} cos\Delta\omega_0 t + i_{n2} cos(2\omega_o + \Delta\omega_2)t \tag{5.36}$$

The square wave function is modelled as:

$$f(t) = \frac{2}{\pi}(cos\omega_o t + \frac{1}{3}cos3\omega_o t + \cdots) \tag{5.37}$$

The convolution between the noise and the square wave function is truncated to the frequency of interest and given by:

$$\begin{aligned} i_{n,out} &= \frac{i_{n0}}{\pi}(cos(\omega_o + \Delta\omega_0)t + cos(\omega_o - \Delta\omega_0)t) + \\ &\quad \frac{i_{n2}}{\pi}(cos(\omega_o + \Delta\omega_2)t + \frac{1}{3}cos(\omega_o - \Delta\omega_2)t) \end{aligned} \tag{5.38}$$

From the above equation, the low frequency noise $i_{n0}cos(\Delta\omega_0 t))$ is mixed into a pair of the sidebands around the carrier and injected into the tank. These are AM sidebands and therefore not important. However, any varactor connected to the resonator will convert AM noise into FM noise, which will produce phase noise [32]. The output noise current caused by the noise around the second harmonic $i_{n2}cos(2\omega_o + \Delta\omega_2)t$ are separated into PM and AM components:

$$\begin{aligned} i_{n,out} &= \frac{i_{n2}}{\pi}\frac{2}{3}(cos(\omega_o + \Delta\omega_2)t + cos(\omega_o - \Delta\omega_2)t) + \\ &\quad \frac{i_{n2}}{\pi}\frac{1}{3}(cos(\omega_o + \Delta\omega_2)t - cos(\omega_o - \Delta\omega_2)t) \end{aligned} \tag{5.39}$$

To calculate the total noise, all the noise located at DC and even harmonics must be included. Since all the noise sources are uncorrelated, the total output noise can be obtained by powerwise summing the noise due to each component. Additionally, only the PM component is included. The calculated result of the total phase noise is given by: [33]

$$L(\Delta\omega) = \frac{kT\gamma g_{m,tail}R^2}{V_o^3}(\frac{\omega_o}{2Q\Delta\omega})^2 \tag{5.40}$$

TOTAL PHASE NOISE OF CMOS DIFFERENTIAL LC OSCILLATORS DUE TO THERMAL NOISE From the equations (5.26), (5.35) and (5.40), the total phase noise of a CMOS differential LC oscillator due to thermal noise is derived:

$$L(\Delta\omega) = \frac{4kTR}{V_o^2}(1 + \frac{2\gamma I_0 R}{\pi V_o} + \frac{\gamma g_{m,bias}R}{4}(\frac{\omega_o}{2Q\Delta\omega})^2 \tag{5.41}$$

where γ is the noise factor of a single MOSFET, R is the equivalent parallel resistance of the LC tank, V_o is the voltage amplitude of the oscillator output, $g_{m,tail}$ is the small signal transconductance of the tail transistor, and Q is the quality factor of the tank.

Equation (5.41) consists of three terms. The first is due to noise in the resonator tank, The second term is due to noise in the differential pair. The third term results from the biasing current source. This completely specifies the phase noise in the white noise region.

FLICKER NOISE INDUCED PHASE NOISE In the previous analysis of phase noise, the low frequency noise in the differential pair contributes to the output noise at DC and second harmonic frequencies. The low frequency noise in the tail current only causes AM output noise. However, the flicker noise in MOSFETs does contribute to phase noise near the oscillation frequency. Phase noise measurements show that the slope of the phase noise spectrum in CMOS VCOs increases from -20 to -30 dB/decade as frequencies approach the carrier. Some mechanisms of flick noise up-conversion are presented in [34] [35] [41].

Flicker noise upconversion due to the oscillation frequency dependency on the bias current As discussed before, in a LC differential oscillator, the current flowing over the differential pair is more like a square-wave, which is rich in harmonics. Normally, these harmonics are neglected for the LC tank, but they must flow somewhere in the circuit. In fact at these high frequencies, the capacitor in the tank offers the lowest impedance path and upsets the exact reactive power balance between the L and the C required for steady state. As a result, the actual steady-state oscillation frequency does not coincide with the tank natural frequency $\omega_0 = \frac{1}{\sqrt{LC}}$, but shifts down until the reactive power in the inductor increases to equal the reactive power in the capacitor due to fundamental and all harmonics. The frequency shift, $\Delta\omega$, from the natural frequency ω_0, can be expressed as [42]:

$$\frac{\Delta\omega}{\omega_0} = \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2(1-n^2)}{(1-n^2)^2 + n^2/Q^2} m_n^2 \tag{5.42}$$

The normalized change in frequency depends on the harmonic levels m_n, and the quality factor Q of the tank. If noise modulates the harmonic level, it will cause frequency modulation that contributes to phase noise. The amount of

the harmonic content is a function of the bias current I_0. A larger bias current produces a larger oscillation amplitude, which generates a current waveform that is switched more quickly and contains a higher harmonic content. The sensitivity $\partial\omega/\partial I_0$ is responsible for indirect FM due to flicker noise in I_0.

Flicker noise upconversion due to differential pair In a LC differential oscillator, the oscillation causes a voltage waveform with twice the oscillation frequency at the common node of the differential pair. So, as shown in Figure 5.6, the parasitic capacitance at the tail presents a negative capacitance at the differential output [43]. This speeds up the oscillation frequency. Flicker noise in the differential pair modulates the duty cycle voltage at the tail capacitance, and therefore the effective negative capacitance. This results in random FM that upconverts the flicker noise in the differential pair into close-in phase noise.

In the current-limited regime, the tail current governs the steady-state oscillation amplitude. Therefore, flicker noise in the tail current produces low frequency random AM. The random AM envelope modulates the effective capacitance of the varactor, converting AM into FM. The FM sidebands appear as close-in phase noise.

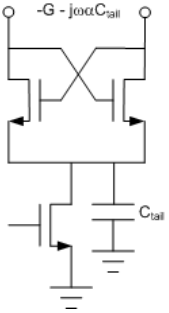


Figure 5.6: Parasitic capacitor at the tail node appears as reactances across the resonator.

In [32], Hegazi analyzed and explained how the varactor converts AM noise into FM noise. An LC oscillator behaves like a quasi sinusoidal model. This means that although the sustaining square wave current is rich in har-

monics, the harmonics do not play an important role within the tank due to fairly high quality factor of the tank. The fundamental component of the square current defines the steady-state amplitude. The harmonics in the square current take the path of the least impedance, which is the capacitor. The resulting harmonic voltage amplitudes across the tank are related as:

$$Fundamentalvoltage \propto \frac{IQ}{\omega_0 C} \tag{5.43}$$

$$nthharmonicvoltage \propto \frac{1}{n}\frac{I}{n\omega_0 C} \tag{5.44}$$

$$\Rightarrow Fundamental/nthharmonic = n^2 Q \tag{5.45}$$

It can be seen that in a tank with a reasonably high quality factor Q, the amplitudes of the third and higher harmonics can be neglected compared to the fundamental.

Flicker noise upconversion through the varactor A varactor is usually a voltage-dependent capacitor whose capacitance depends on a control voltage V_c. Figure 5.7 shows a typical accumulation MOS varactor and its characteristic. The standalone varactor is specified by its small-signal capacitance C_{ss} versus V_c. This is defined in terms of the instantaneous charge Q and the voltage V across the varactor:

$$C_{ss} = \frac{dQ}{dV}|_{V_c} \tag{5.46}$$

When V_c is fixed, the small-signal capacitance of the varactor changes periodically with the oscillation because the oscillation amplitude is normally large in order to minimize phase noise. The periodic small-signal capacitance of the varactor can be represented as a Fourier series:

$$C_{ss} = \sum_{n=0}^{\infty} C_{2n} cos(2n\omega_0 t) \tag{5.47}$$

After counting for the harmonics in the output voltage and the mixing that occurs, an effective capacitance that is seen by the oscillator is given by:

$$C_{eff} = C_0 - \frac{1}{2}C_2 \tag{5.48}$$

The first term C_0 is the time-average capacitance, which includes any fixed capacitance in parallel with the varactor. The second term C_2 is the second-order Fourier coefficient of the nonlinear varactor driven by the oscillation. C_{eff} depends on the average voltage V_c present across the varactor. It depends also on the amplitude of oscillation. Any fluctuations in the oscillation amplitude due to noise can cause fluctuations in C_{eff} and thus in frequency, this is a process called AM-to-FM conversion.

5.2 Phase noise and jitter of CMOS ring oscillator

CMOS ring oscillators are usually implemented with either single-ended inverters or differential delay stages. Their phase noise or jitter generation mechanism are different from that of LC tank based oscillators. Several publications [36] [37] [27] [39] studied and discussed phase noise and jitter in CMOS ring oscillators. In the following, we summarize the phase noise and jitter analysis in CMOS ring oscillators from the publications.

5.2.1 Relation between jitter and phase noise

The time jitter in a normal periodic signal can be considered as fluctuations in phase at the discrete set of zero-crossing instant t_i. The fluctuations are caused by the phase noise of an oscillator, which defines a continuously evolving stochastic process $\phi(t)$. Thus, after one cycle of nominal period $\tau_0 = \frac{1}{f_0}$, jitter and phase are related as follows:

$$\tau_i = \frac{\phi(t_{i+1}) - \phi(t_i)}{2\pi}\tau_0 = \frac{\Delta\phi_i}{2\pi f_0} \tag{5.49}$$

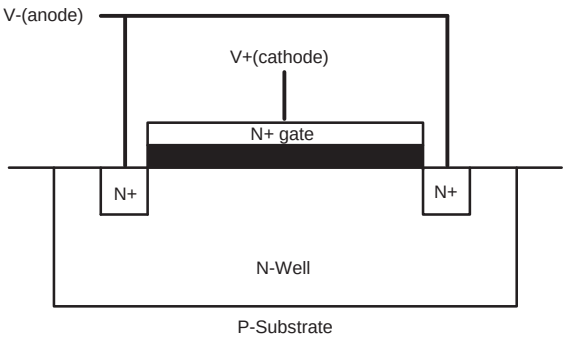
The power spectral density (PSD) of $\Delta\phi$ can be expressed as:

$$S_{\Delta\phi}(f) = S_\phi(f)|1 - e^{-j2\pi f/f_0}|^2 = 4S_\phi(f)sin^2(\pi f/f_0) \tag{5.50}$$

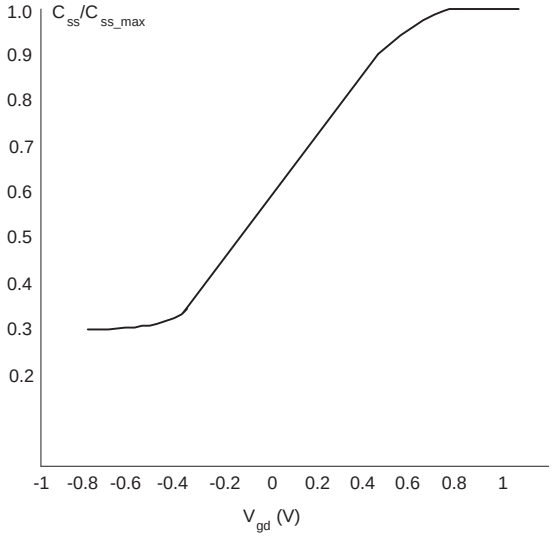
From (5.49) and (5.50) follows the PSD of jitter:

$$S_\tau(f) = S_\phi(f)\frac{sin^2(\pi f/f_0)}{(\pi f_0)^2} \tag{5.51}$$

This is the spectrum of the jitter quantity τ sampled at f_0, and is therefore defined over the frequency range $(0, f_0)$. In practice, more important than the spectral density of jitter is its mean-square value σ_τ^2, as would be measured



(a) Cross section of a typical accumulation MOS varactor



(b) Example of a small signal capacitance versus voltage curve MOS varactor

Figure 5.7: Typical accumulation MOS varactor and its characteristic.

on a digital oscilloscope. Using the Wiener-Khinchine theorem, σ_τ^2 can be calculated from the PSD:

$$\sigma_\tau^2 = \int_0^\infty S_\tau(f)df = \int_0^\infty S_\phi \frac{sin^2(\pi f/f_0)}{(\pi f_0)^2 df} \tag{5.52}$$

This is the general form of the link between jitter and phase noise.

In [40], Demir shows that in an oscillator with white noise sources alone, the Single-Side-Band (SSB) phase noise PSD at a frequency offset f is given by:

$$L(f) = \frac{S_\phi(f)}{2} = \frac{S_w}{f^2} \tag{5.53}$$

where S_w is a coefficient specific to an oscillator and its noise source. In this case, the expression in (5.52) can be evaluated exactly:

$$\sigma_\tau^2 = \frac{2S_w}{\pi f_0^3}\int_0^\infty \frac{sin^2 x}{x^2}dx = \frac{S_w}{f_0^3} \tag{5.54}$$

Thus, the relation between phase noise PSD and jitter variance is finally given by:

$$L(f) = \sigma_\tau^2 \frac{f_0^3}{f^2} \tag{5.55}$$

5.2.2 Phase noise in inverter-based ring oscillator

INVERTER JITTER DUE TO WHITE NOISE An simple inverter ring oscillator is shown in Figure 5.8. For simplicity, we assume that the input of the inverter is a GND-to-VDD step signal, and the current of the NMOS transistor equals its saturation current even if it will enter triode region during the propagation delay. The saturation current of the NMOS transistor is:

$$I_{NSAT} = \frac{\mu C_{ox}}{2}\frac{W}{L}(VDD - V_{NTH})^2 \tag{5.56}$$

This current is accompanied by a noise current i_n from the transistor. The spectral density of the noise current is given by:

$$S_{i_n} = 4kT\gamma_N g_m = 8kT\gamma_N \frac{I_{NSAT}}{VDD - V_{NTH}} \tag{5.57}$$

We define the propagation delay t_d as the time from the input step to when the output ramp crosses the next inverter's toggle point, which is supposed

to be at 1/2 VDD. Along with the saturation current I_{NSAT}, the noise current i_n integrates on the load capacitor C over a time window t_d to form a noise voltage v_n that modulates the time of the threshold crossing. The dynamics of the threshold crossing is described by:

$$\int_0^{t_d} \frac{I_{NSAT} + i_n}{C} = \frac{VDD}{2} \tag{5.58}$$

and the jitter can be related to the variance of the propagation delay t_d:

$$\sigma_{t_d}^2 = \frac{1}{I_{NSAT}^2} \langle (\int_0^{t_d} i_n)^2 \rangle \tag{5.59}$$

Thus, as already analyzed in the last section, the spectral density of t_d is:

$$S_{t_d} = \frac{t_d^2}{I_{NSAT}^2} sinc^2(f t_d) S_{i_n} \tag{5.60}$$

and then using Wiener-Khinchine theorem to find the mean-square value:

$$\langle t_d^2 \rangle = \int_0^\infty S_{t_d} df = \frac{t_d}{\pi I_{NSAT}^2} S_{i_n} \int_0^\infty \frac{sin^2 x}{x^2} dx \tag{5.61}$$

Using (5.57) this simplifies to:

$$\sigma_{t_d}^2 = \frac{4kT\gamma_N t_d}{I_{NSAT}(VDD - V_{NTH}} \tag{5.62}$$

This is a compact expression for the jitter of propagation delay caused by current noise integration on the load capacitor C.

In addition to this jitter, prior to each switching event, a random noise voltage with mean-square value of $\frac{kT}{C}$ resides on C, arising from the noise in the PMOS/NMOS transistor triode resistance. Thus, the total propagation jitter of an inverter stage due to white noise is:

$$\sigma_{t_d}^2 = \frac{4kT\gamma_N t_d}{I_{NSAT}(VDD - V_{NTH}} + \frac{kTC}{I_{NSAT}^2} \tag{5.63}$$

The period of a ring oscillator is defined by the time it takes for a transition to propagate twice around the ring. for a ring oscillator comprising M inverter stages, the nominal oscillation frequency f_0 is:

$$f_0 = \frac{1}{M(t_{dNMOS} + t_{dPMOS}} = \frac{2}{MCVDD}(\frac{1}{I_{NSAT}} + \frac{1}{I_{PSAT}}) = \frac{I}{MCVDD} \tag{5.64}$$

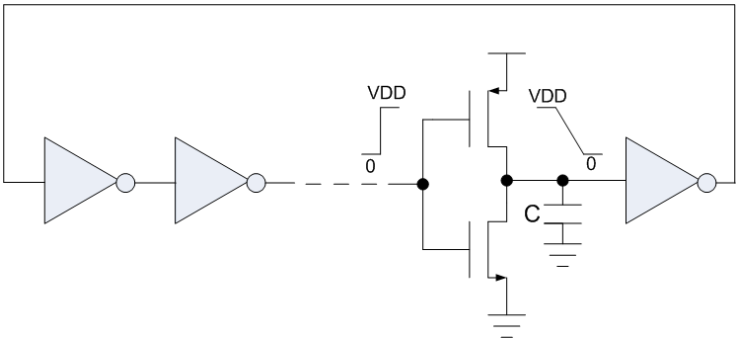


Figure 5.8: A simple inverter-based ring oscillator.

by assuming that the PMOS and NMOS have the same saturation current I to charge/discharge the load capacitor during pullup/pulldown transitions, and the toggle point for both of rising and falling event is symmetric at $\frac{VDD}{2}$.

Every propagation delay is jittered by the noise in the pullup or pulldown process. These noise events are uncorrelated and can be added in the mean-square. Therefore, the variance of period jitter is:

$$\sigma_\tau^2 = M(\sigma_{t_{dNMOS}}^2 + \sigma_{t_{dPMOS}}^2) \tag{5.65}$$

Using (5.63) (5.64), and assuming that NMOS and PMOS transistors have the same threshold voltage V_{th}, we get the jitter variance of the ring oscillator:

$$\sigma_\tau^2 = \frac{kT}{If_0}\left(\frac{2(\gamma_N + \gamma_P)}{VDD - V_{TH}} + \frac{2}{VDD}\right) \tag{5.66}$$

Using (5.55), the SSB phase noise due to white noise is now found from the jitter:

$$L(f) = \frac{2kT}{I}\left(\frac{\gamma_N + \gamma_P}{VDD - V_{TH}} + \frac{1}{VDD}\right)\left(\frac{f_0}{f}\right)^2 \tag{5.67}$$

The following conclusions can be drawn from this compact expression for phase noise:

1. The phase noise is independent of the number of inverter stages, and only dependent on the frequency of oscillation f_0.

2. The only technology dependent parameters affecting phase noise and jitter are the threshold voltages of MOS transistors V_{th} and excess noise factor γ.
3. For low phase noise and jitter designs, using as high a supply voltage as possible, and burn as much current as the budget allows.

PHASE NOISE DUE TO FLICKER NOISE In an inverter based ring oscillator, the pullup and pulldown currents contain flicker noise which may not fluctuate over a single transition, but varies slowly over many transitions. Suppose I_{Nk} and I_{Pk} are the pulldown and pullup currents supplied, respectively, by the NMOS transistor and the PMOS transistor in the kth inverter stage of a M-stage ring oscillator. Then the oscillation frequency is expressed as:

$$f_0 = \frac{2}{CVDD}(\Sigma_{j=1}^{M}(\frac{1}{I_{Nj}} + \frac{1}{I_{Pj}}))^{-1} \tag{5.68}$$

In a symmetrically designed inverter, the pull-up and pull-down current are equal. The sensitivity of f_0 to the pulldown current I_{Nk} is:

$$\frac{\partial f_0}{\partial I_{Nk}} = \frac{CVDDf_0^2}{2I_{Nk}^2} = \frac{f_0}{2MI} \tag{5.69}$$

Using the narrowband FM expression [32], the SSB phase noise resulting from flicker noise in the kth pull-down current can be deduced:

$$S_{f_0}(f) = (\frac{\partial f_0}{\partial I_{Nk}})^2 S_{i_{Nk}}^{1/f}(f) \tag{5.70}$$

$$L(f) = \frac{S_{f_0}(f)}{4f^2} = \frac{S_{i_{Nk}}^{1/f}(f)}{4f^2}(\frac{f_0}{2MI})^2 \tag{5.71}$$

where $S_{i_{Nk}}^{1/f}$ is the flicker noise PSD of the pull-down current I_{Nk}. Then, the total phase noise of the M-stage ring oscillator due to flicker noise is:

$$L(f) = \frac{1}{16MI^2}(S_{i_N}^{1/f}(f) + S_{i_P}^{1/f}(f))(\frac{f_0}{f})^2 \tag{5.72}$$

One of the most used flicker noise models is:

$$S_{v_n}^{1/f} = \frac{K_f}{WLC_{ox}f} \tag{5.73}$$

where K_f is an empirical coefficient. The corresponding current flicker noise is:

$$S_{in}^{1/f} = g_m^2 S_{v_n}^{1/f} = (\frac{2I}{VDD - V_{th}})^2 \frac{K_f}{WLC_{ox}f} \tag{5.74}$$

Using this flicker noise model, the final expression for SSB phase noise induced by flicker noise is obtained:

$$L(f) = \frac{C_{ox}}{8MI}(\frac{\mu_N K_{fN}}{L_N^2} + \frac{\mu_P K_{fP}}{L_P^2})(\frac{f_0^2}{f^3}) \tag{5.75}$$

This expression gives design insight:

1. To lower flicker noise upconversion into phase noise, choose large W/L to burn as much current as the budget allows.
2. Use MOS transistors with the longest channel length which is possible.
3. As the ring oscillator's average current does not depend on the number of stages M, use the largest number of stages.

5.2.3 Phase noise in differential ring oscillators

A differential ring oscillator consists of several differential delay stages connected in series. The advantage of differential ring oscillator is that the noise from the supply and the substrate appears as common mode on both outputs, and is rejected by the next stage. A typical differential delay stage is shown in Figure 5.9. It consists of a differential pair, a tail current transistor, capacitor loads and resistor loads. In actual circuits, the resistor R_L is realized with a single or compound MOSFET working in triode region, embedded in an amplitude control loop.

The propagation delay of the differential delay stage is defined as the time t_d between an input step and the zero crossing of the differential output voltage. The differential peak output voltage swing is:

$$V_{op} = I_b R_L \tag{5.76}$$

As the loads are RC circuits, the propagation delay and the oscillation frequency are determined by decaying exponentials:

$$t_d = \frac{C_L V_{op} ln2}{I_b} = R_L C_L ln2 \tag{5.77}$$

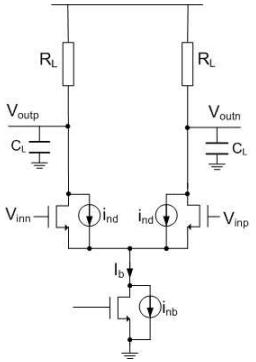


Figure 5.9: A typical differential delay stage in ring oscillators.

$$f_0 = \frac{1}{2Mt_d} \tag{5.78}$$

The differential pair has an input transition range of:

$$V_{id} = \pm\sqrt{2}V_{eff} \tag{5.79}$$

over which it steers the tail current. V_{id} is the input differential voltage, and V_{eff} is the effective gate voltage on the differential pair at balance.

PHASE NOISE DUE TO WHITE NOISE We analyze the jitter at the moment of the zero crossing of the output differential voltage by looking at the fluctuations in voltage of the zero crossing moment. As before, jitter is found by dividing the noise voltage by the slope of the differential output voltage V_{od} at zero crossing. The slope is:

$$\frac{dV_{od}}{dt} = \frac{I_b}{C_L} \tag{5.80}$$

At first, we consider the noise due to the load resistors. This noise is continuously coupled into the load capacitors, and its differential mean square values is:

$$\overline{v_{nR_L}^2} = \frac{2kT}{C_L} \tag{5.81}$$

In the next, we consider the noise in the bias current transistor i_{nb}. The noise current of the tail transistor is periodically steered from one side to another during the transition process. By assuming the tail current is steered all at once, the differential output noise can be expressed as [39]:

$$\overline{v_{nb}^2} = \frac{kT}{C_L}\gamma g_{mb} R_L \tag{5.82}$$

where g_{mb} is the small signal transconductance of the tail transistor.

At the end, we consider the noise in the differential pair. During the transition time, noise i_{nd} in the differential pair modulates the fraction of the tail current being steered from one side to the other. To simplify analysis, we assume that the noise current PSD in both transistors are the same as in the balanced condition during the transition process. The equivalent circuit for the flowing noise current during the transition period can be shown in Figure 5.10.

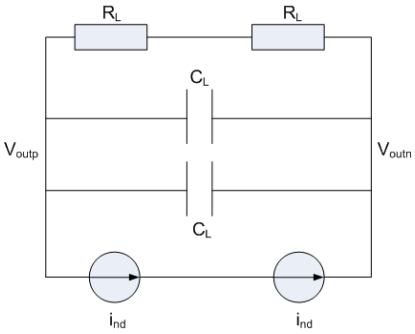


Figure 5.10: Equivalent circuit with the noise current in the differential pair during the transition period.

The PSD of i_{nd} is:

$$S_{i_{nd}} = 4kT\gamma\frac{I_b/2}{V_{effd}} = \frac{2kT\gamma I_b}{V_{effd}} \tag{5.83}$$

where V_{effd} is the effective gate voltage of the differential pair at balance. The mean square value of the differential noise voltage after the transition time t_d is [39]:

$$\overline{v_{nd}^2} = \frac{3}{8C_L}4kT\gamma\frac{I_b R_L}{V_{effd}} \tag{5.84}$$

By summing the uncorrelated noise contributions expressed by (5.81) (5.82) (5.84) and using (5.80) to calculate the period jitter, we obtain the variance of the period jitter:

$$\sigma_\tau^2 = 2M\sigma_{t_d}^2 = 2M\frac{\overline{v_n^2}}{(I_b/C_L)^2} \tag{5.85}$$

$$\sigma_\tau^2 = \frac{2kT}{I_b f_0 ln2}[\gamma(\frac{3}{4V_{effd}} + \frac{1}{V_{effb}}) + \frac{1}{V_{op}}] \tag{5.86}$$

Using (5.55), SSB phase noise due to white noise in the differential ring oscillator is obtained:

$$L(f) = \frac{2kT}{I_b ln2}[\gamma(\frac{3}{4V_{effd}} + \frac{1}{V_{effb}}) + \frac{1}{V_{op}}](\frac{f_0}{f})^2 \tag{5.87}$$

PHASE NOISE DUE TO FLICKER NOISE Flicker noise in the differential pair does not cause phase noise. The flicker noise of the differential pair can be considered as an input offset voltage that varies slowly. In response to a transition in the differential input, the offset voltage either advances or retards the rising edge, and vice-versa the falling edge. When the input offset is constant over one period, it changes the duty cycle of the output without affecting the period. Duty cycle variations create second harmonic. Therefore, the flicker noise in the differential pair is upconverted to $2f_0$, but does not appears around the oscillation frequency f_0.

Flicker noise in the tail current modulates the delay directly. While the fluctuations originating in the tail current of each stage are uncorrelated, the delay variations in all stages will add in phase and cause a large phase deviation and noise. The sensitivity of the oscillation frequency to tail current k_I can be derived from (5.77) and (5.78):

$$k_I = \frac{df_0}{dI_b} = \frac{f_0}{I_b} \tag{5.88}$$

Then the phase noise due to the noise in the bias current is obtained by using the narrowband FM expression [32]:

$$L(f) = \frac{k_I^2}{4f^2}S_I(f) = \frac{1}{4I_b^2}(\frac{f_0}{f})^2 S_I(f) \tag{5.89}$$

Using the expressions given previously for flicker noise (5.73) and (5.74), the resulting SSB phase noise due to flicker noise in the tail current of each differential delay stage is:

$$L(f) = \frac{K_f}{WLC_{ox}f}\frac{1}{V_{eff}^2}\frac{f_0^2}{f^3} \tag{5.90}$$

5.3 In-band phase noise

For the frequency range smaller than the PLL closed loop bandwidth, the major noise sources are:

1. reference noise.
2. PFD noise.
3. charge pump noise.

In the following, we analysis the in-band noise contributed by PFD and charge pump.

5.3.1 Phase noise due to PFD

The PFD is a main contributor to the in-band PLL phase noise. Thermal noise within the PFD gives rise to timing jitter on the edges of the output pulses. This may be considered equivalent to a certain input timing jitter of Δt seconds RMS on the reference input of a noise-free PFD and can be related to an equivalent phase jitter at the PFD input. For a PFD operating frequency of f_i, the phase jitter is given by:

$$\Delta\phi_{in} = 2\pi f_i \Delta t \tag{5.91}$$

In practice, Δt is very small (in the order of the picosecond). The PFD, being a sampling devices with an output pulse train of low duty cycle in a locked loop, is a good approximation of an impulse sampler, thus, having an equivalent noise bandwidth of half the sampling frequency and virtually uniform spectral density over its frequency range. The equivalent phase noise power spectral density can be expressed as [22]:

$$S_{\phi in}(f) = \frac{\Delta\phi_{in}^2}{f_i/2} = 8\pi^2 f_i \Delta t^2 \tag{5.92}$$

As we will see in the next section, the phase noise transfer function of the PFD phase noise in a closed loop PLL is equivalent to the divider ratio, $N = f_o/f_i$, for the frequency range within the loop bandwidth. So, the PLL in-band noise caused by the PFD is given by:

$$S_{\phi out}(f) = 8\pi^2 f_i \Delta t^2 N^2 = \frac{8\pi^2 \Delta t^2 f_o^2}{f_i} \tag{5.93}$$

This equation shows a 10 dB/decade decrease in output phase noise with the PFD operating frequency. Therefore, it is clearly an advantage in PLL designs, to operate PFDs at the highest possible frequency in order to reduce the in-band noise caused by PFD.

5.3.2 Phase noise due to charge pump

The thermal noise of the charge pump current introduces phase noise in the PLL output. Leakage current and mismatch of the charge pump in a PLL cause spurs in the sideband of the PLL output frequency. These spurs appear at multiples of the input reference frequency, thus are usually called reference spur.

PHASE NOISE DUE TO THE THERMAL NOISE CURRENT OF THE CHARGE PUMP
When a PLL is in lock, the PFD generates short synchronized UP and DOWN pulses during each reference cycle to eliminate dead zone. Both UP and DOWN currents in the charge pump include thermal noise and flicker noise generated by MOSFET transistors. Because the UP and DOWN pulses are very short, the flicker noise in the UP and DOWN current can be neglected. The equivalent average thermal noise current density over one reference period is:

$$\overline{i_n^2} = \overline{i_{ncp}^2}(\frac{\Delta T}{T_i})^2 \tag{5.94}$$

where i_{ncp} is the total noise current of the charge pump, ΔT is the width of the UP and DOWN pulses and T_i is the period of the input reference clock. This average noise current is divided by the charge pump gain K_ϕ to obtain the equivalent phase noise $\Delta\phi_{in}$ that refers to the PFD input. Then, by using (5.77) as for the noise of PFD, we obtain the PSD of the equivalent phase noise at the input of the PFD:

$$\overline{\Delta\phi_{in}^2} = \frac{i_n^2}{K_\phi^2} = \frac{(2\pi i_{ncp}\Delta T)^2}{(I_{cp}T_i)^2} \tag{5.95}$$

$$S_{\phi_{in}} = \frac{\overline{\Delta\phi_{in}^2}}{f_i/2} = \frac{8\pi^2 i_{ncp}^2 \Delta T f_i}{I_{cp}^2} \tag{5.96}$$

Thus, the PLL in-band output phase noise caused by the charge pump noise is expressed by:

$$S_{\phi_{out}} = \frac{8\pi^2 i_{ncp}^2 \Delta T f_i N^2}{I_{cp}^2} \tag{5.97}$$

Because $i_{ncp}^2 \propto I_{cp}$, from this equation we see that the in-band phase noise caused by the noise in the charge pump can be reduced by:

1. increasing the charge pump current I_{cp},
2. decreasing ΔT the width of the UP and DOWN pulses for dead zone elimination,
3. decreasing the division factor $N = \frac{f_0}{f_i}$.

PHASE NOISE DUE TO THE LEAKAGE CURRENT OF THE CHARGE PUMP At low reference clock frequency, leakage effects are the dominant cause of reference spur. When the PLL is in locked condition, the charge pump will generate short alternating pulses of current with long periods in between which charge pump is tri-stated. When the charge pump is in the tri-state, it is ideally high impedance. In practice, there is parasitic leakage current through the charge pump. The leakage current causes periodic variation of the VCO control voltage as shown in Figure 5.11, which results in FM modulation to the VCO. To simplify the analysis, we assume that a simple capacitor is used as the loop filter. The voltage deviation of the VCO control line over one reference cycle is:

$$\Delta V = \frac{I_l}{C f_r} \tag{5.98}$$

where I_l is the leakage current and f_r the reference frequency. The FM modulation index is therefore:

$$\beta = \frac{K_{vco}\Delta V}{2f_r} = \frac{K_{vco} I_l}{2C f_l^2} \tag{5.99}$$

The leakage spur can be calculated from the modulation index as follows [13]:

$$LeakageSpur = 20log(\frac{\beta}{2}) = 20log(\frac{K_{vco} I_l}{4C f_r^2}) \tag{5.100}$$

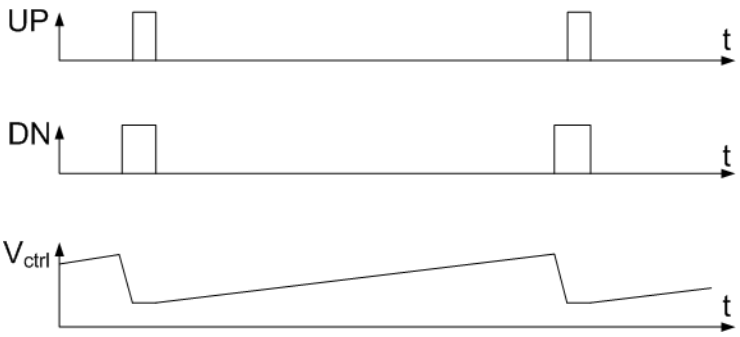


Figure 5.11: Variations of the VCO control voltage caused by the leakage current of the charge pump for a locked PLL.

PHASE NOISE DUE TO THE MISMATCH OF THE CHARGE PUMP A charge pump can have mismatch between its source and sink currents, and mismatch between the turn-on times of the source and sink currents. When a PLL is in lock, the mismatches cause unequal turn-on times for source and sink currents, that result in spurs in the VCO control voltage as shown in Figure 5.12. The spurs of the VCO control voltage result in the spurs in the PLL output frequency. In [13], Banerjee gives the relation between the output frequency spur and the frequency spur of the VCO control voltage:

$$PLLoutputfrequencyspur \propto 40log(FrequencyspurofVCO) \tag{5.101}$$

5.4 PLL jitter and phase noise analysis

PLLs are normally used to implement a variety of timing related functions, such as frequency synthesis, clock and data recovery, and clock de-skewing. Any jitter or phase noise in the output of the PLL generally degrades the performance margins of the system in which it resides and so is of great concern to the designer.

Jitter and phase noise are different ways of referring to an undesired variation in the timing of events at the output of the PLL. Jitter is an undesired perturbation or uncertainty in the timing of events. Generally, the events of

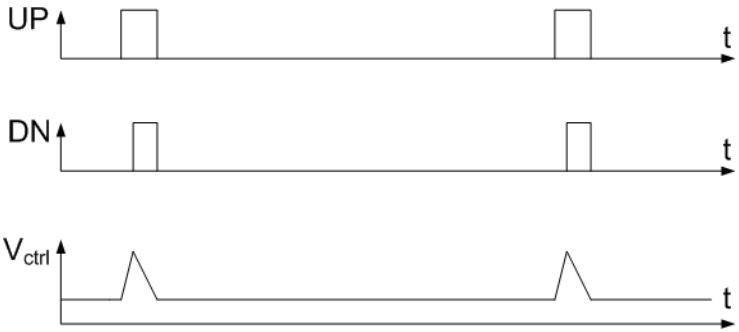


Figure 5.12: Spikes of the VCO control voltage cause by the mismatch of the charge pump for a locked PLL.

interest are the transitions in a signal. In [23], Kundert models jitter in a signal by starting with a noise-free signal v and displacing time with a stochastic process j. The noise signal becomes:

$$v_n(t) = v(t + j(t)) \tag{5.102}$$

with j assumed to be a zero-mean process and v assumed to be a T-periodic function. j has units of seconds and can be interpreted as a noise in time. Alternatively, it can be reformulated as a noise in phase, or phase noise, using:

$$\phi(t) = 2\pi f_0 j(t) \tag{5.103}$$

where $f_0 = 1/T$ and:

$$v_n(t) = v(t + \frac{\phi(t)}{2\pi f_0}) \tag{5.104}$$

In [39], Abidi depicts the analytic relationship between jitter and phase noise:

$$\sigma_j^2 = \int_0^\infty \frac{sin^3(\pi f/f_0}{(\pi f_0)^2} \tag{5.105}$$

where σ_j^2 is the mean-square value of the jitter, $S_\phi(f)$ is the power spectrum density (PSD) of the phase, f_0 is the output frequency, and Δf is the frequency offset. For white noise, a simple equation can be obtained:

$$L(\Delta f) = \sigma_j^2 \frac{f_0^3}{\Delta f^2} \tag{5.106}$$

where $L(\Delta f)$ is the PSD of the phase noise at the frequency offset Δf.

The type of jitter produced in PLLs can be classified as being from one of two canonical forms [23]. For the blocks such as the PFD, CP and FD, a transition at their output is a direct result of a transition at their input. The jitter exhibited by these blocks is referred to as synchronous jitter, it is a variation in the delay between when the input is received and the output is produced. In the other side, the VCO is autonomous. It generates its output transitions not as a result of the transitions at their inputs, but rather as a result of the previous output transitions. Therefore, the jitter produced by VCO is referred to as accumulating jitter, it is a variation in the delay between an output transition and the subsequent output transitions. Figure 5.13 shows a linear time-invariant phase domain model of the PLL with representative noise sources. These noise sources can represent either the noise created by the blocks due to intrinsic noise sources (thermal, shot, and flicker noise sources), or the noise coupled into the blocks from external sources, such as from the power supplies, the substrate, etc. Most of them are sources of phase noise, and denoted ϕ_{ref}, ϕ_{fd}, and ϕ_{vco}, because the circuit is only sensitive to phase at the point where the noise is injected. The one exception is the noise produced by the PFD/CP, which in this case is considered to be a current, and denoted i_{det}. Then the transfer function from the various noise sources to the output are:

$$G_{ref} = G_{fd} = \frac{\phi_{out}}{\phi_{ref}} = \frac{NG_{fwd}}{N + G_{fwd}} \tag{5.107}$$

$$G_{vco} = \frac{\phi_{out}}{\phi_{vco}} = \frac{N}{N + G_{fwd}} \tag{5.108}$$

$$G_{det} = \frac{\phi_{out}}{i_{det}} = \frac{2\pi G_{ref}}{K_{det}} \tag{5.109}$$

where G_{fwd} is the PLL forward gain defined by:

$$G_{fwd} = \frac{K_{det}K_{vco}H(\omega)}{j\omega} \tag{5.110}$$

These noise transfer functions allow certain overall characteristics of phase noise in PLLs to be defined. As $\omega \to \infty$, $G_{fwd} \to 1$ because the VCO and low-pass loop filter, and so G_{ref}, G_{fd}, $G_{det} \to 0$ and $G_{vco} \to 1$. At high frequencies, the noise of the PLL is dominated by the VCO. Clearly this must be so because the low-pass loop filter blocks any feedback at high frequencies.

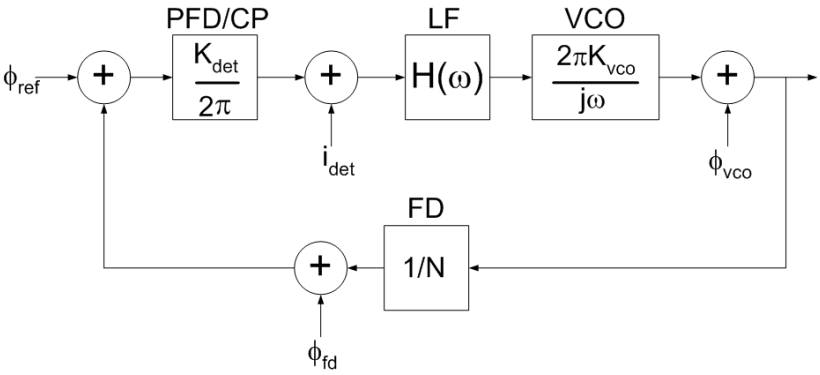


Figure 5.13: Phase-domain PLL model including the noise sources.

As $\omega \to 0$, $G_{fwd} \to \infty$ because of the $1/j\omega$ term from the VCO. So at DC, G_{ref}, $G_{fd} \to N$ and $G_{vco} \to 0$. At low frequencies, the noise of the PLL is dominated by the reference input, PFD/CP and FD, and the noise from the VCO is suppressed by the gain of the loop.

The noise transfer functions of the PLL suggest a design trade-off: increasing the loop bandwidth suppresses more noise of the VCO , but the noise from the reference input and the other components (PFD, CP, FD) is less suppressed; decreasing the loop bandwidth suppresses more noise from the reference input, PFD, CP and FD, but the VCO noise is less suppressed.

5.5 Summary

In this chapter, we analysed the phase noise in VCO and PLL. We presented three most important phase noise models for LC VCO: Leeson's linear time-invariant model, Hajimiri's linear time-varying model and Samori's non-linear model. Samori's model is the best for LC VCO phase noise analysis, and is used for us to obtained the analytical phase noise equations for LC VCO caused by both of thermal noise and flicker noise. The phase noise analysis of ring oscillator based VCO is mainly based on Abidi's model. In-band phase noise of PLL is mainly contributed by PFD and charge-pump. For PFD, the phase noise is mainly caused by transistor thermal noise. For charge pump,

the phase noise is caused by thermal noise, timing mismatch and leakage current. The deduced phase noise equations indicates the ways to minimise VCO and PLL phase noise. In the next chapter, we will present the low phase noise VCO and PLL design methodologies which are obtained from the phase noise analysis presented in this chapter.

Chapter 6

Low phase noise and low power design techniques

In this chapter, we will present the circuit-level low phase noise design methods for LC VCO . Because LC VCO exhibits much lower phase noise than ring oscillator based VCO, it is dominated in low phase noise PLL design. therefore, we concentrated on low phase noise design methods for LC VCO. In principle, phase noise is traded off by power consumption for VCO and PLL design. We will also present some general low power PLL design considerations.

6.1 Low phase noise VCO design

The phase noise of LC VCOs are normally expressed by Leeson's equation:

$$L(\Delta\omega) = \frac{1}{V_o^2}\frac{kT}{C}\frac{\omega_o}{Q}\frac{2}{\Delta\omega^2}F \tag{6.1}$$

where V_o is the VCO output amplitude, C is the tank capacitance, Q is the tank quality factor that is mainly determined by the quality factor of the on-chip inductor, and F is the noise factor that is the constant proportionality of the noise contributions from various circuit elements. Being circuit specific, the noise factor is dependent on oscillator topology in terms of device sizes, current, and other circuit parameters.

Equation (6.1) reveals that doubling the tank capacitance while keeping the oscillation frequency and amplitude constant, gives a 3 dB reduction in phase noise. The physical interpretation of this result is as follows: the tank inductance value and the series resistance has to be halved in order to keep the oscillation frequency constant for a doubled capacitance, assuming the quality factor of the inductor is independent on the inductor value; the phase noise in LC-tank is mainly caused by the thermal noise of the series resistance of the inductor because the quality factor of the tank capacitor is usually much higher. As the resistance value is halved, the phase noise voltage at the oscillator output is reduced by a factor of $\sqrt{2}$ or 3 dB. However, in order to keep the oscillation amplitude constant, the current has to be doubled, which means the power consumption of the oscillator is doubled.

In practical VCO designs, power budget is normally specified, which means a maximum current value cannot be exceeded with a fixed supply voltage. In these cases, doubling the tank inductance while keeping the oscillation frequency and the current, gives a 3 dB reduction in phase noise. The oscillation amplitude is given by:

$$V_o^2 \propto I_o R_p = I_o Q \omega L \tag{6.2}$$

The current of the oscillator is set to the maximum available value $I_o = \frac{P_{max}}{VDD}$ for having an oscillation amplitude as high as possible. With a doubled tank inductance value, the effective tank resistance and the oscillation amplitude are also doubled, assuming the quality factor is independent on the inductance value. For a constant oscillation frequency, the tank capacitance value should be halved. From Equation (6.1), we see that the phase noise is proportional to $\frac{1}{V_0^2 C}$. Therefore, with a doubled oscillation amplitude and a halved capacitance, the phase noise is reduced by 3 dB.

To reduce the phase noise, it is necessary to reduce the circuit noise factor F. Design techniques to reduce the phase noise due to the circuit have been widely studied and investigated in recent years. In the following we summarize the low phase noise design techniques for LC-tank VCO.

6.1.1 Noise filtering

As analyzed in Chapter 5, the dominating contribution to phase noise is due to the tail current transistor, whose noise at twice the frequency of oscillation is down-converted into phase noise by the switching operation of the differen-

tial pair transistors, while its low frequency noise (both white and 1/f) is up-converted into phase noise through the nonlinearities of the LC-tank, which transform amplitude noise into phase noise (AM-FM conversion). The use of an on-chip LC filter can effectively suppress the noise of the noise from the tail transistor [43] [44]. Figure 6.1 shows the schematic of a VCO with the noise filter to suppress the noise of the tail current transistor. The capacitor C_f provides a low impedance path for the noise at $2f_o$ of the tail current transistor. The inductor L_f ensures a high impedance common node for the differential pair. The big off-chip inductor L_{lf} degenerates the low frequency noise by the factor $|1 + jg_m\omega L_{lf}|^2$, where g_m is the transconductance of the tail transistor [45].

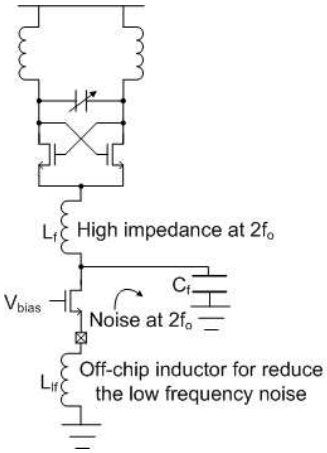


Figure 6.1: A LC VCO with the noise filter.

However, the noise filtering technique has some disadvantages: the on-chip inductor L_f and capacitor C_f increase the chip area; the off-chip inductor increases the risk of noise coupling from the off-chip signals.

6.1.2 Discrete tuning with capacitor bank

From the analysis of Chapter 5, the close-in phase noise of a LC VCO is mainly caused by AM-to-FM conversion of low frequency noise dominated by flicker

noise in the tail current transistor. Reducing the gain of the VCO can effectively suppress this noise upconversion. However, the VCO gain should be high enough because of tuning range requirement and the process variation. One way to reduce the VCO gain is to break the frequency band of VCO into many subbands by using capacitor banks [46] [47]. An example of capacitor bank switching is shown in Figure 6.2. A three-bit binary-weighted switched capacitor bank tunes the oscillator central frequency to 8 discrete frequencies. Then, a small MOS varactor continuously tunes the VCO frequency around these central frequencies, giving rise to a family of overlapping tuning curves to guarantee continuous frequency coverage over the whole tuning range.

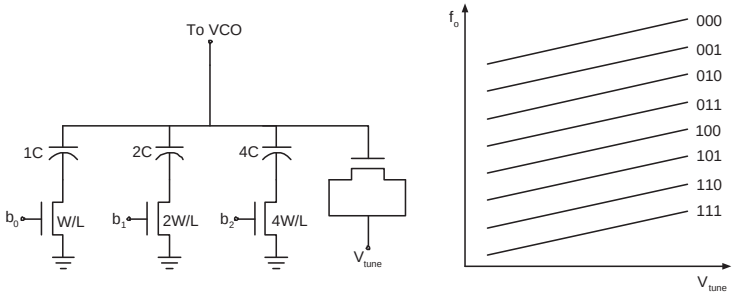


Figure 6.2: A three-bit binary-weighted capacitor bank.

MOS transistors are normally used as the switch for capacitor bank. In the on-state, the switch represents a small series resistance. The quality factor of the switch and the capacitor is given by:

$$Q = 1/(\omega_o C R_{on}) \tag{6.3}$$

The quality factor increases with the larger size of the switching transistor due to the reduction of the on-resistance. The tuning ability of capacitor bank is defined as the ratio of the on-capacitance to the off-capacitance. When the switch is on, the capacitance is basically that of the capacitor. When the switch is off, the capacitance drops to the series combination of the capacitor and the parasitic capacitance of the switching transistor. Therefore, the tuning ability decreases with the larger size of the switching transistor. A trade-off exists between the quality factor and the tuning ability of the capacitor bank. The

switching transistor usually has a square-gate layout in order to reduce the parasitic drain junction capacitance and improve the tuning ability.

6.1.3 Differential varactors and differential tuning

Differential varactors controlled by a differential tuning voltage, as shown in Figure 6.3, can be used to reduce low-frequency noise upconversion [48]. The varactors labelled with C_{var+} have capacitance that increases with the applied voltage, while the varactors labelled with C_{var-} decrease with the applied voltage. Thus, if a differential voltage is applied, C_{var+} varactors see a positive voltage, while C_{var-} varactors see a negative voltage. For a differential input tuning voltage, both varactors increase in capacitance. However, for a common mode voltage, the increase in capacitance from C_{var+} varactors is offset by the decrease in the capacitance from the C_{var-} varactors, so the total capacitance is unchanged. Low-frequency noise (e.g. $1/f$ noise injected from the differential pair transistors or the tail current transistor) is equivalent to a common-mode input due to the low impedance of the inductor at low frequencies. Common-mode or low-frequency noise rejection is only effective if the differential varactors are exactly symmetrical. With perfect symmetry, the common-mode noise is completely rejected; however, for any residual error in symmetry, common-mode noise rejection is reduced. To optimize the symmetry of the varactors, a non-zero bias voltage on the varactors is usually required.

6.1.4 Harmonic tuned LC tank

As described by Hajimili'e phase noise model, the most noise-sensitive moment of VCOs is the zero crossing point of the VCO output voltage. The phase noise resulting from a noise injected around the zero crossing point is proportional to the voltage slope at the zero crossing point. Therefore, increasing the slope of VCO output voltage can reduce phase noise. The VCOs with harmonic tuned LC tank can reduce the phase noise by maximizing the slope of the output voltage wave at the zero crossing point and by suppressing the second harmonic at the tail node [49]. Figure 6.4 shows a LC VCO with harmonic tuned LC tank and its output voltage waveform. The output voltage of a VCO with harmonic tuned LC include both the fundamental and the third harmonic frequency component and has a waveform more like a square wave.

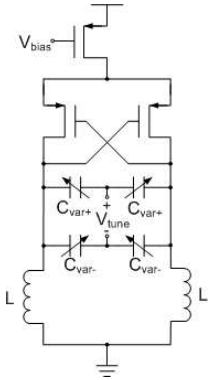


Figure 6.3: A differential tuning LC VCO.

Therefore, the slope of the output voltage of a VCO with harmonic tuned tank is steeper than that of a standard LC VCO and the phase noise is reduced.

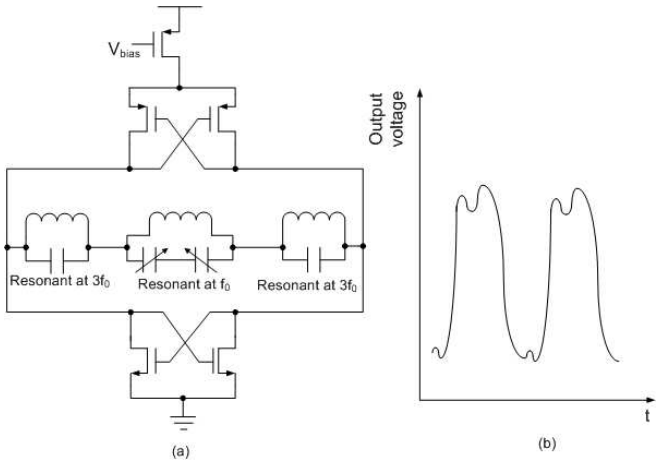


Figure 6.4: A complementary VCO with LC tuned tank: (a) schematic and (b) output voltage waveform.

6.1.5 Tail current shaping

By simply placing a capacitor C_p in parallel to the tail transistor, as shown in Figure 6.5, the phase noise can be effectively reduced. This technique is called tail current shaping [50]. Its basic idea is to shape the tail current into narrower current pulse while maintaining the same average value, so that most of the energy is delivered to the resonator at the less phase sensitive instant and the differential pair are turned off at the most sensitive instant, i.e., zero-crossing. Actually, the tail current shaping technique improves the phase noise through three mechanisms:

1. The amplitude of the oscillation is increased.
2. The drain currents are narrower pulse and injected more current when the output is close to its peak, at which the sensitivity of the VCO's output phase is minimum.
3. The capacitor C_p is a noise filter for the tail current source and reduces its contribution to the phase noise [43].

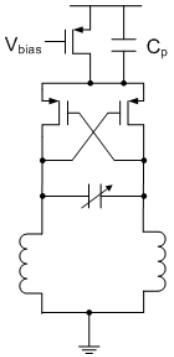


Figure 6.5: A VCO with an extra capacitor parallel to the tail transistor for tail current shaping.

6.2 Low Power PLL Design Techniques

6.2.1 Low power LC VCO design considerations

The general LC resonator tank can be shown as in Figure 6.6, neglecting the capacitor losses, because the series resistance of the inductor normally dominates the tank loss.

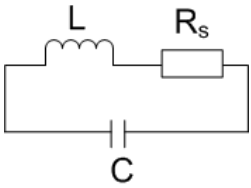


Figure 6.6: General LC resonator tank.

Using the energy conservation theorem, the maximal energy stored in the inductor must equal the maximal energy stored in the capacitor:

$$\frac{CV_{peak}^2}{2} = \frac{LI_{peak}^2}{2} \tag{6.4}$$

with V_{peak} the peak amplitude voltage of the sinewave voltage across the capacitor and I_{peak} the peak amplitude current of the sinewave current through the inductor. This current flows to the resistor R_s, so the effective loss in the tank can be calculated as:

$$P_{loss} = \frac{RI_{peak}^2}{2} = \frac{RCV_{peak}^2}{2L} = \frac{RC^2\omega_c^2V_{peak}^2}{2} = \frac{RV_{peak}^2}{2L^2\omega_c^2} \tag{6.5}$$

This loss must be compensated by the active part of the VCO to sustain the oscillation. Therefore, P_{loss} is the fundamental minimum power consumption of a LC VCO. The equation leads to some general conclusions for the power consumption of any LC VCO:

1. Power consumption decreases linearly for lower series resistance of the tank inductor.
2. For a given oscillation frequency, power consumption decreases quadratically when the tank inductance is increased or the tank capacitance is decreased.

6.2.2 Low power design considerations for other PLL blocks

The other general low power PLL design considerations are:

1. Using passive loop filters instead of active loop filters.
2. Using analog frequency divider with low output voltage swing, at least for the first stage of the divider when the VCO output frequency is high, because the power consumption of digital frequency divider dramatically increases as the input frequency becomes higher.

6.3 Summary

In this chapter, we focused on circuit state-of-the-art design techniques for LC VCO. Low phase noise design techniques, such as Noise filtering, discrete tuning, harmonic tuned LC tank and tail current shaping, are introduced. Some general low power VCO and PLL design principles are described. In the next chapter, we will present two realized PLL design. Some low phase noise and low power design techniques presented in this chapter are practised in these PLL realizations.

Chapter 7

PLL Design and Realization

Two PLL prototype chips are designed and realized by using some of the low phase noise and low power design techniques discussed in the last chapter. The first PLL is used in a Camera Link interface. The second PLL is a fractional-N PLL used in an atomic clock system.

7.1 A low-power and low-jitter CMOS PLL for clock generation

Camera Link is a communication interface for video applications. The block diagram of a Camera Link transmitter is depicted in Figure 7.1. It consists of a PLL, a parallel-to-serial converter and low-voltage-differential-signaling (LVDS) drivers. The function of the PLL is to generate a clock with a 7 times higher frequency than that of the input reference clock. The generated clock is used by the parallel-to-serial converter to convert the 28-bit parallel input data into 4-bit serial data. The main design requirements for the PLL are:

1. Low output jitter. The jitter in the PLL output increases the Bit Error Rate (BER) of the Camera Link interface. Therefore, the output jitter should be as small as possible.
2. Wide lock range. The input data rate is not fixed. A wide lock range of the PLL enables a flexible input data rate.
3. Low power consumption. Low power consumption is always desirable for saving energy. This is especially important if the circuit would be used in a portable system powered with battery.

4. Small silicon area. Smaller silicon area reduces the costs.

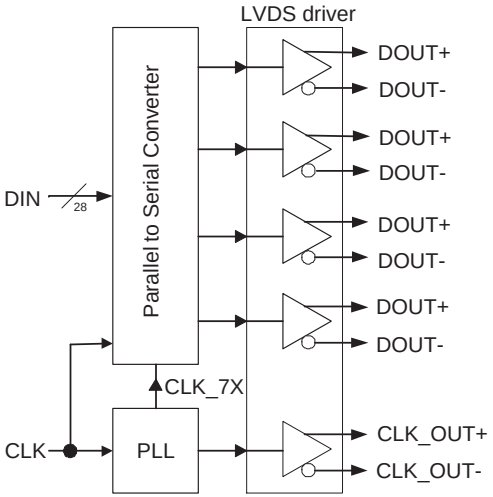


Figure 7.1: Block diagram of a Camera Link transmitter.

Considering the above requirements, A ring oscillator based PLL is chosen because the VCOs based on ring oscillator allows larger lock range and needs smaller silicon area compared to LC VCOs, although they usually have higher phase noise. The prototype design was integrated with AMS 0.35μm CMOS process.

Since the jitter of ring oscillators is proven to be inversely proportional to the power consumption [36] [51] [43], a trade-off between jitter and power consumption must be found. The implemented design features simultaneous low jitter and low power consumption thanks to:

1. A novel charge pump that effectively minimizes non-idealities such as charge sharing, clock feedthrough, current and timing mismatches.
2. A fully differential ring oscillator based VCO that exhibits a good power supply and substrate rejection ratio (PSRR).
3. A dynamic logic PFD and a second order passive-loop filter to reduce the power consumption.

Input frequency range	20 MHz - 60 MHz
Output frequency range	140 MHz - 420 MHz
Operation temperature range	-40°C - 125°C
Power supply voltage	3.3 Volt
Technology	AMS 0.35 μ m

Table 7.1: PLL design specification.

7.1.1 Design specification

The preliminary design specification defined by the industrial partner is given in Table 7.1.

7.1.2 Circuit design and implementation

The block diagram of the designed PLL is shown in Figure 7.2. The components of the PLL include a dynamic logic PFD, a low-noise charge pump, a second order passive loop filter, a three stage differential ring oscillator based VCO and a 1/7 digital frequency divider. The circuit design and implementation of each component is described in the following.

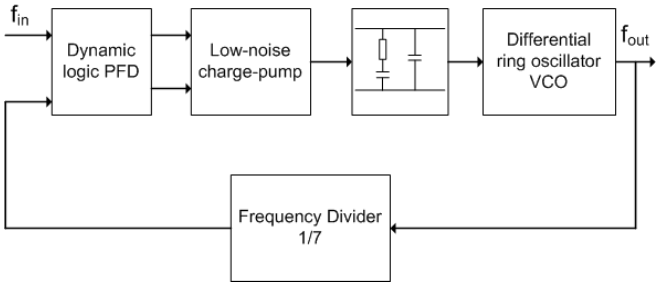


Figure 7.2: Block diagram of the designed PLL for Camera Link transmitter.

LOW JITTER CHARGE PUMP A novel charge pump circuit as shown in Figure 7.3 is implemented for minimizing the non-idealities and achieving low jitter performance [52]. Two transistors M_n and M_p remove most of the charges

stored on the parasitic capacitances of nodes a and b during the turned-off periods of UP and DN signals, thus charge-sharing effects is greatly minimized [53]. The operational amplifier OPA and the transistors M1 compose a feedback amplifier to force V_x to equal the output voltage V_{out}. The current mirror transistors M1-M8 are matched each other, resulting in matched currents: $I_{up} = I_{dn} = I_x$, regardless of the output voltages [54], By carefully designing the size of the inverters, the delays of UP and DN input path can be matched each other regardless of the process variations [55], so that time mismatch is minimized. Two capacitors C_a and C_b effectively suppress the voltage spikes caused by clock feedthrough. Resistor R_m and Capacitor C_m provide Miller compensation for the feedback amplifier. This novel single-ended charge-pump achieves low-jitter and low-power consumption while requiring simple design and small area. The opamp is implemented with a single stage, symmetrical structure as shown in Figure 7.4. The bandwidth requirement is quite low because the feedback amplifier just needs to correct the DC offset between V_x and V_{out}.

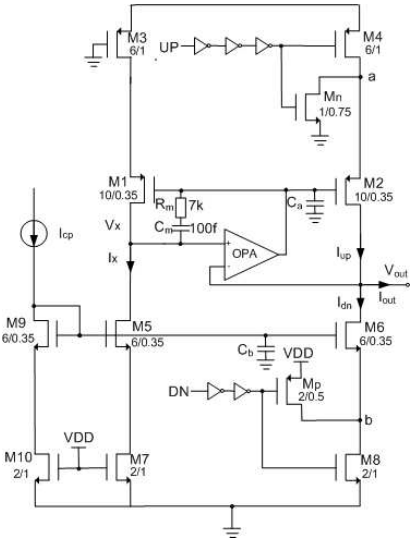


Figure 7.3: Schematic of the implemented novel low-jitter charge-pump.

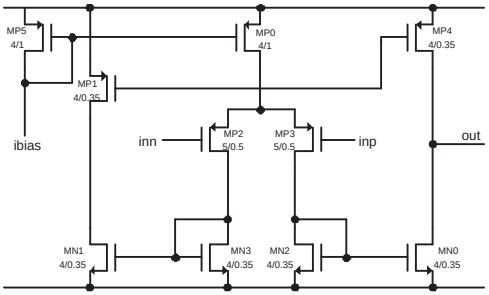


Figure 7.4: Schematic of the opamp.

The charge-pump circuit is simulated with Cadence Spectre. Figure 7.5 shows one simulation result. In the simulation scenario, the charge-pump receives wide DN pulses and narrow UP pulses, resulting in discharging the output node. The spikes of the I_{out} are mainly due to charge-sharing despite the effective reducing technique.

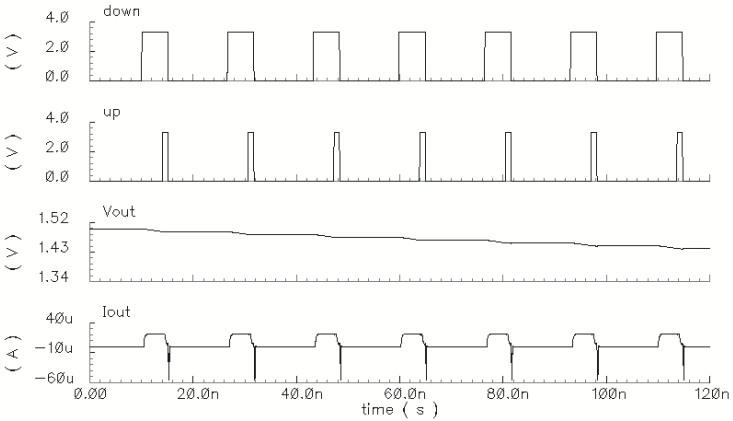


Figure 7.5: Simulated waveforms of the charge-pump circuit.

DIFFERENTIAL RING-OSCILLATOR BASED VCO The implemented VCO consists of three components, as shown in Figure 7.6. The voltage-to-current converter converts the input control voltage into a biasing current for the current-controlled oscillator (CCO), which features an oscillation frequency proportional to the biasing current. The level shifter converts the CCO output signal with a small amplitude into a rail-to-rail signal, which is necessary to drive the frequency divider.

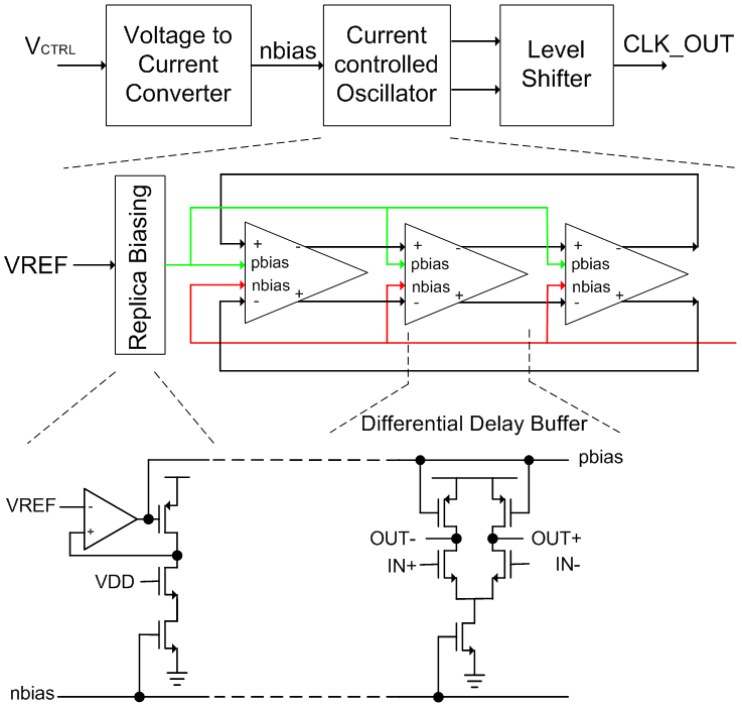


Figure 7.6: VCO block diagram and schematics.

The CCO circuit consists of a fully differential three-stage ring oscillator with a replica biasing circuit for keeping the output amplitude constant regardless the biasing current [9]. The schematics of the CCO and the delay

buffer are shown in Figure 7.7and Figure 7.8 respectively.

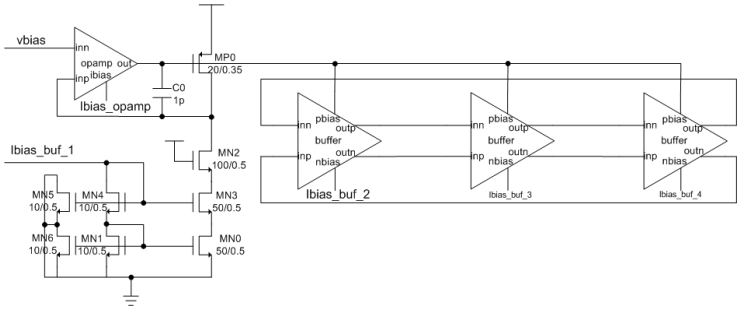


Figure 7.7: Schematic of the CCO circuit.

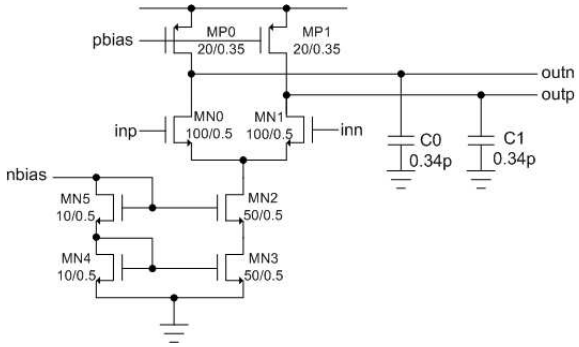


Figure 7.8: Schematic of the delay buffer circuit.

The replica biasing circuit is composed with the opamp and the transistors MP0, MN2 and MN3. The feedback loop sets the MP0 gate voltage to the reference voltage vbias so that the drain-to-source voltage of MP0 equals (VDD-vbias). Because MP0. MP2 and MP3 are copied from the delay buffer and have the same biasing current as the delay buffer, the output swing of the delay buffer is also fixed to (VDD-vbias). The nominal delay time t_d of each

buffer is expressed as:

$$t_d = \frac{V_{sw} C_l}{I_{bias}} \tag{7.1}$$

where V_{sw} is the output swing of the delay buffer, C_l is the total capacitive load at the output of the delay buffer, and I_{bias} is the biasing current of the delay buffer. Because V_{sw} is held constant by the replica biasing circuit and the capacitive load is also constant, the frequency of the oscillator has to be adjusted by the basing current.

The delay buffer includes a source coupled differential pair with resistive loads which are implemented by PMOS transistors operating in triode region. It has a good ability to reject common mode noise thanks to its fully differential structure. The basic design principles of the delay buffer are summarized here [1] [56]:

1. To ensure that the three-stage ring oscillator can oscillate, the minimum small signal voltage gain per stage a_v should be equal to 2. a_v is approximately equal to the ratio of the voltage swing to the overdrive voltage of the NMOS differential input pair:

$$a_v = g_m R_l \approx \frac{I_{bias}}{V_{gs} - V_{thn}} \cdot \frac{V_{sw}}{I_{bias}} = \frac{V_{sw}}{V_{gs} - V_{thn}} \tag{7.2}$$

2. To keep the PMOS load transistors operating in triode region, the voltage swing should be smaller than the overdrive voltage of the PMOS transistor:

$$V_{sw} \leq (V_{sg} - V_{thp}) \tag{7.3}$$

3. The differential input pair transistors should operate in saturation region:

$$(VDD - V_{sw}) \geq (VDD - V_{thn}) \Rightarrow V_{sw} \leq V_{thn} \tag{7.4}$$

4. The variance of the timing jitter of the buffer induced by thermal noise can be expressed as [56]:

$$\sigma_{\Delta t_d} = \sqrt{\frac{C V_{sw} t_d}{(V_{gs} - V_{thn})^2 I_{bias}}} \tag{7.5}$$

where C is a design independent constant. For constant output swing V_{sw} and bias point of the differential NMOS pair $(V_{gs} - V_{thn})$, the jitter is reversely proportional to the power consumption. Therefore, for a

given power specification, an oscillator with fewer stages is preferred because each stage can have more power and has a smaller jitter. This is why we have chosen a three-stage ring oscillator.

The design of the delay buffer follows the following steps:

1. Determine the voltage swing. The threshold voltage of the NMOS transistor in AMS 0.35 μm technology is about 0.5 Volt. Considering Equation (7.4), the output voltage swing is set to 0.4 Volt.
2. Set the biasing current of each stage: $I_{bias} = 0.5$ mA at 280 MHz (the central frequency of the PLL tuning range).
3. Set the load capacitance of the delay buffer to 0.5 pF (including the input capacitance and the parasitic capacitance of routing).
4. Set the small signal voltage gain of the differential pair to 3.
5. Set the bias point of the PMOS load transistor. The threshold voltage of PMOS transistor is about 0.65 V. Considering Equation (7.3), we choose $(V_{sg} - V_{thp}) = 1.4$ V to ensure the PMOS load operating in linear region.
6. Calculate the size of the PMOS load transistor by the following equation:
$$R_l = \frac{V_{sw}}{I_{bias}} = \frac{1}{K_p \frac{W_p}{L_p}(V_{sg} - V_{thp} - V_{sw})} \tag{7.6}$$
where $K_p = 58\ \mu A/V^2$ with this technology. The calculated PMOS size is $\frac{W_p}{L_p} = 60$.
7. Calculate the size of the NMOS differential pair. For a predefined small signal gain $a_v = 3$ and the biasing current $I_{bias} = 0.5$ mA, the size of the NMOS transistor can be calculated by:
$$a_v = g_m R_l = \frac{V_{sw}}{I_{bias}} \sqrt{2K_n \frac{W_n}{L_n} I_{bias}} \tag{7.7}$$
with $K_n = 170\ \mu A/V^2$, the calculated size of the NMOS transistors is $\frac{W_n}{L_n} = 9.1$.

The calculated transistor sizes provide a start point for the design. The actual transistor sizes are finally determined by simulation.

The total load capacitance on the output of each delay buffer determines the maximum output frequency of the VCO. For a given biasing current, a larger load capacitance requires a higher biasing current in order to achieving the same maximum output frequency. With predefined biasing current

I_{bais} = 0.5 mA, the load capacitor is set to C_l = 0.4 pF. With this value, the simulated maximum output frequency is 350 MHz in the worst case. After the post layout simulation, C_l should be reduced to 0.34 pF due to the parasitic capacitance of the layout. With the new value of the load capacitor, the difference between the schematic simulation and the post-layout simulation is smaller than 5%.

The level shifter is implemented with a folded-cascade amplifier. Its schematic is shown in Figure 7.9. The circuit is described as:

1. Transistors MN1-MN3 and MP1-MP2 form the differential input stage.
2. Transistors MP3-MP4 and MN4-MN5 form a folded-cascode stage, which transforms differential input to single-ended output.
3. Transistors MP5 and MN6 consist the inverter output buffer.
4. Transistors MN7-MN8 and MP6 provide the biasing current.

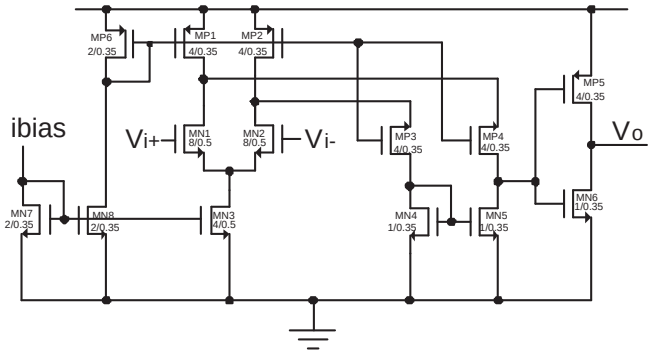


Figure 7.9: Schematic of the level shifter.

The simulated waveforms of the VCO circuit is shown in Figure 7.10. For the simulation, the VCO input control voltage is set to 0.8 V. The simulated VCO output frequency is 261 MHz, and the simulated output voltage amplitude is about 0.25 V.

Figure 7.11 shows the 8 corner simulation results. These corner simulations simulate the VCO with variations of process, supply voltage and temperatures. For the worst case (case4), the maximum VCO output frequency

is 350 MHz.The range of the VCO control voltage is limited by the output voltage range of the charge pump, which is about 0.5 V - 2.4 V.

Figure 7.12 compares the schematic simulation results and the post-layout simulation result under the typical simulation conditions. The difference between both simulations is small than 5%.

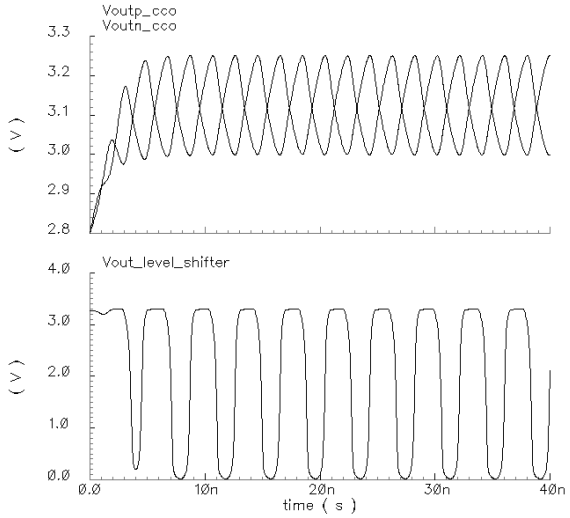


Figure 7.10: The waveforms obtained from the VCO transient simulation. Upper: the outputs of the VCO, Lower: the output of the lever shifter.

PHASE-FREQUENCY DETECTOR Figure 7.13 shows the schematic of the implemented phase-frequency detector (PFD) based on dynamic logic circuit [10]. This PFD needs fewer transistors and consumes less power compared to the conventional PFDs based on the static logic circuit. The sizes of the transistors are given in Table 7.2. Figure 7.14 and Figure 7.15 show the simulated waveforms.

LOOP FILTER The schematic of the loop filter is shown in Figure 7.16. The implemented loop filter is a second-order passive low-pass filter. When the

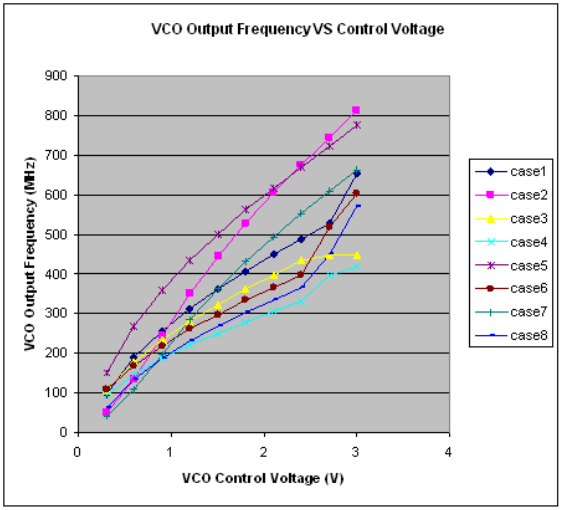


Figure 7.11: Corner simulation results of the VCO output frequency in function of the input control voltage.

global reset signal *nreset* is active, the loop filter output voltage *vctrl* is set to the initial voltage *vinit*. As described in Chapter 2, the bandwidth and stability of the PLL is dependent on the impedance of the loop filter. As a rule of thumb, the maximum loop bandwidth of a charge pump should be lower than 1/10 of the input reference frequency. In our design, we choose the loop bandwidth that equals to 1.25 MHz considering the minimum input reference frequency of 20 MHz. The values of the capacitors and resistor of the loop filter can be calculated with the following equations [57]:

$$Z_{loop_filter}(s) = \frac{sT_0 + 1}{s(sT_1 + 1)(C_0 + C_1)} \tag{7.8}$$

$$T_1 = \frac{sec\phi_{pm} - tan\phi_{pm}}{\omega_{bw}} \tag{7.9}$$

$$T_0 = \frac{1}{\omega_{bw}^2 T_1} \tag{7.10}$$

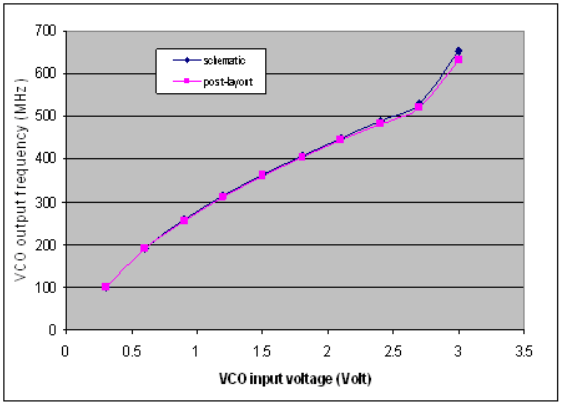


Figure 7.12: Comparison of the schematic simulation and the post-layout simulation of the VCO.

MN0, MN3-MN4, MN7-MN11	2/0.35
MN1-MN2, MN5-MN6	4/0.35
MP0-MP2, MP5-MP7, MP10-MP13	4/0.35
MP3, MP8	2/0.35
MP4, MP9	6/0.35

Table 7.2: The transistor sizes of the PFD.

$$C_1 = \frac{T_1}{T_0}\frac{I_{cp}}{2\pi}\frac{K_{vco}}{T_1 N_{fd}}\sqrt{\frac{1+(\omega_{bw}T_0)^2}{1+(\omega_{bw}T_1)^2}} \tag{7.11}$$

$$C_0 = C_1(\frac{T_0}{T_1} - 1) \tag{7.12}$$

$$R_0 = \frac{T_0}{C_0} \tag{7.13}$$

where $I_{cp} = 20\ \mu A$ is the charge pump current, $K_{vco} = 220$ MHz is the VCO gain, $N_{fd} = 7$ is the division ratio of the frequency divider, $\omega_{bw} = 1.25$ MHz is the loop bandwidth and $\phi_{pm} = 50$ degrees is the loop phase margin. With

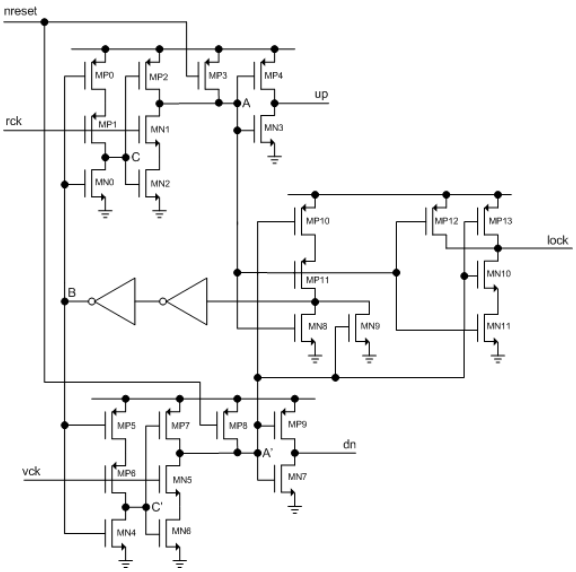


Figure 7.13: Schematic of the PFD.

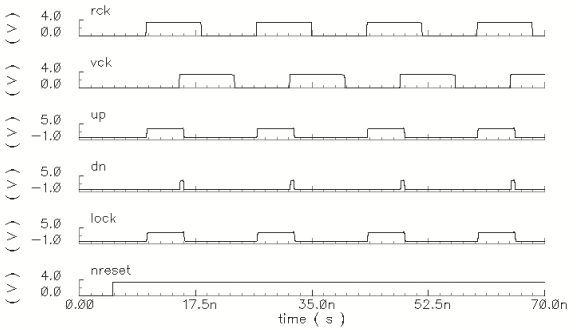


Figure 7.14: Simulation of the PFD with $f_{rck} = f_{vck}$ and rck is 5 ns before vck.

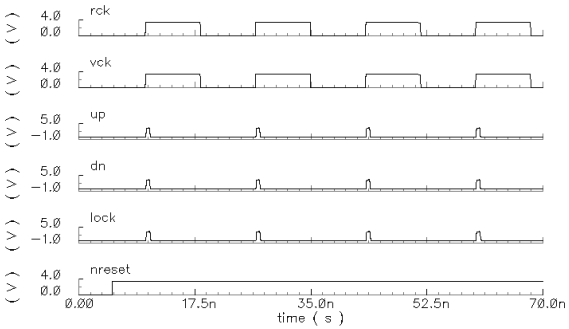


Figure 7.15: Simulation of the PFD with 60 MHz synchronized input signals.

these predefined parameters, the values of the loop filter components are obtained: $R_0 = 18$ kohm, $C_0 = 24.3$ pF and $C_1 = 3.7$ pF. Considering the parasitic capacitance at the VCO input and the connection line, the final value of C_2 is set to 3 pF. Table 7.3 summarizes the values of the components.

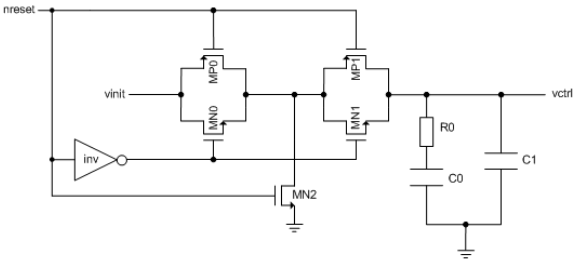


Figure 7.16: Schematic of the loop filter.

FREQUENCY DIVIDER The schematic of the frequency divider is shown in Figure 7.17. It is a pure digital circuit and implemented with the standard cells from the AMS library. The transient simulation results of the designed PLL is shown in Figure 7.18.

MN0, MN1	4/0.35
MN2	10/0.35
MP1, MP2	4/0.35
R0	18 kΩ
C0	24 pF
C1	3 pF

Table 7.3: The values of the loop filter components

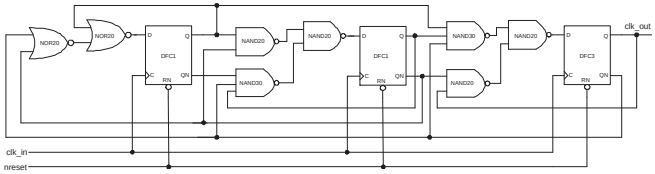


Figure 7.17: Schematic of the frequency divider.

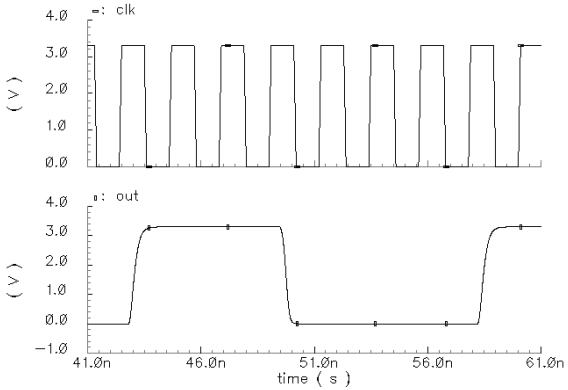


Figure 7.18: Transient simulation of the frequency divider with a 450 MHz input clock.

7.1.3 Layout and post-layout simulation

The layout of the whole PLL is shown in Figure 7.19. The area of the layout is 410 x 210 μm^2. Half of the chip area is occupied by the loop filter due to its large capacitor. The three delay buffers in the VCO are symmetrically layouted to improve common mode noise rejection ability.

A transient simulation with the whole PLL including the extracted parasitic capacitance and resistance due to the layout was performed. Figure 7.20 shows the simulated VCO input control voltage. The lock time of the VCO is about 1.5 μs.

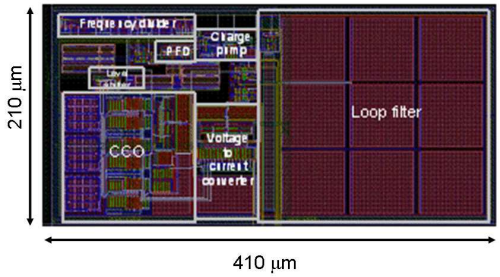


Figure 7.19: The layout of the PLL chip.

7.1.4 Measurement and characterisation

A special test board shown in Figure 7.21 was developed for characterizing the designed PLL circuit. LeCroy serial data analyzer SDA 6020 was used for the measurement. Three chips were measured.

At first, The VCO was tested with an external input control voltage. The test shows that the vco output frequency is a linear function of the input control voltage in the range of 50 MHz - 550 MHz, and the VCO gain is about 205 MHz/V. The test results are close to the simulation results. Figure 7.22 shows

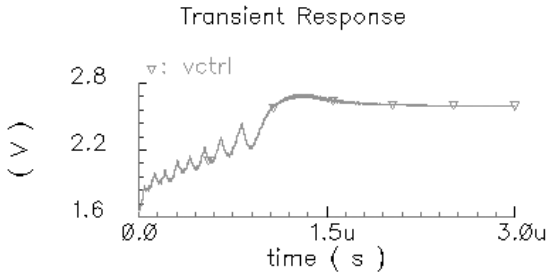


Figure 7.20: Post-layout transient simulation of the VCO input voltage.

the measured VCO output frequency in function of the input control voltage under different temperatures.

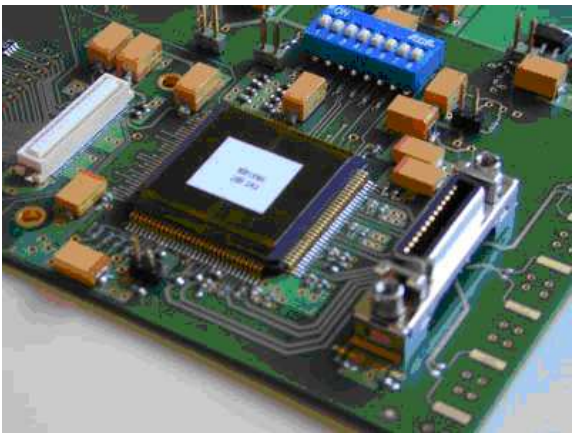


Figure 7.21: PLL test board.

The measurement shows that the PLL has a lock range from 100 MHz - 560 MHz at room temperature (25°C). The measured root-mean-square jitter is 7 ps at 350 MHz output frequency, and the peak-to-peak jitter is 65 ps at 350 MHz output frequency as shown in Figure 7.23.

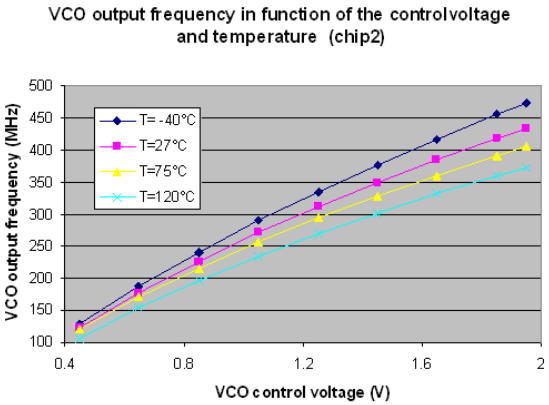


Figure 7.22: Measured VCO output frequency in function of the input control voltage.

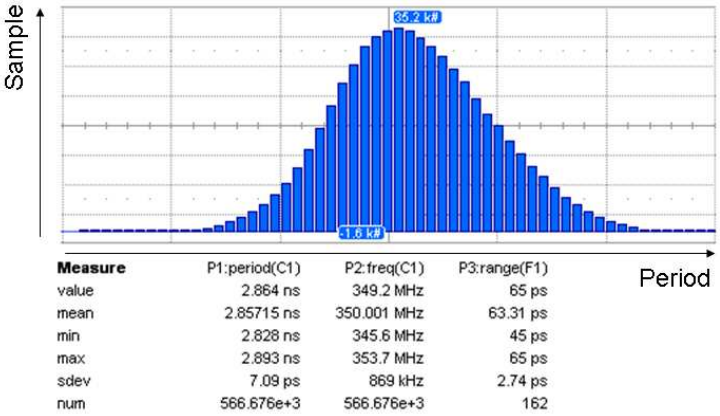


Figure 7.23: Measured period jitter of the PLL.

7.1.5 Conclusion

Table 7.4 summarizes the measured parameters of the realized PLL and compares them with some similar PLL designs.

The realized PLL exhibits an optimal jitter-power consumption product, while occupying a significant smaller area and featuring a larger lock range. The achieved low jitter performance of this PLL benefits from using the following techniques:

1. The fully differential structure of the VCO minimizes the common mode noise.
2. The bias transistor and the differential pair of the VCO delay buffer are designed to have large effective gate voltages to reduce the jitter according to the jitter analysis in chapter 5.
3. The novel charge pump is designed to minimize the charge sharing, mismatch and leakage current, therefore, the jitter caused by charge pump is largely reduced.

	this work	[58]	[59]	[60]
Nominal freq. (MHz)	350	340	300	270
RMS jitter (ps)	7.1	8.4	3.1	4
P-P jitter (ps)	65	62	22	32
Power cons. (mW)	12	100	44	24
Lock range (MHz)	100-560	340-612	300-400	100-500
VDD (Volt)	3.3	2.5	3.3	1.8
Area (mm^2)	0.09	0.67	4	0.16
Technology (μm)	0.35	0.4	0.6	0.18

Table 7.4: Performance comparison of the realized PLL with some published PLLs.

7.2 A 1.5 GHz fractional-N PLL for frequency synthesis

The goal of this second realization is to develop an integrated low-power PLL suited for atomic clock applications. The main system specifications are:

1. The whole PLL is realized into a CMOS or BiCMOS process with a minimum number of external components.

2. Low power consumption. The total power consumption is in order of 20 mW.
3. Generating a signal to be used in a wide range of applications covering Rubidium and Cesium based atomic clocks suitable for CPT techniques and microwave interrogation techniques.
4. Frequency tuning resolution = 1 Hz. This specification means that a Σ-Δ fractional-N PLL has to be implemented in order to realize a small frequency tuning resolution with a large PLL loop bandwidth.
5. PLL output phase noise < 100 dBc/Hz @ 100 MHz.
6. Supply voltage range 1.5 - 1.8 Volt.

The basic block diagram of the PLL is shown in Figure 7.24. The prototype chip includes a PFD, a charge pump, a VCO, a 1/8 frequency prescaler and a RF output buffer. The Multi-Modulus Divider (MMD) with a Σ-Δ modulator is a pure digital circuit and is implemented on a FPGA that can be flexibly programmed.

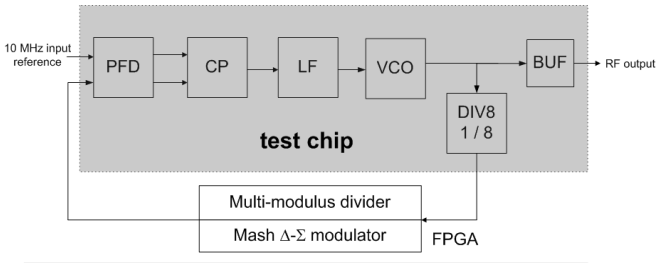


Figure 7.24: Block diagram of the PLL.

7.2.1 System-level simulation of the PLL

Before starting to design the PLL in transistor level, it is preferred to make some simulations at system level in order to determine some important parameters, such as PLL loop bandwidth, VCO phase noise, the order of Σ-Δ modulator, the transfer function of the loop filter and the charge pump current, according to the specifications.

TRANSFER FUNCTION LEVEL SIMULATION The first step is to running simulations at the transfer function level with a program named PllDesign [61]. PllDesign allows fast and straightforward design of phase locked loops at the transfer function level. In particular, the program takes as input a desired closed loop transfer function description and then automatically calculates the open loop parameters that must be chosen to achieve the design. The resulting closed loop pole/zero locations, transfer function, and step response can be plotted out. The impact of non-idealities, such as open loop gain and open loop pole variations, parasitic poles and zeros, on the closed loop response can be explored by simply entering the variation values into the tool and observing the resulting closed loop pole/zero locations, transfer function, and step response. In addition, an estimation of PLL noise performance can be viewed by entering noise parameters, such as the magnitude of detector noise and VCO noise, and observing the resulting phase noise and rms jitter at the PLL output.

For the designed PLL, Table 7.5 lists the pre-defined parameters for simulation. The in-band noise represents the total noise generated from the components inside PLL except the VCO and the Σ-Δ modulator, and is assumed being dominated by white noise. The third pole of the loop filter is assumed to be at 600 kHz. The definition of the PLL closed loop bandwidth involves a trade-off between the suppression of in-band noise and the suppression of the VCO noise because the PLL behaves as a low-pass filter for the in-band noise, and as a high-pass filter for the VCO noise. Figures 7.25 - 7.27 show the simulated phase noise with the different loop bandwidth settings. From the simulation results, we conclude that the best choice of the loop bandwidth is 120 kHz because both of the Σ-Δ noise and the VCO noise are well suppressed. For the frequency range much lower than the loop bandwidth, the phase noise is dominated by the in-band noise. For the frequency range much higher than the loop bandwidth, the phase noise is dominated by the Σ-Δ modulator noise.

SIMULATION AT BEHAVIOR MODEL LEVEL The behavior simulations are made with a simulator named CppSim [62]. CppSim is a general behavior simulator that leverages C++ language to achieve very fast simulation time, and a graphical framework to allow ease of design entry and modification. At first, we simulated the behavior of a PLL with a third-order Σ-Δ modulator and a third-order loop filter. The parameters for the simulation are the same as

Input reference frequency (MHz)	10
Output frequency (GHz)	1.5179
VCO tuning gain (kHz/V)	500
Charge pump current (μA)	100
In-band noise (dBc)	-100
Order of Σ-Δmodulator	3
Order of loop filter	3

Table 7.5: Configuration of the PLL simulation.

those defined in Table 7.5. Figure 7.28 shows the simulated transient behavior of the VCO control voltage. Figure 7.29 shows the simulated phase noise of the PLL output.

For comparison, we simulated also the PLL with a third-order Σ-Δ modulator and a second-order loop filter. Figure 7.30 and Figure 7.31 show the simulated VCO control voltage and the output phase noise respectively. In this case, the VCO control voltage is much more noisy than the plot of Figure 7.28, and the output phase noise is increased due to insufficiently suppressed noise generated by the Σ-Δmodulator. So, we conclude that a third-order loop filter is absolutely necessary for a PLL with a third-order Σ-Δmodulator.

SIMULATIONS OF THE EFFECTS DUE TO MISMATCH AND LEAKAGE CURRENTS OF CHARGE PUMP Usually charge pumps in PLLs exhibit nonidealities, such as mismatch between UP and DN current, leakage current, etc. With CppSim, we can simulate the effect due to mismatch and leakage current of the charge pump. We assume the mismatch current is 1% of the nominal current of the charge pump, which is 100 μA. Figure 7.32 shows the simulated phase noise with 1 μA mismatch current. Figure 7.33 shows the simulated phase noise with 1 μA mismatch current and 100 pA leakage current. The phase noise increases about 7dBc inside the loop bandwidth in comparison with the phase noise shown in Figure 7.29. The leakage current has negligible effect on the output phase noise.

From the above simulations at the system level, we determined and confirmed some system parameters:

1. The PLL loop bandwidth is about 120 kHz.
2. A third-order loop filter is necessary for suppressing the noise of the

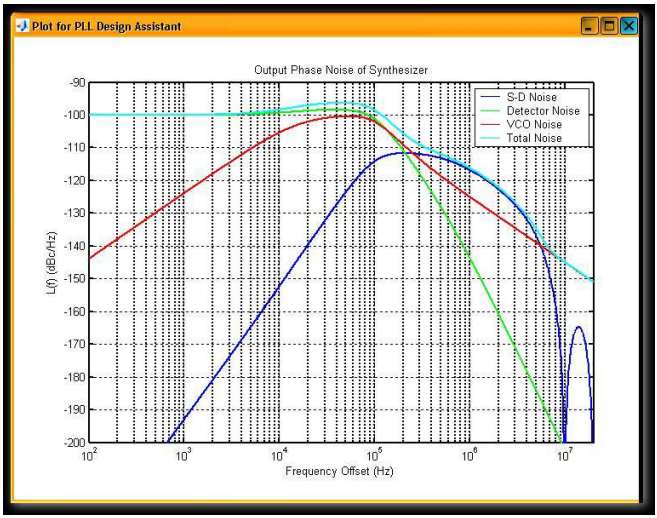


Figure 7.25: Simulated PLL output phase noise with 100 kHz loop bandwidth.

Σ-Δ modulator.

3. the charge pump current is 100 μA assuming the mismatch current is 1% and in-band noise < -100 dBc.

7.2.2 Schematic and layout design of the prototype chip

The prototype chip was designed with UMC CMOS 0.18 μm RF process. The main block diagram of the chip was already shown in Figure 7.24. This section presents the detailed schematic design of each blocks.

DESIGN OF THE VCO The VCO is one of the the most critical components in this PLL. The VCO design specifications are given in Table 7.6. Because the gain of the VCO is as low as 500 kHz/V, it may be assumed that the PLL output phase noise is mainly contributed by the VCO. According to the phase noise theory presented in Chapter 5, the closed-in phase noise of LC VCOs is caused by the upconversion of flicker noise of the biasing transistors and the differential pair transistors. Since PMOS transistors have $\sim$ 10 dB

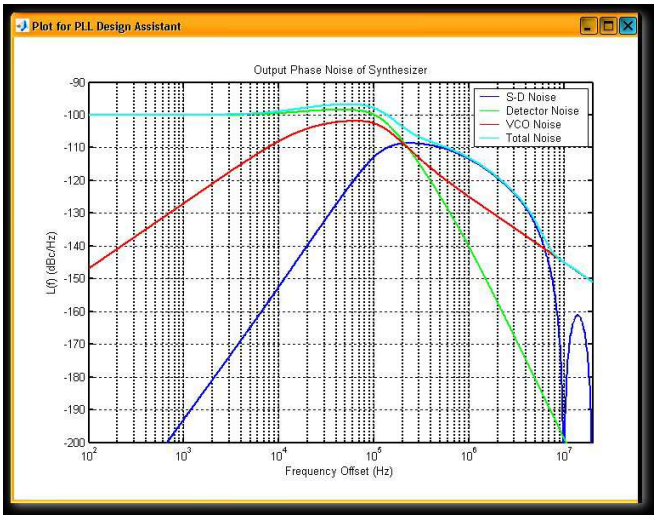


Figure 7.26: Simulated PLL output phase noise with 120 kHz loop bandwidth.

lower flicker noise compared to that of NMOS transistors for a typical 0.18 μm CMOS process, PMOS only VCOs can achieve better phase noise performance [29].

The schematic of the VCO is shown in Figure 7.34. The PMOS differential pair (PM1 and PM2) generates the negative resistance to compensates for the resistive loss of the LC tank. The transistor PM0 provides the bias current for the differential pair. The capacitor C1 is added to the common mode node of the tail current transistor to suppress common mode node variations, which result in flicker noise upconversion of the differential pair [41]. PM3 and PM4 are common-source connected output buffers for the measurement of the VCO. The inductors and the varactors are provided by the technology library [63]. The quality factor of the inductors at 1.5 GHz is about 5. Because the minimum varactor from the library is still too large to achieving the VCO gain as small as 1 MHz/V, two small series capacitors are put between the varactors and the differential pair output nodes. According to the specifications, the VCO gain is about 1 MHz/V. However, process, supply voltage and temperature variations will cause the frequency shift far from the target central

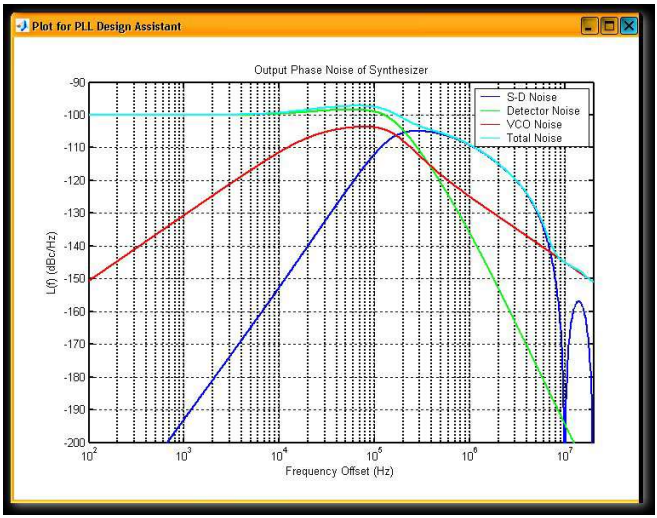


Figure 7.27: Simulated PLL output phase noise with 150 kHz loop bandwidth.

frequency. A coarse frequency tuning is implemented with a 7-bits digitally controlled capacitor bank.

The design procedure is described as follows:

1. Determine the tank inductor. According to [64], the tank loss is mainly caused by the resistance of the inductor and can be expressed as:

$$P_{loss} = \frac{V_{peak}^2}{QL\omega_c} \tag{7.14}$$

where V_{peak} is the peak amplitude voltage of the VCO output, Q is the quality factor of the inductor, and ω_c is the oscillation frequency. V_{peak} is usually designed with the maximal value to minimize the phase noise. The maximal value of V_{peak} depends on the power supply voltage. The oscillation frequency is specified and cannot be changed. As analyzed in Chapter 6, a larger tank inductor results in less power consumption. In this design, the maximal inductor value that can be used is limited by the total tank capacitance.

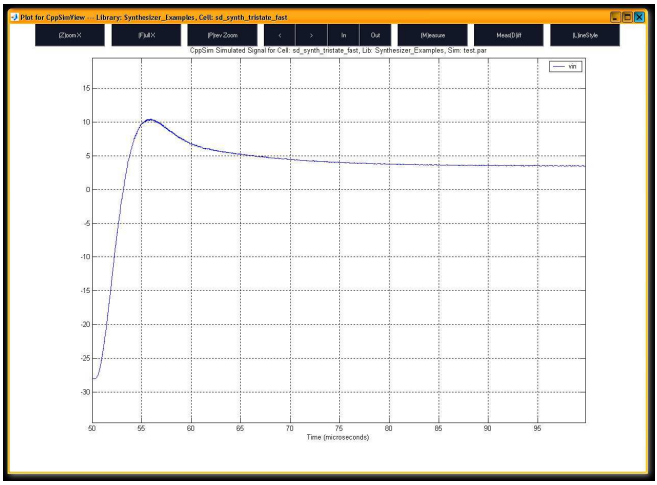


Figure 7.28: Transient response of the VCO control voltage of the PLL with a 3rd order Σ-Δ modulator and a 3rd order loop filter.

2. Determine the values of the capacitors and varactors. The varactors are taken from the UMC library and realized by MOS transistors working in the accumulation mode. The minimum varactor from the library is taken due to the extremely low VCO gain. However, the simulations showed that even the minimum varactor was still too large to achieve the specified VCO gain. Therefore, a small series capacitor is inserted between the varactor and the VCO output node in order to reduce the VCO gain. The capacitors for the digitally controlled capacitor bank are also taken from the UMC RF library. The smallest capacitor from the library is still too large for the tuning resolution. The unit capacitance of the bank is realized with 3 minimum size capacitor connected in series. The switch transistor is also taken from the library. There is a trade-off for choosing the size of the switching transistor. A switching transistor with large size has small turn-on resistance and is better for the overall quality factor, but it has a large source capacitance, that reduces frequency tuning range.
3. Determine the PMOS transistor size of the differential pair. The differ-

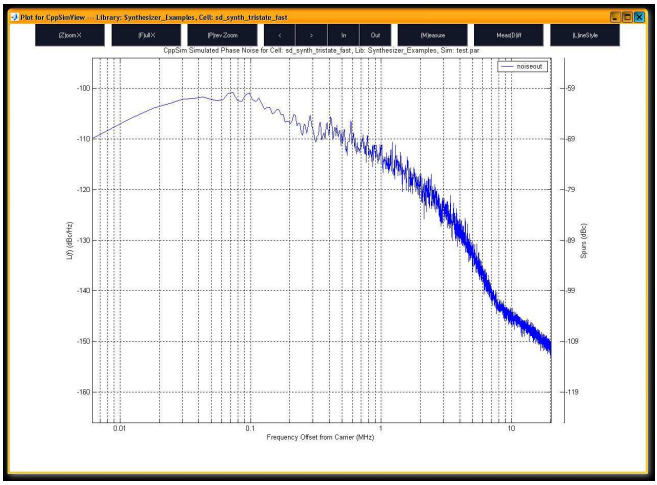


Figure 7.29: Simulated output phase noise of the PLL with a 3rd order Σ-Δ modulator and a 3rd order loop filter.

ential pair generates a negative resistance given by:

$$R_{neg} = \frac{2}{g_m} \tag{7.15}$$

where g_m is the effective transconductance per transistor. The start-up condition of the VCO requires:

$$g_m R_p \geq 1 \tag{7.16}$$

where R_p is the total parallel resistance of the LC tank. The transistors have the minimum length to reduce the parasitic drain capacitance.

The values of the components are finally determined through simulations and are summarized in Table 7.7.

Figure 7.35 shows the simulated VCO frequency in function of the VCO control voltage with the different coarse tuning bits. The simulated coarse tuning range of the VCO output frequency is about 150 MHz (from 1.46 GHz to 1.61 GHz). The fine tuning gain is 1.04 MHz/V for the lowest coarse tuning

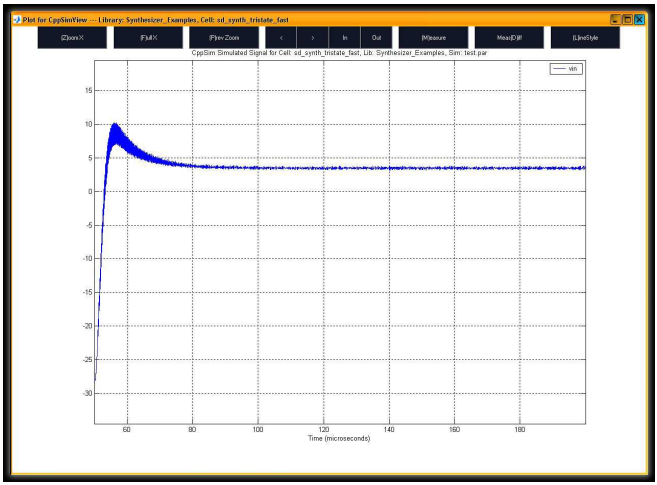


Figure 7.30: Transient response of the VCO control voltage of the PLL with a 3rd order Σ-Δ modulator and a 2rd order loop filter.

band (D6-D0 = 1111111) and 1.6 MHz/V for the highest coarse tuning band (D6-D0 = 0000000).

The simulated phase noise curves for different bias currents between 4 mA and 20 mA are shown in Figure 7.36. The phase noise at 100 kHz from the carrier is about -105 dBc. At 100 kHz from the carrier, smaller bias current is better for phase noise. At 1 MHz from the carrier, the larger bias current results in smaller phase noise.

Figure 7.37 shows the simulated VCO differential output swing in function of the VCO bias current. The differential output swing linearly increases as the bias current goes higher at the beginning, and becomes saturated as it approaches 2VDD.

DESIGN OF THE PRESCALER The VCO output is divided by eight by a prescaler before it is connected to the Σ-Δ multi-modulus-divider (MMD). As shown in Figure 7.38, the prescaler consists of three serially connected divide-by-2 stages and two output buffers.

The output buffers convert the low swing output of the last divide-by-2

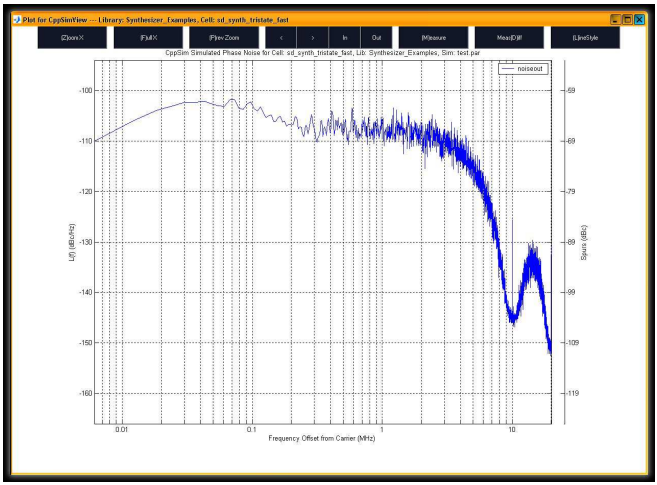


Figure 7.31: Simulated output phase noise of the PLL with a 3rd order Σ-Δ modulator and a 2rd order loop filter.

stage into a rail-to-rail signal. It is essentially a CMOS inverter that has resistive feedback to its input to provide DC biasing. The input signal is AC coupled to the inverter through a capacitor. The coupling capacitors C1 and C2 are selected to be much larger than the parasitic capacitance at the inverter input, so that the input signals are almost not attenuated. The feedback resistors R1 and R2 have to be large enough, so that the high frequency components of the inverter output do not affect the inverter input. Table 7.8 presents the values of the components of the output buffer.

The divide-by-2 stages are implemented with CML circuit as introduced in Chapter 3. Figure 7.39 shows the schematic of the divide-by-2 stage. The divide-by-2 stage consists of two CML D-flip-flops (DFF) connected in feedback with each other. The first DFF is implemented with MN1-MN6 and R1-R2. The second is implemented with MN7-MN12 and R3-R4. The basic operation principle of the DFFs is explained as follows. When the input signal VIN+ is high and VIN- is low, MN5 is on. Thus, the differential pair MN1 and MN2 compares the input signals on their gates, and passes the results to the output nodes. When the VIN+ becomes low and VIN- becomes high,

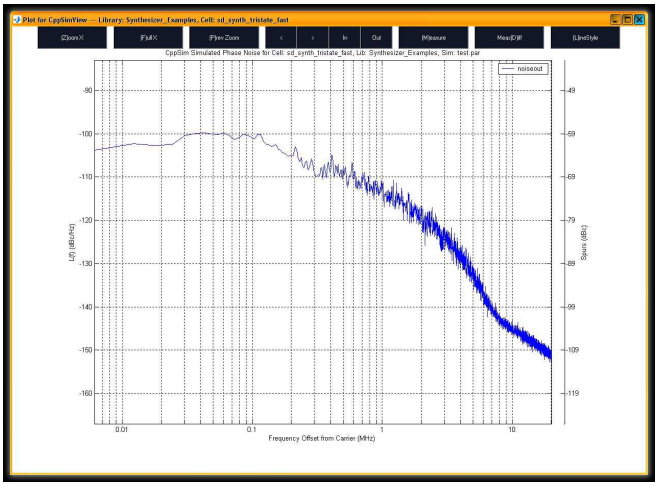


Figure 7.32: Simulated phase noise with 1% mismatch current of charge pump.

MN5 is off and MN6 is on. The cross connected pair MN3 and MN4 acts in positive feedback as a latch. During one cycle of the input clock signal, the output of the DFF changes only once (either from high to low, or from low to high). So, the output frequency is half the input frequency. The input signal of the divider-by-2 stage is AC coupled through C1 and C2. The bias current is sinked into diode-connected MN13, whose gate voltage sets the DC voltage of the input signal.Table 7.9 lists the values and sizes of the components.

Figure 7.40 shows the outputs waveforms of the divide-by-2 stages and the output buffer from a transient simulation with VDD=1.5 and 1.5 V peak-to-peak differential input signal. The simulated current consumption is given in Table 7.10.

DESIGN OF THE LOOP FILTER The schematic of the loop filter is shown in Figure 7.41. The implemented loop filter is a third-order passive loop filter. When the global reset signal *nreset* is active, the loop filter output voltage *vctrl* is set to the initial voltage *vinit*. The procedure to calculate the values of the resistors and the capacitors is given in [57]. The parameters used for calculaton

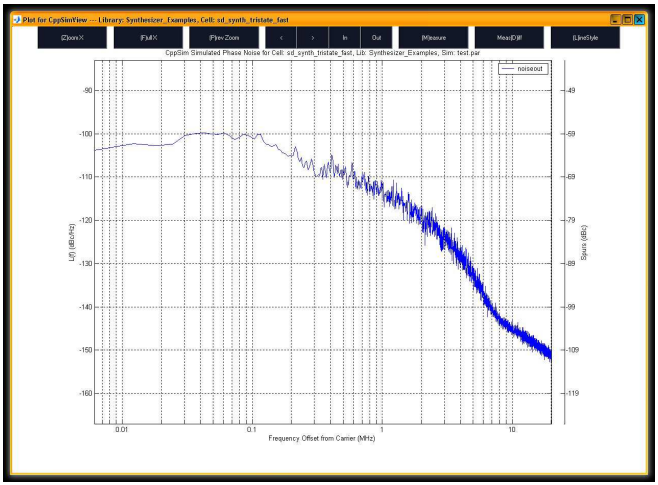


Figure 7.33: Simulated phase noise with mismatch and leakage current of charge pump.

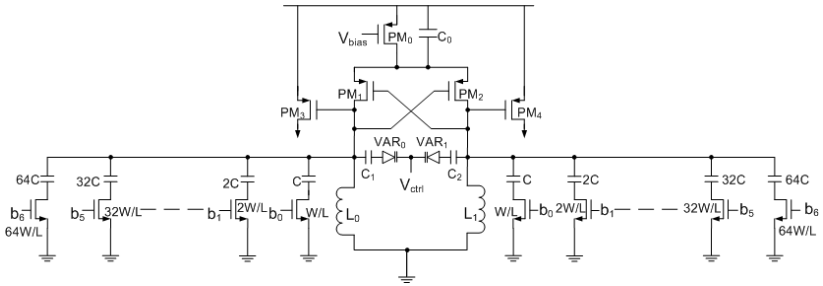


Figure 7.34: Schematic of the VCO.

are summarized in Table 7.11. f_{p2} and f_{p3} are the frequencies of the second and the third poles, respectively. Table 7.12 lists the values of the components of the loop filter. Capacitor C3 of the third pole is assumed to be given by the parasitic capacitance on the node.

Frequency (GHz)	1.518
Power consumption (mW)	5
VDD (V)	1.5 - 1.8 V
coarse tuning range (MHz)	128
Fine tuning range (MHz)	1
Phase noise (dBc)	-100 @ 100 kHz

Table 7.6: The VCO design specifications.

Inductor	2.1 nH
W/L of varactor	120/1
C1, C2	100 fF
C unit	103/3 fF
W/L of PM1, PM2	100/0.18
W/L of the switch	50/0.18
w/L of PM0	350/0.5
W/L of PM3, PM4	25/0.18

Table 7.7: Component values of the VCO.

DESIGN OF THE CHARGE PUMP The schematic of the charge pump is shown in Figure 7.42. The sizes of the transistors are given in Table 7.13. When the signal DN is high, the differential pair MN2/MN3 steers the whole bias current to the right side. Then, through the current mirrors, the current is passed to the output. The same case happens when the input signal UP is high. MN5-MN8 and MP3-MP6 are cascode current mirrors with wide output swing.

W/L of MP1 and MP2	4/0.18
W/L of MN1 and MN2	4/0.18
R1 and R2	54 kΩ
C1 and C2	607 fF

Table 7.8: The component values of the output buffers of the prescaler.

W/L of M1 and M2	25/0.18
W/L of M3 and M4	25/0.18
W/L of M5	25/0.18
W/L of M6	25/0.18 fF
MN13	25/0.18 (1st stage) 100/0.18 (2nd stage) 100/0.18 (3rd stage)
R1-R4	3 kΩ (1st stage) 3.7 kΩ (2nd stage) 5.75 kΩ (3rd stage)
R5 and R6	127 kΩ
C1 and C2	305 fF
W/L of PM3, PM4	25/0.18

Table 7.9: The component values of the divider-by-2 stages.

	Average Current (mA)
1st stage	2.22
2nd stage	1.61
3rd stage	1.2
output buffers	0.46
total	5.5

Table 7.10: The simulated current consumption of the divide-by-2 stages with an 1.5 GHz input frequency.

f_{in}	10 MHz
f_{out}	1.5 GHz
Loop BW	120 kHz
phase margin	50 degree
K_{vco}	1 MHz
I_{cp}	200 μA
f_{p3}/f_{p2}	5

Table 7.11: PLL design parameters.

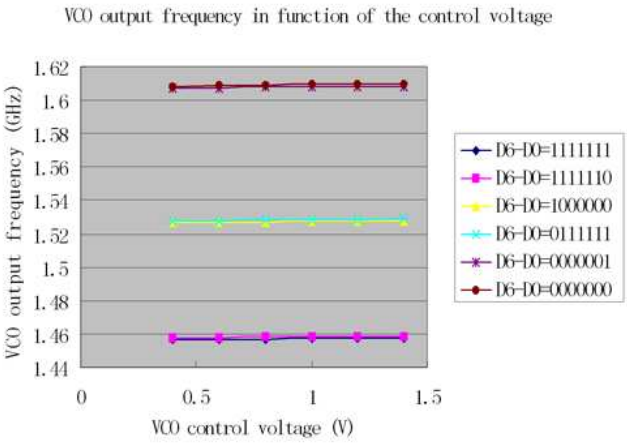


Figure 7.35: Simulated VCO output frequency with Ibias = 6 mA and VDD = 1.8 V.

DESIGN OF THE PFD The PFD is a dynamic logic circuit as already used in the first chip. The schematic of the PFD is shown in Figure 7.43. The values of the components are given in Table 7.14.

TEST CHIP AND LAYOUT The block diagram of the test chip is shown in Figure 7.44. The chip includes a bandgap to generate the reference voltage, and a biasing block to provide the bias currents for the other blocks. The VCO control voltage can be provided from an external source when measuring the VCO alone. The charge pump current, the bias current of the VCO and the prescaler bias current can be adjusted through the external resistors connected to the pads ICP, IVCO and IDIV.

Figure 7.45 shows the layout of the test chip. The size of the PLL core is 1420 x 940 μm^2. The total chip size including the pads is 1985 x 1488 μm^2.

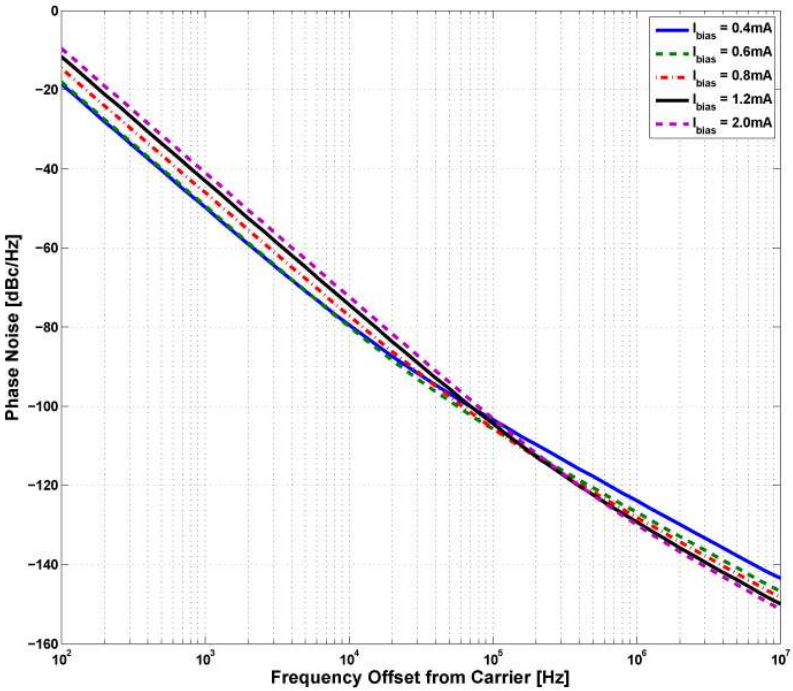


Figure 7.36: Simulated VCO phase noise with different bias currents and D6-D0 = 1000000.

7.2.3 Measurement of the test chip

The test chip has been measured and characterized with a specially designed PCB.

MEASUREMENT OF THE VCO The measured VCO output frequency is partially listed in Table 7.15. The comparison between the measurement results and the simulation results is summarized here:

1. The measured VCO tuning range is from 1.28877 GHz to 1.45486 GHz, which is about 10% lower than the simulated tuning range (1.46 GHz -

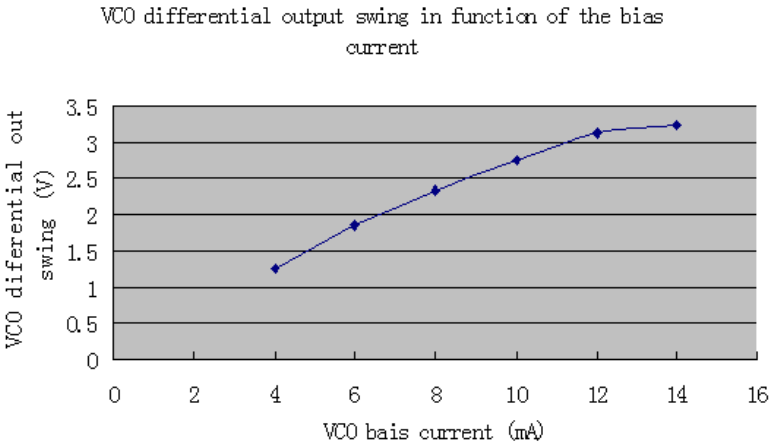


Figure 7.37: Simulated VCO differential output swing in function of the bias currents, D6-D0 = 1000000, VDD = 1.8 V.

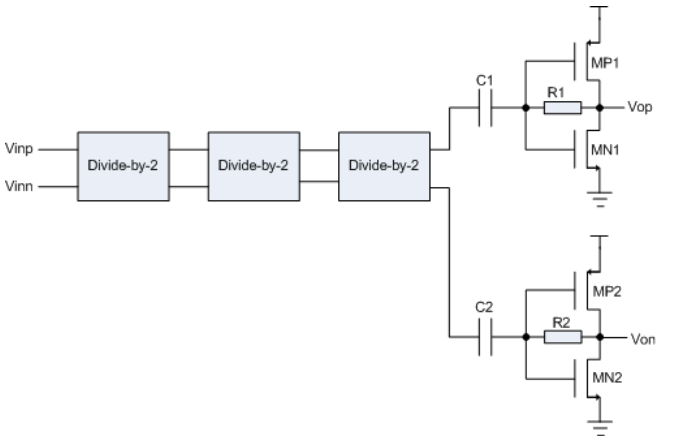


Figure 7.38: The schematic of the prescaler.

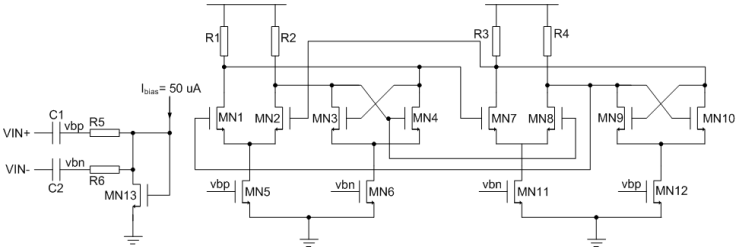


Figure 7.39: Schematic of the divide-by-2 stage.

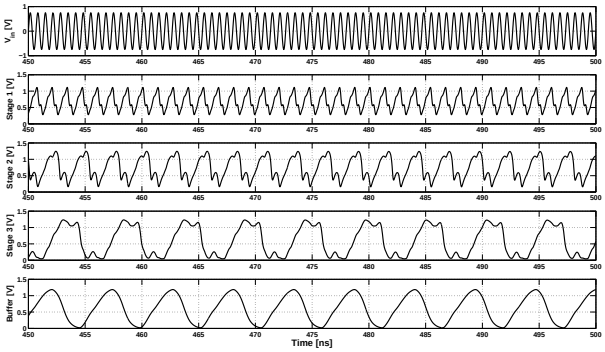


Figure 7.40: The simulated output waveforms of the divide-by-2 stages and the output buffer of the prescaler.

1.61 GHz). This can be explained as the parasitic capacitance reduces the output frequency range. The simulations with the extracted resistance and capacitance of layout show a frequency tuning range of 1.376 GHz - 1.479 GHz.

2. The measured VCO gains for the different coarse tuning codes are between 100 kHz/V - 200 kHz/V, whereas the schematic simulations show the gains between 1 MHz/V - 1.3 MHz/V. The measured gains are 6 to 10 times smaller than the simulated gains. One possible reason for gain

MP0	2/0.18
MP1-MP3	1/0.18
MN0-MN3	1/0.18
C0	5.35 pF
C1	0.74 pF
R0	763 kΩ
R1	2.29 MΩ

Table 7.12: The calculated component values of the loop filter.

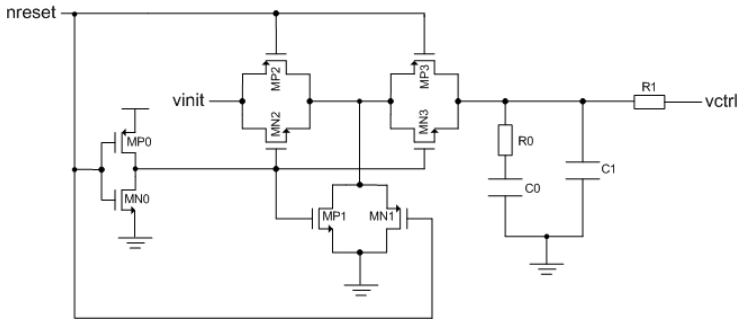


Figure 7.41: The schematic of the loop filter.

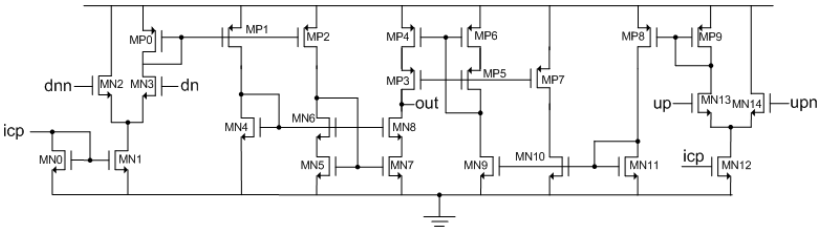


Figure 7.42: The schematic of the charge pump.

reduction is that the simulation model of the varactor is not correct because the vacractor is not biased in the valid biasing voltage range. The

MN0	10/2
MN1, MN12	20/2
MN2-MN3, MN13-MN14	10/0.24
MN4	5/0.5
MN5-MN8	20/0.5
MN9-MN11	20/1.5
MP0-MP2, MP8-MP9	20/1.5
MP3-MP6	30/0.3
MP7	5/0.3

Table 7.13: The transistor sizes of the charge pump.

MN0-MN2, MN4-MN6, MN8-MN9	1/0.18
MN3, MN7	2/0.18
MN10-MN11	1/1
MP0-MP2, MP4-MP7, MP9-MP11	2/0.18
MP3, MP8	2/0.24
MP12-MP13	2/1

Table 7.14: The transistor sizes of the PFD.

varactors in the VCO is biased between -VDD to 0 V. In the redesign, it may be better to bias the varactors between -0.5VDD to +0.5VDD.

3. The measured VCO output frequencies are not continuous between the frequency bands set by the coarse tuning codes. This is because of the small VCO gains. For the redesign, the gain of the VCO should be increased, and the overlap between the adjacent frequency bands should be large enough.

The measured VCO phase noise is -97.4 dBc/HZ at 100 kHz from the carrier as shown in Figure 7.46. It is about 6 dB higher than the simulated value. The possible reasons for this phase noise degradation is:

1. The parasitic capacitance, which mostly comes from the capacitance coupling to the substrate and is not extracted for the simulation, could have low quality factor and increases the phase noise.
2. The varactors are not well biased and their quality factor could be lower than that used for the simulation.

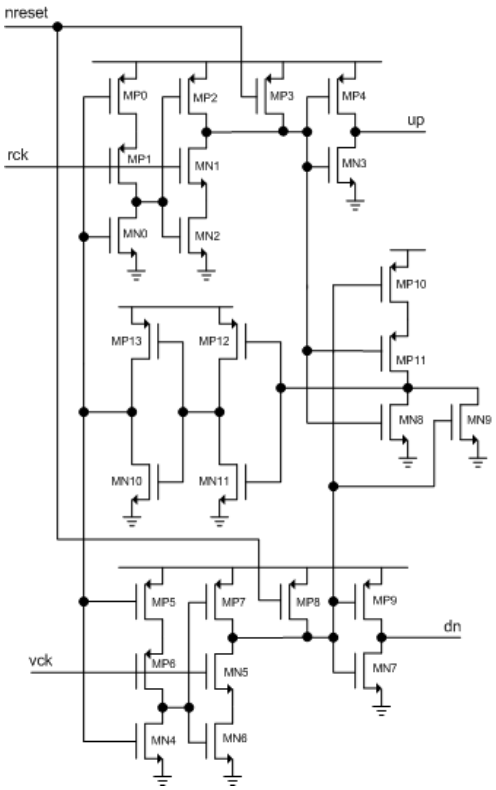


Figure 7.43: The schematic of the PFD.

3. The high frequency output buffer includes external inductors and capacitors on the PCB. The additional off-chip noise could be introduced through these component and increase the measured phase noise.
4. The error of the instrument used for the phase noise measurement. It would be better to measure a reference VCO with the known phase noise in the future.

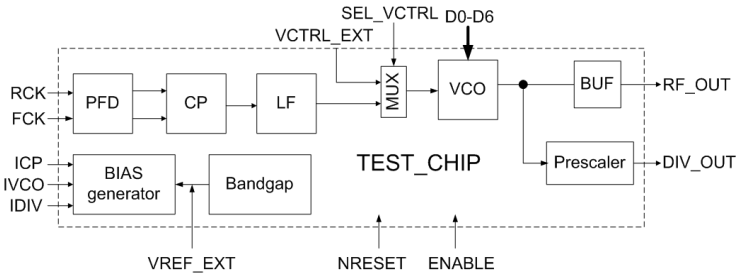


Figure 7.44: Block diagram of the PLL test chip.

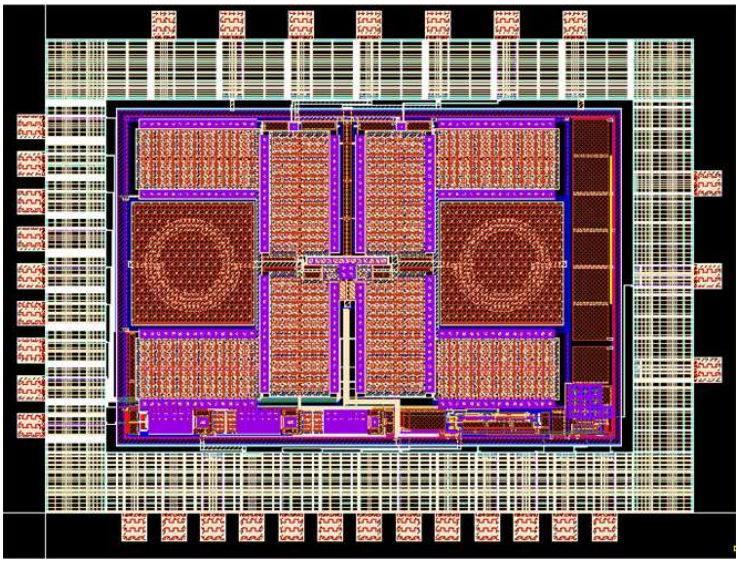


Figure 7.45: Layout of the PLL test chip.

Vctrl (V)	f_{vco} (GHz) D6-D0 = 0	f_{vco} (GHz) D6-D0 = 1	f_{vco} (GHz) D6-D0 = 62	f_{vco} (GHz) D6-D0 = 63	f_{vco} (GHz) D6-D0 = 126	f_{vco} (GHz) D6-D0 = 127
0.2	1.45474	1.45301	1.36026	1.36790	1.28891	1.28877
0.4	1.45476	1.45303	1.36934	1.36798	1.28894	1.28880
0.6	1.45477	1.45304	1.36939	1.36803	1.28898	1.28885
0.8	1.45478	1.45305	1.36940	1.36804	1.29002	1.28889
1.0	1.45480	1.45307	1.36949	1.36813	1.29004	1.28891
1.2	1.45482	1.45308	1.36953	1.36817	1.29010	1.28896
1.4	1.45486	1.45313	1.36956	1.36819	1.29013	1.28900

Table 7.15: Measured VCO output frequency for several coarse tuning codes.

Figure 7.46: The measured VCO output phase noise.

7.2.4 Measurement of the PLL

With a frequency divider implemented in a FPGA, the test PLL chip can be connected in a closed loop and measured. The output phase noise of the

closed PLL is -87 dBc at 100 kHz offset from the carrier as shown in Figure 7.47. Because of the reduced VCO gain, the closed loop bandwidth of the PLL is much smaller than the designed value (120 kHz). The phase noise out of the bandwidth frequency should be dominated by the VCO noise only if the PLL is well locked. However, the measured PLL phase noise is 10 dB higher than the measured VCO noise. The reason for this noise increase is not clear. One possibility is that the PLL was not locked so that the phase noise due to the PFD, the charge pump and the frequency divider were added to the PLL output phase noise with the VCO noise together.

Figure 7.47: The measured output phase noise of the PLL.

7.2.5 Conclusions

The measurements showed some performance degradations compared to the schematic simulations. The most serious problem is the low VCO gain, which is mainly caused by an design error in the multiplexer. The multiplexer is used to select the source of the VCO control voltage, which is either from the external input out of the chip or from the loop filter output. The error in the multiplexer causes the VCO control voltage is largely attenuated. On the other hand, the parasitic capacitance due to the layout further reduced the VCO gain. The VCO phase noise is 6 dB higher than the simulation. The possible explains are: (a) The VCO parasitic capacitance to the substrate has low quality factor, and was not simulated (b) The varactor is not biased on its best operating range, and was not well simulated. The PLL phase noise is even worse than the VCO because it could not go into lock due to the low VCO gain.

Chapter 8

Conclusions

The main focus of this thesis has been on study, analysis and design of low phase noise, low jitter and low power CMOS PLL. The dominated phase noise source in a PLL is the VCO. The other blocks, such as PFD and charge-pump, contribute to in-band phase noise. Understanding the generating mechanism of phase noise in VCO and other PLL blocks is the theoretic basis to design low phase noise PLLs.

In this thesis, the phase noise mechanism of VCOs, including both of ring-oscillator based VCO and LC tank based VCO, were deeply studied and analyzed. Three important VCO phase noise models, Leeson's linear model, Hajimiri's time-variant model and Samori's non-linear model, were studied and compared. Samori's model turned out to be the best for analyze the phase noise of LC VCO, because it can explain phase noise generated from both of thermal noise and flicker noise, and can be used to easily derive analytic phase noise equations. The key point of Samori's phase noise theory is that the transconductor switching between the cross-coupled transistors in LC VCOs causes a spectrum folding of the wide band noise , such as white noise, into the frequencies near the resonant frequency. The low frequency noise, such as flicker noise, is up-converted into the frequencies around the oscillation frequency mainly due to the two mechanisms: (a) The oscillation frequency is not only dependent on the L and C values of the LC tank, but also dependent on the bias current, resonant frequency. (b) The flicker noise in the tail current causes the random amplitude modulation (AM), and this random AM modulates the effective capacitance of the varactor, thus converting AM

to FM. The phase noise analysis results in some general design guidelines for the optimisation of phase noise performance:

1. The quality factor Q_L of the tank inductor should be as high as possible.
2. The oscillation amplitude has to be as large as possible. Using the maximum bias current allowed by the power budget, and operating VCOs in the edge of voltage limited region can effectively achieve the available maximum amplitude.
3. The gain of the VCO has to be as small as possible in order to minimize flicker noise up-conversion.
4. The flicker noise in the tail transistor is the main contributor to the close-in phase noise.

Abidi's model was studied for the phase noise and jitter process in CMOS inverter-based and differential ring oscillators. A time-domain jitter calculation method is used to analyze the effects of white noise, while random VCO modulation is used for flicker noise. Analysis showed that in differential ring oscillators, white noise in the differential pairs dominates the jitter and phase noise, whereas the phase noise due to flicker noise arises mainly from the tail current.

The analysis of PLL in-band phase noise caused by PFD and charge pump turned out that operating them in the highest possible frequency is a direct way to minimize jitter and phase noise. The non-linearities of charge pump have to be minimized to reduce phase noise.

Several practical design techniques for reducing the phase noise of CMOS LC VCO were presented in this thesis. Noise filtering technique can be used to reduce the phase noise due to tail transistor. Discrete tuning can reduce VCO gain so that the close-in phase noise due to AM-FM up-conversion is minimized. Harmonic tuned LC tank can reduce phase noise through increasing the slope of the VCO output at the crossing point. Tail current shaping can reduce phase noise through shaping the tail current into narrower current, so that most of the energy is delivered to the resonator at the less phase sensitive instant.

Two prototype PLLs were designed and realized. The first PLL chip was realized with AMS 0.35 μm CMOS process and applied as clock generator in a LVDS transmitter. A novel low noise charge pump was designed to minimize the non-linearities, such as mismatch, charge sharing and leakage current. The differential ring oscillator based VCO were designed to achieve low jitter and wide tuning range. The PFD based on dynamic logic circuit

and the passive loop filter are preferred for low power consumption. The PLL achieved an optimal jitter-power consumption product while occupying a small area and featuring a large locking range (140 - 560 MHz). The measured rms jitter was 7 ps at 350 MHz output frequency. The PLL consumed 12 mW with 3.3V power supply, and occupied 0.09 mm^2 silicon area.

The second chip was a 1.5 GHz fractional-N PLL and realized with UMC 0.18 μm CMOS process. It was used as a reference frequency in an atomic clock system. The most challenging specifications are its low close-in phase noise and extremely low VCO gain of 1 MHz/V. A PMOS-only LC-tank based VCO with a 7-bits coarse tuning capacitance bank and noise shaping capacitor was implemented. The test chip integrated also an PFD based on dynamic logic circuit, an wide-swing low voltage charge pump, a divide-by-8 analog prescaler, a third-order passive loop filter. The simulated phase noise is -103 dBc at 100 kHz. The measured VCO phase noise was -97 dBc at 100 kHz. The measured PLL output phase noise was -87 dBc. One serious problem of this chip was that the measured VCO gains are about 10 times lower than the expected value due to a design error for the multiplexor at the VCO input. Another problem is the large parasitic capacitance, which could degrade the VCO phase noise because of its low quality factor. The low VCO gain caused also the PLL to be impossible to become locked.

8.1 Future works

Although in this thesis we tried to do an extensive study on the low phase noise and low power CMOS PLL design theories and technique, the phase noise theories studied in this thesis are not fully completed yet, and many interesting topics remain to be investigated in the future. New design techniques for low phase noise and low power PLL studied are expected to be developed and practised. For example:

1. The exact quantitative relation of the phase noise to flicker noise for LC VCO is not yet available.
2. The phase noise caused by the power supply and the substrate noise is not well studied.
3. The design of high quality inductor. For the second test chip, the inductors from the UMC library have really poor quality factor. The quality factor of the tank is a main limitation of the phase noise performance.

The design techniques presented in the thesis were not fully implemented in the chips. The measured performances of the 1.5 GHz PLL chip did not fulfill the specification. A redesign has to be done. Some tips for improving the performances of the redesign are listed in follows:

1. Using differential charge pump and differential varactor to reduce the common mode noise and mismatch of the charge pump, also the flicker noise upconversion in VCO.
2. Biasing the varactors DC operating point around 0 V. In the prototype design, the varactors always worked on the negative gate-bulk voltage region. This might be the reason that the measured VCO gains are much lower than the measured values.
3. Replacing the tail transistor with a resistor to removing flicker noise upconversion.
4. Increasing the transistor sizes in the PFD and charge-pump to reducing the flick noise in these blocks.
5. Extracting the parasitic resistance and capacitance from the layout. During the prototype design, layout extraction could not be done due to designkit problem.
6. Adjusting the charge pump current and VCO bias current on chip. In the prototype design, the charge pump current and the VCO bias current are adjusted through the resistors out of the chip, which could add extra noise to the chip.

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