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High Sensitivity High Dynamic, Digital CMOS Imager

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ABSTRACT

Key words: Active pixel sensors, CMOS image sensors, high-sensitivity imager, low-noise electronics, high-dynamic imaging, digital camera, analog-digital conversion

CMOS image sensors offer over the standard and ubiquitous charge-coupled devices (CCD imagers) several advantages, in terms of power consumption, miniaturization, on-chip integration of analog-to-digital converters and signal processing for dedicated functionality. Due to the typically higher readout noise of CMOS cameras compared to CCD cameras applications demanding ultimate sensitivity were so far not accessible to CMOS cameras. This paper presents an analysis of major noise sources, concepts to reduce them, and results obtained on a single chip digital camera with a QCIF resolution of 144x176 pixels and a dynamic range in excess of 120 dB.

1. INTRODUCTION

Since the first publications on CMOS-imagers with in-pixel signal buffering in 1991 [1], also known as "Active Pixel Sensor" or APS image sensor [2], their advantages for applications requiring low power, low voltage and "system-on-chip" have been widely accepted. So far applications requiring ultimate sensitivity were thought not realizable with CMOS imagers due to the higher readout noise compared to their CCD counterparts. Ultimate sensitivity is a system requirement. Noise contributions from all components have to be reduced, using low noise circuit design techniques, and developing architectures eliminating the major noise sources. The fundamental noise source in all photo detection applications is the shot noise of the incident light. For a given photon flux, only an increase in the number of collected photons, by increasing pixel area and full well capacity, can reduce this noise contribution. A detection system with ultimate sensitivity should be photon shot noise limited. The other major noise sources in a CMOS imager can be divided in 1. Structural or Fixed Pattern Noise (FPN) and 2. Temporal noise.

FPN arises from process variations and component mismatch. In particular in APS imagers, the threshold voltage variations of the in-pixel voltage follower lead to a different offset from one pixel to the other requiring appropriate circuitry, e.g. double-sampling or correlated double sampling, to suppress these offsets.

Numerous sources contribute to the overall temporal noise of image sensors, such as the reset noise of the integrating photodiode, the channel noise of the in pixel voltage follower (white noise and flicker noise), the shot noise of the dark current and the noise added along the readout signal path.

For digital imagers, the quantization noise of the analog to digital converter (ADC) needs to be considered as well. In order to preserve the full dynamic, no gain, or only very little gain can be added along the readout chain, therefore the

noise contributions of each stage add directly to the signal. Only a system that takes into account all these noise sources and reduces their impact can reach the ultimate possible sensitivity.

This paper is divided into 6 parts. In Section 2 the major noise sources are analyzed and various techniques to reduce their effect are presented. Section 3 and 4 describe techniques to increase sensitivity in image sensors and the concept of floating point ADC respectively. Section 5 presents the circuits implemented and a prototype imager, whereas experimental results are reviewed in Section 6.

2. MAJOR READOUT NOISE SOURCES AND NOISE REDUCTION TECHNIQUES FOR CMOS IMAGE SENSORS.

Most CMOS image sensors use the Active Pixel Sensor (APS) architecture drawn in Figure 1. A reverse biased p-n junction is used as a photodetector. The generated current is integrated on the parasitic capacitance of the photodiode. A source follower is used to buffer the signal voltage. Two switches are used to reset the photodiode voltage and to select the pixel for read out.

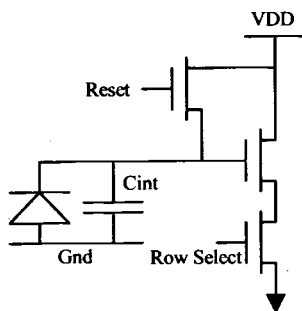


Figure 1: Schematic of classical Active Pixel

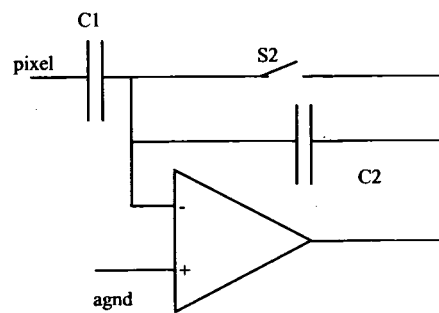


Figure 2: Schematic of the switched capacitor circuit for pixel offset subtraction

2.1 Fixed Pattern Noise

Often the largest noise source in APS imager is due to offset voltage variations between individual pixels. Every pixel buffer amplifier has a different offset voltage due to tolerances in process parameters such as gate oxide thickness, doping levels etc... Since this noise is time invariant, it can be easily corrected for off-chip. Nevertheless, a system reducing the pixel to pixel offset is preferable. This offset can be corrected by computing the difference of the output voltage of the pixel buffer after reset and after integration. This difference can easily be computed in the analogue domain with a switched capacitor circuit (Figure 2).

In the first phase, the pixel is set in reset, and the reset value is sampled on the capacitor C1. The switch S2 is closed to reset the capacitor C2 and to sample the operational amplifier input offset. In the second phase S2 goes open, and the signal value of the pixel is applied. Now the integrated signal value is sampled on C1 and the output of the operational amplifier gives the difference between the reset and the signal value.

2.2 Flicker Noise

This double sampling technique is also advantageous to reduce the $1/f$ (flicker) noise of the in-pixel source follower and associated with charge carrier traps in the semiconductor [3].

2.3 Thermal Noise

The white thermal noise corresponding to the Johnson resistor noise of the channel of the in pixel source follower can be reduced by appropriate operation and dimensioning of the follower transistor. The input-referred gate voltage variance depends on the temperature T , bandwidth B and transconductance g_m , and n the ideality factor according to

$$v_{noise} = \sqrt{\frac{4kT \cdot n}{2 \cdot g_m} \cdot B} \quad (1)$$

The transconductance g_m being at a given current higher in weak inversion, the thermal noise contribution can be reduced by biasing the MOS transistor in weak inversion. The channel noise can also be further reduced by decreasing the bandwidth of the in pixel source follower. This can be done without reducing the overall sensor readout speed if an optimized addressing scheme as described below is used.

The sensor addressing is divided in two half, a double sampling circuit, as drawn in figure 2, is implemented for each column in order to permit pre-loading of the values in one half of the sensor, while the other half of the sensor is read out. The readout timing can be seen in Figure 3. The sensor is operated in a rolling shutter mode, where the number of lines in the reset state controls the exposure time. The four readout phases are repeated constantly. Once the last line is reached, readout begins immediately with the first line again.

In the first of the four phases, the reset values of row i are loaded to the capacitor $C1$ in the left half, while the signal of the previous line is read out in the first quarter of the right side. In the second phase the subtraction of the integrated signal value begins in the left half, while the last quarter of the line $i-1$ is read out.

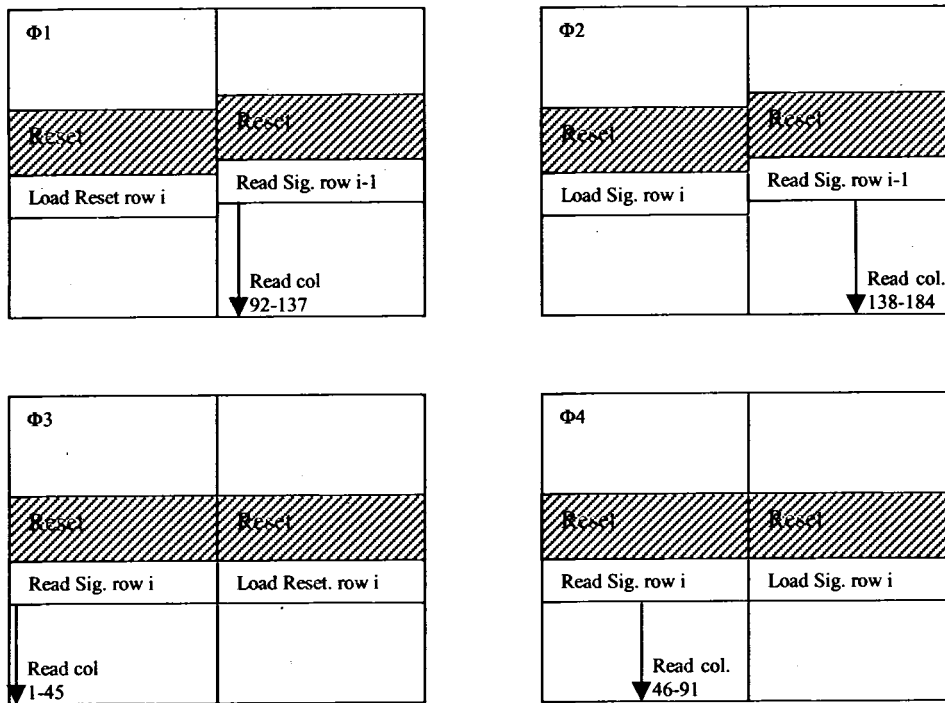


Figure 3: Readout timing with reduced in pixel bandwidth for a sensor with 184 columns

In the third phase, signal readout of line i begins in the first column. In the right half, the line $i-1$ is put now in reset state, and the reset values of line i are loaded to the capacitor $C1$ at the bottom of the column. In phase four, the second

quarter of row i is read out, while in the right half, the integrated signal of the pixels in row i is subtracted from the reset values.

The bandwidth of the double sampling OTA implemented in each column can not be significantly reduced, since although the time interleaved readout scheme was implemented, it has to drive the analogue bus at the pixel rate. But since this OTA has to be implemented on the column pitch, limitations in space and power consumption are less severe than in the pixel and better noise performance even at increased bandwidth can be realized.

Further the shot noise of the source follower bias current has to be considered. Especially if the bias current of the in pixel source follower is reduced to place the transistor in weak inversion. This noise is not thermally generated, but results from the Poisson distribution, of the electrons forming the bias current (Equation 2).

$$i_n^2 = i \cdot q \cdot B \quad (2)$$

3. SENSITIVITY INCREASING TECHNIQUES FOR CMOS IMAGE SENSORS

The sensitivity describes the relation between impinging light and the sensor output signal. Sensitivity is often measured in units of volts per photon or volts per electron. The latter figure, also referred to as “conversion gain”, thus describes the voltage swing arising from one single photogenerated electron on the conversion capacitance. In the case of an APS imager, the conversion capacitance is usually the parasitic capacitance of the photodiode itself. Therefore this capacitance decreases for decreasing photodiodes, leading to the highest voltage swing per incoming photon for a minimum size photodiode. Minimum size photodiodes are however not optimal for high sensitivity image sensing. Due to their small area, they can collect only a small part of the incoming optical signal and moreover limit the maximum full well capacity. Therefore a better figure for the sensitivity is the signal generated by a given optical density (and well defined wavelength) on the sensor surface, as measured for example in volts per joule per square meter or in volts per photons per square meter. For digital image sensing, sensitivity can easily be expressed in Arithmetic Digital Unit (ADU) per photons per square meter. Usually one ADU equals the least significant bit of the AD converter. In this way, the sensitivity already takes into account very important parameters such as fill factor (ratio of photosensitive area to total pixel area) and quantum efficiency, giving therefore more realistic and appropriate criteria for the optimization image sensors than the simple volt per electron figure.

High sensitivity imaging calls for pixels with a high fill factor in order to collect a maximum of the impinging light. Secondly, the ratio between the surface of the photodiode and its parasitic capacitance must be optimized. Proper layout techniques and the use of relatively large photodiodes help to fulfill both requirements. For large photodiodes indeed, the edge capacitance becomes less important leading to an increased ratio between light-collecting surface and conversion capacitance. Moreover the fill factor is increased for increasing pixel size since the surface required for the readout circuitry is independent of the pixel size. The total chip area and the required resolution usually limit pixel size.

4. FLOATING POINT AD CONVERSION

The most fundamental noise source in every light detecting system is related to the quantum noise of the impinging photons. This noise is known as the photon shot noise. For most light sources the number of emitted photons follows a Poisson distribution. The resulting noise (standard deviation of the detected number of photons) is then equal to the square root of the total number of detected photons. Assuming a quantum efficiency η and a conversion capacitance C , the resulting shot noise on the voltage signal is expressed by

$$v_{shotnoise} = \sqrt{n} \cdot \eta \cdot \frac{q}{C} \quad (3)$$

The maximum signal to noise ratio (SNR) is thus limited to:

$$SNR_{\max} = \frac{n}{\sqrt{n}} = \sqrt{n} \quad (4)$$

A photo detection system with ultimate performance should in the broadest possible range be limited only by the shot noise. For a digital imaging system, thus the quantization steps of the AD converter should be smaller than the shot noise of the smallest detectable signal. This constraint will immediately define the required number of bits for an AD converter as a function of the maximum detectable signal V_{\max} , and the shot noise related to the minimal detectable signal $V_{\text{shot noise min}}$ (Equation 5).

$$N_{\text{bit}} = \log_2 \left(\frac{V_{\max}}{V_{\text{shot noise min}}} \right) \quad (5)$$

On the other hand, the required bits for an AD converter, in order to obtain a given SNR, when digitizing a sinusoidal signal of maximum dynamic can be computed using

$$N_{\text{bit}} = \frac{SNR + 1.76}{6.02} \quad (6)$$

According to equations 4 and 6, the effective number of bits of the AD converter decreases for small signals, while equation 5 results in an increasing requirement of resolved bits for decreasing optical signals. In figure 5, the required number of bits, determined by equations 5 and 6 respectively, are plotted versus the total number of impinging photons, assuming a conversion capacitance of 50 fF and a maximum voltage swing of 3 V.

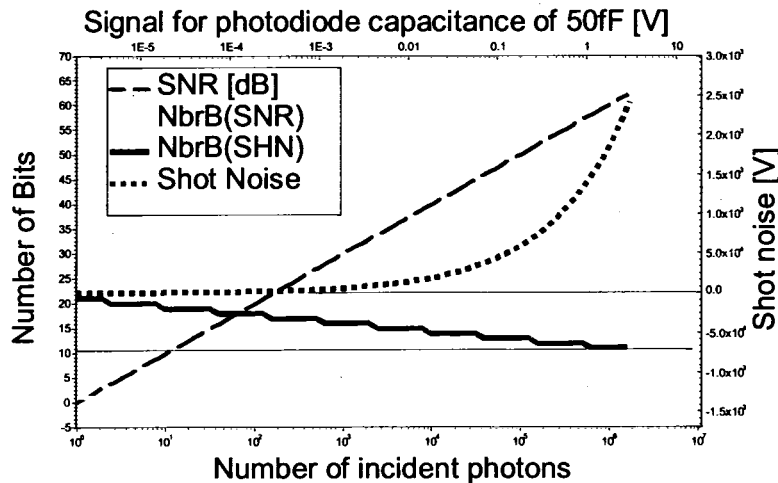


Figure 5: SNR in dB "SNR", number of ADC bits required to equal the ADC SNR and the shot noise SNR "NbrB(SNR)" number of ADC bits required to resolve the shot noise "NbrB(SHN)", and the shot noise in volts "Shot Noise". All curves are for a pixel with a conversion capacitance of 50 fF and a maximum voltage swing of 3V.

From those observations, it follows that an absolute AD converter with high precision either gives out mainly the quantization of the shot noise for big signals, or suppresses signal information by too important quantization steps at small input signals. A mean to overcome these limitations at reduced system cost and without deterring the overall performance of the imaging system is to use a floating point AD conversion, i.e. a representation which gives out a

bitcode divided in an exponent and a mantissa. The novel digital imager described in the following paragraph illustrates this approach.

5. A QUARTER CIF RESOLUTION CMOS DIGITAL IMAGER

A single-chip digital imager with 144 x 176 pixels (QCIF resolution) has been designed and manufactured in a standard 0.5 μm CMOS process. The realized digital image sensor features a very high dynamic range and a frame rate of more than 30 frames per second at very low power consumption.

A pixel pitch of 25 μm has been determined as an optimum size in order to achieve a high fill factor of 65%, while maintaining a reasonable overall chip size of 6.3 x 5.8 mm^2 . The parasitic capacitance of the diode diffusion was about 80 fF.

In order to reduce the thermal noise, the bandwidth of the source follower was reduced to a quarter of the column frequency, as described in section 4. This bandwidth reduction was realized by choosing a pixel bias current of 120 nA, being on the edge where channel shot noise becomes important. The flicker noise is reduced considerably by a double sampling stage. To reduce the flicker noise even further, the in pixel source follower was implemented with non-minimal length.

The capacitors in the double sampling stage were chosen sufficiently big to reduce the effect of the sample and hold noise (kT/C) below the desired noise level of the pixel source follower. To ensure sufficient linearity and accurate settling, a high open-loop gain has been selected for the OTA.

The floating point AD conversion was implemented by means of a programmable gain amplifier with binary gain settings. Using the gain settings as exponent bits and the AD converter output code as mantissa, a frame wise floating point conversion can easily be realized on system level.

To further increase the dynamic range, an optional logarithmic compression at high intensities was implemented.

A ten bit AD converter was implemented on-chip using the Redundant Signed Digit RSD algorithm as described in reference [4]

All timing and control signals for the chip are generated in an internal logic block. A serial interface allows to easily program the exposure time as well as different operation modes of the sensor.

6. MEASUREMENT RESULTS

Figure 6 shows a detailed plot of the fixed pattern noise. The fixed pattern noise could be reduced to less than 0.5% by the double sampling technique. It can be seen that the fixed pattern noise mainly is due to border effects, on the edge of the pixel array.

The measured results for the temporal noise were less satisfying. Using the on chip AD converter, a temporal noise of 0.6 ADU out of 512 was measured. Increasing the gain of the programmable gain amplifier for the ADC did not improve the input referred noise, indicating that the noise is generated before the amplifier. Measurements on an analogue test output indicated, that the noise might be added to the signal path by pass gates, directly addressed out of the control logic. The logic levels showed important spikes, when transitions on the output lines occurred.

The logarithmic compression at high intensities permitted to increase the dynamic range over 120 dB, without an increase in the fixed pattern noise. Spatial resolution tests with the knife-edge method demonstrated that this high dynamic range takes place over 5 pixels only. Figure 7 illustrates the wide dynamic range of the sensor. The filament of the light bulb and the test chart in the background can be seen clearly. The picture presents raw data, i.e. without any off-chip correction

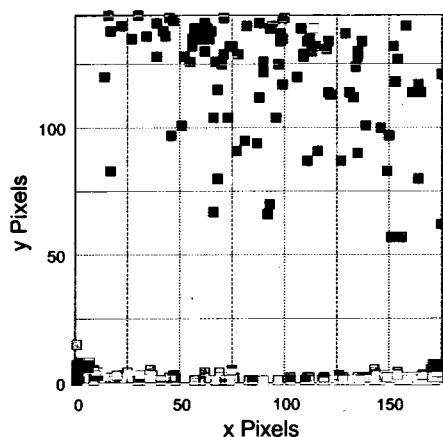


Figure 6: Map of the sensor array. Pixels with a value above 128 ADU (out of 256) appear light, whereas pixels with a value below 123 ADU appear dark.



Figure : Sample image (raw data) demonstrating logarithmic compression for high illumination intensities.

7. CONCLUSIONS

The present work analyses major noise sources in a CMOS image sensor and shows ways to reduce them. The integration of these noise reduction techniques on a digital imager showed good results for the fixed pattern noise cancellation. The temporal noise analysis showed that more work is required to further reduce the effects of digital cross talk to analogue signals. The logarithmic compression for high illumination intensities showed excellent performances, the image quality being presently limited by stray light in the optics. The dynamic range could be significantly extended, without compromise with respect to fixed pattern noise, sensitivity, speed or contrast.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

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