A Low-Jitter and Low-Power CMOS PLL for Clock Multiplication

Xintian Shi, Kilian Imfeld, Steve Tanner, Michael Ansorge and Pierre-André Farine
Institute of Microtechnology
University of Neuchâtel
Breguet 2, 2000 Neuchatel, Switzerland
E-mail: xintian.shi@unine.ch

***Abstract*— this paper describes a phase-locked loop (PLL) designed for clock multiplication in a LVDS transmitter. The PLL consists of a novel low-jitter charge-pump, a fully differential ring-oscillator based VCO, a dynamic-logic PFD, a 2nd order passive loop filter and a digital frequency divider. The PLL exhibits simultaneously low jitter and low power consumption. It has been integrated into a 0.35 µm CMOS process, occupying 0.09 mm² of silicon area. For a 350 MHz output frequency, the circuit features a cycle-to-cycle jitter of 7.1 ps rms and 65 ps peak-to-peak. At that frequency, the PLL consumes 12 mW from a supply voltage of 3.3 V.**

I. INTRODUCTION

Thanks to its high speed, low noise and low power properties, low voltage differential signaling (LVDS) is a widely used interfacing technology addressing the needs of today's high performance data transmission applications. Figure 1 shows the block diagram of a typical LVDS transmitter. For serializing the parallel input data, a phase-locked loop (PLL) is conventionally used for clock multiplication. In this paper, we present a PLL designed for a 7x LVDS serializer, and specified to feature low timing jitter for achieving low bit error rate (BER), and low power consumption for portable applications. In a PLL, the two most important jitter sources are the charge-pump and the voltage-controlled oscillator (VCO). Since the jitter is proven to be inversely proportional to the power consumption [1 – 3], a trade-off between these two parameters must be found. The proposed implementation features simultaneous low jitter and low power consumption thanks to (i) a novel charge-pump that effectively minimizes non-idealities such as charge sharing, clock feedthrough, current and timing mismatches, and (ii) a fully differential ring oscillator based VCO that exhibits a good power supply and substrate rejection ratio (PSRR). Power consumption is further reduced by using a dynamic logic phase-frequency detector (PFD), and a 2nd order passive loop filter.

The paper is organized as follows: In Section 2, low jitter design issues for PLLs are discussed. Section 3 presents the design and implementation of the PLL circuit, and Section 4 the measurement results. Section 5 concludes the paper.

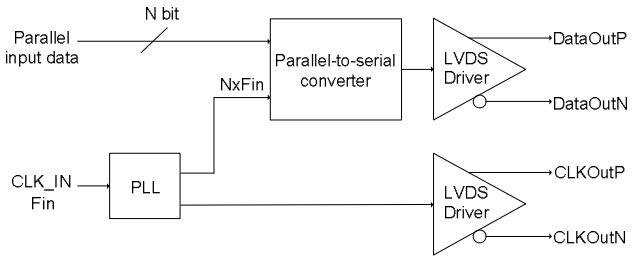

Figure 1: Block diagram of a serial LVDS transmitter.

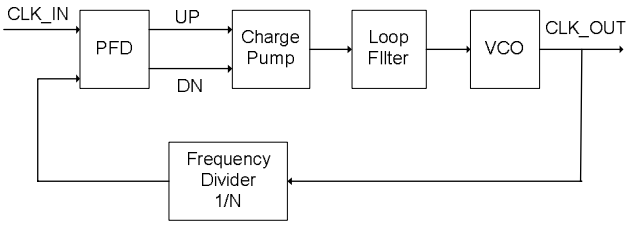

Figure 2: Block diagram of a typical PLL.

II. LOW JITTER DESIGN CONSIDERATION

A typical PLL architecture is depicted in Figure 2. It consists of a phase frequency detector (PFD), a charge-pump, a loop filter, a voltage-controlled oscillator (VCO) and a frequency divider. Each building block contributes to the PLL output timing jitter, but the VCO and the charge-pump are the most important jitter sources.

Ring oscillator based VCO can be implemented by either single-ended or differential delay cells. Single-ended ring oscillators such as current-starved inverters exhibit lower power consumption and lower intrinsic phase noise because they need fewer transistors than differential ring oscillators, but they have poor power supply and common mode noise rejection ration. Since power/ground and substrate noise introduce significant timing jitter in ring oscillator VCOs [1], fully differential ring oscillators are preferred for low jitter design due to their superior PSRR and immunity to common mode noise. The ratio of the cycle-to-cycle jitter $\Delta\tau$ to the VCO period T_{vco} is given by [2]:

$$\frac{\Delta\tau^2}{T_{vco}^2} = \frac{1}{T_{vco}} \cdot \frac{kT}{I_{ss}} \cdot \frac{a_v \xi^2}{V_{GS}-V_T} \quad (1)$$

where ξ is the noise contribution factor (ranging normally from 1.3 to 1.9), I_{ss} is the tail current of a differential delay cell, V_{gs}-V_T is the on-voltage of the differential pair in a delay cell, and a_v is the small signal gain of the delay buffer. To minimize the jitter, the following design principles must be adopted: (i) minimizing a_v, (ii) using long, narrow, low V_T transistors for the input pair of the delay buffer, (iii) for a giving power budget, using a minimal number of delay stages so that I_{ss} is maximized. Because the jitter is inversely proportional to the tail current of the delay cell, a trade-off between power consumption and jitter cannot be avoided.

In a PLL, the charge-pump converts the PFD output signals into currents for charging or discharging the loop filter, whose output regulates the VCO. Therefore, any noise generated by the charge-pump directly causes phase jitter due to VCO frequency variations. The inherent non-ideal behaviors of charge-pumps, such as leakage current, delay mismatch, clock feed-through, current mismatch and charge sharing [3], are the main contributors to the VCO phase jitter. The analytic expression of the phase error is given by:

$$\Delta\Phi = \Delta\Phi_{leak} + \Delta\Phi_{curr} + \Delta\Phi_{mistime} + \Delta\Phi_{charge}$$
$$= 2\pi \cdot \left(\frac{I_{leak}}{I_{cp}} + \frac{\Delta I}{I_{cp}} \cdot \frac{T_{on}}{T_{ref}} + \frac{\Delta T \cdot T_{on}}{T_{ref}^2} + \frac{\Delta Q}{C_l \cdot I_{cp}}\right) \quad (2)$$

where I_{cp} is the charge-pump current, I_{leak} is the leakage current, ΔI is the mismatch current, ΔT is the switch time mismatch, ΔQ is the mismatch charge due to charge sharing, C_l is the total capacitance of the loop filter, T_{on} is the PFD turn-on time and T_{ref} is the period of the input reference clock. The phase error results in a periodic ripple of the VCO control voltage, even when the PLL is locked. This voltage ripple causes the VCO output timing jitter. Several approaches are proposed to minimize the charge-pump non-idealities. Dummy switches can be introduced to minimize the charge sharing effect [4]. An error amplifier can be used to reduce the mismatch current [5]. Switching time mismatch can be minimized by balancing the UP and DN paths [6]. Fully differential charge-pumps can effectively minimize the mismatches, increase supply and substrate noise rejection and voltage swing, but the cost is higher power dissipation, larger area and more complex circuitry.

III. Design and Implementation

In order to fulfill simultaneously low-power and low-jitter operation, we propose a novel single-ended low jitter charge-pump circuit, associated with a fully differential VCO, a dynamic logic PFD, and a second-order passive loop filter. These blocks are described in the next paragraphs.

A. Phase-Frequency Detector

Figure 3 shows the schematic of the implemented dynamic logic PFD. The operation detail of the PFD is described in [7]. Compared to a conventional static logic PFD, the dynamic logic PFD needs fewer transistors and consumes less power. By inserting two invertors in the feedback signal path, the PFD generates short coincident pulses UP and DN, even when the PLL is in lock, so that the dead zones are removed. The reset signal NRESET ensures a valid output logic state after power-on.

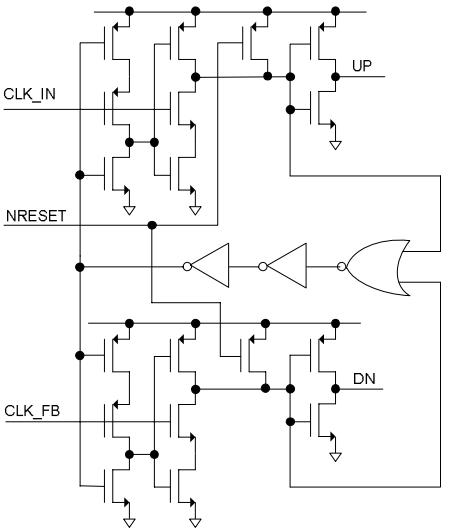

Figure 3: Schematics of the PFD.

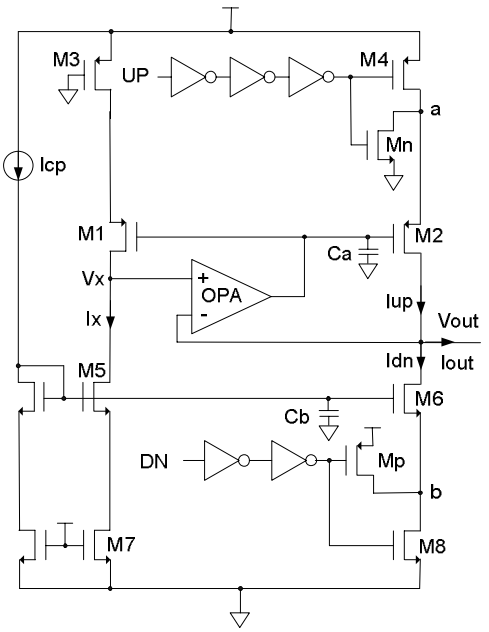

Figure 4: Schematics of the proposed charge-pump.

B. Charge-Pump

A novel charge-pump circuit as shown in Figure 4 is implemented for minimizing the non-idealities and achieving low jitter performance. Two transistors Mn and Mp remove most of the charges stored on the parasitic capacitances of nodes *a* and *b* during the turn-off periods of UP and DN signals, thus charge sharing effect is greatly minimized [4].

The operational amplifier OPA and the transistor M1 compose a feedback amplifier to force V_x to equal the output voltage V_{out}. The current mirror transistors M1 – M8 are matched each other, resulting in matched currents: $I_{up} = I_{dn} = I_x$, regardless of the output voltage [5]. By carefully designing the size of the inverters, the delays of UP and DN input path can be matched each other regardless of the process variations [6], so that time mismatch is minimized. Two capacitors Ca and Cb effectively suppress the voltage spikes caused by clock feed-through. This novel single-ended charge-pump fulfils low jitter and low power consumption while requiring simple design and small area.

C. *Voltage-Controlled Oscillator*

The implemented VCO consists of 3 elements, as shown in Figure 5. The voltage-to-current converter converts the input voltage into a biasing current for the current-controlled oscillator (CCO), which features an oscillation frequency proportional to the biasing current. The level shifter converts the small amplitude CCO output signal into a rail-to-rail CMOS level signal. Each one of these elements is described in the following paragraphs.

Current-controlled oscillator: The CCO circuit shown in Figure 5 is the core of the VCO. It consists of a fully differential, 3-stage ring oscillator with a replica biasing circuit [8]. Each stage includes a source coupled differential NMOS pair, loaded with PMOS transistors operating in triode region. This fully differential structure has a good ability to reject common mode noise due to power supply fluctuation or substrate noise coupling. The replica biasing circuit holds a constant output swing independent of the supply variations. The delay time of each stage is given by:

$$T_d = \frac{V_{sw} \cdot C_{load}}{I_{ss}} \tag{3}$$

where V_{sw} is the output voltage swing, C_{load} is the total capacitive load at the output of the buffer and I_{ss} is the biasing current of the delay buffer.

Voltage-to-current converter: As shown in Figure 6, the output current is expressed as:

$$I_b = \frac{V_{in}}{R0} \tag{4}$$

The current I_b being almost independent to VDD, a good PSRR is achieved. The voltage-to-current converter provides also the biasing current for the level shifter, so that it is adapted to the VCO output frequency. This approach reduces the power consumption compared to a fixed bias current. From (3) and (4), the VCO gain is then:

$$K_{VCO} \propto \frac{V_{in}}{V_{sw} \cdot R0 \cdot C_{load}} \tag{5}$$

Since V_{sw}, $R0$ and C_{load} are all constant, K_{vco} is linearly proportional to the VCO input voltage V_{in}. A VCO with a small K_{vco} is less sensitive to the control voltage noise, but in this work K_{vco} should be large enough to ensure a wide PLL locking range as required by LVDS transmission application.

Level shifter: The level shifter consists of a folded differential amplifier as input stage, and an inverter as output stage, as shown in Figure 7.

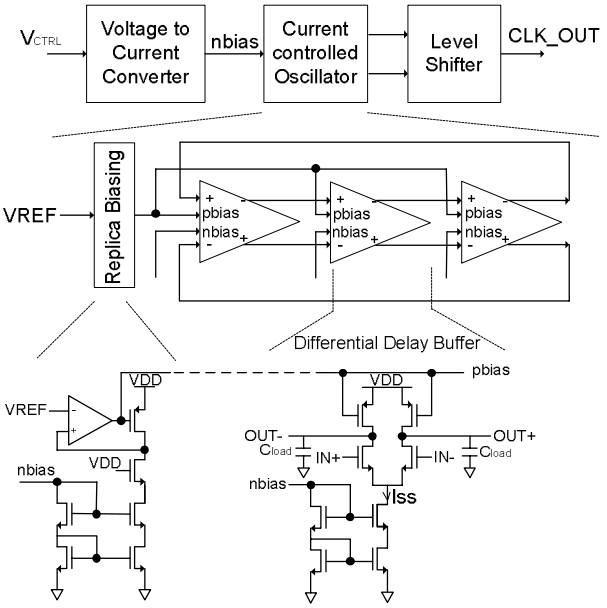

Figure 5: VCO block diagram and schematics.

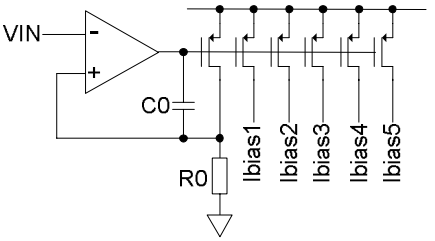

Figure 6: Schematics of the voltage-to-current converter.

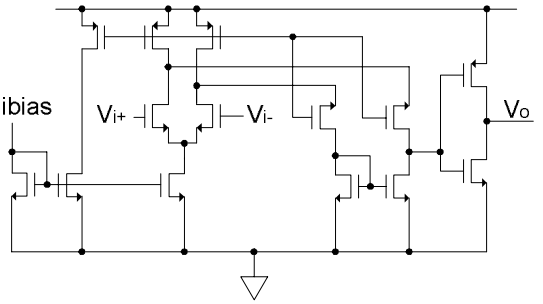

Figure 7: Schematics of the level shifter.

D. *LoopFilter*

The loop filter is a 2nd order passive filter. The values of the filter components can be calculated using the equations presented in [9]. Table I lists the values of the loop parameters and the loop filter components C1, C2 and R2.

Table I: Values used for the designed loop filter.

I_{cp}	K_{vco}	N_{div}	ω_p	ϕ_p	C1	C2	R2
20µA	220MHz/V	7	1.25MHz	50°	3.7pF	24pF	18K

A wide loop bandwidth is desired for suppressing the accumulated jitter generated by the VCO, supposing that the jitter of the input reference clock is negligible. However, for ensuring loop stabilization, the bandwidth should be lower than $1/10^{th}$ of the minimal frequency of the input reference clock, which is 20 MHz in our case.

E. Frequency Divider

The frequency divider is a pure digital logic circuit and divides the input clock with a 1/7 frequency division factor.

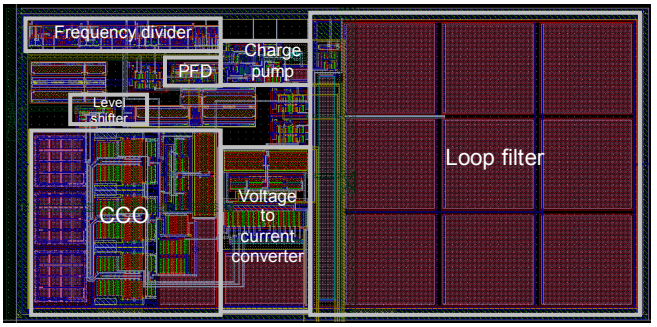

Figure 8: Layout of the designed PLL.

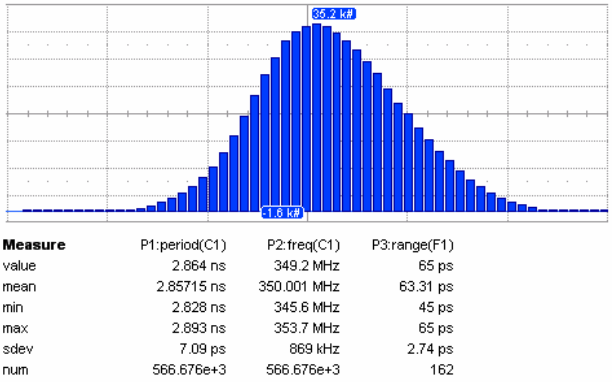

Figure 9: Measured cycle-to-cycle jitter

IV. Fabrication and Experiment Results

The described PLL circuit was fabricated with the AMS 0.35µm CMOS process. Figure 8 shows the layout of the PLL circuit, occupying 410 x 210 μm^2 of silicon area.

The PLL was characterized with a LeCroy SDA 6020 serial data analyzer. Figure 9 shows the measured cycle-to-cycle jitter at 350 MHz. Table II summarizes the main measured PLL parameters and compares them with similar PLL designs. The realized PLL exhibits an optimal jitter-power consumption product, while occupying a significant smaller area and featuring a larger locking range.

Table II: PLL measured parameters and comparison.

	This work	[10]	[11]	[12]
Nominal freq. (MHz)	350	340	300	270
Jitter rms (ps)	7.1	8.4	3.1	4
Jitter p-p (ps)	65	62	22	32
VDD (Volt)	3.3	2.5	3.3	1.8
Power Cons. (mW)	12	100	44	24
Lock range (MHz)	100-560	340-612	300-400	100-500
Silicon area (mm^2)	0.09	0.67	4	0.16
Technology (µm)	0.35	0.4	0.6	0.18

V. Conclusions

This paper presents a low-jitter, low-power, wide lock-range PLL design. The measured jitter is 7.1 ps rms and 65 ps peak-to-peak at 350 MHz, and at that frequency the power consumption is 12 mW with a 3.3 V voltage supply. The PLL features a lock range of 100 MHz – 560 MHz, which allows its use in a wide range of LVDS transmission applications.

References

[1] P. Heydari, "Anylysis of the PLL jitter due to power/ground and substrate noise," IEEE trans. on circuits & systems I, vol. 51, pp. 2404-2416, Dec.2004.

[2] T.Weigandt, B. Kim, P. Gray, "Anylysis of timing jitter in CMOS ring oscillator," IEEE Proceeedings of ISCAS 94, pp. 191-194, May 1994.

[3] W. Rhee, "Design of high-performance CMOS charge pumps in phase locked loop," IEEE proceeedings of ISCAS 99, pp. 545-548, June 1999.

[4] P. Larsson, "A 2-1600 MHz CMOS clock recovery PLL with low-Vdd capability," IEEE JSSC, vol. 34, pp. 1951–1960, Dec. 1999.

[5] J. Lee, M. Keel, S. Lim and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," Electronics Letters, vol. 36, issue 23, pp. 1907-1908, Nov. 2000.

[6] M. Shoji, "Elimination tof process dependent clcok skew in CMOS VLSI," IEEE JSSC, vol. SC-21, pp. 875-880, Oct. 1986.

[7] S. Kim, K. Lee, Y. Moon, D. Jeong, Y. Choi and H. Lim, "A 960-Mb/s/pin inteerface for skew-tolerant bus using low jitter PLL," IEEE JSSC, vol. 32, pp. 691–700, May 1997.

[8] I. Young, J. Greason, K. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," IEEE JSSC, vol. 27, pp. 1599-1607, Nov. 1992.

[9] W. O. Keese, "An analysis and performance evaluation of a passive filter design technique for charge pump phase-locked loops," National Semiconductor application note 1001, May 1996.

[10] D. W. Boerstler, "A low-jitter clock generator for microprocessors with lock range of 340-612 MHz," IEEE JSSC, vol. 34, pp. 513–519, April 1999.

[11] K. Lim, C. Park, D. Kim and B. Kim, "A low noise phase-locked loop design by loop bandwidth optimization," IEEE JSSC, vol. 35, pp. 807–815, June 2000.

[12] S. Williams, H. Thompson, M. Hufford and E. Naviasky, "An improved CMOS ring oscillator PLL with less than 4ps accumulated jitter," IEEE proceeedings of CICC 04, pp. 151-154, Sep. 2004.