Towards an Autonomous Millipede Walking Microsystem

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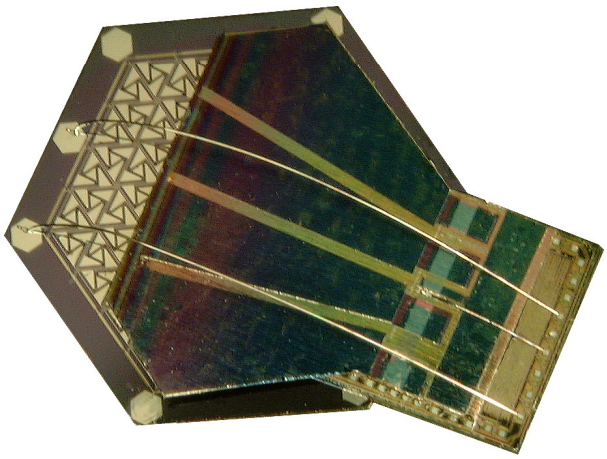
by
David Ruffieux
Ing. Dipl. en Microtechnique, EPFL



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Towards an autonomous millipede walking microsystem

de M. David Ruffieux

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FACULTE DES SCIENCES

La Faculté des sciences de l'Université de Neuchâtel sur le rapport des membres du jury,

MM. N. de Rooij, A. Shah, E. Vittoz (CSEM Neuchâtel) et P. Vettiger (IBM Zürich)

autorise l'impression de la présente thèse.

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J.-P. Derendinger

Abstract

The aim of this work is to demonstrate the possibility of realizing an autonomous microsystem capable of locomotion based on integrated silicon micromachining technologies. An approach based on the collective actuation of a microactuator array has been envisioned so as to take full advantage of the lithographic fabrication process that allows the realisation of very dense repeated planar structures. With this architecture, it is thus possible to couple the tiny motions and forces of each actuator into a macroscopic effect capable of interacting globally with the surface in touch. The elementary structure of the array is inspired from the biological world since it reproduces the structure and functionality of a leg. The actuation principle is based on the piezoelectric effect, which enables to bend a bimorph when a voltage is applied between the two electrodes of the piezoelectric thin film. The actuator is made of three of these bimorphs coupled to a vertical leg acting as a lever. The resulting structure has three active degrees of freedom and is capable of generating elliptical motions in different directions. The fabrication of this microactutor array is based on surface micromachining for the realisation of the bimorph part while the leg and the structural part nesting the actuators are etched through the bulk by deep reactive ion etching. After unsuccessful trials with zinc oxide thin films, the integration of aluminum nitride piezoelectric thin films showed very promising.

In order to achieve an autonomous and mobile microsystem, two more key components are required: one should provision the system with energy while the other take care of its distribution so as to produce a walking pattern. The energy transformation is done by a high voltage solar cell that turn the light of a lamp or the sun into electrical energy. This solar cell is realized with vertical triple stacks of amorphous silicon junctions that are put in series by lithography so as to get a voltage close to $10V$. A low power, specific integrated circuit is required to distribute this energy so as to generate a walking sequence at the pace and in the direction chosen by the remote user. The transmission of information is done optically (infrared) towards the microsystem. The corresponding speed and direction are then decoded so as to control a variable oscillator and a sequencer that switches the high voltage buffers driving the actuators. This circuit has been designed in a standard $5V$ technology though it has to stand voltages as high as $-10V$ and $+20V$ during its operation.

Among the three components, the solar cell and the integrated circuit could be made fully functional. The fabrication of microactuator arrays could be demonstrated but obtaining a fully functional array has not yet been achieved due to the shortcuts that were found on most arrayed devices and the problems encountered in their metallisation. The impossibility of obtaining a perfectly clean platinum bottom electrode after ion milling was identified as the phenomenon responsible for these shortcuts. Individual test actuators could nevertheless be fully characterised and have shown very promising performances in good agreements with simulations. A concept for the assembly of the three components has been validated by gluing and bonding dummy components together. Unfortunately, system level or mechanical coupling experiments could not yet been conducted.

Replacing the bottom platinum electrode by a more convenient material is certainly the way that need to be followed to successfully integrate aluminum nitride in VLSI MEMS designs and demonstrate the operation of the autonomous millipede walking microsystem.

Résumé

Ce travail vise à démontrer la possibilité de réaliser un microsystème autonome sans fil capable de locomotion en utilisant les technologies de microfabrication sur silicium. Une approche basée sur l'utilisation collective d'une matrice d'actionneurs a été retenue, de façon à tirer avantage des procédés de fabrication lithographiques qui permettent la réalisation de structures planaires très denses et répétées. Il est ainsi possible de coupler les petits déplacements et forces de chaque actionneur en un effet macroscopique capable d'interagir globalement avec la surface en contact. L'actuateur élémentaire est inspiré du monde biologique puisqu'il reproduit la structure d'une patte et sa fonctionnalité. Le principe d'actionnement utilise l'effet piézo-électrique qui provoque la déflexion verticale d'un bilame lorsqu'une tension est appliquée entre les deux électrodes de la couche mince active. L'actionneur est constitué de trois des ces bilames couplés à une patte verticale faisant office de levier, ce qui lui confère trois degrés de liberté et permet de décrire des mouvements elliptiques dans différentes directions. La fabrication de cette structure est basée sur les techniques d'usinage de couches minces pour la réalisation de la partie actionneur, alors que les pattes et la partie structurelle logeant les actionneurs sont usinées à travers tout le substrat par attaque plasma profonde. Après des essais infructueux visant à intégrer de l'oxyde de zinc piézoélectrique en couches minces, des résultats très prometteurs ont été obtenus avec du nitrure d'aluminium.

Pour que le système soit effectivement autonome et mobile, deux autres composants clés sont nécessaires. Il faut approvisionner le système en énergie et la distribuer de façon à générer une séquence propre à la marche. L'approvisionnement en énergie est assuré par une cellule solaire haute tension qui transforme l'énergie lumineuse d'une lampe ou du soleil en énergie électrique. Cette cellule est réalisée en silicium amorphe avec une technologie de junctions triples empilées les unes sur les autres et mises en série par voie lithographique afin d'obtenir une tension proche de $10V$. Un circuit intégré spécifique basse consommation est nécessaire pour gérer la distribution de cette énergie afin de produire une séquence propre à la marche dans la direction et à la vitesse désirées par l'utilisateur. La transmission d'information se fait par voie optique (infrarouge) vers le microsystème. L'information de vitesse et de direction est ensuite décodée avant de commander un oscillateur variable et un séquenceur qui contrôle les drivers haute tension dont les sorties sont connectées aux actionneurs. Le circuit a été conçu pour une

technologie standard de *5V,* bien que des tensions allant de *-10V* à *+20V* soient générées durant la séquence.

Le parfait fonctionnement de la cellule solaire et du circuit intégré a pu être démontré ainsi que la fabrication de réseaux de microactionneurs. Cependant, un réseau complètement fonctionnel n'a pas encore pu être fabriqué avec succès à cause de fréquents courts-circuits à travers la couche piézoélectrique et à la difficulté rencontrée dans la métallisation des réseaux. Ces courts-circuits sont très vraisemblablement liés à l'impossibilité d'obtenir une électrode inférieure en platine parfaitement propre après sa gravure par bombardement ionique. Des actuateurs individuels ont néanmoins pu être caractérisés et ont démontré d'excellentes performances en accord avec les simulations. Un concept d'assemblage des trois composants a pu être validé en collant ensemble et connectant électriquement des composants non fonctionnels. Malheureusement, des expériences au niveau système ainsi que la vérification du couplage mécanique des pattes sur le sol n'ont pas encore pu être menées.

Le remplacement de l'électrode inférieur en platine par un matériau plus facile à usiner chimiquement représente certainement la voie à suivre afin d'utiliser avec succès le nitrure d'aluminium pour des applications à haute densité d'intégration et réaliser un démonstrateur du mille-patte autonome.

1. Introduction

1.1 Biologically inspired engineering

Numerous human inventions are directly inspired by the wonders of nature. The wings of a plane for example, are nothing else than a primitive copy of those of a bird, having the same profile that provides lifting force due to different top and bottom air pressures when the wings are placed in an air flow. Nearly all fields of engineering have started paying attention to the world that surrounds us. Chemists develop for example new glues based on those of mussels or attempt to imitate the very stiff spider silk. Boats' propelling systems can advantageously be inspired from marine mammalians for effective drag reduction resulting in lower fuel consumption.

The field of miniaturized integrated products finds an endless source of inspiration in nature, since our world is extensively inhabited by wonderful autonomous tiny animals that exhibit complex behaviors and survive in a harsh and changing environment. VLSI electronic circuits try to emulate the few first neuronal layers of living animals' sensors, such as in vision and audition. Olfaction can be approached through micromachined sensors, which can be made sensitive to different gases and form a cluster capable of differentiating odors. Arrays of tactile sensors can also be implemented at very high densities. It becomes thus possible to integrate smart machines that can sense, analyze and react to a changing environment.

Why not go a step further and try to mimic one of the most striking features of animals: their mobility that allows them to move in their environment, looking for food and mates.

1.2 Locomotion in nature

In nature, a wide diversity of locomotive schemes have been developed by different species in order to best fit their environment. Among all, walking has met a great success for overland two-dimensional motion since it is found on the whole size scale, from insects to huge mammalians. It seems to be one of the most appropriate way to produce motion in different kinds of terrain when friction and adherence forces are generated either as a consequence of gravity forces, surface tension (insect walking on water surface) or chemical interactions (fly walking on a ceiling). However, while taking a closer look at the walking structure of animals of really different weight, one can see that the

structural elements are arranged in different ways. Although the legs are still constructed the same way, i.e. structural elements, joints, and muscles, they do not scale linearly with the size of the animals, nor do they work the same way. An elephant has a leg really different from that of a mouse, though both animals resemble each other. The reason for it is that parameters conditioning the animals do not scale linearly with size. As an example, weight scales with the third power of the size, while bone resistance only with the second power. As a result, an elephant has to have an oversized compressive leg structure to accommodate its heavy weight, while a mouse has a light flexural leg structure. At insect level, weight is not anymore of great concern and the leg thickness can thus be extremely reduced.

1.3 Why microfabrication to mimic locomotion?

When taking inspiration from nature, one should first be sure to pick the right model. Making a twenty kilograms spider-like robot will only yield a pale and awkward imitation of the living one, since oversized flexural elements will increase the total weight of the robot and reduce its performances. Furthermore, to borrow specific structures and architectures from nature, not only the size and weight of the model should match those of the envisioned artificial system, but also to some extent compatibility in how the functionality is given to the structure e.g. the motorisation of an active part. While nature has developed a very sophisticated and highly automated three-dimensional molecular assembly process that will never be equaled, lithographic-based microfabrication represents nevertheless a significant evolution narrowing the gap between the complexity of what nature could do compared to traditional fine machine tooling. With microfabrication techniques, devices made of thousands of coupled active electromechanical microparts designed with a micrometer resolution and requiring no further assembly can be batch fabricated in a few steps, something that is simply unconceivable with more traditional fabrication process. As a result, micromachined parts are thus uniquely very well adapted to partially mimic structurally and functionally some particular blocks of tiny animals such as insect or small arthropod legs, since the planar fabrication process permits the realisation of thin flexural active elements of comparable architecture and size. There are however a few limitations coming essentially from the planar nature of photolithography that prevents the realisation of true three-dimensional structures, but to some extent and with a bit of imagination this limit can be circumvented.

1.4 Microrobotic today

The idea of making moving microrobot is not new. Inspired sometimes by nature, engineers have already realized miniaturised flying, rolling, walking and swimming robots. Everything has thus been done already? Definitively not since only structures tethered to power and based on miniaturised wristwatch electromagnetic motors or smart autonomous structures, but capable of generating passive motion only (i.e. following the variation of an external force field such as a magnetic field or vibrations), have been demonstrated. These structures mainly suffer from the very limited travel range achievable, and the lack of controllability or impossibility of being steered.

1.5 Micromachining

1.5.1 The origin and potential of micromachining

Most of the processes used for micromachining derived from the ones developed by the microelectronic industry. This revolution in the way small mechanical parts are machined was initiated when visionary people became aware that not only integrated circuits (IC) but also micromechanical devices could be batch-fabricated with the same resolution. With these new technologies, it becomes possible to merge sensors, actuators and electronics on the same chip so as to realize smart microsystems or micro electromechanical systems (MEMS) that can be mass-produced at low cost. However, process compatibility is not always achievable meaning that for numerous realisations the microsystem is still made of several pieces of silicon, one for the control electronic and one for the sensors and (or) actuators.

1.5.2 Photolithography and structuring

The fabrication of MEMS and ICs is based on photolithography, which allows the transfer of a two-dimensional pattern on a silicon wafer. After a photosensitive resist layer has been spun on top of the layer that is to be structured, a mask representing the pattern to transfer is applied between the wafer and an illumination source. Once the photoresist has been exposed, illuminated or non-illuminated parts can be selectively dissolved, leaving the wafer with a patterned resist layer that can be transferred to the underlying layer through wet or dry etching. Figure 1-1 depicts a photolithography followed by an etching step.

A device is made of a stack of different layers having their own pattern and where subsequent photolithography can be very precisely aligned with the first one even on opposite sides of the wafer.

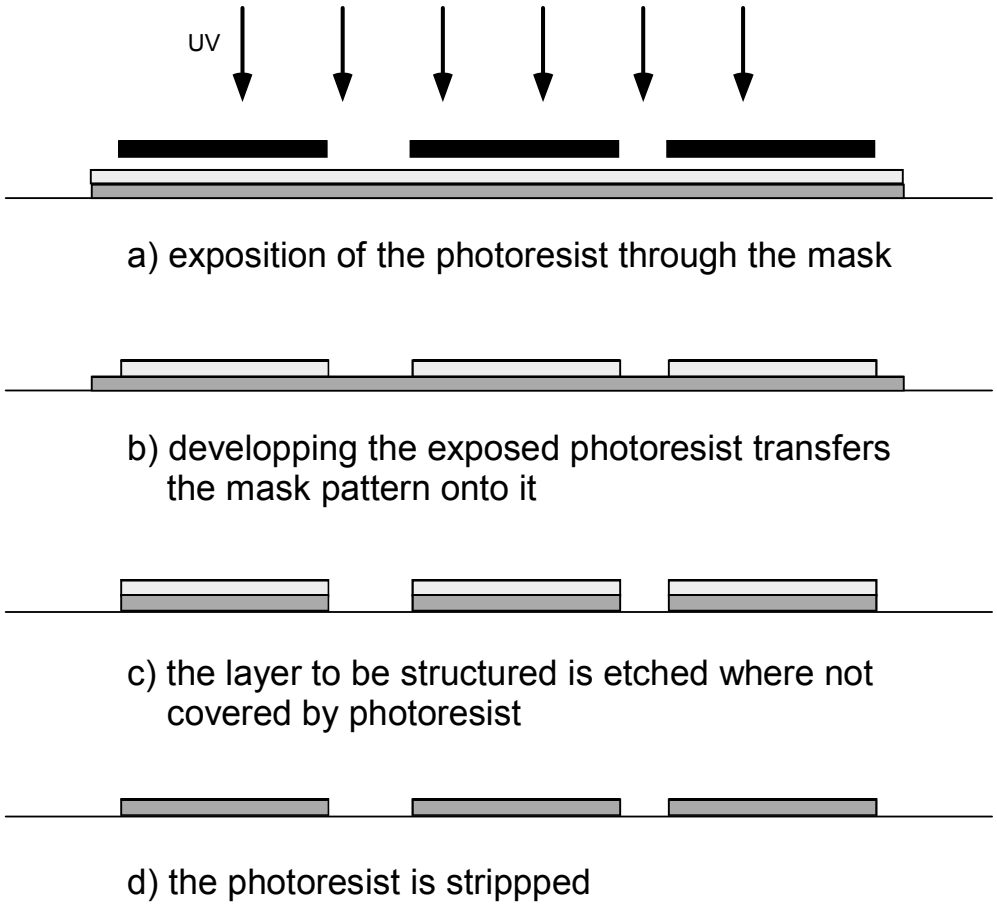


Figure 1-1. Structuration of a thin film: photolithography and etching

1.5.3 Surface micromachining

The surface micromachining denomination gathers all the thin film processes. Film thicknesses range from a few tens of nanometers to a few microns and one can distinguish between structural, sacrificial, insulating, conducting, active and sensing layers. If thin film processes such as the deposition and patterning of oxide, nitride, polysilicon and aluminum layers form the basis of surface micromachining, the introduction of new materials and processes is continuously broadening its field of applications. As a result, very complex planar devices lying within a thickness of only a few microns can be surface micromachined. It is the world of sensors, actuators, micromotors, ...

1.5.4 Bulk micromachining

Bulk micromachining is based on the crystallographic silicon structure that allows specific etchants, such as hydroxide potassium (KOH) to achieve preferential directional etching. The etch rate of these anisotropic etchants depends strongly on crystallographic orientation and allows the formation of truncated pyramidal pit or V-grooves along the <111>

planes. Figure 1-2 shows a cross-section of a silicon wafer after bulk micromachining.

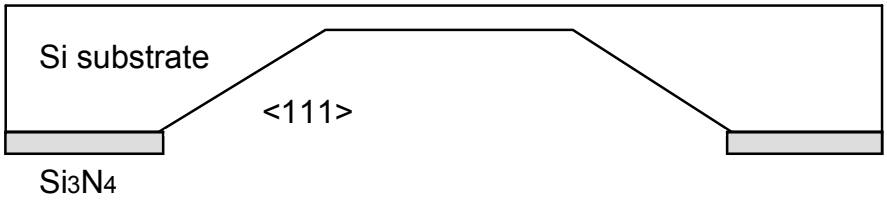


Figure 1-2. Truncated pyramidal pit formed by wet anisotropic etching.

Bulk micromachining can be used for example to define membranes or cantilevers, suspended mass for accelerometer or gyroscope, to etch micro-channels for fluidic application or to remove the silicon substrate where its parasitic capacitance or thermal sinking capability need to be minimized. An advantage of bulk micromachining is that it is compatible with IC technology as a post-processing step.

Very recently, dry anisotropic etching tools that further enhance the potential of bulk micromachining have reached the market. In these systems, anisotropy is not based on crystallographic orientation any more, but on verticality through active passivation of the sidewalls during etching. It becomes thus possible to achieve wafer-through or deep narrow structures of any extruded shape with a resolution of a few tens of microns across a whole wafer. Part of the process developments made in this work deal with deep dry etching and will be further detailed in following sections.

1.5.5 Galvanic forming

Lithographic galvanic forming (LIGA) can be seen as something between bulk and surface micromachining. It consists of lithographically defined micro-molds in PMMA, polyimide or photoresist that can be electroplated with nickel, copper or permalloy for example. Molds thicknesses can vary from a few microns to several hundreds of microns with a very high aspect ratio. In the latter case, X-ray lithography was until recently the only alternative, but materials and processes for conventional UV deep lithography are now being developed. Inductors, magnetic flux concentrators, free standing micromechanical structures can be fabricated above IC for electronic, sensor and actuator applications.

1.5.6 Limitation of micromachining

The proliferation of technological processes developed for micromachining is at the same time an advantage and a drawback. Of

course, it allows the realisation of almost any kind of sensors or actuators. But unlike ICs that realize their functionality and diversity by assembling in different ways a limited number of generic components such as transistors and capacitors that require only one very well optimized technology, each MEMS design requires specific process developments or changes before a functional device can be fabricated. This problem is not so significant for academic institutions, but becomes stringent in a production site. Hopefully, multi project wafers are beginning to appear, forcing more standardized designs with less degrees of freedom. Packaging is another key issue in the successful commercialisation of MEMS. Unlike conventional ICs, sensors and actuators by definition need to interact with their physical environment, thus requiring a more complicated, dedicated packaging that will greatly increase manufacturing and designing costs.

1.6 Goal and outline of the thesis

The aim of this work is to demonstrate the feasibility of an autonomous walking microsystem based on the collective actuation of a micromachined piezoelectric actuator array. Although the array is the key and most innovative component of the microsystem, the design of the ones in charge of the energy transformation and its distribution are critical for achieving autonomy. The transducer that has been chosen for supplying the energy to the system is a high voltage solar cell, which powers the actuators and their associated control electronics. An integrated circuit generates the proper signals to drive the actuators at the desired pace and in the desired direction according to some information transmitted optically. Though it would be conceivable to integrate all these three components on the same substrate, really making a single chip microsystem, the hybrid integration has been preferred at that time.

Besides this introduction chapter, the thesis is divided into five chapters. Chapter 2 deals with the microactuator array design, fabrication and characterisation. Chapter 3 reports on the integrated circuit design and measurements. Chapter 4 presents the design, fabrication and characterisation of the high voltage solar cell. Chapter 5 deals with the microsystem assembly and experiments. Eventually, chapter 6 presents some conclusions and potential applications of the wireless autonomous walking microsystem.

2. A microactuator array suitable for locomotion

2.1 Preliminary

Several groups have been active in the field of microfabricated robotics for self-locomotion applications. Flynn et al. who proposed the 'gnat' robot concept [1] have worked on piezoelectric rotational micromotors for microrobots [2], Yeh et al. have tried building an integrated microrobot based on a complex three-dimensional assembly of polysilicon plates, hinges and micro stepper motors, so as to realize articulated arms with multiple degrees of freedom [3]. In both approaches however, the aim is basically to try to miniaturize or scale down existing six or four-legged robot architecture, rather than exploring new concepts that would better take advantage of the microfabrication specificity.

Since friction is of primary concern in the small domain, conventional architectures based on rotating micromotors gearboxes and wheels should be avoided not only for power efficiency reasons but mostly for wear problems that can quickly render a device inoperable. Conversely, simpler frictionless actuator architectures for motion or force generation and amplification have to be designed based for example on the elastic deformation of active and passive compliant structures. Friction forces should be sought after only for the final mechanical interface where the motion is to be transmitted or coupled to the outside. A step in this direction has been done by Smits, who gave design considerations for a microrobot based on piezoelectric bimorph beams [4].

On the other hand photolithography allows an easy integration of many such simple structures together, favoring an arrayed configuration, where not only a few active parts will make the microrobot, but a whole bunch working cooperatively, taking thus full advantage of the planar fabrication process and the area at disposition.

No description of a microrobot based on a microactuator array could be found in the literature at the beginning of this project, although many people had already been dealing with conveying systems, which are closely related

2.2 Existing microactuator arrays for motion generation

2.2.1 Conveyor based design

In the exploratory field of distributed microactuator arrays, where distributed actuators collectively try to interact with a macroscopic

object, the realisations are still academic, but very impressive. The concept of distributed micro motion systems (DMMS), proposed by Fujita in the early 90th [5,6] has initiated worldwide interest in developing intelligent conveyance systems based on microactuator arrays. In DMMS, arrays of microactuators, microsensors and electronics are to be integrated on the same substrate to provide a flexible smart conveyance system capable of self-reorganisation so as to transport, rotate, align or position an object using the same set of groups of actuators and by partitioning their direction of motion. The research has focused on developing a suitable actuator array and algorithms that could theoretically align a known object unambiguously, regardless of its initial position. Interesting algorithmic work can be found in [7,8]

The realisation of a suitable actuator array proved however quite difficult. The first demonstration of an arrayed conveyor, based on nozzles for air levitation and electrostatic actuators for lateral motion was made by Pister et al. [9]. Konishi and Fujita then realized a system using air for both levitation and lateral actuation by controlling electrostatically the asymmetry of the air flow exiting an array of bi-directional tilted nozzles [10]. A different approach implemented by the same group holds better promises in view of a mobile application. It is based on a ciliary motion system where an array of plates or beams can be raised or lowered in two independent groups producing a net horizontal displacement [11]. The working principle is depicted in Figure 2-1.

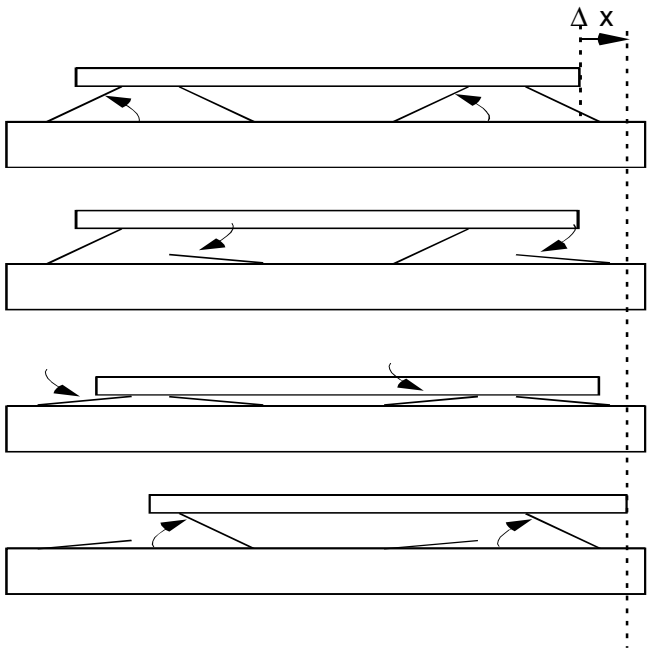


Figure 2-1. Cross-sectional view showing the working principle of a conveying system that mimics ciliary motion. Net horizontal displacement is produced during the last two phases.

It was first demonstrated with thermal bimorph [12], then with electrostatic [13,14] and magnetic actuation [15]. The first one produces high amplitudes of motion (in the hundred-micrometer range) both vertically and laterally at frequencies of up to 10Hz, but at the expense of tremendous power consumption (4mW for a single 500x100x6μm actuator). The two electrostatic realisations based on torsional plates can work at much higher frequencies but their lateral amplitude of motion is limited to a few hundreds of nanometers. The vertical amplitude is given by the initial gap between the two electrodes and is typically about one micron. The microactuator array using an external magnetic field for the actuation of permalloy plates suspended by a cantilever can achieve very large amplitudes of motion and has the advantage and drawback of being completely passive. Since only a global single phase of actuation is possible, motion is induced by the lateral displacement of the object during the lifting phase and its vertical free fall when the external magnetic field is removed.

Most of these realisations could effectively move an object placed on top of the structures along one direction, but characterisation reported in the mentioned papers is very basic and lacks information about stability, reproducibility and controllability.

During the time span of this work, two-dimensional thermal ciliary conveyors, obtained with two interlaced orthogonal conventional 1-D arrays were then demonstrated [16,17] and very recently a reconfigurable thermal ciliary array with on-chip CMOS circuitry [18] very close to the concept of a DMMS.

2.2.2 Self motion based design

While one could think that a microactuator array capable of walking is just a basic ciliary conveyor chip that is flipped upside down, none of the proposed conveyor demonstrated walking ability. Intuitively, the magnetic one should be capable of making lateral jumps since it does not require any wires, but for all the others, the wires are precisely the source of the problem. The reason is that in all these designs, the moving parts and the electrical connections are surface micromachined from the topside and consequently the mechanical and electrical interfaces lie on the same wafer side. Thus, unless the released structures that form the actuators can be raised quite away from the substrate, wires in the bonding area will interfere with the mechanical interface and prevent walking. Ebefors et al. solved this problem and demonstrated the first walking microrobot based on Fujita's ciliary motion system in 1999 [19]. In their design, electrical and mechanical interfaces are separated by

rotating long silicon plates way out of the substrate through the curing of a polyimide joint that can be later thermally actuated. While elegant, their solution has several limitations, such as the huge power consumption (about 1W for a 2 grams payload), the wires that limit both travel range and further miniaturisation and the relatively large actuator size that restrict the number of legs between six and eight for a reasonably sized bug.

2.3 Design and modeling

2.3.1 Requirement for an actuator array suitable for walking and autonomy

Since wires are forbidden if autonomy and miniaturisation are at aim, energy has to be either carried onboard or taken from the environment using transducers. The control of the microrobot faces the same problems, meaning that a wireless remote control capability should be combined with an embedded circuitry that generates the appropriate walking pattern and drives the actuators. Altogether, this means that a microsystem consisting of several chips is required, not just an array of actuators.

Following these simple considerations, the main requirements for an actuator array suitable for walking and autonomy can be stated as follow:

-**Ultra low power consumption** compatible with onboard resources or deliverable transducer power.

-**Well separated electrical and mechanical interfaces** so as to enable multiple chip assembly and interfacing without disturbing the mechanical interactions.

While it would be possible to design an autonomous microrobot meeting these two requirements based on another implementation of the ciliary motion system, it is more interesting to investigate slightly more complicated ways of producing a walking pattern to evaluate whether additional benefits can be obtained.

2.3.2 Gait based on the elliptical motion of a leg tip

In the ciliary motion system, the actuators have only a single degree of freedom (DOF) and the gait is produced by an alternation of nearly orthogonal oblique strokes in quadrature. The resulting lateral stroke defines the horizontal distance the object or array can cover in a single step while the vertical one how high the actuators can raise their legs and thus have the ability to walk over rugged surfaces. From a potential energy and speed point of view, this gait is quite inefficient since the

body has to follow the vertical height variation of the actuators. In nature, the legs of walking animals rather describe some kind of laterally elongated elliptical motions, which are more efficient in terms of potential energy and speed since the heavy body can be maintained at a constant height and the lighter legs cycled much faster. Two different structures capable of producing an in-plane elliptical motion have already been proposed: one in the design considerations for a microrobot given in [4] and the other in [20] for a micro conveyor application but where no performances were reported.

In order to produce an elliptical motion, a structure needs to have at least two active DOF that can be activated in quadrature, such as a swinging and a lifting capability for example. If the structure is given an additional swinging DOF, it can generate an elliptical motion in any direction and thus be used more efficiently, improving the array lifting capability -recall that in a 2-D ciliary array, only a 1-D array is used at any time. When using an elliptical gait to produce motion, at least two phases are needed. During one phase, one or a group of actuators performs its step while the other one gets back to its initial position without being in contact with the ground. During the other phase, the roles are swapped leading thus to two groups of actuators working in alternation or phase opposition as depicted in Figure 2-2.

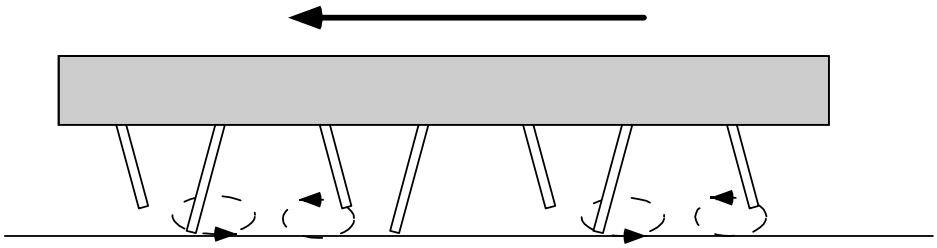


Figure 2-2. Illustration of a two phases elliptical gait.

Another very interesting unique feature made possible with a multiple DOF structure is its multi-dimensional fine positioning capability within the extreme positions that can be reached in a step. It entails new applications where not only open-loop long-range motion should be achieved but also were precise, possibly closed-loop positioning is required.

2.3.3 How to choose a principle of actuation

The choice of an actuation principle should be performed at a very early stage of the conception of a MEMS device since it radically influences its structure and the associated fabrication technology. For this application, power consumption is one of the main criterions. Another

one stems from the necessity of generating 3-DOF motions with a compact, reliable and rather simple structure since many actuators will be connected together. In the following, a review of several actuation principles and the type of motion they can generate is presented so as to help identify the most appropriate.

A wide diversity of actuation principles have been used for the realisations of MEMS actuators. By far the most popular, electrostatic actuation has been studied extensively and can generate a lot of different motions. Comb structures are very popular for large lateral displacement [21,22] and have also been reported for limited vertical motion [23]. The variable gap electrostatic actuators, based on parallel plate capacitors, also generate a force quadratic with respect to the applied voltage and can be found in torsional tiltable plates [24], in limited vertical [25] or lateral stroke actuators [26] and in lateral [27] and out-of-plane bending structures [28]. Rotary and linear stepper electrostatic micromotors were also reported [29,3]. Another concept called the scratch drive actuator (SDA) is based on the vertical parallel plate variable capacitor but where one end of the plate is extended at right angle towards the substrate [30]. The resulting structures crawl on the substrate and can be used in arrayed configurations in rotating or linear motors where very large coupling forces are required. Very dense arrays of SDAs fabricated on a polysilicon sheet that can be released from the substrate have been demonstrated recently as a motorisation for miniature bearing shaft joints [31]. Electrostatic actuation usually requires very high voltages, from *30V* up to a few *100V*, produces tiny forces (except for the last two examples) and is very sensitive to dust, moisture and sticking problems. It is however a great actuation principle for optoelectromechanical devices since interacting with light only requires the ability to produce motion in order to modulate the phase and/or amplitude along an optical path as in [25,32]. Another principle of actuation, very compatible with surface micromachining is based on bimorph structures, where a longitudinal stress can be actively induced in one or two of the main layers composing the stack and make it bend. Stress can for example be induced thermally [12], piezoelectrically [33], magnetically [34] and through phase change in shape memory alloy [35]. The resulting motion is in most cases vertical and can be applied to cantilevers for large displacement or membranes for rotary or linear micromotors [2]. Although integrated magnetic micromotors were reported [36], electromagnetic actuation is not favored by downscaling since resistive losses become overwhelming in microcoils. On the other hand, integrated magnets [37] or permalloy thin plates [38] can be actuated with a global

external magnetic field and find interesting applications in passive or global actuation systems.

One remark worth noting is that multiple DOF actuators are not common at all and can often not obviously be designed from existing uniaxial actuators without requiring extensive process changes. One example can be found in [39] where a piezoelectric beam for a scanning tunneling microscope (STM) has 3-DOF or in [40] where an in-plane comb driven STM X-Y translational stage has 2-DOF. Multiple DOF actuators with lateral and vertical motion capability seem easier to design with bimorph actuation, among which piezoelectricity appears as the best candidate for the envisioned application for different reasons such as robustness, power consumption, voltage level and actuation speed to mention a few.

2.3.4 Thin film piezoelectric materials

There are two piezoelectric materials that have been widely used in micromachining as thin films for actuation: lead zirconate titanate (PZT) and zinc oxide (ZnO). PZT, which is the dominant piezoelectric material for bulk applications, exhibits in thin film form a high transverse piezoelectric coefficient, a rather high breakdown voltage and can be spin coated in sol-gel form or sputtered. However, to prevent PZT from diffusing into silicon and favor a particular phase of crystallisation, a titanium platinum or tantalum platinum layer should be deposited in between, complicating the processing if it has to be patterned. Besides its exotic material composition, which does not make it desirable in a clean room, PZT is ferroelectric and thus needs to be poled prior or while being used. Frequent pinholes do not make it a very robust and reliable material at the time being. Though zinc has not the favor of clean room process engineers either, ZnO is from a processing point of view a rather good candidate since it does not require any antidiffusion layer and can be patterned with almost any acid solution. It offers unfortunately quite a moderate transverse piezoelectric coefficient and breakdown field. Among other drawbacks, the two most severe are the lack of deposition reproducibility and the poor insulating capability of ZnO that result in a lower frequency limit beneath which its use becomes challenging if not simply impossible.

Is there any alternative to these two problematic materials for MEMS applications? This question has found very recently an affirmative answer. The wonder material might well be aluminum nitride, which additionally is by far the best candidate from an IC post-processing compatibility point of view. Though aluminum nitride has long ago been considered as a good potential candidate for thin film piezoelectric

applications, its deposition was until recently inevitably yielding highly stressed layer that would have proven difficult to integrate into microsystems. Dubois was the first to study comprehensively the different parameters involved in the deposition of aluminum nitride thin film on a metallic bottom electrode [41], the prerequisite for subsequent successful integration of more complex devices. He could demonstrate the relation between deposition conditions and the influence of the material and crystalline structure of the bottom electrode on the piezoelectric and mechanical properties of the film. From a coupling point of view, AlN is slightly less attractive than ZnO, but its high breakdown field allows for a much greater stress to be induced in the piezoelectric layer. Its excellent dielectric properties also enable low frequencies applications and thus make it the perfect material for the mobile robot application. From a processing point of view, AlN is chemically very stable but can nevertheless be patterned in hot phosphoric acid. The real only drawback currently associated with its processing is the need for a platinum bottom electrode that has to be patterned physically.

Table 2-1 summarizes the thin film piezo and electrical properties of interest for the three materials with two different compositions for PZT having optimum transverse characteristics.

		ZnO	AlN	$PZT_{(40,60)}$	$PZT_{(45,55)}$
e31,f	[C/m²]	1	1	6.7	8.3
Ebd	[kV/cm]	100	1000	250	250
ε33		11	10	680	1100
k²	[%]	5.2	3.4	7.5	7.1
tanδ		NA	0.002	0.024	0.03

Table 2-1. Reported and calculated transverse piezoelectric coefficient, breakdown field, relative permittivity, transverse coupling coefficient and dielectric loss for thin film piezoelectric materials.

e31,f is the transverse piezoelectric coefficient relating the externally applied vertical electric field to the stress induced in a film clamped in the two horizontal directions. Since the method for measuring *e31,f* has only been proposed very recently [42] and not yet been applied to ZnO, the indicated coefficient corresponds to 80% of its calculated bulk value and is a reasonable estimate of what is attainable in thin film technology.

Ebd is the maximum voltage that can be applied across the film. If *e31,f* remains constant at high field, the product of the two latter parameters is the maximum stress that can be induced piezoelectrically. The displacement and moment -and thus the external force against which the beam can act- resulting from the actuation of the film are both proportional to *e31,f* times the applied electric field. *e31,f* gives thus also an indication about the voltage that will be required in the application. Assuming same film thicknesses, PZT would therefore be much more attractive for low voltage applications, since a stress about 7-8 times as big can be induced in the film compared to ZnO and AlN for the same actuation voltage. The relative permittivity of the thin film, ε33 is directly proportional to the electrical energy that is stored in the film. The transverse coupling coefficient k^2 is equivalent to the bending electro-mechanical energy conversion efficiency of an optimum piezoelectric bimorph. Impaired by its large dielectric constant, PZT in thin film form -unlike its bulk counterpart- does not overwhelmingly dominate the two other materials when considering efficiency only. The last parameter that is reported in the table accounts for the dielectric losses. As a direct consequence of the residual conductivity of the ZnO thin films, which can easily vary by seven orders of magnitude, a realistic value for the dielectric loss can not be given. The very low loss of AlN entails very interesting low power applications for devices working at mechanical resonance or as sensors.

2.3.5 Piezoelectric beam modeling

There are basically two types of piezoelectric bimorph beams, the symmetrical one, consisting of a stack of two piezoelectric thin films sandwiched between three electrodes, and the unsymmetrical beam, where only one piezoelectric layer and its two electrodes are deposited on top of a structural layer. In the symmetrical configuration, the two outer electrodes can be driven with the same signal resulting in an antiparallel electric field distribution across the piezoelectric thin film. Consequently, the longitudinal stresses induced in the two active layers will be of opposite sign leading to the build-up of a pure bending moment. In the unsymmetrical configuration, a structural layer replaces the second piezoelectric thin film so that a bending moment can still be induced in the beam upon excitation of the active material. The unsymmetrical configuration has been adopted in this work because it is much simpler to fabricate, although less attractive in terms of useful electromechanical coupling efficiency since a force is also induced in the longitudinal beam direction. The resulting longitudinal strain is however negligible and does not affect the beam behaviour. This configuration

raises nevertheless another problem: the unsymmetrical material and stress distribution across the composite beam leads to a fabrication induced static beam bending which is difficult to control precisely.

In the following calculations based on small displacement linear theory, the modelling of an unsymmetrical piezoelectric beam depicted in Figure 2-3 is presented.

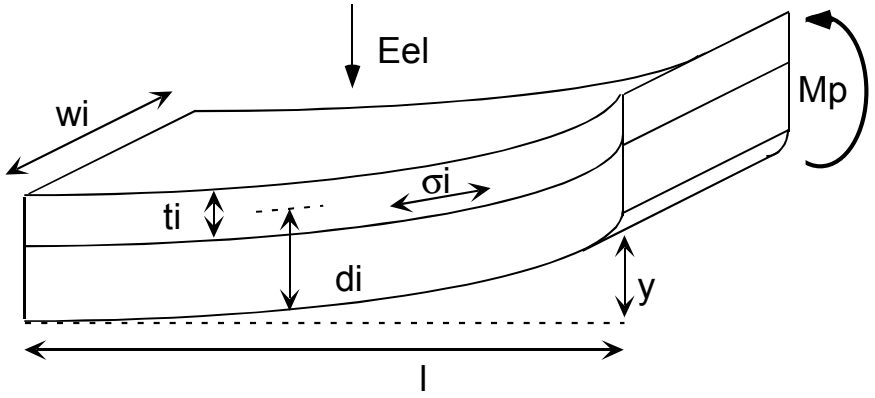


Figure 2-3. Drawing of a piezoelectric beam to help identify important parameters.

The residual stresses, σi present in the different materials forming the composite beam yield a bending moment equal to

$$Mb = \sum_i w_i \cdot t_i \cdot \sigma_i \cdot (d_i - ym), \tag{2-1}$$

with

$$ym = \frac{\sum_i d_i \cdot t_i \cdot c_i}{\sum_i t_i \cdot c_i}. \tag{2-2}$$

where for material *i, ci* is the Young modulus, *wi, ti, di* are the width, thickness and distance to the beam edge from the middle of layer *i,* and *ym* is the neutral axis.

An electric field *Eel* applied across the thin film piezoelectric material changes its state of stress yielding a bending moment equal to

$$Mp = w_p \cdot t_p \cdot e_{31,f} \cdot Eel \cdot (d_p - ym), \tag{2-3}$$

where *e31,f* is the coefficient relating the applied vertical electric field to the longitudinal stress induced in the piezoelectric film. The resulting deflection at the tip of a beam of length *l* as a function of both internal and piezoelectrically induced stresses is

$$y = \frac{(Mb + Mp) \cdot l^2}{2 \cdot EI}, \tag{2-4}$$

with *EI* the equivalent stiffness of the composite beam given by

$$EI = \sum_i c_i \cdot w_i \cdot \left[\frac{t_i^3}{12} + t_i \cdot (d_i - ym)^2 \right]. \tag{2-5}$$

At that point, it is interesting to note that the deflection does not depend on the width of the beam, but on the square of its length and if all layers are scaled, the inverse of its thickness.

The maximum stress that can be induced electrically in the piezoelectric film is limited by the material breakdown field and is typically a few tens of *MPa*. As compared to the residual stress of the different deposited material, which typically ranges between hundreds of *MPa* to one *GPa*, one can see that a tight stress control and choice of material combination is necessary to position the beam ideally, so as to get slightly protruding legs.

The bending mechanical energy stored in the deformed beam due to the piezoelectric effect can be written as

$$Wb = \frac{1}{2} \cdot \frac{Mp^2 \cdot l}{EI}, \tag{2-6}$$

while the electrical energy is the one that is stored in the dielectric capacitance of the film and is approximately

$$Wel = \frac{1}{2} \cdot w_p \cdot t_p \cdot l \cdot \varepsilon_{33} \cdot \varepsilon_0 \cdot Eel^2 . \tag{2-7}$$

The ratio of the two latter equations gives the bending electromechanical conversion efficiency

$$\eta = \frac{e_{31,f}^2}{\varepsilon_{33} \cdot \varepsilon_0 \cdot c_p} \cdot \frac{w_p \cdot t_p \cdot (d_p - ym)^2}{\sum_i \frac{c_i}{c_p} \cdot w_i \cdot \left[\frac{t_i^3}{12} + t_i \cdot (d_i - ym)^2 \right]}, \tag{2-8}$$

where the first term is the transverse coupling coefficient k^2 characterising the piezoelectric material (typical value of a few %, see Table 2-1) and the second a geometrical factor taking into account the composite structure of the beam. Depending on the relative mechanical properties of the structural and piezoelectric materials, an optimal thickness ratio can be calculated with this equation.

The effects of the absolute geometrical dimension are now discussed based on the above equations. Scaling up the thickness of all the layers forming the bimorph results in a linear increase of the bending energy. Since the beam tip deflection is inversely proportional to this scaling

factor, the force that can be exerted on the bimorph to compensate the piezo-induced deflection increases quadratically. Beside the technological factors limiting the thickness of the composite beam, the voltage and the energy that should be applied to generate the same electric field increase, becoming problematic in a wireless application, since the voltage has to be generated and switched onboard and the energy is limited. Scaling down the two lateral dimensions of the beams results in a quadratic bending energy decrease, which is also affecting the beam deflection in the same way, meaning that the external force that cancels a piezo-induced displacement remains constant. Now consider a given area and a fixed thickness so that the overall bending energy remains constant. Lateral downscaling means that the number of beams occupying this area increases quadratically. The overall force that compensates for the piezo-induced deflection follows the same increase rate, while the deflection decreases accordingly. There is thus a quadratic adaptation between force and deflection as the lateral dimensions are scaled. However, the resonance frequency of one such beam is as shown just below, inversely proportional to the square of its length, leading to a constant frequency deflection product, directly responsible for the leg tip speed. In that case, the consumed power increases accordingly, but both high-force and high-speed devices can be achieved simultaneously.

The low quasi-static electromechanical conversion efficiency of a piezoelectric bending bimorph given by equation (2-8) indicates that the electrical behavior of the actuator is overwhelmingly dominated by the capacitor of the piezoelectric thin film. At mechanical resonance however, the motional part of the structure, which can be modeled by an equivalent *RLC* circuit placed in parallel with the dielectric capacitance of the film *Co*, might become important, depending on the resonator quality factor. The ratio of motional to static capacitance is equivalent to the quasi-static electromechanical conversion efficiency derived above. The equivalent inductance is related to the resonator mass and its energy to the kinetic one. Knowing *C* and the beam resonance pulsation ωo given by

$$\omega_o = \frac{1.8751^2}{l^2} \cdot \sqrt{\frac{EI}{\rho A}}, \tag{2-9}$$

where ρA is the weight per unit length of the beam cross-section, the equivalent inductance can be derived from

$$\omega_o = \frac{1}{\sqrt{L \cdot C}}. \tag{2-10}$$

The energy dissipated in the resistor R stands for the mechanical losses of the resonator and can be related to the quality factor Q of the beam by

$$Q = \frac{1}{\omega_o \cdot R \cdot C}. \tag{2-11}$$

The losses are difficult to estimate analytically, since they include the energy lost at the beam boundary due to non-perfect clamping. For the beam considered in these calculations or the actuator geometry proposed in this work, this mechanism is the main source of losses and is responsible for the low Q value of the resonator. The electromechanical conversion efficiency at resonance can be written as

$$\eta_o = \frac{Q^2 \cdot \eta_{qs}}{1 + Q^2 \cdot \eta_{qs}}, \tag{2-12}$$

where η_{qs} is the quasi-static efficiency obtained from (2-8). One can see that even with low Q values, the dynamic efficiency increases very rapidly. Another point worth mentioning is that the beam deformation and the force it can exert at resonance are both multiplied by the resonator Q value. If the beam performs some external work during part of its trajectory, a global resonance regime can still be established and the energy that is coupled to the outside can simply be taken into account in the losses represented by R that takes thus different values during a cycle. It would however be quite difficult to detect electrically the mechanical resonance of the beam, since at such low Q value, the admittance of the beam does not change significantly.

2.3.6 Description of the individual actuator

The actuator structure invented in this work has all the features required for an autonomous microrobot. It can generate elliptical motions with relatively high vertical and large lateral amplitudes with two or more beams, which are coupled together to form a tiltable plate to which a pillar acting as a mechanical lever is attached. Since the pillar extends across the whole wafer thickness, it also provides a separation of the microactuator interfaces. The topside of the array is then free for stacking chips, power supply or performing any fixed electrical interface, while the bottom one is left for the mechanical interactions to take place.

Figure 2-4 shows a schematic of such a 2-DOF actuator that can easily be analytically analised (see §2.3.5) and is presented here for this purpose. It is made of two piezoelectric bimorph beams clamped at one of their end and coupled to a central plate holding a pillar by two torsional hinges at their other extremity.

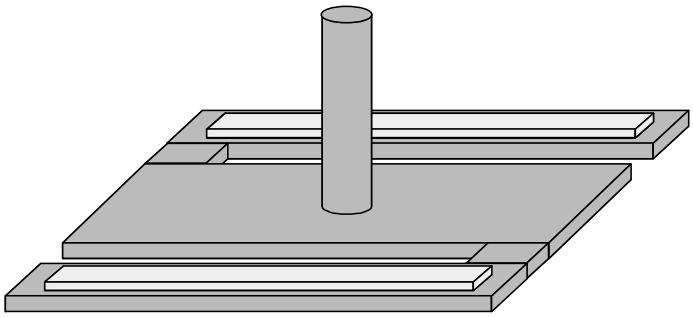


Figure 2-4. A simple bimorph actuator with two active degrees of freedom capable of generating an elliptical motion in one direction.

If a cantilever is considered alone, then, its tip can be moved upward or downward when an electric field is applied across the piezoelectric thin film as derived later in §2.3.5. If the hinges stiffness is not to high, most of this motion can be transmitted to the central plate and the pillar. If two equal harmonic voltages are applied to the two bimorphs, then the pillar tip can also be moved upward and downward. When the voltages are opposite, the plate can be tilted to the left or to the right, meaning that the pillar tip is given a swinging motion. If the voltages are in quadrature, then the pillar tip effectively describe an elliptical like motion. Two neighboring actuators just need to be excited with half a cycle phase lag to produce the complementary elliptical motions.

The three active degrees of freedom actuator is based on the same principle, but requires three independent beams coupled in a triangular configuration as depicted in Figure 2-5.

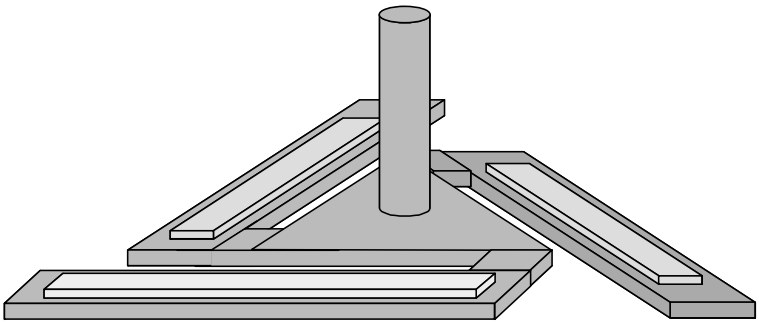


Figure 2-5. A bimorph actuator with three active degrees of freedom capable of generating an elliptical motion in any directions.

The pillar tip can here reach any point within an ellipsoid, but if the excitatory signals are restrained to the four mentioned above (in quadrature and complementary), then the actuator array could be moved in six directions, each separated by 60°. For a given direction, two beams

need to be moved together, while the other one in quadrature, as in the 2-DOF actuator. This configuration is very efficient, since it uses every beam regardless of the direction of motion.

2.3.7 Analytical modeling of the 2-DOF actuator

The behavior of the 2-DOF actuator proposed in the previous paragraph can be analytically modeled. It has been shown in §2.3.5 that the deformation of a beam due to a piezo-induced stress is equivalent to the deformation produced by a uniform moment. In order to calculate the deformation of the complete structure, the imaginary split method can be used. One can simply imagine that the central plate is split in two at half its length, calculate the deformation of one side due to internal and external loads and apply opposite external forces and moments so as to restore the continuity of the material (same deflection and slope). Figure 2-6 shows a drawing of a split 2-DOF actuator.

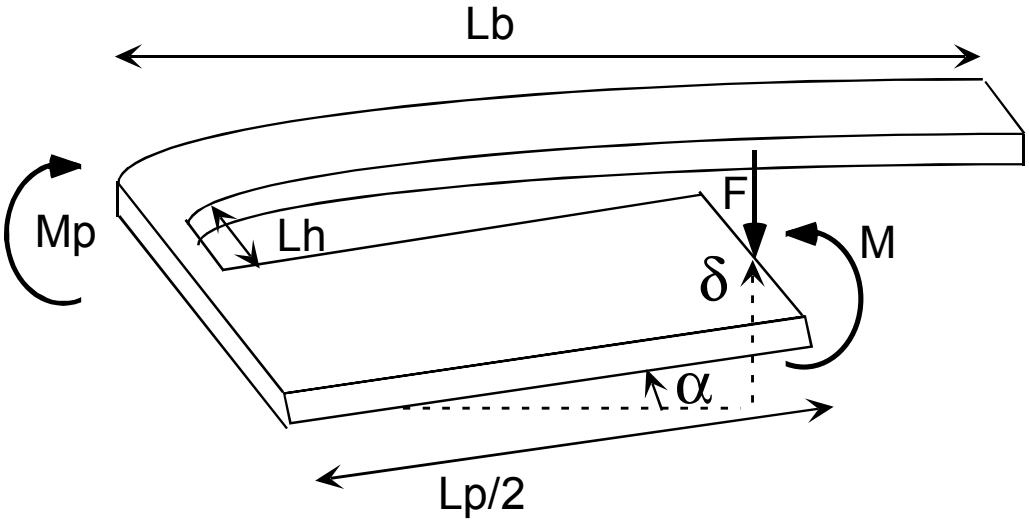


Figure 2-6. Schematic of a split 2-DOF actuator with its geometrical parameters, internal-external loads, slope and deflection at imaginary split plane.

In the following we assume small deformation linear theory and thus neglect the geometrical stiffening induced by large deformations.

The slope α and the deflection δ of the imaginary half structure due to a piezoelectric moment is at half the plate length

$$\alpha = \frac{M_p \cdot w \cdot L_b}{EI_b}, \tag{2-13}$$

$$\delta = \frac{M_p \cdot w \cdot L_b \cdot \left(L_b - L_p\right)}{2 \cdot EI_b}, \tag{2-14}$$

where *Mp* is the piezoelectric moment per unit width, *w* and *Lb* the beam width and length, *Lp* the plate length and *EIb* the beam bending stiffness.

When both bimorph are excited by the same voltage and curl upward, only a moment is needed to restore material continuity *(α=0)*. This moment acts on the central plate, the torsional hinge and the piezoelectric beam. By summing all the individual deformations due to this moment and subtracting it from (2-14), one gets the deflection of the real system. If we assume that the central plate stiffness is much higher than that of the beam and the hinge, the response of the actuator to a uniform piezoelectric excitation, which we define as the transversal actuation compliance of the actuator is then

$$C_{tran} = \frac{\delta}{M_p} = \frac{\dfrac{L_b^2 \cdot L_h \cdot w}{2 \cdot EI_b \cdot KG_h}}{\dfrac{L_h}{KG_h} + \dfrac{L_b}{EI_b}}, \tag{2-15}$$

where *KGh* is the torsional stiffness of the hinge, *Lh* its length.

If the two bimorph are excited with opposite voltages, opposite forces will cancel the deflection of the central point *(δ=0)*. The response of the actuator to an antisymmetric piezoelectric excitation, which we define as the angular actuation compliance of the actuator can then be written

$$C_{ang} = \frac{\alpha}{M_p} = \frac{\dfrac{L_b^4 \cdot w}{12 \cdot EI_b^2} + \dfrac{L_b^2 \cdot L_p \cdot L_h \cdot w}{4 \cdot KG_h \cdot EI_b}}{\dfrac{L_b^3}{3 \cdot EI_b} - \dfrac{L_b^2 \cdot L_p}{2 \cdot EI_b} + \dfrac{L_p^2 \cdot L_b}{4 \cdot EI_b} + \dfrac{L_p^2 \cdot L_h}{4 \cdot KG_h}}. \tag{2-16}$$

The computation of the transversal and angular spring constants of the actuator submitted to forces and moment representing external loads yields

$$K_{tran} = \frac{F_{ext}}{\delta} = 2 \cdot \frac{\dfrac{L_h}{KG_h} + \dfrac{L_b}{EI_b}}{\dfrac{L_b^4}{12 \cdot EI_b^2} + \dfrac{L_b^3 \cdot L_h}{3 \cdot KG_h \cdot EI_b}}, \tag{2-17}$$

$$K_{ang} = \frac{M_{ext}}{\alpha} = 2 \cdot \frac{\dfrac{L_b^3}{3 \cdot EI_b} - \dfrac{L_b^2 \cdot L_p}{2 \cdot EI_b} + \dfrac{L_p^2 \cdot L_b}{4 \cdot EI_b} + \dfrac{L_p^2 \cdot L_h}{4 \cdot KG_h}}{\dfrac{L_b^4}{12 \cdot EI_b^2} + \dfrac{L_b^3 \cdot L_h}{3 \cdot KG_h \cdot EI_b}}. \tag{2-18}$$

With ideal hinges (KG=0), the compliance and stiffness of the actuator can be rewritten

$$C_{tran} = \frac{L_b^2 \cdot w}{2 \cdot EI_b}, \qquad C_{ang} = \frac{L_b^2 \cdot w}{L_p \cdot EI_b}, \tag{2-19}$$

$$K_{tran} = \frac{6 \cdot EI_b}{L_b^3}, \qquad K_{ang} = \frac{3}{2} \cdot \frac{L_p^2 \cdot EI_b}{L_b^3}. \tag{2-20}$$

The deformation of the structure due to piezoelectric excitation is thus equivalent to the deformation of the beams considered alone with a central plate joining their two extremities. The transversal stiffness of the structure is evidently the sum of the beams ones while the angular one is equivalent to that of a single beam *Kb,* times *Lp²/2*. One can rewrite this equation as

$$K_{ang} = \frac{M_{ext}}{\alpha} = K_b \cdot \frac{L_p^2}{2} = \frac{F_b \cdot L_p}{\delta_b \cdot \frac{2}{L_p}}, \tag{2-21}$$

to prove that the beams deform so that internal opposite reaction forces, *Fb* balance the external moment. Figure 2-7 shows the deformation of an ideal 2-DOF structure due to external loads and how they are balanced internally.

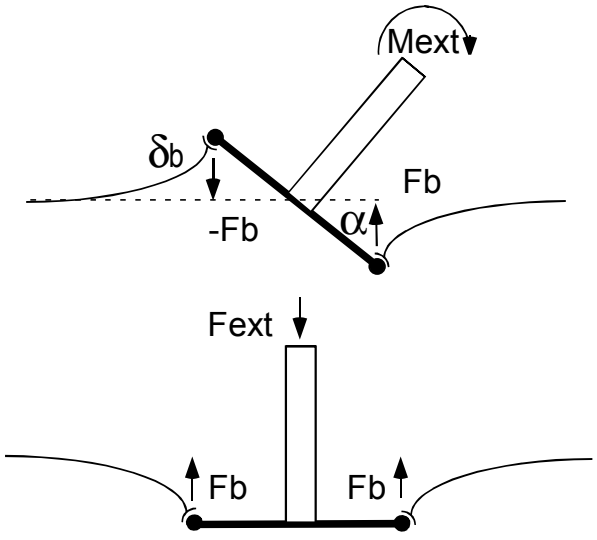


Figure 2-7. Illustration showing the deformation of an ideal 2-DOF structure due to external loads and how they are balanced internally.

During their operation, the legs will have to work against very similar external loads: the weight of the system including an eventual payload and lateral friction forces generated at the leg ground interface that turn into a bending moment in the bimorph plane. Consequently, the beams

have to work against forces only. It has been shown in [43] that the best shape for such piezoelectric beams is triangular. By comparing a beam of constant width with a triangular one of same length and same surface (thus twice as large at its base) it is easy to show that the external force which cancels the piezoelectric induced displacement –identical in both cases- is 33% greater for the tapered beam. This gain in the energy that can be externally coupled is a consequence of the adequation between excitation and loading curves which are both quadratic in the latter case, while the deformation of a beam of constant width due to an external force is of order three.

Normalising (2-15) to (2-18) with their respective ideal hinge compliance and stiffness, one gets

$$C_{tran}^{rel} = \frac{L_h \cdot EI_b}{L_h \cdot EI_b + L_b \cdot KG_h}, \tag{2-22}$$

$$C_{ang}^{rel} = \frac{3 \cdot L_c^2 \cdot L_h \cdot EI_b + L_p \cdot L_b^2 \cdot KG_h}{3 \cdot L_p^2 \cdot L_h \cdot EI_b + \left(4 \cdot L_b^3 - 6 \cdot L_b^2 \cdot L_p + 3 \cdot L_p^2 \cdot L_b\right) \cdot KG_h}, \tag{2-23}$$

$$K_{tran}^{rel} = \frac{4 \cdot L_h \cdot EI_b + 4 \cdot L_b \cdot KG_h}{4 \cdot L_h \cdot EI_b + L_b \cdot KG_h}, \tag{2-24}$$

$$K_{ang}^{rel} = \frac{4}{3} \cdot \frac{3 \cdot L_p^2 \cdot L_h \cdot EI_b + \left(4 \cdot L_b^3 - 6 \cdot L_b^2 \cdot L_p + 3 \cdot L_p^2 \cdot L_b\right) \cdot KG_h}{4 \cdot L_p^2 \cdot L_h \cdot EI_b + L_b \cdot L_p^2 \cdot KG_h}. \tag{2-25}$$

The transversal response of the actuator to a piezoelectric excitation becomes hyperbolic with respect to the hinge stiffness. The angular response is not affected so strongly by the hinge stiffening at least for some geometry. The transversal stiffness can only be made four times bigger if the hinges stiffen and the system is then equivalent to a beam twice as long, but fixed at both ends.

The first requirement for a walking actuator is its ability to produce motion. *Cang* will directly influence the unit step of the mobile microsystem, while *Ctrans* its ability to walk over rugged surface. On the other hand, actuator stiffness or their ability to sustain external forces is of great concern, if the system wants to carry a payload or be capable of good accelerations. The actuation compliance stiffness product seems thus to be a good parameter to seek to maximize. It yields

$$C_{tran} \cdot K_{tran} = \frac{w}{L_b} \cdot \frac{12 \cdot L_h \cdot EI_b}{4 \cdot L_h \cdot EI_b + L_b \cdot KG_h}, \tag{2-26}$$

$$C_{ang} \cdot K_{ang} = \frac{w}{L_b} \cdot \frac{6 \cdot L_p \cdot L_h \cdot EI_b + 2 \cdot L_b^2 \cdot KG_h}{4 \cdot L_h \cdot EI_b + L_b \cdot KG_h}. \quad (2\text{-}27)$$

The transverse compliance stiffness product is again hyperbolic, meaning that the hinge stiffness really has to be minimized. The width of the beam on the other hand increases the stiffness while keeping the compliance unchanged. A trade-off has to be made for the beam length, since achieving large amplitudes of motion is as much important.

2.3.8 FEM simulation of the 3-DOF actuator

A similar analytical tool has been implemented for the 3-DOF actuator for a rapid evaluation of the effects of several parameters. Retained structures have then been modeled with ANSYS ™, a finite element simulation tool that features coupled piezoelectric-mechanical analysis. Figure 2-8 shows the deformation of the structure when the same voltage is applied to the three beams.

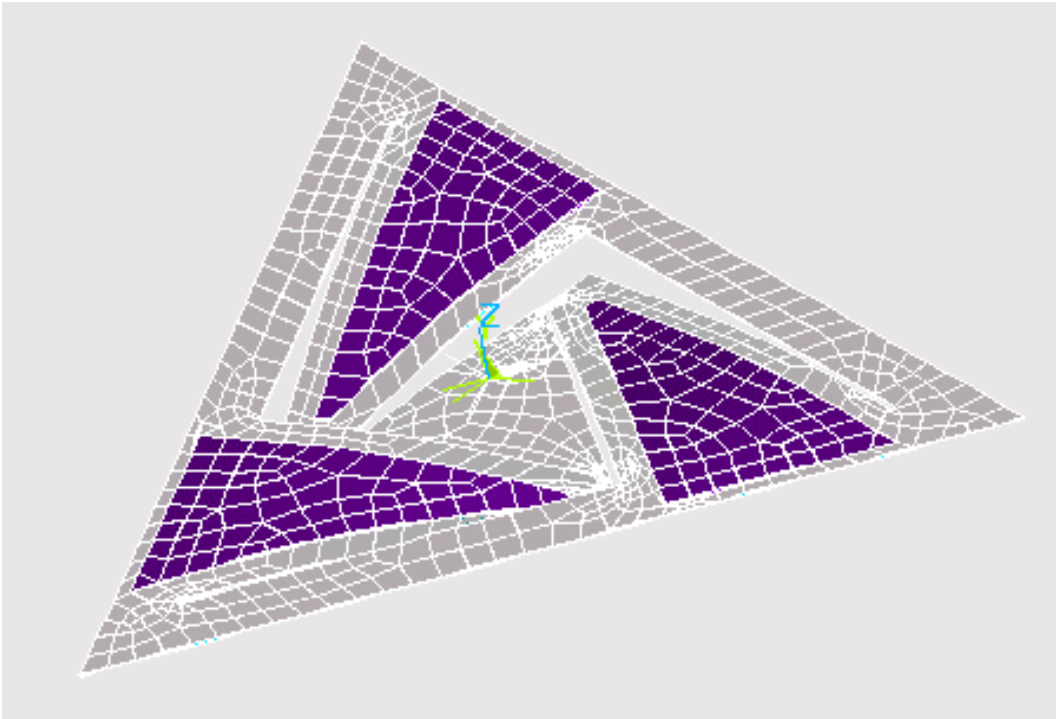


Figure 2-8. Simulated strain of the piezoelectric/structural layer induced by a uniform voltage applied to the piezoelectric material.

Comparative simulation of a single beam shows that the motion of the coupled structure amounts to 89% and 80% of that of a single beam for the vertical and tilting mode respectively indicating that the formulations developed in §2.3.5 are fairly accurate for a quick estimate of the quasi

static device performances. Important parameters such as initial deflection due to internal stress, stiffness, response to piezoelectric excitation, resonance frequency and stress distribution can be estimated and help find an optimal geometry.

Another very important effect that can be quantified with ANSYS is the geometric stiffening of the structure induced by large deformations. Figure 2-9 shows the evolution of the deformation of the central plate when the residual stress of the piezoelectric layer is increased in comparison with linear deformation theory. A direct consequence for our application is a reduction in the amplitudes of motion achievable, since the actuation compliance is proportional to the slope of the curve shown in Figure 2-9. A curve fitting very well the one of Figure 2-9 has been obtained when the deformation of the structure is the consequence of a transversal force. In that case, convergence is faster and deformations of up to 40µm, corresponding to half that of the linear case were simulated. This gives an idea about the evolution of the stiffening for larger residual stress. Since this structural stiffening is extremely sensitive to the geometry of the actuator, it is difficult to predict the behaviour of laterally scaled or slightly different designs.

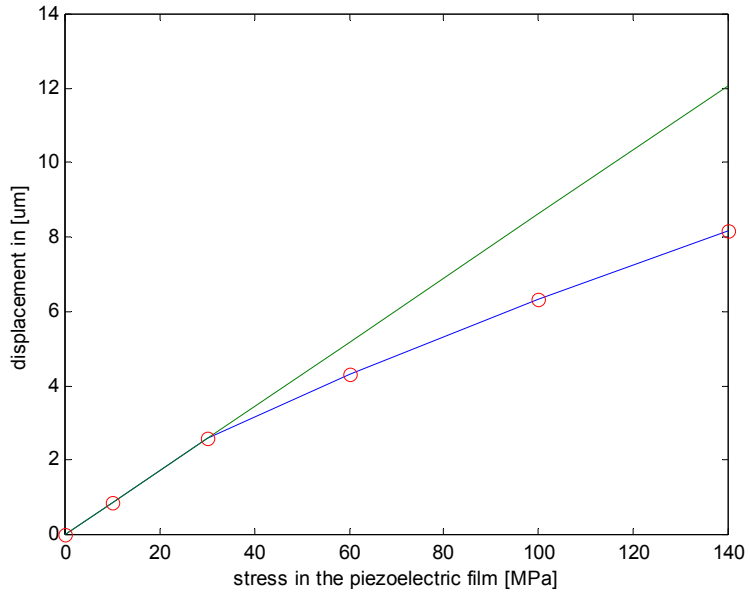


Figure 2-9. Illustration of the structural stiffening due to large deformations as a function of the residual stress present in the piezoelectric thin film in comparison with linear deformation theory. Size of the side of the actuator is 500µm.

2.3.9 Description of the microactuator array

The free ends of the beams need to be fixed to a rigid frame, where electrical signals can be brought to the piezoelectric elements. The

actuators can be arranged into a hexagonal network as depicted in Figure 2-10. The triangular grid frame supporting the actuators also provides the stiffness of the microactuator array.

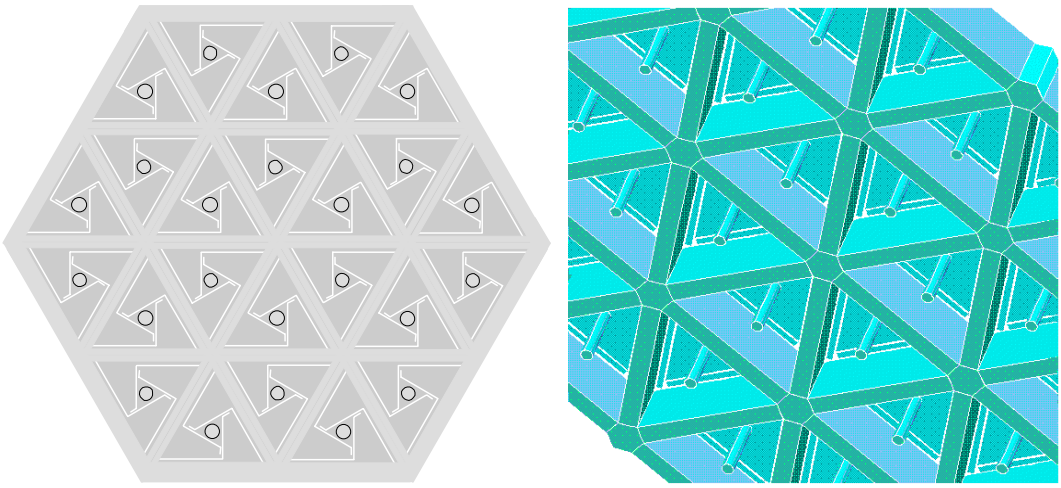


Figure 2-10. Assembling the individual actuators into a hexagonal array.

2.3.10 Estimated maximum lifting force and lateral acceleration

All the actuator arrays having legs make use of friction to transmit the motion of individual actuators to either their holding structure via the ground in a mobile application or an object placed on top of them in a conveying one. It seems interesting to investigate theoretically the potential performances offered by the choice of an elliptical gait.

The total load the system has to carry is split among whole the legs that are in contact with the ground or the object at a given moment –let's assume half of them first-, rapidly compensating for a possible process induced difference of the initial deflection between actuators. Assuming that the physical interactions with the ground reduce to static and dynamic friction forces typical of macroscopic objects, the maximum force that can be transmitted laterally is proportional to the load multiplied by the static friction coefficient between the two materials in contact. If the active force the device can generate gets bigger, the legs simply start slipping and the transmitted lateral force is slightly reduced because the friction becomes dynamic until the device has gained sufficient speed to reach a static regime again. The maximum possible device lateral acceleration is thus simply the product of the friction coefficient times the terrestrial acceleration, g. It is easy to show that the minimal lateral force a leg can generate as a function of the piezoelectric moment Mp induced in a tapered beam is given approximately by

$$f_{lat}^{leg} = 2 \cdot \frac{M_p}{l_b} \cdot \frac{h_{ct}}{h_{leg}}, \tag{2-28}$$

where *hct* is the central triangle height, *hleg* the leg height and *lb* the beam length. Multiplying (2-28) by half the number of legs yields the lateral force the device can generate.

What happens now if the load is that big that the legs returning to their initial position can not be raised away from the ground or the object? The individual vertical forces exerted on the two groups of legs now in permanent contact with the interface can nevertheless be made actively different. Assuming that the same voltage is applied initially to the three beams, the vertical force exerted on one leg can be written

$$f_{vert}^{leg} = \pm 3 \cdot \frac{M_p}{l_b} + \frac{L}{nb_{leg}}, \tag{2-29}$$

where *L* is the total load, *nbleg* the number of legs and ± the sign of the piezoelectric moment indicating whether the pressure on the leg is increased or reduced. Setting the negative version of (2-29) to zero yields the critical load *Lc* imposing a permanent contact of all the legs. Multiplying (2-29) with μs, the static friction coefficient yields the friction forces that need to be overcome for a leg to start sliding when the lateral actuation is initiated. Comparing (2-28) with these friction forces yields the following inequation that rules the legs behaviour

$$\frac{M_p}{l_b} \cdot \left(\frac{2 \cdot h_{ct}}{h_{leg}} \mp 3 \cdot \mu_s \right) > \mu_s \cdot \frac{L}{nb_{leg}}. \tag{2-30}$$

If this inequation is satisfied twice (± sign), the two groups of legs start sliding laterally in opposite directions and the device is accelerated in the desired direction at a rate given by

$$a_{lat} = \mu_d \cdot g \cdot \frac{L_c}{L}, \tag{2-31}$$

until a static regime is attained for the leading legs. The acceleration should then slightly increase since the static friction coefficient is bigger than the dynamic one. If the inequation is satisfied only once (+ sign), the trailing legs still slip and a static regime is initiated directly for the leading legs. The resulting lateral force of the device is the difference of the lateral force of the leading legs and the friction of the trailing ones. When this difference vanishes, or equivalently the inequation is no longer satisfied, the device remains stuck. Since the operation of the array is possible only as long as the legs are protruding from the

substrate, the initial deflection of the legs can be increased by adjusting the internal stress of the piezoelectric layer for 'heavy duty' applications. However, a microactuator array designed to carry large loads will not be optimal when not fully loaded, since the stiffening due to the large initial deformation will reduce its step length and speed.

Let's now take a numerical example. For the structure analysed with FEM just above, the actuator array counts *150* actuators and weights *20mgr*. The vertical force each leg can exert is about $10\mu N$ at *10V*. The total load the system can carry in the first mode described above is thus *150mgr* (half of the legs in contact). Assuming then a friction coefficient of *10%,* we can calculate that for another *180mgr*, both groups of legs slip at power on. And it is only with a total load of *730mgr* that the array stays immobilised unable to move. In all the proposed motion modes, the maximum speed that can be attained is set by the step length times the driving frequency as long as it remains below the lateral mechanical resonance frequency of the legs. At *3kHz*, just below this resonance, the array should be capable of speeding at up to *7.2cm/s*. Great care should nevertheless be taken with these stumbling numbers, it is only modeling by now.

2.4 ZnO for low frequencies piezoelectric applications?

2.4.1 Modeling of the electrical behavior of insulated ZnO thin films

The electrical behavior of zinc oxide thin films is a bit odd. Although bulk ZnO is a semi-conducting material, the ZnO thin films are quite conductive, behaving as a degenerated semi-conductor, for which excess zinc or oxygen vacancies are supposed to be responsible. The thin films can thus be considered as heavily n-doped with an ionized donor concentration highly depending on the quality and mystery of the deposition. The mobility of these donors is however limited, meaning that above a given frequency, the behavior of the film changes from semi-conducting to dielectric. This relaxation frequency can be written as

$$f_{rel} = \frac{1}{RC} = \frac{\sigma}{\varepsilon}, \tag{2-32}$$

where σ and ε are the conductivity and the permittivity of the film. For most ZnO thin films, this relaxation frequency is in the MHz range, explaining why most realisations are operating in the VHF or above range [44]. For low frequency applications, the direct biasing of the ZnO thin film rather results in a thermal behaviour than a piezoelectric one, since a large DC current would flow between the electrodes. While some technological ways aiming at minimising the conductivity have been

investigated by incorporating for example lithium in the sputtering target [45] or applying post-deposition heat treatment [46,47], the most widely established or believed way to circumvent the excess conductivity of ZnO is to add an insulating layer between the piezoelectric film and one or both of its electrodes. Is it sufficient? And how does an electric field build up inside ZnO in that case?

In [48], the single sided insulated ZnO structure is compared to that of a MOS diode. Consequently, an electric field could effectively build up inside the ZnO film if it can be partially or totally depleted. The electric field distribution across the depleted zone is linear, being maximal at the oxide interface and zero at the depletion zone boundary. The depletion width, which depends on the square root of the voltage, reaches a maximum when charge inversion occurs at the semiconductor oxide interface. At low frequencies, thermal and photo-induced electron hole pair generation provides the minority carriers that populate the inversion region at a sufficient rate to compensate for the external voltage variations. As a result, the electric field inside the ZnO can not be further increased, and an augmentation of the biasing voltage is directly lost across the dielectric. The condition for charge inversion is related to the donor concentration N_D, which can be estimated from conductivity measurement using the following equation

$$\sigma = q \cdot \mu_n \cdot N_D, \tag{2-33}$$

where q is the charge of an electron and μ_n its mobility inside ZnO. The maximal width of the depletion is given by

$$W_M = \sqrt{\frac{4 \cdot \varepsilon_{ZnO} \cdot k \cdot T \cdot \ln\left(\frac{N_D}{n_i}\right)}{q^2 \cdot N_D}}, \tag{2-34}$$

where ε is the permittivity of the semiconductor, kT/q the equilibrium thermodynamic voltage and ni, the intrinsic carrier concentration. A ZnO of poor resistivity has thus a great concentration of donors, which results in a very short depletion depth. The consequence for a bimorph actuator is that only a part of the piezoelectric layer becomes stressed and contributes to the beam deflection. On the other hand, if the biasing polarity is reversed, the MOS diode is put into the accumulation mode, meaning that majority carriers accumulate close to the oxide semiconductor interface and that no electric field builds up inside the piezoelectric material. For processing reasons, interface charges might be trapped in the oxide and put the semiconductor in the depletion mode without any external voltage being applied to the structure. In that case, a

bimorph beam can effectively be moved in both directions. This structure presents however several drawbacks. Firstly, the bimorph behavior becomes non-linear with respect to the applied voltage. Secondly, the electric field that can build up is unidirectional and can only be modulated from zero to a maximum value determined by the inversion condition. Finally, the maximum depletion depth, which depends on the material quality, can be very small and the location of the insulator not ideal, being too close to the bimorph neutral axis and leading to a very inefficient structure.

The second structure, where ZnO is insulated from both electrodes has been proposed in [49], but its modeling is not reported. From a technological point of view, this configuration is favored since an amorphous layer is provided for highly oriented ZnO growth and the thin film can be passivated allowing eased subsequent processing. The structure is equivalent to that of a MOS diode [50] but the structure symmetry and the fact that no charges could flow into or out of the semiconductor have be taken into account. Consequently the structure should be insensitive to the direction of the applied external polarisation and the neutrality of charges has to be respected at any time in the semiconductor. When the structure is externally biased, a depletion region is induced at the most negative interface, while accumulation of electrons takes place at the other interface. In the case where the maximum depth of depletion is smaller than the piezoelectric thickness, the behavior is quite similar to the MOS diode case, meaning that an electric field effectively builds up inside the layer from the most negative interface. This field is given by

$$E_{ZnO}(x,Vext) = \frac{q \cdot N_D \cdot (w(Vext) - x)}{\varepsilon_{ZnO}}, \tag{2-35}$$

with

$$w(Vext) = 2 \cdot \frac{\varepsilon_{ZnO}}{\varepsilon_{ox}} \cdot \left(\sqrt{d_{ox}^2 + \frac{Vext \cdot \varepsilon_{ox}^2}{2 \cdot \varepsilon_{ZnO} \cdot q \cdot N_D}} - 2 \cdot d_{ox} \right), \tag{2-36}$$

where *w,x* and *dox* are the depletion depth, distance from the interface and thickness of the insulator respectively. However, due to the structure symmetry, this field can build up from either interface of the semiconductor depending on the sign of the external polarisation. For actuation purposes, the advantage of such a structure over the single sided insulated one is that the beam responds to both polarities and can thus be better exploited. Additionally, the effectiveness in the case where the electric field builds up from the outer electrode of the beam is

maximal, since the stress is induced away from the neutral axis. Again, when the inversion condition is reached, the field inside the piezoelectric saturates and an additional voltage increase is lost across both dielectrics.

If the impurity concentration can be lowered by improving the deposition process or by applying post-deposition heat treatment, then the maximum depletion width can be bigger than the thickness of the layer itself. In that case, the layer will be completely depleted at a voltage that can be derived from (2-36) with $w(V_{dep})=d_{ZnO}$ before inversion takes place. If the external voltage is further increased, a constant electric field given by

$$E_{ZnO}^{lin} = \frac{Vext - V_{ext}^{dep}}{d_{ZnO} \cdot \left(1 + \frac{2 \cdot d_{ox} \cdot \varepsilon_{ZnO}}{d_{ZnO} \cdot \varepsilon_{ox}}\right)}, \tag{2-37}$$

is added to the film, which behaves as a dielectric until *Vext* is big enough so that the surface potential inside the ZnO reaches the inversion condition at an external voltage given by

$$V_{ext}^{inv} = \frac{2 \cdot k \cdot T}{q} \cdot \ln\left(\frac{N_D}{ni}\right) \cdot \left(1 + \frac{2 \cdot d_{ox} \cdot \varepsilon_{ZnO}}{d_{ZnO} \cdot \varepsilon_{ox}}\right). \tag{2-38}$$

From that point on, the additional charges that accumulate on the electrodes are directly compensated at each oxide semiconductor interfaces through the formation of an inversion channel on one side and the accumulation of majority carriers on the other one. The electric field inside the piezoelectric thin film then saturates and an additional voltage drop across both oxides compensates for the increase of the external bias. The maximum quasi-static voltage that can be applied across the piezoelectric film is thus limited by the bandgap voltage of ZnO, which is 3.2V. Figure 2-11 shows the charge and electric field distribution and an energy band diagram for a completely depleted doubly insulated ZnO structure once inversion has occurred. *Qd* corresponds to the depletion charges, *ΔQl* to the ones responsible for the constant field inside ZnO and *ΔQi* to the ones in the inversion canal. If the minority carrier charge variation rate in the inversion layer induced by the external voltage variation exceed the thermal and optical generation rate, the structure behaves as a dielectric even if the inversion condition is reached. As a result, a higher electric field can probably be generated in the semiconductor.

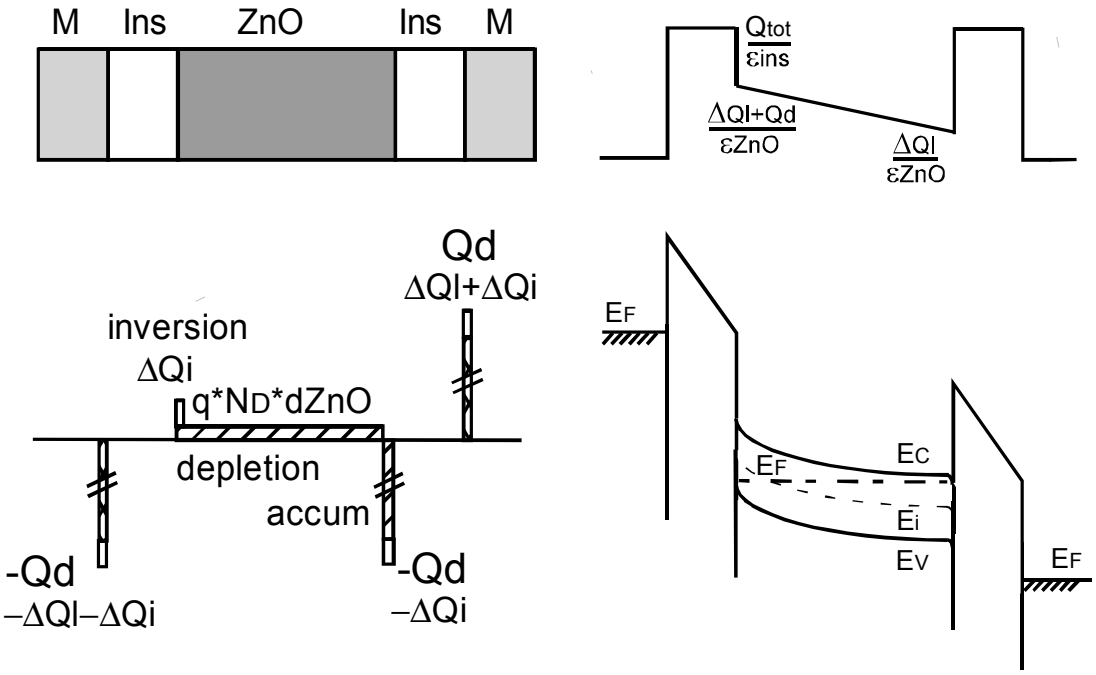


Figure 2-11. Structure, charge (bottom left), electric field distribution (top right) and energy band diagrams after strong inversion has occurred in the doubly insulated ZnO film for low frequencies applications.

An efficient way of verifying this model is to measure C-V curves to look at the voltage dependency of the capacitance of the structure. Since the applied voltage modulates the depth of the depletion, a change in the capacitance of the structure is to be expected. For small values of *Vext*, the capacitance is that of the two oxides in series. As the depth of depletion increases, the overall capacitance is lowered, since the influence of the depletion capacitance (ε_{ZnO}/w) becomes significant. When the depletion depth reaches the thin film thickness, the overall capacitance is minimum and corresponds to the dielectric capacitance of the three layers. This capacitance remains unchanged until it returns to its maximum value after strong inversion has occurred (at low frequencies). If the maximum depth of the depletion is lower than the film thickness, the capacitance decreases towards an intermediate value.

2.4.2 Characterisation of ZnO thin films

Figure 2-12 shows a θ-2θ x-ray diffraction measurement of a sample taken from a finished device integrating a ZnO thin film.

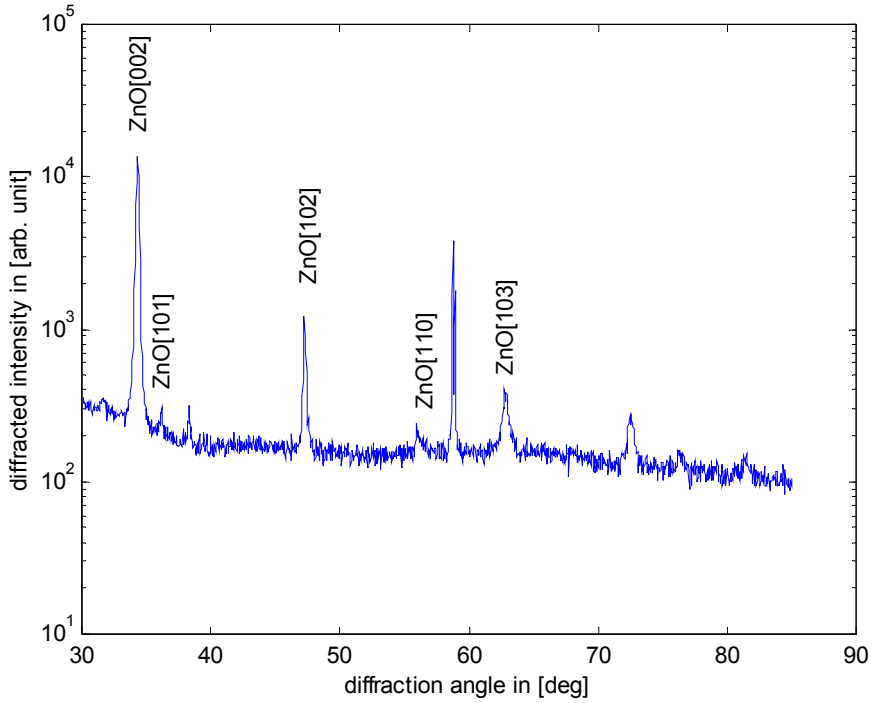


Figure 2-12. X-ray diffraction measurement of a device integrating a ZnO thin film.

The peaks corresponding to the first order diffraction for different crystalline orientations of ZnO are annotated. The main peak at 34.4°, whose relative intensity amounts to about 80%, corresponds to the desired c-axis orientation responsible for the piezoelectric effect. According to Müller [51], a necessary but not sufficient condition for obtaining good piezoelectric activity requires that about 98% of the material be oriented in the c-axis direction.

To get an idea about the electrical properties of the sputtered ZnO thin films, different measurements can be performed on the doubly insulated structure. Figure 2-13 shows the frequency dependence of the overall capacitance of the stack that allows the determination of the relaxation frequency of the semi-conducting ZnO thin film. As mentioned in the previous section (equation (2-32), this frequency corresponds to a change in the electrical behaviour of the film from semi-conducting to dielectric, setting the lower limit below which the use of ZnO becomes problematic. The measured capacitance at low frequency corresponds well to that of the two oxides only, while the value at high frequency is equivalent to that of the complete structure.

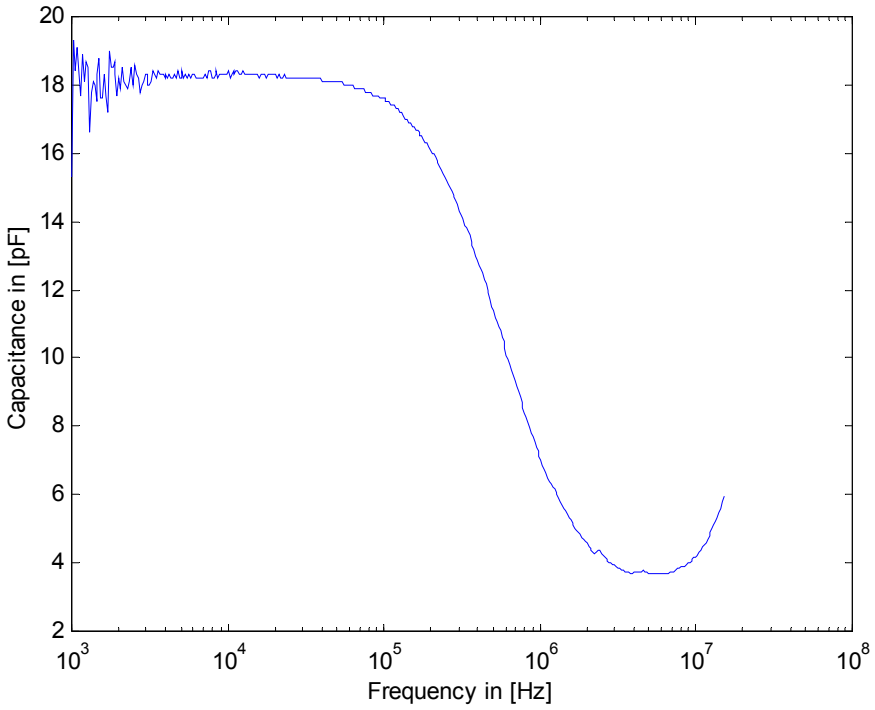


Figure 2-13. Capacitance frequency dependence for the doubly insulated ZnO structure. The change from a semiconducting to dielectric behaviour is clearly visible.

To see whether an electric field can built up inside ZnO at low frequencies, the voltage dependency of the capacitance of the doubly insulated structure can be measured. According to the model presented in §2.4.1 that takes the symmetry of the structure into account, the capacitance of the stack should exhibit the behaviour of a symmetrical back to back *MOS* diode structure. The capacitance at low bias should match that of the insulating layers and decay to a lower value as the ZnO film becomes depleted due to a higher bias until the inversion condition is reached. The equivalent maximum depletion width that can be extracted indicates how deep the electric field penetrates inside the material and thus what part of the layer can be piezoelectrically strained. The doubly insulated structures did not show a clearly symmetrical *C-V* behaviour nor a significant change in capacitance. A slight decay could however be observed on either side at relatively high bias. The particular *C-V* measurement that is shown in Figure 2-14 for its high capacitance contrast corresponds probably to a structure where one of the insulating layer is deficient since the capacitance value is twice as high as expected. The equivalent depletion width that can be extracted corresponds unfortunately to only *20nm*! Difficult in these conditions to induce a piezoelectric strain in the layer.

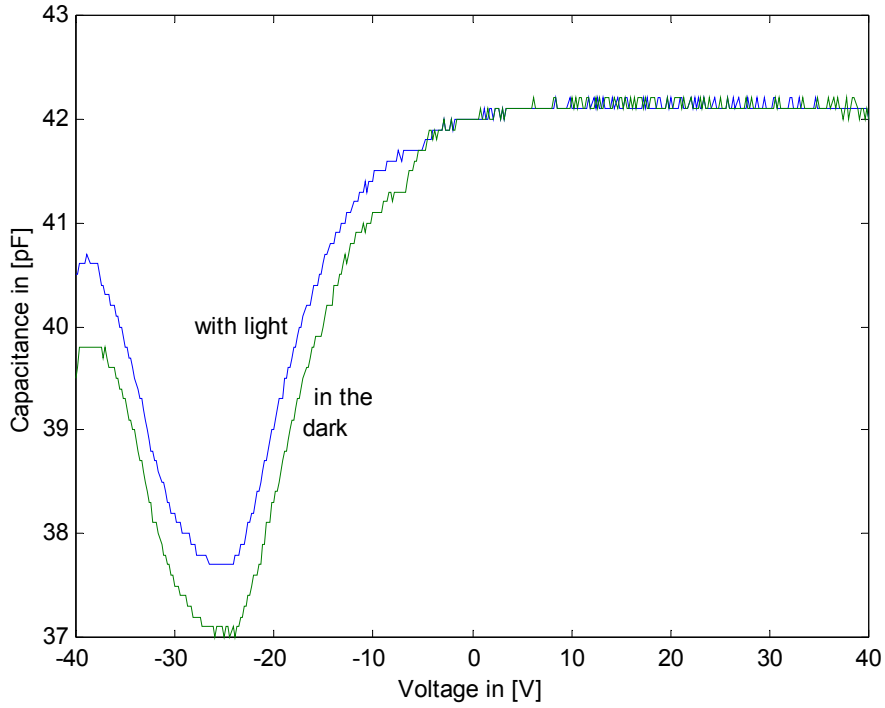


Figure 2-14. Capacitance voltage dependency at 100kHz of a metal insulator ZnO metal structure and illustration of the photoconductivity of ZnO.

The photoconductivity of ZnO is illustrated on the same figure. When the sample is illuminated, additional photogenerated carriers reduce the maximum depletion width as expected.

With these simple measurements, two independent mechanisms responsible for the bad results obtained with ZnO have been demonstrated. The model that has been proposed to quantify the electrical field that can build up inside the doubly insulated structure could not be verified due to the very bad electrical properties of the deposited thin films.

2.5 Fabrication

2.5.1 Preliminary

The processes that have been developed to fabricate the different versions of the microactuator array are based on a combination of surface and bulk micromachining. While bulk micromachining was until lately limited to anisotropic wet etching, the recent availability of deep dry etching tools capable of etching vertical structure through an entire wafer is greatly widening the potential of bulk micromachining (see e.g. [52,53] for examples of applications). Particularly, the combination of wafer-through deep reactive ion etching (DRIE) with piezoelectric thin

film actuation is offering new opportunities for actuators or arrays, such as the possibility of having simple multiple degrees of freedom, high speed, high stroke, low power actuators that can generate more complex motions with conveniently separated interfaces allowing multiple chip module assembly.

Two different piezoelectric materials have been investigated in this work. Zinc oxide was selected initially because of the simplicity of its associated processing and the availability of an old sputtering equipment devoted to its deposition. There was however neither a methodology in the way its integration into devices was undertaken nor any knowledge of the quality of the deposited film, maybe because it had already been used somewhat successfully in some former projects at the Institute of Microtechnology of the University of Neuchâtel. The characterisations of the crystalline and electrical properties of the films that were eventually motivated by the repeated disappointing results demonstrated that the conditions for obtaining piezoelectric thin films were way from being attained (see §2.4.2). Aluminum nitride on the other hand, benefited from a solid characterisation work at the material level, a necessary prerequisite for the successful integration of complex devices. Furthermore and contrary to ZnO thin films in general, a very stable and reproducible process could be developed for high quality AlN thin films deposition. The reader interested in details about deposition conditions, material characterisation is referred to [54].

The innovative technological developments that have been achieved for the microactuator fabrication are the integration of aluminum nitride for MEMS applications, the development of a suitable DRIE process to etch vertical tiny structures only 30μm wide across a whole silicon wafer and the integration of a few hundreds of actuators into a single device.

Considerable investigations on the stress of different thin films have also been necessary to obtain slightly protruding legs and reliable flat membranes to ensure the device functioning and a good yield within an actuator array.

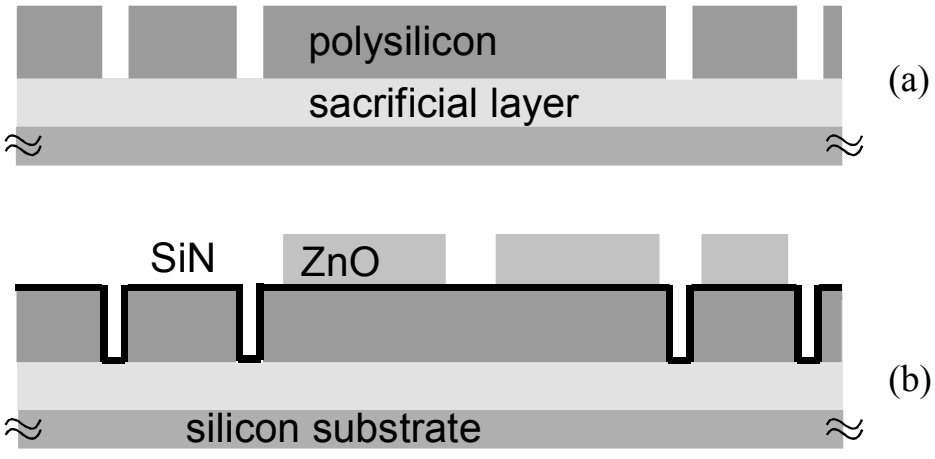
Interesting development aiming at circumventing AlN underetching problems have led to a very simple solution that completely eliminates the underetch and enables a very fine patterning of the piezoelectric thin film.

2.5.2 Process sequence for the ZnO and AlN array fabrication

In this section, a quick description of the two fabrication processes that were developed for the integration of the microactuator array is

presented. Following sections will give detailed considerations on particular processing steps.

Figure 2-15 shows a cross-section of the fabrication process associated with the ZnO microactuator array fabrication. On a double side polished *300µm* thick silicon wafer, a thermal oxide layer is grown to serve as sacrificial and etch-stop layer on one side and as masking material for deep dry wafer-through etching on the other one. A LPCVD polysilicon layer is then deposited, doped and patterned to form the common bottom electrode, the interconnects and the structural elastic elements, consisting of beams, hinges and central plates (a). A thin PECVD nitride layer is then conformaly deposited to provide insulation and an amorphous seed layer favoring well oriented ZnO growth [39]. The piezoelectric material is then sputtered and patterned to form the actuators on top of the polysilicon beams (b). Another nitride layer then passivates the ZnO to prevent unwanted etching during further wet processing steps. Following the vias and beams edges opening (c), the aluminum is finally evaporated (or sputtered) and patterned in one or two steps to form the thick interconnecting lines and the thin top electrode (d). The bottom thermal oxide is then structured before the wafer is etched through until the topside etch-stop oxide is reached. This sacrificial oxide is then removed in buffered hydrofluoric acid (BHF) to release the actuators (e). Compressive stress present in some of the upper layers of the beams will then push the legs a few microns downwards and ensure protruding legs needed for walking.



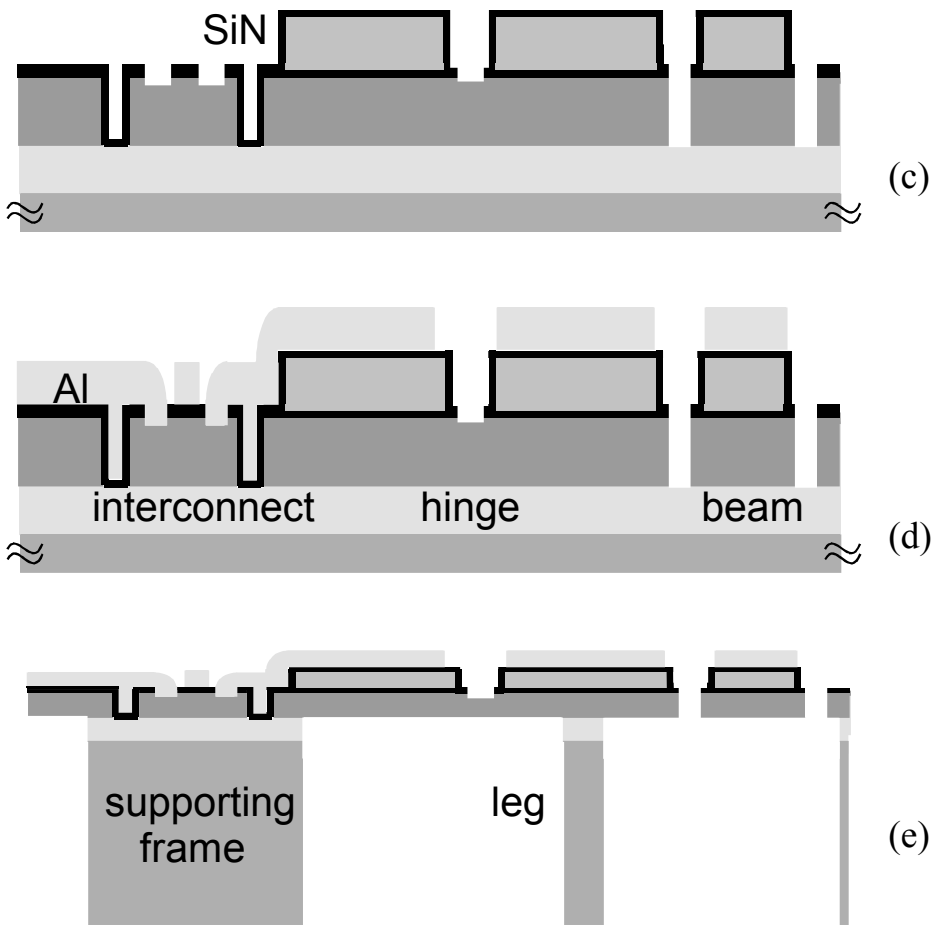


Figure 2-15. Process flow for the fabrication of the ZnO microactuator array: (a) polysilicon depostion, doping and patterning; (b) insulating nitride and ZnO deposition, ZnO patterning; (c) passivating nitride deposition and vias opening; (d) metallisation of the array; (e) wafer-through dry etching and sacrifical layer removal.

The process that has been developed to fabricate the AlN microactuator array has been made compatible with the mask set that was used with the ZnO. A lot of modifications in the fabrication sequence were nevertheless necessary to fabricate successfully the AlN array, whose processing steps are illustrated in Figure 2-16. Deposited on top of a sacrificial oxide and a low stress structural nitride layer, the tantalum/platinum bottom electrode required for well oriented AlN growth, needs to be patterned by ion milling to define the common bottom electrode, interconnects and the top part of the structural elastic elements, consisting of beams, hinges and central plates (a). The AlN is then sputter deposited at about *400°C* before it is patterned in hot phosphoric acid to open vias and the beams edges using the former 'nitride' mask (b). The excellent chemical stability and dielectric properties of AlN eliminate the need for any additional passivation or insulation, meaning that unlike ZnO, AlN is advantageously deposited directly between two conducting electrodes and can also serve as an

insulator between two conducting levels. Postponing the patterning of the structural layer after that of the AlN or ultimately at the end of the process ensures that the interconnection area remains free of unnecessary significant steps, favoring a robust metallisation of the array. This metallisation is performed in two steps so as to get thick and robust aluminum interconnections and a thin top electrode made either of titanium, platinum or aluminum to yield an optimal actuator structure (c). A backside thick resist photolithography is then performed before the wafer is etched through, until the topside etch-stop oxide is reached. This sacrificial oxide is then removed in BHF either releasing the structures or allowing a dry release step if the patterning of the structural layer has been postponed until the end of the process (d).

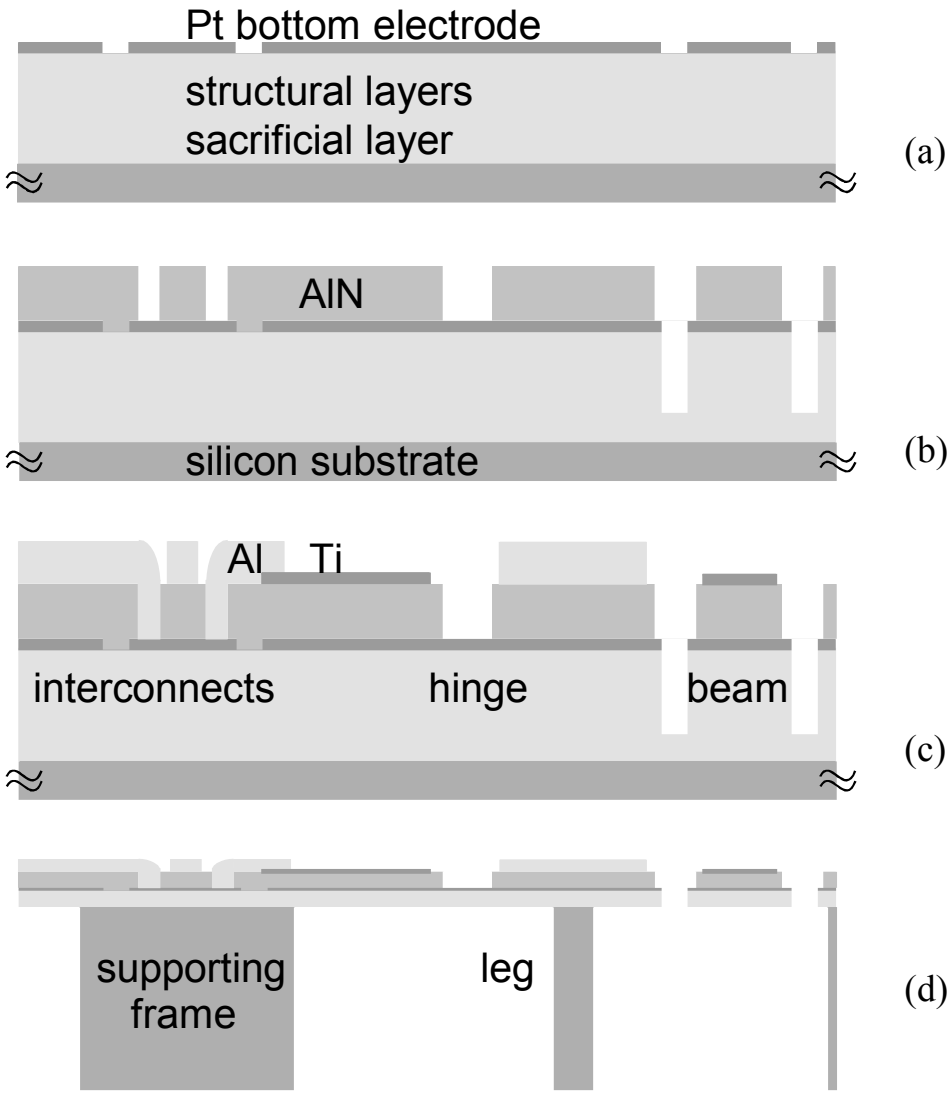


Figure 2-16 Process flow for the fabrication of the AlN microactuator array: (a) Ta/Pt bottom electrode deposition and patterning; (b) AlN sputtering/patterning (vias and beams), patterning of the structural layer; (c) metallisation; (d) DRIE and releasing.

2.5.3 Stress optimised sacrificial and structural layers

In the ZnO process, thermal oxide is the natural candidate to serve as the sacrificial and etch-stop layer, since it stands the high temperature annealing step needed to dope the polysilicon and reduce its as-deposited stress. Unfortunately, thermal oxide is quite compressive (in the range of *-300MPa*), often leading to membrane buckling once the bulk silicon has been etched underneath. Fragile polysilicon hinges were often found broken after the wafer-trough etch step. Reducing the thermal oxide thickness would solve the problem provided that enough masking material remains available on the other side to etch through. In the AlN process, the temperature budget is more favorable since the structural layer does not require any doping. CVD oxide can advantageously replace the thermal oxide since it exhibits an as-deposited stress that is a slightly tensile and remains positive up to *650°C*. Its thickness can thus be increased so as to help maintain the membrane flat and provide sufficient etch stop capability.

Intuitively, for the bimorph to bend down upon release, the stress distribution across the composite beam should be slightly compressive above the neutral axis thus in the piezoelectric thin film and slightly tensile underneath that is in the structural material. While sputter deposited piezoelectric thin film can easily be made compressive, it is much harder to obtain a slightly tensile structural material. Doped and high temperature annealed polysilicon films exhibit a slightly compressive residual stress of about *–30MPa* that is satisfactory for the ZnO process but incompatible with the low stress sacrificial CVD oxide that is necessary to obtain high fabrication yields within an array. An alternative is to use low stress PECVD nitride but it suffers from low deposition rate and low throughput. Semi-amorphous polysilicon can be made tensile if deposited at *570°C* and annealed at around *600°C* [55] but the deposition rate drops considerably at such temperatures. The annealing step has to be time controlled since the polysilicon stress changes from compressive to quite tensile if annealed for too long. Reproducibility is thus not guaranteed. A combination of low stress polysilicon and nitride was finally retained so as to satisfy some trade-off and allow fine stress adjustment.

2.5.4 Bottom electrode for obtaining highly oriented AlN films

A specific sputtering process at about *300°C* is required for obtaining a platinum film that exhibits the <111> crystalline orientation favoring the growth of c-axis AlN thin films. Consequently lift-off is not appropriate to pattern this layer and one has to deal with ion milling. With such a

physical patterning step, the resist gets severely damaged and burned residues are inevitably left on the structures even after an extensive cleaning procedure. Unfortunately these residues react probably with nitrogen during the deposition of AlN and lead to the formation of cauliflower-like hillocks of unknown composition. Figure 2-17 shows a SEM picture illustrating this phenomenon. The shortcuts between the global top and bottom electrodes that are found on all arrayed device are most likely related to these defects that are probably conductive or easily etched during subsequent processing before the top electrode is deposited. Having a single hillock under a metal line in an array results in its malfunction indicating how serious this problem is.

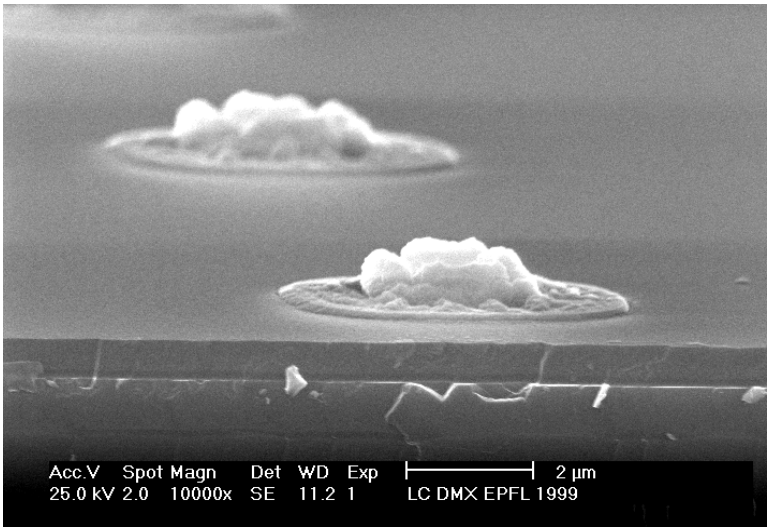


Figure 2-17. SEM picture showing the effect of resist residues on the growth of AlN.

2.5.5 ZnO and AlN thin film patterning

As already mentioned, ZnO can be wet etched in almost any acid solution. However, in order to control and limit the underetch, a solution containing phosphoric acid, acetic acid and water in a [1:1:110] proportion has proven efficient. In that case, the underetch is limited to about *2-4µm* for a *1µm* thick layer.

AlN on the other hand is chemically much more stable and thus much harder to pattern. Good results can however be obtained with hot phosphoric acid on polycristalline thin films, leading to an underetch comparable to that of ZnO. The deposition of a thin layer of CVD oxide on top of the AlN proved efficient to completely eliminate the underetch problem. As a consequence, an excellent resolution patterning which might be required in some applications is possible. Dry etching of AlN is very difficult not only chemically but also physically due to its extreme hardness. The ceramic laboratory of the EPFL has nevertheless obtained

interesting results with a chlorine ECR ion beam [56] offering an alternative to wet etching but at the expense of a reduced selectivity towards the bottom electrode and problems in resist stripping.

2.5.6 Interconnects and top electrode realisation

The fabrication of the actuator array is seriously complicated by the necessity of connecting the actuators together. In order to generate complementary elliptical patterns in one of six directions, the beams forming the actuators need to be driven in six independent groups. In order to minimise the number of required bondpads and simplify the processing, a structure with a bottom electrode common to all the actuators has been retained. Consequently, the top electrodes should be partitioned in six groups as shown in the left part of Figure 2-18. At each node of the array however, interconnections between two layers of conducting material insulated from each other have to be performed so that the signals corresponding to these six groups of beams can be propagated. A possible interconnection layout is shown in the right part of Figure 2-18. In order to minimise the number of masks and the required layers of conducting material, interconnections with conductive strips defined in the bottom electrode layer have been implemented.

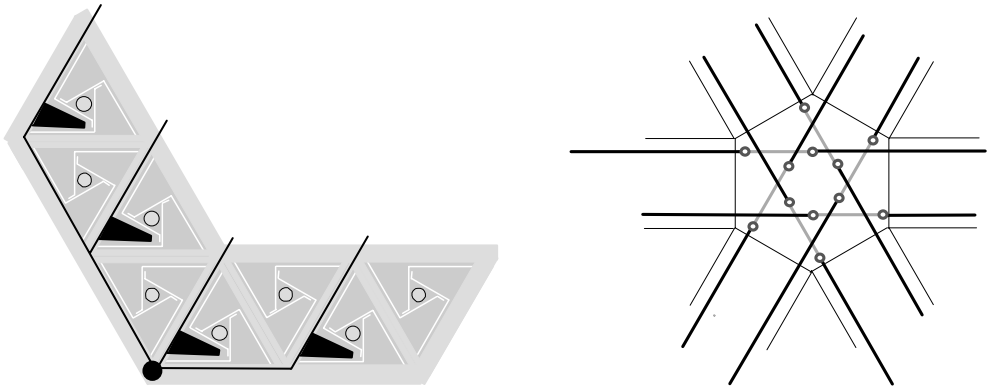


Figure 2-18. Schematic of the electrical signals feeding with interconnections: left) bonding pad and feeding lines, right) interconnections at every node of the grid

The challenge in the metallisation of the ZnO array is the coverage of the steep polysilicon and ZnO steps encountered in the interconnection region and at the ZnO boundaries respectively. Both kinds of steps are about $1\mu m$ high requiring a thick aluminum layer and the use of a planetary system if the metal is evaporated. Sputtering was also found very efficient to cover these steps. The following aluminum wet etching is in both cases a critical step, since underetching tends to interrupt the aluminum lines under the step area. It should be noted that the need for achieving a good coverage of several thousands of steps does not make

the process really robust, since a single metal interruption precludes the use of all the beams connected further away along the same line.

Interconnection contacts add to the challenge, since for each insulated crossing, two contacts between aluminum and doped polysilicon need to be done. In order to obtain good ohmic contacts at the polysilicon aluminum interface, the doping level of the polysilicon has to be quite high so as to minimize the contact resistance and achieve a sheet resistance of a few tens of ohms per square. Figure 2-19 shows a picture of the step coverage, the interconnections and contacts at one node of the array. The electrical behaviour of such an interconnection is that of two back to back schottky diodes, -one of them entering the reverse breakdown operating region- in series with the resistance of the polysilicon wire that dominates at high field.

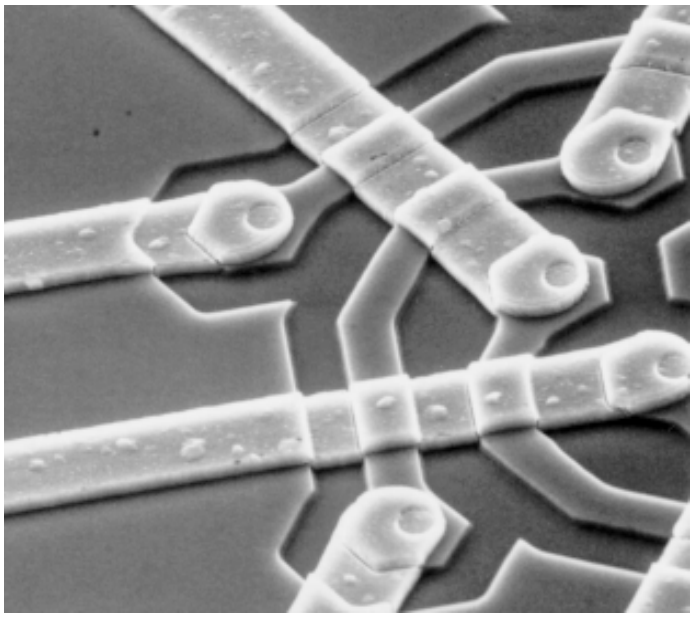


Figure 2-19. SEM picture showing the interconnection region where step coverage, aluminum to polysilicon ohmic contacts have to be guaranteed. Lines are 10μm wide.

In the AlN array metallisation, electrochemical effects take place, greatly compromising its success unless great care is taken. The problem arises from strips of platinum that need to be contacted across the AlN to make the interconnections. If aluminum is in contact with a more noble metal, it gets very rapidly oxidized when both are immersed in an alkaline solution such as in the resist developer. It has been observed that corrosion occurs preferentially at locations away from where the platinum makes contact with the solution and very kindly in the steps area, leading to broken resist lines that were blown away in a few tens of seconds by the intense gaseous release taking place underneath.

Reducing the steps height under the aluminum tracks, by postponing the patterning of the structural layer after that of the AlN greatly reduced this problem. In that case, electrochemical effect can still take place in the developer but mostly closer to the beams edges thus sufficiently far away from the interconnecting lines. On the other hand, if the structural layer is patterned after the metallisation, aluminum conformaly covers every pieces of platinum and nothing visible happens in the developer.

In an optimised two-steps metallisation where a thin top electrode and thick and robust feeding lines are desired, care should be taken to avoid the formation of an oxidised layer between the two metals if the materials have to be deposited and patterned one after the other. This problem was encountered with titanium and aluminum and could probably be solved if the second metal is deposited after a back-sputtering step. Different combinations of lift-off and/or wet etching have been investigated with different top electrode materials to find a robust way to metallise the array but with limited success. In these trials, special attention was also paid to the AlN layer in order to minimise its exposition to wet etchants especially after a probable cause for the short-circuits across the piezoelectric layer had been identified (formation of hillocks of unknown composition during the growth of AlN).

Figure 2-20 shows a picture of a few actuators after a two-steps metallisation.

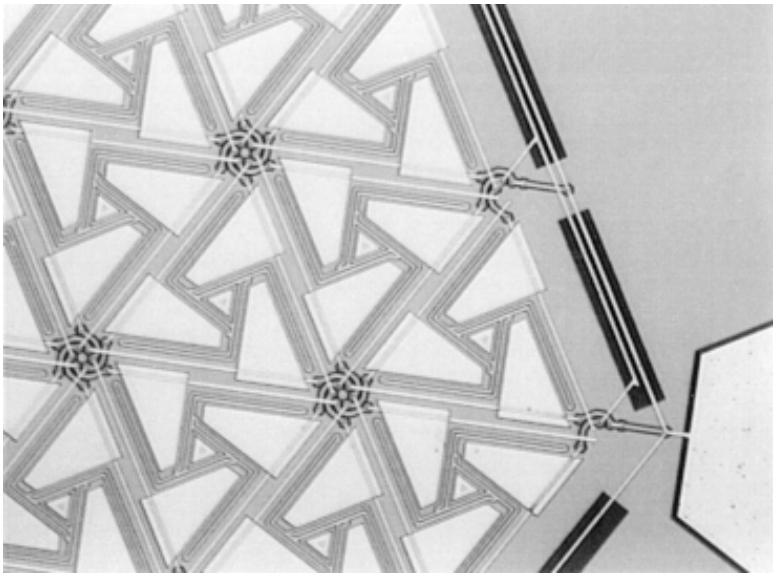


Figure 2-20. Picture showing a few actuators after an all aluminum metallisation.

2.5.7 Wafer-through etching

There are two commercially available competing process families for anisotropic deep dry etching, although both are based on SF_6 chemistry and achieve anisotropy by active passivation of the sidewalls. One is based on oxygen passivation at cryogenic temperature [57], which is done simultaneously with etching, while the other uses the polymerisation of decomposed C_4F_8 at room temperature [58], but where an alternation of etching and passivating phases takes place. One of the main advantages of cryogenic cooling is that the selectivity of the masking material versus silicon can be very high. It is thus possible to use a thin layer of thermal silicon dioxide, both for the masking and etch stop layers. Positive resist however does not stand the thermal shock and cracks when frozen unless a dehydration and a deep UV treatment is done just prior to etching. The advantage of the SF_6-C_4F_8 process is its operation at ambient temperature, which permits the use of positive resist, but at the expense of a reduced selectivity, which means that a resist layer of about ten micrometers is required for wafer through etching.

The early developments made for the microactuator array fabrication were done on the cryogenic Alcatel METlab etcher because it was available at CSEM. Later, an ambient etching system from STS was evaluated at the IMT and eventually some trials were performed at Alcatel on the new 601 etcher, which combines both ambient and cryogenic processes in a single equipment.

The METlab consists of an ICP (inductively coupled plasma) chamber, where SF_6 and O_2 are decomposed into radicals and atoms that are then accelerated towards the wafer by a secondary plasma. The interactions with the substrate surface are both physical and chemical and depend on the secondary plasma DC potential. The ions need to have sufficient kinetic energy to remove the passivation layer on horizontal surfaces before atoms of fluor can chemically interact with silicon and remove it, but leave the passivation on the vertical sidewalls so that anisotropic etching can be achieved. Together with SF_6, oxygen is introduced into the plasma to provide passivating radicals that interact with and deposit onto the silicon surface to form some SiO_x compounds. The exact balance of these two competing processes -etching and passivation- can only be obtained at cryogenic temperature, at about *-95°C* and by carefully adjusting O_2 and SF_6 flows, pressure, temperature, DC bias and ICP power. Depending on which process dominates, the slope of the sidewalls can be adjusted from negative to positive. If etching is too important, the sidewalls will have a negative slope, meaning that a hole

gets wider at the bottom. When passivation dominates, the slope of the sidewalls become positive and holes can not be etched very deep since loads of needles or 'grass' form into cavities and prevent further etching (black silicon formation). For this application, vertical profiles are requested, requiring sharp parameters tuning during the process, especially since wafer through etching is at aim and if a good yield is desired (inhomogeneities of the slopes across the wafer). A negative slope would indeed quickly slash the long and narrow pillar leaving the device inoperable, while a positive slope would initiate black silicon formation and prevent wafer through etching. When the etch-stop layer is reached, the etching conditions change. The base of the silicon pillars tends to be etched away by the reactive atoms that are not adsorbed any more on the surface of the bottom of the hole where they previously reacted with silicon. There might be some different electrical potentials between oxide and silicon due to charging effects that deflect the incoming ions towards the base and damage it as can be seen in Figure 2-21.

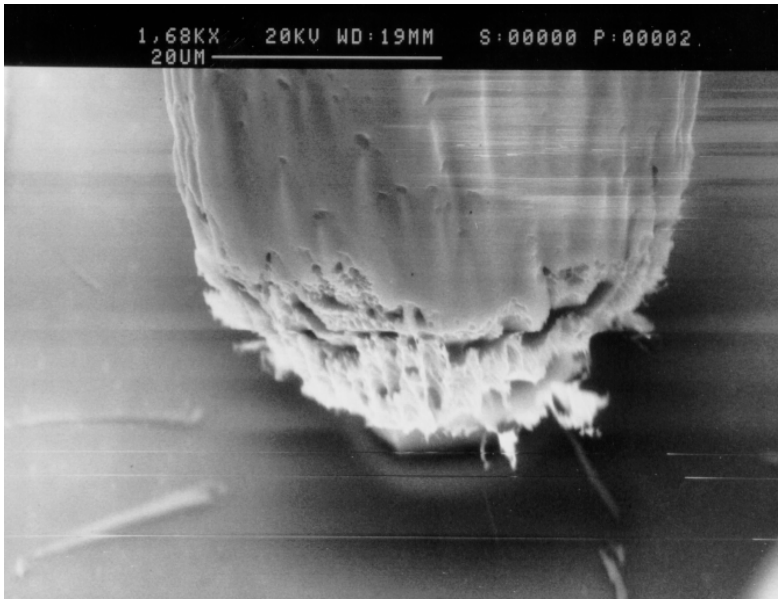


Figure 2-21. Damaged pillar base due to overetching with the same conditions as during normal etch.

A solution to this problem has been found by increasing the DC bias and the partial O_2 pressure during the overetch time necessary to compensate for the lateral etch rate variations. In that case, micro masking is initiated, but the corresponding needles are easily slashed once the interface is reached by the same charging effect. The resulting undamaged pillar is shown in Figure 2-22.

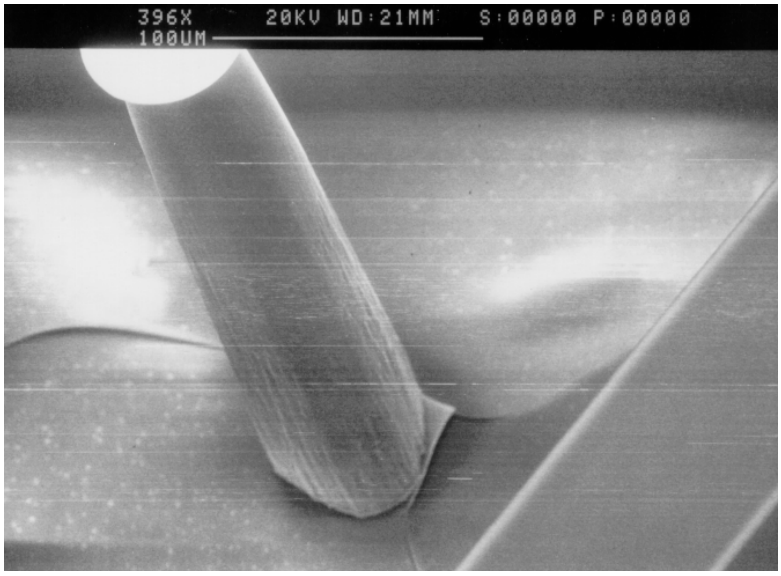


Figure 2-22. Undamaged pillar base after modification of the parameters during the overetching phase. Note the tearing of the SiO2 layer due to compressive stress.

A stable process with minimized under-etching could be developed on the METLab, as can be seen on Figure 2-23, which shows a view of two legs and the frame of the microactuator array after wafer-through etching.

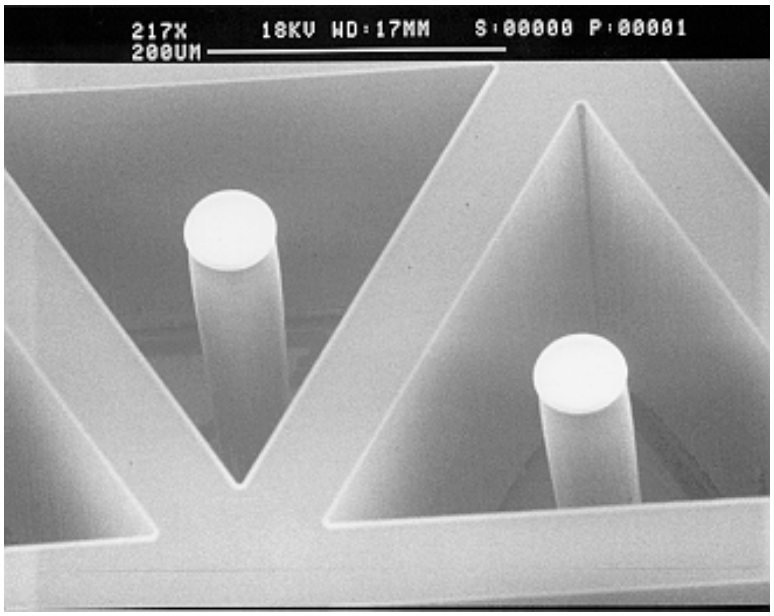


Figure 2-23. SEM view of two legs and the frame of the microactuator array after wafer-through etching with the optimised cryogenic process developed on the METLab.

However, reproducibility within months was of big concern, since the quartz dome of the machine was gently being etched away by the RF coupling until implosion, adding a variable and uncontrolled amount of oxygen into the reactor. To remedy to these undesirable effects, the

machine underwent extensive modifications, such as the replacement of the quartz dome by an alumin cylinder that left it inoperable for the pillar fabrication. A machine qualification would be needed before such a sensitive process could be performed again.

Investigations on the STS system were then initiated. Good results were obtained until the interface was reached, but as soon as the pillar was getting insulated from the bulk silicon, excessive local heating and charge effects led to a dramatic under-etch of the pillar base. This degradation of anisotropy at the oxide interface, though also encountered on the METLab, is more severe on the STS and along with its poor radial etch rate homogeneity, is responsible for the bad yield obtained with this machine. Another problem specific to wafer through applications arises from the electrostatic clamping system of this machine. In order to avoid the rupture of wide area membranes in the etcher, a handle wafer is used once part of the wafer has been etched through. The resulting thermal properties of the interface between the two wafers are critical for the success of the tedious etching that is performed now to compensate for the 15% radial etch rate inhomogeneity. During this step that can last for a good hour, passivation is increased at the consequence of an etch rate reduction in order to preserve the legs that have already been opened. The resist layer that holds the two wafers together might be considerably heated so that it does not offer a good protection on the electrodes against buffered hydrofluoric acid anymore during the release step. Conversely, the clamping system of the two Alcatel machines is mechanical, meaning that the wafer can be conveniently glued on a piece of blue tape (similar to the one that is used for dicing wafers) prior to etching and the temperature slightly decreased so as to take into account the reduced thermal conductivity of the assembly. Significant differences were found on the resulting released structures.

Some tests were then performed on the new Alcatel 601 etcher at ambient temperature (SF_6-C_4F_8 process. The first trials with a non-optimized process produced with excellent uniformity structures such as pictured in Figure 2-24 at a mean etch rate of *8μm/min* as opposed to *3-4μm/min* for the METLab and the STS system. The process was unchanged during the whole etch and no pillar slicing was observed. The needles that can be seen from half the etched depth indicates that passivation slightly dominates and induces some micro-masking.

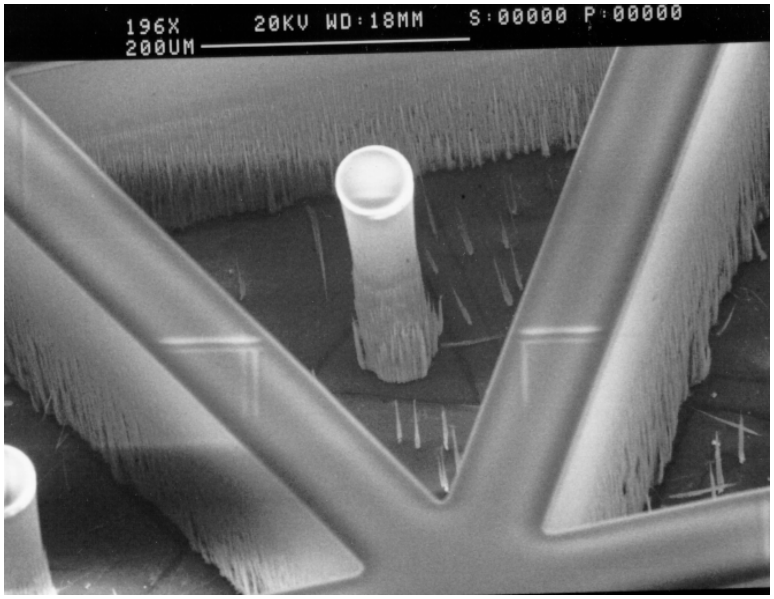


Figure 2-24. Structure etched on the new Alcatel 601 at ambient temperature without parameters modification during the process.

The radial etch rate homogeneity of a DRIE equipment is thus one of the most critical parameter to take into account when evaluating such a system. Both cryogenic and ambient etchers have pros and cons and the choice of a particular etching process has a direct influence on the sacrificial and masking material that should be used for the device fabrication.

2.5.8 Actuator releasing

Releasing the actuators in buffered hydrofluoric acid (BHF) at the end of the fabrication process is a very sensitive step, since forces induced by polar solvent such as water, might break the structures. Soaking the microactuator array in a non-polar solution, such as isopropyl alcohol prior and after any wet etch step reduces such effects. Since BHF is very agressive to the metals that are used in the array, a protective resist should be spun on top of these structures before the DRIE step and stripped in acetone or in a plasma asher after the removal of the sacrificial oxide. The released structures will eventually bend downward, according to the stress distribution of the composite beam and ensure protruding legs.

When the top electrode can stand a maskless SF_6 plasma step, the structuration of the structural layer can be postponed until after the removal of the sacrificial oxide. It results in a dry release step that is less critical than the wet one and ensures that no BHF gets in contact with the top electrodes. Figure 2-25 shows a bottom view of part of a released microactuator array while Figure 2-26 a complete top view.

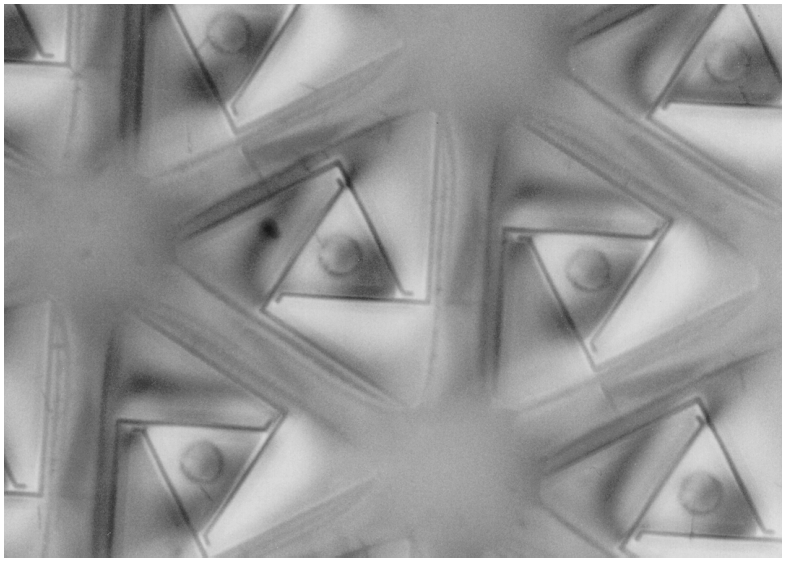


Figure 2-25. Picture showing part of a released microactuator array.

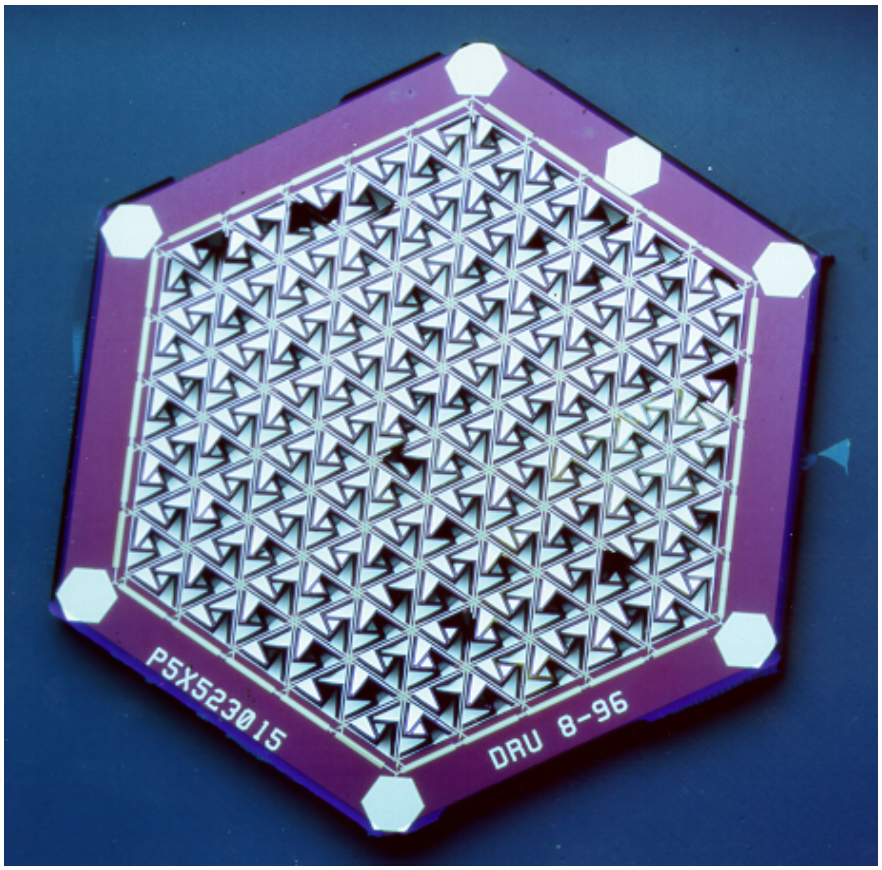


Figure 2-26. Picture of the fabricated array

2.6 Measurements

2.6.1 Preliminary

The piezo-induced motions and the electrical impedance of individual actuators and beams can be characterized so as to estimate the performance of a few different designs. Testing the arrays under a probe station is a very useful way of verifying the electrical connectivity of non-shorted devices since the motion of working actuators can easily be observed under a microscope. For quantitative motion measurements, test actuators or arrays can be glued on a small piece of printed circuit board (PCB) drilled in its center to avoid any mechanical interaction with the legs and bonded. The actuators are then excited with harmonic or square wave signals with different phase lags (0, π, $\pi/2$) to measure their vertical, swinging and elliptical motion with their legs being left floating.

2.6.2 Measuring setup for 3-DOF structures

The characterisation of a structure with two angular and one translational degrees of freedom is not so obvious. Measurements of tilting and vertical motions have been decoupled so as to keep simple measuring setups. The quasi-static vertical motion of the actuator can be monitored with a confocal microscope combined with an autofocus. An interferometric system is very appropriate to characterise its frequency behaviour. The setup that is required to characterise the quasi-static and dynamic two-dimensional tilting motion had to be developed specifically. Based on the deviation of a laser beam that is reflected on a tilted surface, the measuring setup is depicted in Figure 2-27. Focusing the beam is necessary to avoid diffraction, since the structure features are small enough. The laser light is first combined with an illuminating source in a beamsplitter (BS). A second BS is used to redirect the light towards the focusing lens and the actuator placed in the lens focal plane. The beam is then reflected by the central plate of the structure, and hits the lens slightly sideways, depending on the plate tilt. The lens transforms the beam back into a parallel one, restoring its initial size and vertical propagation direction. The beam then crosses the second BS again, before being separated on a third BS to be projected onto a CCD camera via another lens and on a four-quadrant photodiode. A confocal arrangement yields a sharp image on the CCD camera when the actuator is located in the focal plane of the bottom lens where the laser beam reaches its minimum size. The four-quadrant photodiode is necessary to reconstruct the tilting amplitude of the actuator, if the lateral shift of the beam, which is equal to *f/30/deg* (where *f* is the bottom lens focus), is too small to produce distinguishable features on a wall.

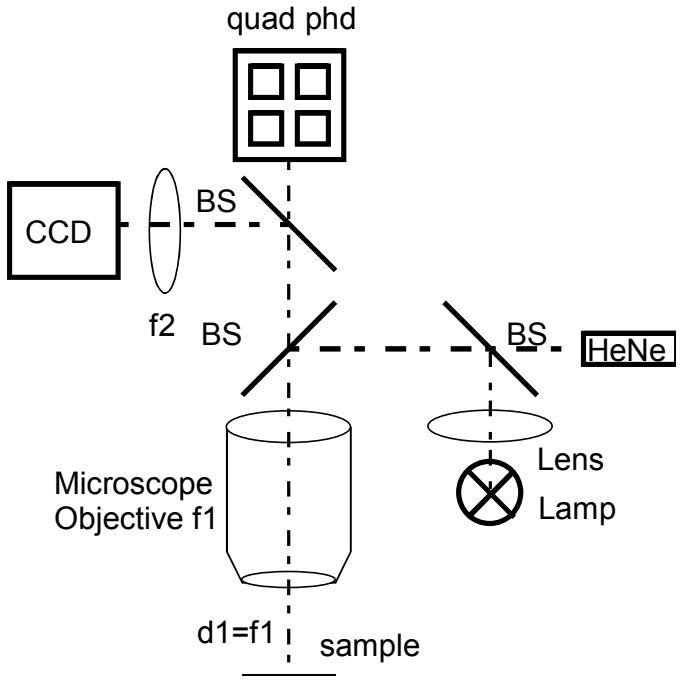


Figure 2-27. Measuring set-up for the characterisation of the tilting motion of the actuator.

2.6.3 Beam and actuator electrical impedance measurements

Figure 2-28 shows the measured electrical impedance of a beam near its first resonance frequency that has been acquired with an HP4194A. Curve fitting yields a Q-factor of 110, a motional over static capacitance ratio of 0.1% and a $tan\delta$ of 1.7%.

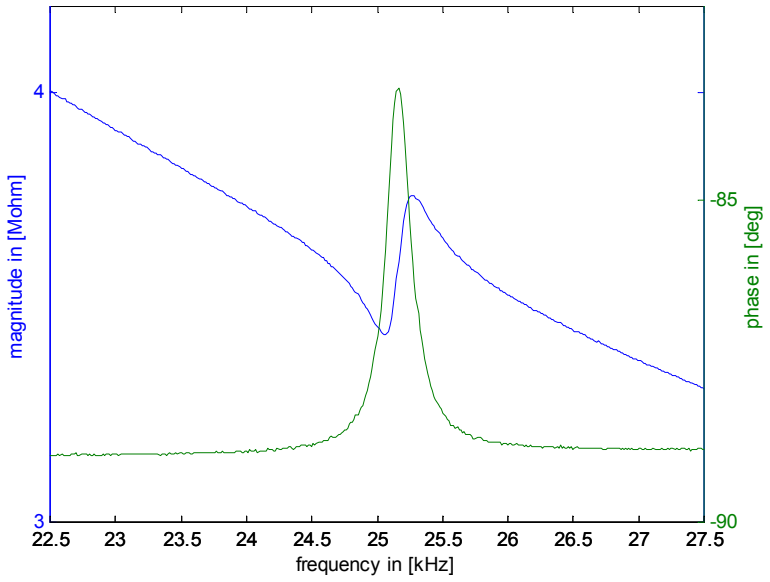


Figure 2-28. Impedance measurement of a single beam.

The capacitance ratio is about an order of magnitude lower than expected and is the consequence of a lower piezoelectric coefficient, the parasitic capacitance of the bonding pad and the part of the top electrode that is clamped on the substrate. Since test structures are located at the periphery of the wafer, a reduced piezoelectric activity is to be expected due to the limited homogeneity of the sputtering equipment. The rather large value of the dielectric loss is probably related to some resist residues that affect the quality of the AlN layer.

The electrical impedance measurement of test actuators did not show a well defined first resonance frequency. The three bimorph beams making the actuator showed slightly different electromechanical resonance most likely due to lithographic misalignments. Since the actuator arrays did not show any electrical resonance at all and hence the possibility of detecting it automatically, only a quasi-static driving mode is appropriate.

2.6.4 Quasi static operation of beams and actuators

Figure 2-29 shows the quasi-static response of the same beam when the electric field is varied linearly between *±200kV/cm* i.e. *±10V* bias voltage together with the theoretical value. The difference in motion amplitude is the consequence of a lower piezoelectric coefficient. The breakdown field was close to *1000kV/cm*.

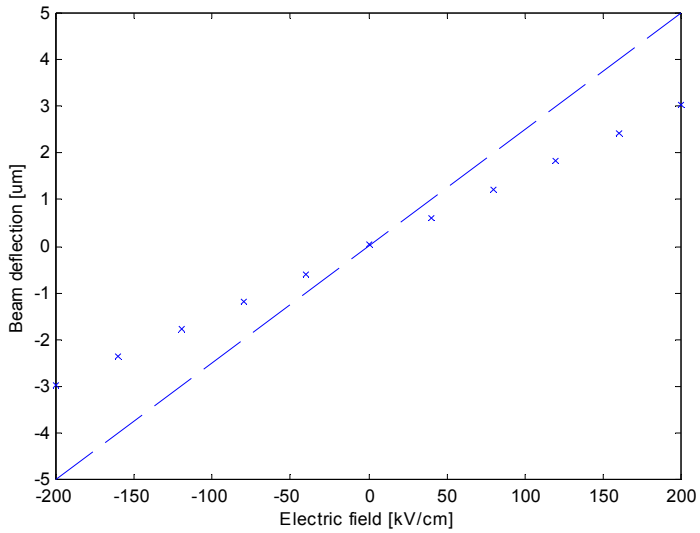


Figure 2-29. Measured beam displacement versus electric field compared with simulated value (dashed line)

The measurement of the actuator behaviour could be performed on a device where the piezoelectric activity was optimal and the initial bending due to residual stress very low. The quasi-static extreme

positions that the leg tip reaches in the discrete driving mode are shown in Figure 2-30. The vertical amplitude was obtained with the confocal microscope while the lateral one with the tilting setup described earlier when the actuator was connected to either *+10V* or *–10V* as it is planned in the system. Similar amplitudes were obtained for the other directions. The motion amplitudes are in good agreements with those of the structure that has been simulated with FEM in §2.3.8 although the two structures are slightly different.

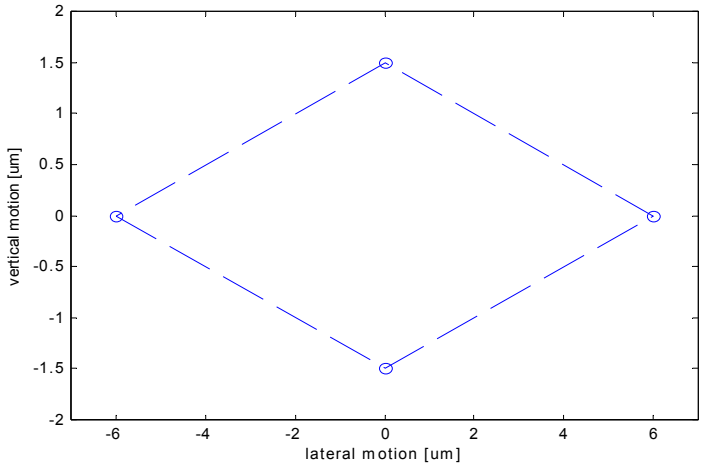


Figure 2-30. Measured quasi-static tip of the leg trajectory in the discrete driving mode at ±10V.

2.6.5 Dynamic actuator behaviour

Figure 2-31 shows an interferometric measurement of the vertical frequency response of an actuator where a Q of 14 can be extracted for the main resonance at 33kHz.

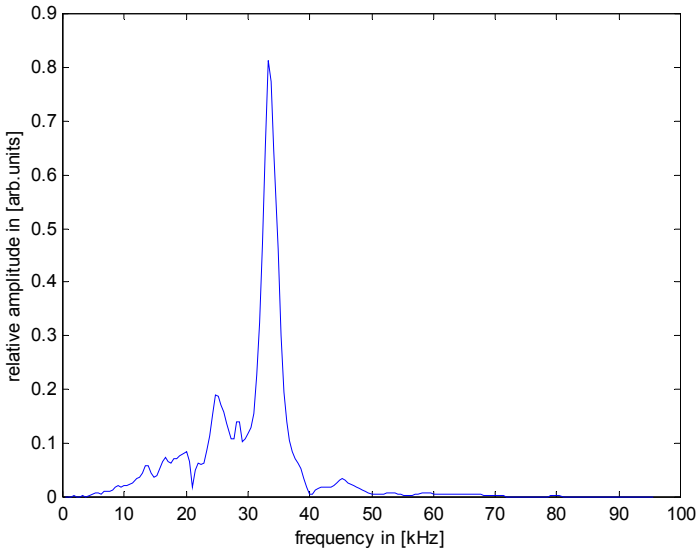


Figure 2-31. Vertical frequency response of an actuator

The dynamic tilting mode behaviour could not be monitored electrically with the 4-quadrant photodiode due to the limited bandwidth of the associated electronics.

2.7 Conclusions

In this chapter, the design and fabrication of a piezoelectric microactuator array capable of locomotion have been presented together with the quasi-static and dynamic characterisation of individual actuators. Rather than implementing another version of the ciliary motion principle that has been widely applied to micro-conveyors, the realised device is innovative in many aspects. First, its gait is based on elliptical leg trajectories mimicking the one of animals. The individual actuators can perform three-dimensional high amplitude strokes in any direction due to their three active degrees of freedom structure. This multiple DOF structure additionally helps improve the lifting capability of the array since all the actuators participate to the motion generation regardless of the direction of motion. Furthermore, the proposed actuators elegantly solve the delicate problem of interfacing both electrically and mechanically a device that has to couple some work to the outside thanks to deep reactive ion etching that allows a separation of the two interfaces on different substrate sides. This feature was identified as being a mandatory prerequisite for the realisation of a multi chip mobile autonomous microsystem. Eventually, the choice of a piezoelectric actuation principle offers many advantages, such as low power consumption, the high force, amplitude, speed product it can generate and the simplicity and robustness of the bimorph actuator structure.

After considerable efforts aiming at integrating zinc oxide as the active material that have been impaired by the poor electrical and crystalline quality of the deposited thin films, important process developments were focused on the integration of aluminum nitride. Based on the know-how initially developed at the Ceramic Laboratory of the EPFL, the integration of a VLSI MEMS design proved however considerably difficult. Though individual actuators could relatively easily be made functional and characterised, obtaining a fully functional array has not yet been possible. The reason are the shortcuts that were frequently found on arrayed devices due to the impossibility of getting a perfectly cleaned platinum bottom electrode after ion milling and the difficulty of making interconnections with platinum. The replacement of this platinum bottom electrode by a more convenient material could certainly trigger the widespread use of AlN in sensors and actuators MEMS applications

since its advantages over competing piezoelectric materials are overwhelming.

Three different deep reactive ion etching systems were evaluated, two being from the first generation and based either on cryogenic or ambient etching, while the third one was incorporating both processes and many improvements. Satisfactory processes could be developed on either systems but the radial etch rate homogeneity was found being the most critical parameter to get functional devices at a wafer level. The developments were first initiated on a cryogenic etching system, which gave very satisfactory results that could however not be reproduced once the machine underwent extensive modifications. The poor radial homogeneity of the first generation ambient etching system (15%) combined with the necessity of using a handle wafer at the end of the process required tremendous efforts to get standing legs on a significant part of the wafer. Eventually, tests conducted on a second generation system with much improved radial homogeneity and doubled etch speed proved excellent.

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3. A low power ASIC for the millipede control

3.1 Preliminary

One of the challenges in realising a remotely controllable wireless moving microsystem is that the driving signals have to be generated onboard. Consequently, the actuator driver needs to be integrated as well and a wireless data link established so as to remotely control the system. All this functionality can be implemented on an integrated circuit, which will serve as the interface between the user and the microsystem. The integrated circuit has two functions. Firstly, it has to receive, shape and decode the information transmitted via a wireless link. Secondly, it has to generate the proper driving signals for the piezoelectric actuators. The main features constraining the circuit design are the low power consumption at a voltage supply of $2V$ and a high voltage handling capability. Additionally, the whole system is powered by a small solar cell, meaning that the peek power consumption (i.e. during transitions) is also limited and that sensitive blocks should have a high PSRR (power supply rejection ratio).

3.2 General considerations on the wireless link

The choice of the wireless link is limited since ideally no external component should be added to the system as a transducer. The choice of an IR (infrared) link has been motivated by the simplicity of the associated transducer, which is merely a reverse biased, CMOS process compatible p-n junction. Since both powering and communication make use of light, crosstalk between each other could be of great concern. Powering will require a strong background illumination covering the whole visible and near IR spectrum. If a halogen lamp provides this light, network oscillation at 50Hz will produce a considerable modulation of the output light. Both signals will be picked up by the photodetector resulting in a strong DC current and a signal at 100Hz that could interfere with the transmitted data. On the other hand, information signals are likely to degrade the power supply stability since they will also be detected by the solar cell. The near infrared window is well suited to carry the controlling information since the sensitivity of monocrystalline silicon at this wavelength is much higher than that of the amorphous silicon of the solar cell. Encoding the controlling information at high frequencies (several tens of kHZ range) and high-pass filtering the output current of the photodiode will suppress the DC and low frequencies modulation components.

3.3 Chip architecture

Figure 3-1 shows a schematic of the chip architecture. Its operation is purely sequential and can be described as follow. The incoming pulsed infrared signal carrying the encoded information for the control of the microsystem is converted into an electrical signal by the photodiode. This signal is then amplified so as to restore logical levels before the bit and word decoding is performed. A sequencer controlled by a counter and a variable oscillator (DCCO) then takes care of the control signal generation according to the information that has been decoded. Eventually the high voltage driver actuates the six groups of piezoelectric bimorph.

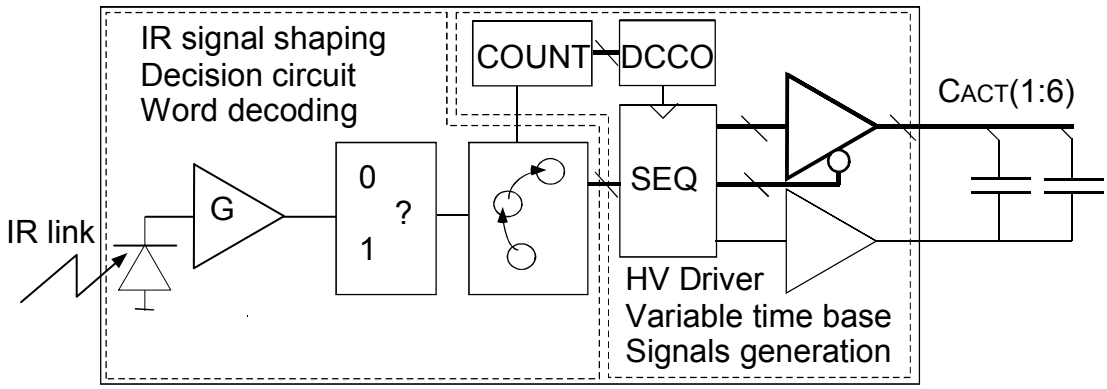

Figure 3-1. Chip architecture. The circuit can be divided into a communication part that handle the reception and treatment of the information transmitted optically and a driving part that takes care of the variable time base and driving signal generation.

3.4 Communication blocks

The only input of the communication part is the information contained in the modulated light intensity and converted by the photodiode. Once this signal has been shaped and its information extracted the pace and direction the actuators should be given is readily available. The communication blocks that perform these functions are briefly described further below, but let us first consider the optimisation of the transducer.

3.4.1 Optimisation of the transducer

The transducer that is used to convert the optical information into an electrical signal, is a reverse biased photodiode. In a CMOS process, the most adequate junction to perform this task is a diffusion-substrate junction. Infrared photons will be absorbed quite deep into the bulk of the substrate due to their lower absorption coefficient compared to visible photons. The diffusion length before recombination is on the order of a hundred of micrometers in a lightly doped substrate, meaning

that an electron-hole pair can easily drift toward the shallow surface diffusion and get separated at the junction interface. A combination of *n-well, n+* diffusions in a p-type substrate will contribute to filter some of the higher energy photons that will be quickly absorbed close to the surface (i.e. in the *n+* doped area) and forced to recombine before having drifted toward the junction interface due to the higher defect density. A grounded polysilicon shield above the photodiode could lead to the same effect. The minimum pulse width that can be detected generally depends on the biasing current of the front-end and the parasitic capacitor of the photodiode. The photodiode area can be quite considerable if a significant signal current need to be detected, leading to a large parasitic junction capacitance when the diffusion extends over the whole surface of collection. However, due to the long diffusion length of the electron-hole pair and the electric field that anyway leads minority carrier (i.e. electrons) toward the junction, it is possible to reduce considerably the surface of the diffusion without loosing too many carriers. Arranging minimum sized junction at regular interval (related to the diffusion length) over the surface of collection is thus a very efficient way to reduce the parasitic capacitance at no expense. Again, a p+ shallow diffusion can be added in the interspace to filter visible photons.

3.4.2 Front-end

The photocurrent flowing through the junction will consist of a strong DC current due to the powering illumination, a low frequency modulation at 100Hz if a lamp is being used as the illumination source, and a pulsed current due to the signal whose intensity will depend on the emitter location. The front-end has to be able to restore a rail to rail logical level signal following the variation of the emitting photodiode regardless of the intensity and variation of the background illumination. Amplification and filtering should thus be closely related, since the signal current could be quite weak compared to the DC current. It is thus not possible to use the traditional photocurrent amplifier consisting of an operational amplifier with a feedback resistor before filtering the signal. Filtering can be done at first with a RC filter whose capacitor directly drives the closed loop amplifier as depicted in Figure 3-2. The photodiode is modeled by a p-n junction, the associated parasitic capacitor *Cj* and the photocurrent *iph*. Resistor *R1* reverse biases the diode at a potential depending on the photocurrent. The feedback resistor *Rf* makes the input of the amplifier a virtual ground, thus *C1+Cj* and *R1* form a high-pass filter. The current flowing through *C1* has to go through *Rf*, if the amplifier has a high input impedance. Assuming an ideal

amplifier, the transimpedance of the block is simply the feedback resistor.

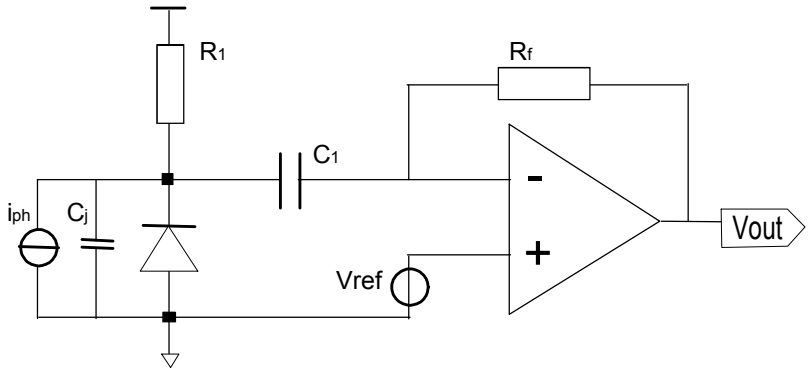

Figure 3-2. Typical front-end for pulsed photocurrent amplification with a strong background illumination leading to a large DC photocurrent.

This front-end, which would be typical of a discrete implementation presents however several drawbacks. Firstly, it needs quite high resistor and capacitor values to set the lower bound of the HP filter in the tens of kHz range and get significant transimpedance gain, typically a megohm and several tens of picofarads for the filter and another megohm for the feedback resistor. Secondly, the amplifier needs to have a sufficiently high transconductance to effectively keep its input virtually grounded and prevent the signal current from flowing preferentially through the parasitic capacitance of the photodiode.

From an integrated and power consumption point of view, active filtering seems more interesting to get rid of the DC and low frequency photocurrent. It can elegantly be done with a modified current conveyor that exactly delivers the low frequency photocurrent while maintaining a constant input potential. The bandwidth of the conveyor is limited intentionally in the tens of kHz to realise a bandpass filter. Above these frequencies, the input node of the current conveyor simply acts as a transimpedance amplifier. This configuration, which is almost equivalent in functionality to the more traditional circuit of Figure 3-2, only needs three transistors and a small capacitor. It will be described extensively later in the block design section. The output signals of both kinds of front-end amplifiers are still too weak to directly feed the input of a comparator and consequently additional voltage amplification is required before a pulse can be detected unambiguously. Figure 3-3 shows a block level schematic of the whole front-end.

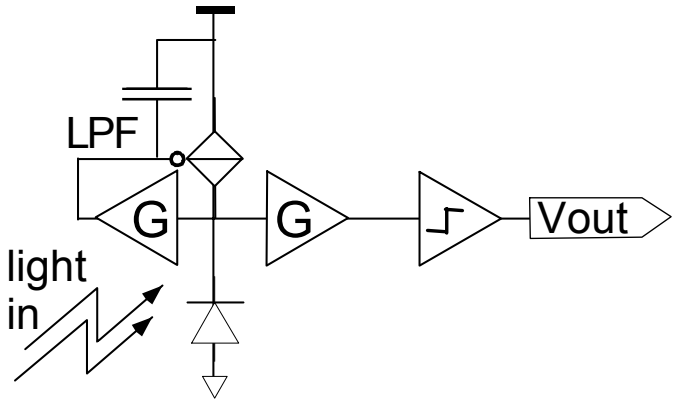

Figure 3-3. Front-end for optical pulse detection under a strong background illumination with logical level output.

3.4.3 Communication protocol and decision circuit

There are different ways of encoding information optically. In a pulse-based protocol, the instantaneous optical output power of the emitting photodiode can be maximised by keeping its duty cycle minimum. The energy corresponding to the maximum continuous power that can be handled by the photodiode can thus be delivered in a burst of narrow but very energetic pulses. To take full advantage of this concept, the width of a pulse has been chosen constant and close to the minimum that can be detected by the front-end with reasonably low power consumption. Encoding is done by different time lag between pulses, so as to simplify the discriminator circuit that does not need to resynchronise itself with the emitter clock. For a robust detection, the decision should not be based on the absolute inter-pulse time but rather on the relative difference between a *one* and a *zero*. Consequently, the decision circuit has to be made adaptive. In the implemented encoding scheme, a *one* is encoded by a time lag between pulses of τ, while a *zero* by 3τ. If the probability of each code is equal, the mean inter-pulse time duration will be 2τ. The discriminator should continuously adapt its threshold so as to set it to the mean inter-pulse duration regardless of the absolute time τ. Figure 3-4 illustrates this communication and decoding protocol.

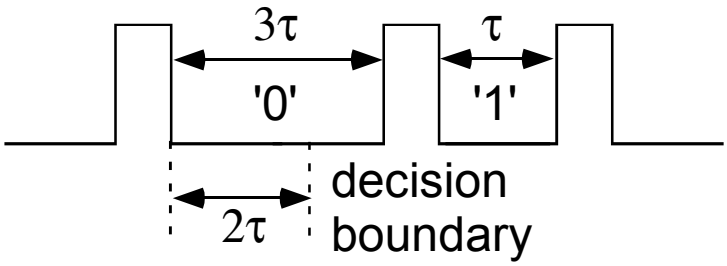

Figure 3-4. Encoding *zeros* and *ones* by different interpulse duration. The decision boundary of the decoding circuit should be based on the mean interpulse duration.

Figure 3-5 depicts a discrimination circuit implementing this concept at a component level. Right after the end of a pulse, *Ccomp* is charged to *VDD* by the astable multivibrator controlling ϕm, before being discharged by a current source controlled by the output of a step integrator. When a new pulse is detected, the voltage remaining on *Ccomp* is compared to *Vref* at the input of the step integrator. The possible voltage difference produces a charge transfer to the output of the integrator that adjusts the discharge rate of the capacitor *Ccomp*. If only *ones* or *zeros* were sent, the output voltage of the step integrator *Vint* would adjust so as to have discharged *Ccomp* exactly at *Vref* at each incoming pulse. Nothing would allow us to discriminate *zeros* and *ones* however, but if the information is encoded as described above, i.e. τ for *ones*, 3τ for *zeros* and an equal probability of each code, then *Vint* would adjust so that the voltage stored on *Ccomp* reaches *Vref* at the mean inter-pulse time 2τ. *Vref* is inherently chosen as the threshold voltage of the discriminator, which consists of a current comparator made of a constant current source *Iref* and a controlled current source *I(Vcomp)* that switches when *Vcomp* is equal to *Vref*. Now, regardless of the absolute mean inter-pulse duration, *zeros* and *ones* will produce a voltage *Vcomp* shifted from the threshold *Vref* by ± *(VDD-Vref)/2* at comparison time, making the decision circuit very robust to variations of the absolute time τ. The gains of the integrator and the controlled current source *I(Vint)* have to be set so that the adaptation to the mean interpulse time is done after ten to twenty samples, meaning that about ten to twenty consecutive *ones* or *zeros* would effectively be read as *ones* and *zeros*. A rapid adaptation is required because leakage currents tend to erase the information stored on *Cint*. In this way, the discrimination circuit would quickly recover after a communication interruption.

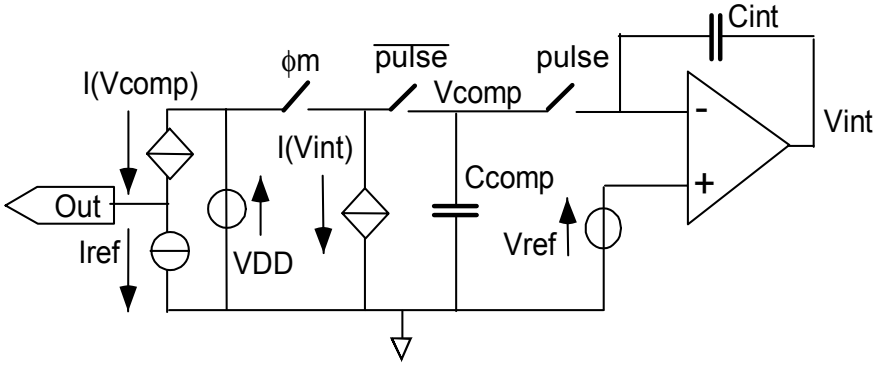

Figure 3-5. Adaptive discrimination circuit for bit decoding

3.4.4 State machine decoder

The integrated circuit also contains a digital part needed to process the information transmitted through the infrared link. Every incoming pulse allows a bit to be read by latching the output value of the discrimination circuit into the state machine that decodes instructions. The whole logic is clocked on the incoming edge of each pulse. Different instructions have been incorporated into the design. There are five instructions needed to control the direction of motion of the actuator array (forward/backward, left/straight ahead/right) and two for increasing or decreasing the value of a 6 bit counter that controls the pace of the actuator array. An eighth one means end of communication (EOC) and puts the state machine in a waiting mode. These instructions are encoded on eight bits and decoded on a single three variables state machine. If only one 8-bit instruction would need to be decoded, the state machine would consist of a three bit counter with conditional increment, meaning that the increment is performed only if the bit value is correct and the counter is reset otherwise. If the six first bits are correct, a valid seventh bit will bring the counter into its last state, meaning that it is necessary to latch the instruction flag until the eighth bit is validated. This decoding state machine can be imagined as an eight bit binary tree with only a single valid path. To decode more instructions, additional paths need to be valid. Eight valid paths can be implemented if three of the eight bits are only memorised but do not condition the progression in the tree. To achieve a robust decoding that detects transmission errors, the remaining bit values can be made dependant on the value of the three operation encoding bits so as to ensure several bits difference between any two of the eight valid bytes. This concept, known as Hamming codes, is widely used in telecommunication. In our case the Hamming distance (number of bits being different between any two bytes) can be three, meaning that up to two errors could be detected. If an error occurs, it would reset the state machine and avoid misinterpretation of the transmitted byte. If a valid byte is successfully read, the three encoding bits only need to be decoded to raise the corresponding instruction output bit flag, which can be memorised if needed. Figure 3-6 shows the binary tree with the eight valid paths. To ensure that the state machine is in a known state, it has been decided that every valid byte would start with a *one* and that no valid code contains more than two successive *zeros*. Sending thus three consecutive *zeros* will reset the state machine if no error occurs.

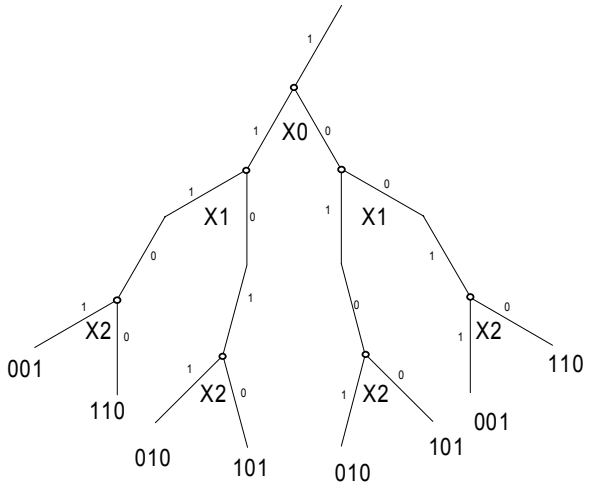

Figure 3-6. Binary tree showing the eight valid paths depending on the value of the bits X0, X1, X2. When a read bit does not allow the progression in the tree, the word is discarded and the path reset.

An additional feature of the design is that individual ICs can be given a tag or an address, meaning that the control of the speed and direction of the mobile microsystem can be done selectively. Different microrobots could thus be operated simultaneously and individually. A simple one byte decoder, such as described previously, has been added to decode the programming instruction needed to tag an individual circuit. The five first bits encode the programming instruction while the three remaining allow to differentiate up to 8 groups of circuits. After power-on, the first time the circuit sees the programming instruction, it memorises the last three bits of the code. Subsequent instructions can then be directly given to the decoder that handle controlling. When the end of communication instruction is sent, only the programming decoder is kept active and waits for the programming instruction with the correct last three bits to be send again before enabling the control decoder. For efficient power consumption management, the inactive logic is inhibited by the gated clock technique.

3.5 Driving blocks

This section presents the blocks related to the actuator driver: a programmable time base, which sets the pace of the actuators, a sequencer that generates the proper sequence of driving signals according to the direction which has been set on the decoder and the driver itself.

3.5.1 Driving concept

The microactuator array can electrically be viewed as a set of six capacitors having one electrode in common. We have seen in §2.3.6 that the six groups of piezoelectric bimorph can be driven by four sinusoidal waves in order to generate the proper alternating elliptical motions. However, a discrete driving scheme with only a few stable points is much simpler to implement. Figure 3-7 shows four instantaneous views of the cross-section of the two groups of actuators at specific times *t1,t2,t3,t4* during a cycle, and Table 3-1 describes the corresponding voltages at the points of actuation *a,b,c,d*. One can see that the elliptical motion is well sampled and particularly that all the extreme positions are reached a stable way with only two discrete voltages *V*+ and *V*-, which could easily be applied to the actuators through high-voltage switches.

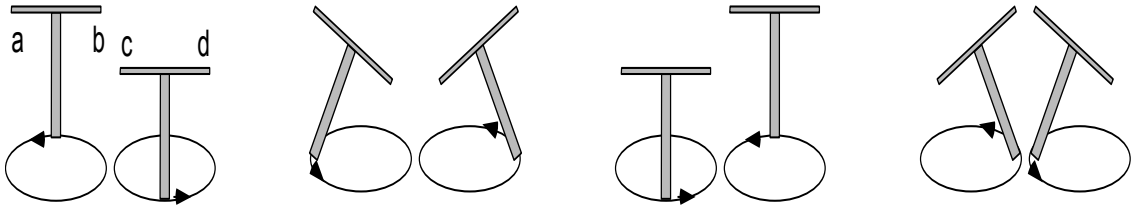

Figure 3-7. Snapshots showing the cross-section of the two groups of actuators during some specific time of the actuation cycle.

	t1		**t2**		**t3**		**t4**	
a	V+	h	V+	o	V-	h	V-	o
b	V+	o	V-	h	V-	o	V+	h
c	V-	h	V-	o	V+	h	V+	o
d	V-	o	V+	h	V+	o	V-	h

Table 3-1. Voltages driving the actuator corresponding to the cross-sections of Figure 3-7. The table also shows holding state (h) and zero crossing transitions (o) between two snapshots.

During some transitions, an actuator sees its polarity reversed. An efficient way to spare some energy is to short the capacitor before reconnecting it to the power supply during a zero-crossing transition. Recycling charges between actuators is not interesting, since usually both are needed simultaneously at the same peak potential during part of the cycle in order to reach the outer positions. Recycling charges to power the other blocks of the IC seems more attractive, but has not been

implemented since voltage adaptation requiring complicated extra circuitry is necessary.

The piezoelectric bimorph were designed to be driven with ±*10V*, so each capacitor should be able to store independently *0V*, *+10V* and *-10V* between its two electrodes. Different driving schemes can be foreseen. A very simple one would be to put the common node at *+10V* and any other at either *0V, +10V* or *+20V* giving the desired *–10V, 0V, +10V*. The main drawback of such a scheme being the use of a *20V* voltage source, which is twice as much as what is effectively coupled to the actuators. On the other hand, if we take advantage of the storing effect of capacitors and accept to introduce some sequencing, meaning that two capacitors can not be charged simultaneously to *+10V* and *-10V*, then a very interesting driving scheme becomes possible. It only requires a *10V* voltage source (named VDDH hereafter), but the ability to connect it a bipolar way. To charge a capacitor to *10V*, the common node should be *grounded* and the other one connected to *VDDH*. Connecting both nodes to *VSS* would discharge the capacitor. If the capacitor is to be charged to *-10V*, then the common node should be put to *VDDH*, while the other one *grounded*. An actuator that has to hold its voltage should have its own electrode floating so that no charges could be removed or added even if the common electrode voltage is changed. Since each capacitor has to sample and hold the three different voltages at different times of a cycle, it means that two independent switches per actuator are needed. The change of polarity is achieved through two complementary switches that alternately connect the common node to *VDDH* and to *ground*. Figure 3-8 shows a switch level representation of this driving concept.

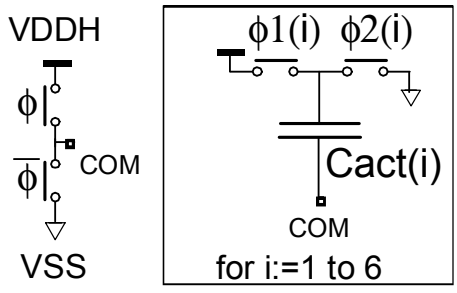

Figure 3-8. Switch level representation of the driver.

During a cycle, charges at *+10V* and *-10V* will alternate, as it will be described later in the sequencer section. If an actuator has been charged to *+10V* and is left floating during the charge of another one to *-10V*, its individual node potential will reach *+20V*, since the common node has to be raised to *+10V*. On the other hand during a new charge to *+10V*, the actuator that has to hold *-10V* will see its own electrode drop down to

-10V since the common node has to be *grounded*. The own electrode of each capacitor, and thus each output of the driver see potential as high as *-10V* and *+20V* during the cycle. This will put stringent constraints on the design of the switches.

3.5.2 Sequencing

The sequencer has to generate all the signals that command the switches for any of the six directions. It has been shown in the previous section that a walking cycle can be decomposed in four main phases. During each of these phases, different groups of actuators need to be charged to *+VDDH* and *-VDDH* according to a sequence, which depends on the direction that has been set on the decoder. Figure 3-9 shows a representative of the six groups of actuators, named *a* to *f* and the six directions of motion *1-6*.

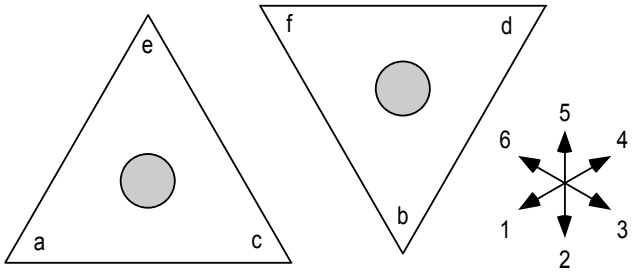

Figure 3-9. Bottom view of the two groups of actuators and possible directions of motion.

Each tip of both triangles can be independently raised or lowered when the corresponding actuator is charged to V+ or V-. Charges to opposite polarities can not be done simultaneously due to the choice of a bipolar power supply mode. It has been arbitrarily decided that a charge to *V+* precedes a charge to *V-*. Table 3-2 shows in what sequence and to what potential the actuators have to be charged if direction *1* or *2* are selected. Sequences for other directions can easily be obtained by permutations.

d1	**t1**	**t2**	**t3**	**t4**
V+	a	e,c	f,b	d
V-	f,b	d	a	e,c

d2	**t1**	**t2**	**t3**	**t4**
V+	b	a,c	f,d	e
V-	f,d	e	b	a,c

Table 3-2. Switches sequence and polarity needed to move in the indicated direction

The sequencer first generates the four time windows *t1-t4* independently of the direction of motion. Every fourth clock is assigned to *t1*, while every following to *t2* and so on. When the clock is high, the polarity is set to *V+* and to *V-* respectively. Then, the corresponding switches signal sequence is generated according to the selected direction of motion.

3.5.3 Time base

A variable oscillator is needed to control the pace of the actuators. Oscillation frequency should be adjustable from *0* to *40kHz* so that the actuators can be driven at up to *10kHz*. Controlling should be done in discrete steps so as to allow direct interfacing with the logic. Details about implementation will be found in the referring section in the block design part.

3.6 Polarisation / Resetting blocks

Some extra blocks needed to ensure the circuit functioning are briefly described hereafter. An on-chip polarisation block is required to generate the proper bias for amplifiers, filters and delay cells. It has to be a self starting, self generating circuit since no reference current or voltage can be applied externally. A power on reset block will take care of the logic resetting, tag clearing and put the microsystem in a waiting mode at every ‘sunrise’.

3.7 Circuit design for important blocks

§3.7.1-§3.7.3 report on the design of the blocks associated with the front-end, §3.7.4 a calculation of the front-end noise and §3.7.5, the front-end expected performances. §3.7.6-§3.7.8 address the design of the blocks associated to the driver, while §3.7.9 reports the conditions affecting the precision of the polarisation blocks.

3.7.1 Bandpass transimpedance amplifier

The first block of the front-end depicted in Figure 3-10 is a modified current conveyor, whose bandwidth is intentionally limited so as to realise the lower corner frequency of a bandpass filter. At low frequencies, transistor *M2* supplies exactly the photocurrent *iph* generated on the photodiode and *V2* is adapted trough *M1* in order to compensate the variation of *iph* while maintaining *V1* almost constant. At higher frequencies, *Cf* absorbs the current variations of *M1* and hence *V2* is kept constant meaning that the photocurrent variations are not

compensated anymore. *V1* is thus varying according to the source transimpedance of *M2 (1/n·gm2)*. The transfer function of the block is

$$\frac{V_1}{i_{ph}} = \frac{s \cdot C_f + g_{DS1}}{(s \cdot C_1 + n \cdot g_{m2}) \cdot (s \cdot C_f + g_{DS1}) + g_{m1} \cdot g_{m2}}, \tag{3-1}$$

where *C1* is the parasitic capacitance at node *1* and *gm1* and *gDS1*, the transconductance and output conductance of transistor *M1*. The low and high corner frequencies of the filter and the gains in the band and at low frequency are approximately equal to

$$fc_l = \frac{1}{2 \cdot \pi} \cdot \frac{g_{m1}}{n \cdot C_f}, \; fc_h = \frac{1}{2 \cdot \pi} \cdot \frac{n \cdot g_{m2}}{C_1} \tag{3-2}$$

$$G_B = \frac{1}{n \cdot g_{m2}}, \; G_{DC} = \frac{g_{DS1}}{g_{m1} \cdot g_{m2}}. \tag{3-3}$$

If transistor *M1* is operated in weak inversion and its channel length is not too short, low frequencies are attenuated by more than 55dB compared to frequencies in the band.

Transistor *M2* is operated in the moderate to strong inversion region, so as to accommodate a steady current range that can vary within an order of magnitude without changing as much its transconductance and thus the gain. The inversion factor of *M2* and *M1* should nevertheless be chosen so as to ensure that the current source biasing *M1* remains saturated under the maximum illumination condition since the gate to source voltage over *M2* and thus *V2* increase rapidly due to the combination of substrate effect and strong inversion.

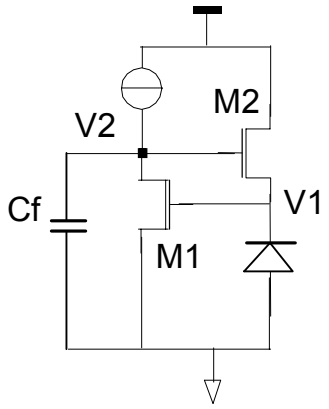

Figure 3-10. Schematic of the bandpass transimpedance amplifier.

3.7.2 Bandpass operational transconductance amplifier (OTA)

The next stage, depicted in Figure 3-11, is a bandpass open loop OTA with differential inputs. One of the inputs is driven directly by the photodiode node, while the other is biased at the diode *DC* potential by *M7*. At low frequencies, *Chp* has no effect, thus ideally *M3* and *M4* see the same current even if their gate potentials slightly differ. The output current of the OTA *iout* is zero, since *M5* and *M6* mirror and subtract the current flowing through *M3* from that of *M4*. At higher frequencies, *Chp* becomes equivalent to a short and the current flowing through *M3* and *M4* is not equal anymore if a potential difference is applied to their gates. If the bandpass of the mirror is big enough, the output transfer function is

$$\frac{I_{out}}{V_{in}} = \frac{2 \cdot s \cdot C_{HP}}{n \cdot g_{m3,4} + 2 \cdot s \cdot C_{HP}} \cdot \frac{g_{m3,4}}{1 + s \cdot \tau_{out}}, \tag{3-4}$$

where *gm3=gm4* are the transconductance of the differential pair and $1/\tau_{out}$ the bandwidth of the output node.

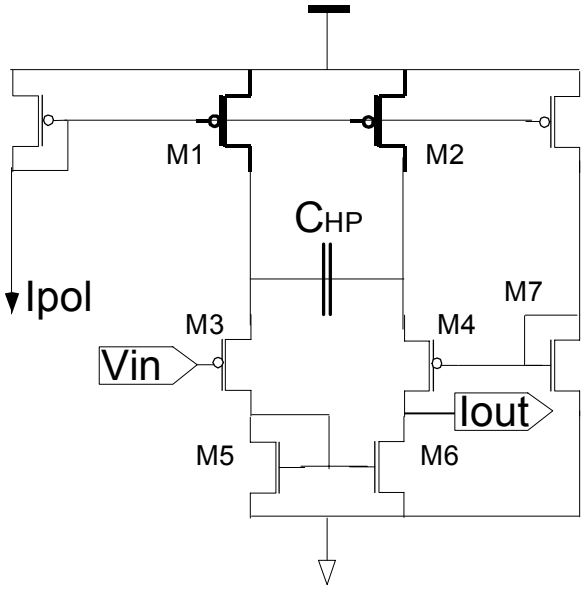

Figure 3-11. Bandpass operational transconductance amplifier.

In the real case however, mismatch always occurs between transistors due to differences in threshold voltages V_T and in current gains β. The output of an OTA thus always has an offset, meaning that *iout* is nonzero when ΔVin is zero. In this configuration however, *Chp* cancels the ΔV_T offset of *M3* and *M4* by storing their offset voltage difference on its electrode. There is no simple way however to get rid of the current mismatch of *M1*, *M2* and *M5*, *M6*, but let us see how to minimise it. The difference ΔId in the drain current *Id* of two well-matched transistors with same gate and source voltages *VG,VS* can be written

$$\frac{\Delta Id}{Id} = \frac{\Delta\beta}{\beta} + \frac{gm}{Id} \cdot \Delta V_T \,. \tag{3-5}$$

where β, $\Delta\beta$, ΔV_T are the current gain, its mismatch and the threshold voltage mismatch. Supposing gaussian distribution and no correlation between $\Delta\beta$, ΔV_T, the variance of the relative current difference is then

$$\sigma^2\left(\frac{\Delta Id}{Id}\right) = \frac{\sigma^2(V_T)\cdot 4}{VG - V_T} + \sigma^2\left(\frac{\Delta\beta}{\beta}\right). \tag{3-6}$$

The variance $\sigma^2 V_T$ and $\sigma^2\beta$ are technology dependent and can be stated

$$\sigma^2(V_T) = \frac{A^2}{W \cdot L} + B^2\,,\ \sigma^2(\beta) = \frac{C^2}{W \cdot L} + D^2\,, \tag{3-7}$$

where A,B,C,D are constants and W,L transistor width and length.

The influence of ΔV_T can be minimised if the transistors are put in very strong inversion. However, the gate voltage of *M5-M6,* has to ensure that *M3* stays in saturation. The simplified condition can be written

$$V_{GM5} \le \frac{V_{TN} + V_{TP} + VDD(n-1)}{n}, \tag{3-8}$$

where V_{TN} and V_{TP} are the N and PMOS threshold voltage and $n=3/2$. In addition, the current mirror has to have a bandwidth big enough to accommodate the pulses. The length of *M5* and *M6* is thus limited so as to keep their gate capacitance *Cg* and transconductance *gm* reasonable since the bandwidth of the mirror is proportional to

$$BW = \frac{g_m}{C_G} \propto L^{-3/2}\,. \tag{3-9}$$

M1 and *M2* each consist of five transistors identical to *Mpol* in parallel. and matching between their currents is critical. Given the reference current *Ipol*, each transistor of *M1* and *M2* can be related to *Mpol* by the same variance, σId^2. The total mismatch current distribution of *M1* and *M2* is simply the sum of the variances

$$\sigma^2 Id_{M1,2} = \sum \sigma_i^2 Id\,. \tag{3-10}$$

The variance of the OTA offset current, *Ioff* relative to *Ipol* is then

$$\sigma^2\left(\frac{I_{off}}{I_{Pol}}\right) = 2\cdot 5\cdot \sigma_p^2\left(\frac{\Delta Id}{I_{Pol}}\right) + \sigma_n^2\left(\frac{\Delta Id}{5\cdot I_{Pol}}\right), \tag{3-11}$$

where the left term is the variance of *(Id$_{M1}$-Id$_{M2}$)* and the right one the variance of the current mirror (the factor 5 stand for the current flowing through the mirror referred to *Ipol*). The standard deviation calculated for the OTA is 6.7% of *Ipol*, which is about *2nA*.

3.7.3 Fast current comparator

The output current of the bandpass OTA, which is made of a negative intermittent current *ipulse* and a static offset current due to mismatch *Ioff* is then fed into a current comparator. Only the statistical distribution of *Ioff* is known, but neither its sign nor amplitude. Consequently, the reference current that sets the comparator threshold should be chosen big enough so as to ensure that mismatch can not hinder the circuit functioning. If this precaution is taken, the only effect of *Ioff* is to increase or decrease the effective current *ipulse* needed to switch the comparator and thus to alter the front-end sensitivity. In order to achieve a very sensitive, fast current comparator, two additional gain cells and a feedback loop are required. Figure 3-12 shows a schematic of the proposed current comparator.

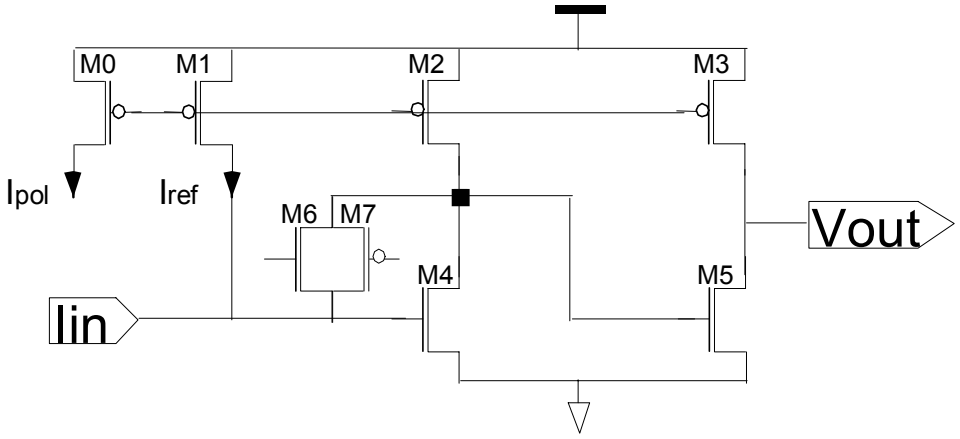

Figure 3-12. Fast current comparator.

In the idle state, transistor *M1* biases the comparator in a known state, by forcing a current *Iref* bigger than an estimate of *Ioff* through *M6*. The rest potential of the gate of *M4* is adapted so that it sinks the current of *M1* and *M2*. That of *M5* is set by the source of *M6,* which is pulled down through the amplifying effect of *M4*. If this potential is low enough so that *M5* sinks a current lower than that of *M3*, the output of the comparator is high. When a pulse of light draws a negative current *Iin* bigger than *Ioff+Iref*, the gate of *M4* begins to drop, hence its drain to rise until *M7* enters in conduction. *M5* now sinks a current bigger than that of *M3* so that *Vout* is pulled down. The feedback transistors *M6* and *M7* limit the excursion of the gate potential of *M5*, but can be considered

as opened during transitions, maximising the gain of the stage formed by *M2* and *M4*. The bias of the feedback transistors have to be carefully designed, while taking into account transistor mismatch so as to minimise switching time without hindering the circuit functioning.

The threshold of the output stage of the comparator is

$$Vth = V_{TN} + \ln(\frac{Id_{M3}}{IS_{M5}}) \cdot n \cdot U_T , \tag{3-12}$$

where *IS* is the specific current of the transistor and $UT=kT/q=26mV$ at room temperature. Its variance is equal to

$$\sigma^2 \Delta_{Vth} = \sigma^2 \Delta_{VT} + (n \cdot UT)^2 \cdot \left(\sigma^2 \left(\frac{\Delta Id_{M3}}{Id_{M3}} \right) + \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) \right). \tag{3-13}$$

The lower bound or the idle state of the comparator input can be written

$$VS_{M6} = \frac{VG_{M6} - V_{TN}}{n} - \ln\left(\frac{I_{ref}}{IS_{M6}} \right) \cdot U_T , \tag{3-14}$$

if we assume that *M6* is in saturation. The associated variance is

$$\sigma^2 \Delta VS = \frac{\sigma^2 \Delta VG + \sigma^2 \Delta VT}{n^2} + UT^2 \cdot \left(\sigma^2 \left(\frac{\Delta IM6}{IM6} \right) + \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) \right). \tag{3-15}$$

Ideally, VS_{M6} has to be slightly lower than *Vth* and adjusted by means of well-controlled parameters that do not depend on the technology. Considering (3-12) and (3-14), the gate voltage of *M6* has to be close to

$$VGM6 \approx (1+n) \cdot VTN . \tag{3-16}$$

Such a gate voltage can be generated with two diode-connected transistors in series biased by a current *Ipold*. Gate voltage and variance can be written

$$VG_{M6} = (1+n) \cdot V_{TN} + (1+n) \cdot n \cdot U_T \cdot \ln\left(\frac{I_{pold}}{IS_{dico}} \right), \tag{3-17}$$

$$\sigma^2 \Delta_{VG} = (n^2+1) \cdot \sigma^2 \Delta_{VT} + (n^2+1) \cdot (n \cdot U_T)^2 \cdot \left(\sigma^2 \left(\frac{\Delta I_{pold}}{I_{pold}} \right) + \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) \right). \tag{3-18}$$

The voltage difference between idle and threshold state is the difference of equations (3-12) and (3-14) and can be written

$$\Delta V = Vth - VS_{M6} = U_T \cdot \ln\left(\frac{{I_{M5}}^n \cdot I_{M6}}{{I_{pold}}^n \cdot I_{pold}} \cdot \left(\frac{S_{Mpol}}{S_{M5}} \right)^n \cdot \frac{S_{Mpol}}{S_{M6}} \right), \tag{3-19}$$

where *S=W/L*. The associated standard deviation is the square root of the sum of equation (3-13) and (3-15)

$$\sigma\Delta V \approx \sqrt{\left(2 + \frac{2}{n^2} \right) \cdot \sigma^2 \Delta V_{TN} + {U_T}^2 \cdot \sigma^2 \left(\frac{I_{off}}{I_{ref}} \right)}. \tag{3-20}$$

Calculation of (3-20) gives a standard deviation of about *12mV*. *ΔV* can then be adjusted by choosing *Ipold* and the geometry of the transistors, in order to have sufficient margin (note that a larger margin, e.g. a 6σ design is preferable since the calculation assumes well matched identical transistors). If *M6* is not in saturation, it is easy to show that the margin is increased, since *VSM6* is somewhat lower.

The upper bound of the comparator is set by the feedback resistor *M7* (whose gate is grounded) that clamps the intermediate output of the comparator at a level close to *Vth* for fast back-switching at the end of the pulse.

3.7.4 Front-end noise calculation

The noise generated by the different elements of the front-end must be calculated to ensure that it will not impede the circuit functioning. Transistors are characterised by two main sources of noise, a thermal one or shot noise one, for transistors operated in strong and weak inversion respectively, modeled as a current source connected between drain and source with a respective power spectral density (PSD) of

$$I_n^2 = 4 \cdot kT \cdot \frac{2}{3} \cdot gm, \tag{3-21}$$

$$I_n^2 = 2 \cdot q \cdot I, \tag{3-22}$$

and a flicker noise also called 1/f noise, since its PSD is inversely proportional to the frequency. Flicker noise is assumed to have negligible influence in the front-end since second order filtering gets rid of all the low frequency components whose power may exceed the one of the other sources of noise. Photodiodes also exhibit shot noise with the same PSD as the transistor in weak inversion. Figure 3-13 shows the source of noise in the front-end up to the comparator input. The noise generated in the comparator is negligible since it is divided by the square of the gain when referred to the input. The noise associated with the transistors

biasing the OTA is neglected since in the band it is cancelled by differentiation.

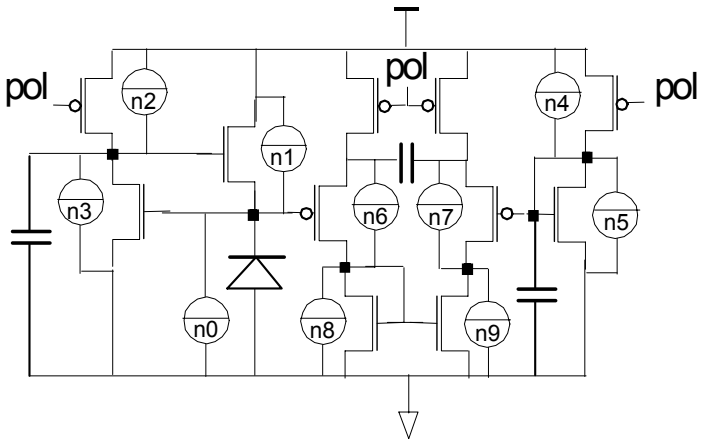

Figure 3-13. Sources of noise in the front-end

By computing the Kirshoff law for each of the three nodes external to the OTA, one can calculate the equivalent voltage noise spectrum at its inputs. The current noise power associated with the input pair of the OTA is first converted into an equivalent voltage source. However, the impedance of the input nodes shapes the noise spectrum. The voltage noise can thus be transformed into a current noise again but connected between the outputs of the two transistors facing the differential pair. Since all the sources of noise are assumed uncorrelated, superposition applies. The equivalent voltage noise spectrum at the right input of the OTA is

$$Vrin_n^2 = \left(I_{n4}^2 + I_{n5}^2 + I_{n7}^2 \cdot \left(\frac{gm_5}{gm_7} \right)^2 \right) \cdot \left| \frac{1}{gm_5 + s \cdot C} \right|^2 , \tag{3-23}$$

and for the left input

$$\begin{aligned} Vlin_n^2 = & \left(I_{n2}^2 + I_{n3}^2 + I_{n6}^2 \cdot \left(\frac{gm_3}{gm_6} \right)^2 \right) \cdot \left| \frac{gm_1}{(n \cdot gm_1 + s \cdot C1) \cdot (gm_3/n + s \cdot Cf)} \right|^2 \\ & + \left(I_{n0}^2 + I_{n1}^2 \right) \cdot \left| \frac{gDS + s \cdot Cf}{(n \cdot gm_1 + s \cdot C1) \cdot (gm_3/n + s \cdot Cf)} \right|^2 \end{aligned} \tag{3-24}$$

It is easy to show that the integration of (3-23) yields an integrated noise power that is favored by a low biasing current which help reduce the contribution of the differential pair. The noise due to *M7* accounts thus in this design, for only 7% (*ID5/ID7*) of the one generated by *M5*, which is independent of the biasing current. The current sources biasing *M3* and *M5* add about 40% of the noise of those two. The transistor delivering the photocurrent produces a noise power, which depends on the

illumination level. At 10% of the sun illumination, the transistor is in moderate inversion and contributes to the same amount of noise as the photodiode. Under one sun, this contribution reduces to 40%.

Now that the spectral distribution of the noise at the input of the OTA is known, calculation of the OTA output current noise distribution is straightforward and yields

$$Iout_n^2 = Vin_n^2 \cdot \left| \frac{2 \cdot s \cdot gm_{6,7} \cdot C_{HP} + s^2 \cdot gm_{6,7} \cdot C_{HP} \cdot \tau_{mir}}{\left(n \cdot gm_{6,7} + 2 \cdot s \cdot C_{HP}\right) \cdot (1 + s \cdot \tau_{mir}) \cdot (1 + s \cdot \tau_{out})} \right|^2, \qquad (3\text{-}25)$$

where the term in absolute value is the OTA transfer function taking into account, the bandwidth of the current mirror $1/\tau_{mir}$ and the output bandwidth of the OTA, $1/\tau_{out}$, which is simply the ratio of the input conductance of the current comparator in the biased state over the node capacitance. The noise introduced by the current mirror of the OTA needs to be superimposed to the one calculated in (3-25). Its distribution is equal to

$$I\ mir_n^2 = \left(I_{n8}^2 + I_{n9}^2\right) \cdot \left| \frac{1}{(1 + s \cdot \tau_{mir}) \cdot (1 + s \cdot \tau_{out})} \right|^2. \qquad (3\text{-}26)$$

The standard deviation of the rms noise current at the output of the OTA is thus

$$\sigma\left(I_{noise}^{rms}\right) = \sqrt{\int_0^\infty \left(Iout_n^2 + I\ mir_n^2\right)}, \qquad (3\text{-}27)$$

if the amplitude distribution of the noise is assumed to be gaussian.

The calculation of (3-27) yields a rms current of about *2nA* for both *Iph=200nA, 2000nA* corresponding to the range of photogenerated current expected during functioning. Among the different source of noise, the one generated by the circuitry biasing the right part of the OTA amounts to 10% of this value, the left counterpart to 8%, the noise introduced by the photocurrent to about 47% and the one due to the current mirror to 35%. Intuitively one would expect the contribution of the photocurrent noise to increase with increasing current. This is true when the transimpedance remains constant, but if a transistor in strong inversion provides the gain, the latter is reduced with increasing currents. Consequently, the integrated voltage noise does not vary if the bandwidth is limited by some other parts of the circuit. The large part introduced by the current mirror of the OTA is due to the poor signal current gain (<1) that is performed in the first two stages.

3.7.5 Expected front-end performance

The calculation of the mismatch and the noise at the input of the comparator have led to a standard deviation of about *2nA* for each of the two main effects that may cause problem in the front-end functioning. Their cumulated effect yields a standard deviation of *2.8nA*, since their variances have to be added. Consequently the reference current of the comparator can be chosen as 3σ to achieve a safe design. In the actual circuit, this current has been set to only *6nA*, because the effect of noise was underestimated at integration time.

The sensitivity of the front-end is set by the reference current of the comparator and the current gain that is achieved at the output of the bandpass OTA. This gain depends on the photogenerated current and is the ratio of the transconductance of the OTA over that of the transistor delivering the photocurrent to the diode. The output current of the OTA is thus varying from about 50% to 16% of the signal current picked up by the photodiode as the photocurrent increases from *200nA* to *2000nA*. The minimum photodiode signal detectable by the front-end varies thus from *12nA* to *36nA* or from 6% to 1.8% of the illumination as the latter increases by a factor of ten. This sensitivity might seem disappointing at first since the circuit is capable of suppressing *80dB* of parasitic signal at *100Hz* and would thus work unaltered if the photocurrent would be as high as $60\mu A$, with 10% of oscillation at *100Hz*. It is partly due to some tradeoffs that were imposed by a low power consumption but it also shows the limitation of the chosen front-end architecture.

3.7.6 Time base

The digitally programmable current controlled oscillator that has been implemented is shown in Figure 3-14. It consists of a 6-bit pseudo-conductance *R-2R* network [1] where logarithmic current division is achieved with transistors leading to a very compact layout and an oscillator where the alternate discharge of two capacitors by the *R-2R* network is controlled by a SR latch connected in a cross-coupled feedback configuration. The *R-2R* network switching is achieved by a 6-bit counter that can be incremented or decremented via remote control. Clocking can thus be linearly adjusted by steps of about *650Hz* from idle to *40kHz*. This oscillator exhibits a strong temperature dependency but it is not of concern since no precision is required in the application.

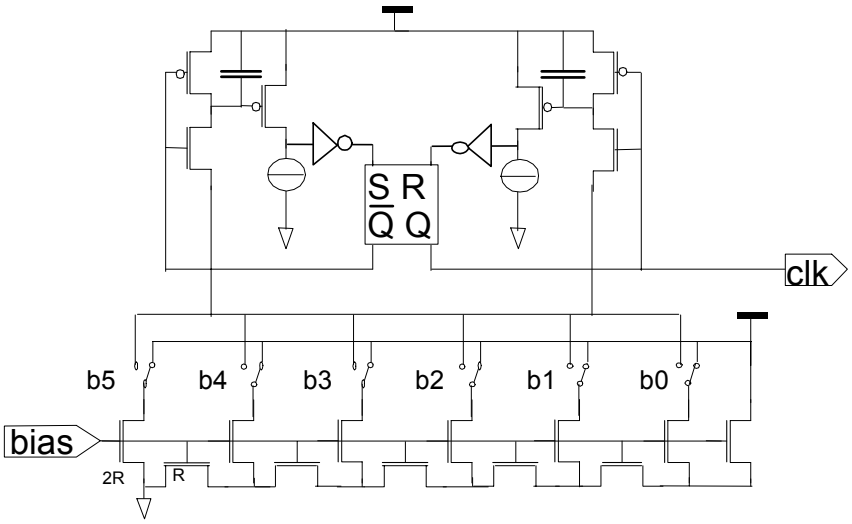

Figure 3-14. Schematics of the variable oscillator controlled digitally by a 6 bit DAC

3.7.7 Actuator driver

The driver that has been implemented in this circuit is based on the typical high-voltage digital driver [2] illustrated in Figure 3-15. It consists of a modified CMOS inverter, where a level shifter is added between the gates of the two transistors and the drains of the transistors are modified to stand the full voltage swing.

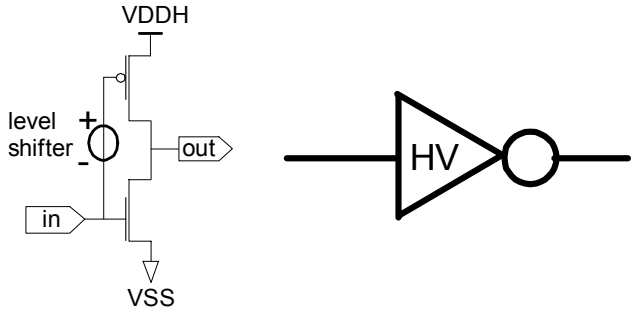

Figure 3-15. Typical high voltage digital driver and the symbolic representation adopted here.

The level shifter is necessary to store the voltage difference between the high and low voltage sources and thus allows the stage to be driven by a low voltage signal. Additionally, it limits the voltage excursion of the PMOS gate within *VDD* referred to the high voltage source so as to avoid degradation due to hot carriers injection in the transistor gate oxide. High voltage CMOS transistors are not mandatory in this design since *VOC* -the open voltage of the solar cell- is never higher than the transistor breakdown voltage specified for the chosen technology (Mietec-C07a) and since the chip is experimental. As mentioned in §3.5.1, the buffers driving the individual nodes of each group of

actuators require a 3-state output, since the actuators must be left floating during part of the cycle. It has also been shown that the high impedance state has to be able to stand voltages as high as *–VOC* and *+2VOC*. Figure 3-16 shows a schematic of the actuator driver that has been designed to meet these requirements.

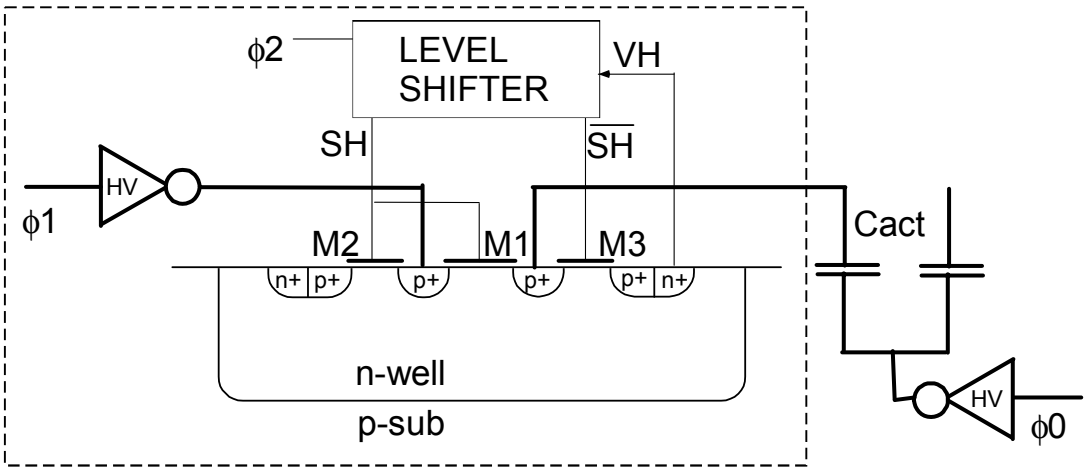

Figure 3-16. Actuator driver with its 3-state buffer (dashed box) capable of handling voltages exceeding the high voltage supply by an equal positive and negative amount.

A single high voltage inverter driven by *ϕ0* switches the common node of all the actuators between *VOC* and *VSS*, while a distinct buffer -enclosed in the dashed box in Figure 3-16- switches each of the six individual nodes of the actuators in a 3-state mode. Transistor *M1* is added in the current path between the high voltage inverter driven by *ϕ1* and the individual actuator node so as to realise both a high-Z and conduction state depending on the potential of its gate. A level shifter with complementary outputs controlled by *ϕ2,* tracks the highest voltage present on any of the two driving terminals of *M1* so as to provide the reference potentials necessary to have *M1* either blocked or conducting. *M2* and *M3* power and provide the high voltage reference to the level shifter while additionally biasing the well of *M1* so as to avoid a parasitic vertical PNP bipolar transistor onset and substrate effects that would alter the conduction of the switch.

In order to charge *Cact* to *VOC*, *ϕ1* should be down, *M1* conducting and the common node grounded. Since the current that the solar cell can supply is very limited, its connection to *Cact* will pull its voltage nearly down to zero. All the level shifters should thus be designed to follow quickly the level of their supply while maintaining their output states. The capacitor *Cact*, so as the voltage on the solar cell start then slewing towards *VOC* at a pace proportional to *ICC* (the short-circuit current of the solar cell). When *VOC* is reached, *ϕ2* can be put high, hence blocking

M1 and *M2* and turning *M3* on. The level shifter is from now on supplied by the charges stored on *Cact* implying that its power requirement should be minimised. Now $\phi 0$ is put down, e.g. to charge another actuator to -*VOC,* hence the common node starts slewing up towards *VOC*. Since the capacitor considered just above already has a potential difference of *VOC*, its other node connected to *M1* goes up to *2VOC*. So do the gate and bulk of *M1* through the level shifter and *M3*, ensuring that *M1* and *M2* remain blocked. If the output of the inverter driven by $\phi 1$ is left high, the drain-bulk junction of *M1* is reverse biased by no more than *VOC* and hence *Cact* can hold most of its charge since the transistor is operated below its breakdown voltage. When *Cact* has to be discharged, the common node should be grounded, $\phi 1$ put high, *M1* and *M2* turned on. *M2* ensures that the source and bulk potential of *M1* are equal, avoiding substrate effect that would prevent *Cact* from discharging through *M1*. To charge *Cact* to -*VOC*, the common node need to be high and the switches left as for the discharge. $\phi 1$ has to stay high as long as the charges want to be left on *Cact*. If the common node goes down in the meantime (e.g. to charge another actuator to *VOC*), the drain of *M1* goes down to *–VOC*. Since the three transistor gates and bulk are all grounded and the drain to bulk voltage of *M1* remains below the breakdown voltage of the transistor, no charge leaks through *M1* towards the capacitor.

3.7.8 Level Shifter design

In high voltage applications, the design of the level shifters should take into account the possible degradation of PMOS transistors due to hot carriers that can be injected into their gate oxide. This degradation can be reduced if the maximum gate to bulk voltage is identical to that of conventional low voltage PMOS transistors. Since the PMOS bulk potential is equal to that of the high voltage source, the gate potential has to be shifted towards this level. Figure 3-17 shows the schematic of a basic static level shifter meeting this requirement and whose outputs quickly track *VDDH* variations, as opposed to dynamic level shifters.

M1 and *M5 (M4, M6)* form a current mirror branch. When *Vin* is high (*VDD*), the currents flowing through *M1* and *M5* are equal and since *M5* is diode connected, the potential drop of the node *SH* is close to *VDD*. However, if *Vin* goes down, *M1* alone is not able to reach *VDDH*. *M2* should be used as a pull-up transistor and two basic mirror cells need to be cross coupled and driven complementarily, so that if *SH* is low, its complementary output is pulled up by *M3* and reciprocally (*M2*).

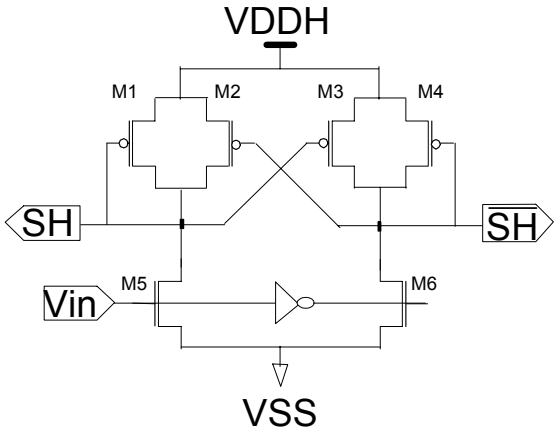

Figure 3-17. Basic static level shifter tracking quick variations of *VDDH*.

However, such a cell has a very high static power consumption, which depends on the driver output current requirement *Idriver*, the high voltage excursion ΔVh (usually *5V*) and the desired switching time τs. The static current can be written

$$I_{M5} = \frac{\Delta Vh \cdot L^2 \cdot I_{driver} \cdot 2 \cdot n}{\mu_p \cdot \left(\Delta Vh - V_{Tp}\right)^2 \cdot \tau_s}, \tag{3-28}$$

where *L* is the length of the driving transistor, *n=1.5,* μp and V_{Tp} the mobility and threshold voltage of the PMOS. The parasitic capacitance of *M1, M2, M3* and *M4* has to be negligible compared to the gate capacitance of the PMOS driving transistor for (3-28) to hold. We see that ΔVh has to be maximised (e.g. *5V*) to lower the static current. In our application however, the current to be switched is really low since *1mA* would discharge the capacitor in a few microseconds, which is satisfactory. If a switching time of $0.5\mu s$ is desired, I_{M5} should be equal to *600nA* according to (3-28). With such a bias, *Cact,* which has to power the level shifter, would be rapidly discharged. Moreover, to create a voltage drop of *5V* on a PMOS and sink only *600nA*, the transistor length should be 250 times its width, meaning that the gate capacitors of *M1* to *M4* are no longer negligible.

One of the easiest ways to circumvent this problem is to use several diode-connected transistors in series. A voltage drop of about V_T can be achieved on each transistor with a very low weak inversion driving current. Substrate effect will also help pull down the voltage if the transistors are placed in the same well. Transistors should be minimally sized in order to reduce their parasitic capacitance. The voltage drop that

can be attained with *k* diode-connected transistors in series and placed in the same well is given by

$$\Delta Vh = \left[n \cdot U_T \cdot \ln\left(\frac{I_{pol}}{2 \cdot n \cdot \beta \cdot U_T^2} \right) + V_{Tp} \right] \cdot \left(1 + n + n^2 + ... + n^{k-1} \right). \qquad (3\text{-}29)$$

We see that with *k=3*, $\Delta Vh \approx 4.75 \cdot V_{Tp}$, which is about 5 volts if the high V_T PMOS is used.

To limit the current flowing through the PMOS, a current source should be placed beneath the NMOS input transistors. This source can be split into a very low static bias and a dynamic edge sensitive larger one, which boosts switching on every transitions of *Vin*. Figure 3-18 shows the schematic of the implemented low static current level shifter.

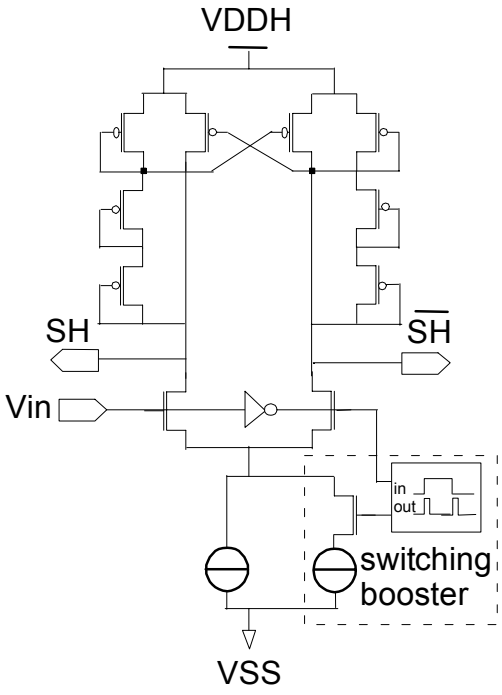

Figure 3-18. Low static current level shifter

Special attention should be paid to the two input NMOS transistors if the level shifter is used in the 3-state buffer part that sees *2·VOC* during part of the driving cycle. In fact, the drain of these two transistors would not be able to stand such a high voltage without being modified. HVNMOS or NDMOS (high voltage NMOS) can very easily be designed in a standard technology by modifying the drain region of the transistor [3]. The reason limiting the drain voltage the transistor can stand is the n+ p-sub junction breakdown under its gate. An efficient way to increase this breakdown is to place the drain contact inside a lightly doped region

such as in the n-well, since the n-well p-sub junction of the PMOS nearly holds a hundred of volts. The geometry of the gate also has to be modified in order to spread the electric field distribution at the corner of the n-well diffusion. Lowering the doping of the drain will in turn increase its resistivity, something not desirable when driving high current, but without any consequence here since these transistors only see small current.

3.7.9 Current reference

The internal polarisation circuit that generates the proper bias for analog blocks is made of a degenerated current mirror loop. The reference current source is proportional to the absolute temperature (PTAT) and is set by the value of a resistor and the geometry of the transistors. Figure 3-19 shows the schematic of the circuit generating the biases.

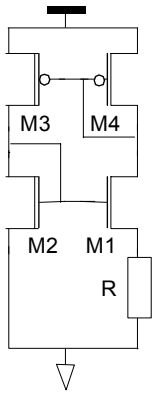

Figure 3-19. Simplified schematic of the polarisation block generating on-chip biases.

Transistors *M1* to *M4* impose the source potential of *M1* while the resistor sets the reference current. If *M1, M2* are in weak inversion, it yields

$$V_S = \ln\left(\frac{S1 \cdot S3}{S2 \cdot S4}\right) \cdot U_T, \tag{3-30}$$

$$I_{REF} = \frac{V_S}{R}. \tag{3-31}$$

The transistor mismatch and parameter spreading (mainly resistor sheet resistance variation) limit the precision of this current reference. Its variance can be written

$$\sigma^2\left(\frac{\Delta I}{I_{REF}}\right) = \sigma^2\left(\frac{\Delta V_S}{V_S}\right) + \sigma^2\left(\frac{\Delta R}{R}\right), \tag{3-32}$$

where $\sigma^2(\Delta Vs)$ is

$$\sigma^2(\Delta V_S) = U_T^2 \cdot \sum_{i=1..4} \sigma^2\left(\frac{\Delta\beta}{\beta_i}\right) + \frac{1}{n^2} \cdot \sum_{i=1..2} \sigma^2(\Delta V_{Ti}) + U_T^2 \cdot \frac{2 \cdot \beta_4}{n \cdot I_{REF}} \sum_{i=3..4} \sigma^2(\Delta V_{Ti}),$$

(3-33)

if *M3* and *M4* are in strong inversion, so as to minimise their contribution to the total mismatch.

The resistor potential, *Vs* should be chosen a few *UT* to guarantee a certain precision since calculation of (3-33) gives a standard deviation of about *2mV*. For efficient power consumption management, *M3* and *M4* can be identical (same current flowing in the two branches) thus meaning that *M1* has to be larger than *M2*. A good matching of these two transistors is essential, since they are operated in weak inversion. The gate potential of *M4* (which is in strong inversion) can be used to provide current source where needed in the analog part of the circuit. Current sink can be obtained with another branch, where the mirroring NMOS is operated in strong inversion as well. Capacitors can be added to stabilise the polarisation and prevent ringing, which may occur due to the low conductance of the input mirror (low power) and if some output mirror drains experience fast variations (e.g. in simple current comparators).

3.8 Measurements

3.8.1 Preliminary

In a first step, the IC is characterised with conventional power supplies so as to measure its power consumption and its high voltage driving capability. Though the IC input and outputs reduce to a photodiode and the high voltage drivers during its intended operation mode, additional testing capabilities have been included in the design. The different photodiodes that have been integrated can be individually characterised and coupled to the circuit at the expense of up to three intrachip additional bonds. In order to facilitate the measurement of the circuit, the input of a current mirror can be driven externally to emulate the photogenerated current and simulate different illumination and signal conditions. This interface was however not designed carefully enough and only a voltage driving mode can generate an internal current having the required bandwidth. The transimpedance amplifier sensitivity can thus not be measured accurately since the voltage difference that a function generator can achieve corresponds to a relatively large current difference. Additional measurements can be performed on individual

blocks by accessing or setting some internal nodes of the circuit, such as to characterise the adaptive discriminator, the oscillator, the polarisation circuit or the high voltage driver. The whole circuit functionality can then be verified with the by-pass photocurrent before the best diode signal is fed into the circuit. Finally, testing with the solar cell can validate the autonomous approach. Figure 3-20 shows a photograph of the fabricated IC.

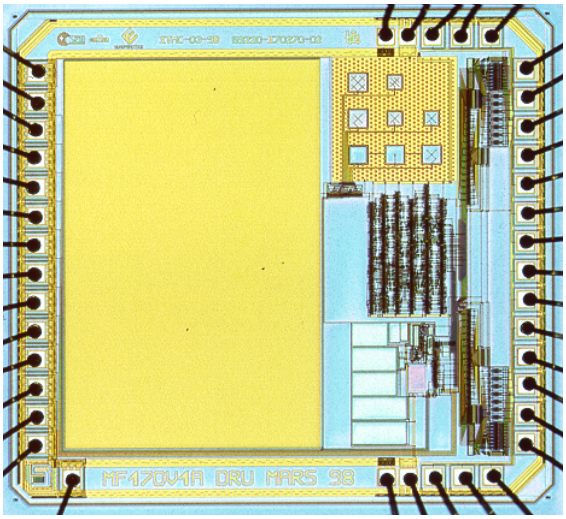

Figure 3-20. Photograph of the fabricated IC (size is 2.8x3mm²)

3.8.2 Measuring set-up

A few ICs have been packaged and mounted on a veroboard containing a FPGA that generates the proper excitatory signals. An electrometer is used to measure the overall response of the photodiodes. Current and voltage sources together with a function generator and an oscilloscope are used to verify the circuit functionality. The measured signals are then acquired with a PC. Figure 3-21 shows a schematic view of the measuring set-up.

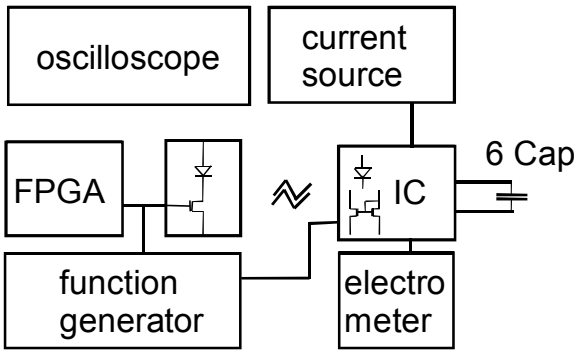

Figure 3-21. Measuring set-up for the integrated circuit characterisation.

3.8.3 Transimpedance photoamplifier and adaptive discriminator measurement

The functionality of the transimpedance photoamplifier and the adaptive discriminator has been verified with a frequency generator triggered by the output signal of the FPGA. The generator reproduces the FPGA logical signals, but at voltages that can be set on the generator. It is thus possible to emulate the photodiode although the current pulses are pretty strong and not typical of IR ones, since the minimum voltage difference that can be applied by the generator is *200mV*. It would be possible to bias the input current mirror with a steady current and use a capacitive divider to superimpose a fraction of the generator signal to better emulate the optical pulses, but dividing ratio of *250* to *800* would be required to control the current pulses in the *nA* range as the steady current is increased from *200nA* to *2000nA*.

Since the IC could be remotely operated successfully at a distance of about *40cm* with a few emitting diodes, the sensitivity measurement is not that important anyway. Figure 3-22 shows a measurement of the output of the pulse shaping circuit together with that of the decision circuit for a short sequence of pulses emitted by the photodiode. The bit value is latched on each falling edge of the pulse shaping circuit. After the end of a pulse, the decision circuit goes high and bases its decision on the elapsed time before the next pulse is detected. The decision boundary is clearly visible in Figure 3-22 at approximately two third of the time encoding a zero as expected.

Figure 3-23 shows the measurement of a complete instruction picked up optically by the front-end and decoded by the discriminator circuit. The instruction is made of four bytes with additional zero padding that avoids ambiguities. The instruction is composed of an ID, which addresses selectively different chips, two instructions encoding the direction of motion (e.g. backward and left) or the increment/decrement of the speed, and eventually an end of communication (EOC) byte that puts the system back to the identification mode. The total instruction is approximately *900µs* long. The instruction of Figure 3-23 is decoded as 000-11110100-0-11101001-0-11100110-0-11100110-0 and means: CHIP #4, INC, EOC, EOC and thus increments the counter value of the chips that are given the number ‘4’ tag by one.

The adaptive discriminator takes about one instruction at power-up or after a long interruption to be tuned to the mean interpulse time duration. After an interruption of a few seconds, a few pulses are mistaken due to the erasing effect of the leakage current on the memorizing capacitor.

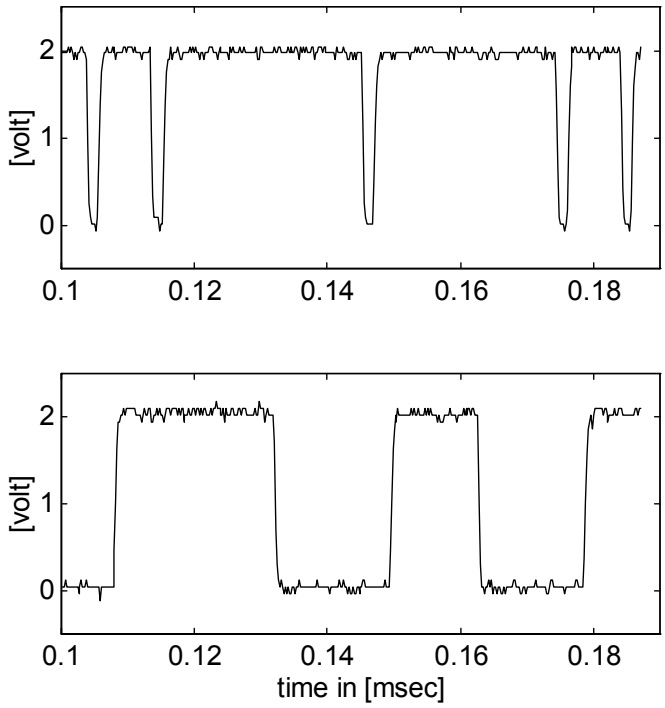

Figure 3-22. Measurement of the pulse shaping (top) and decoding circuit (bottom) for a few 3µs pulses emitted optically. The bit value is read on the incoming edge of each pulse and the word represented in the figure is thus '01001'.

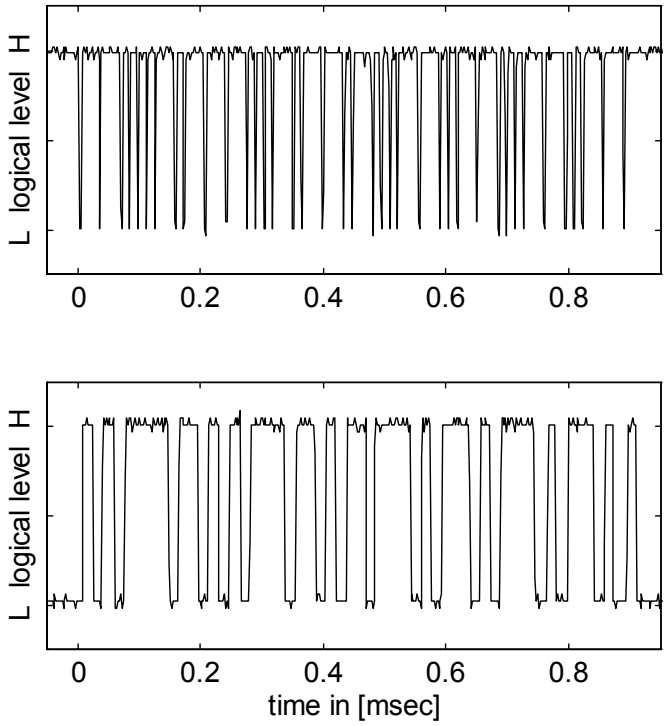

Figure 3-23. Pulse shaping and decoding of a complete instruction transmitted optically.

3.8.4 Measurement of the high voltage driver and sequencer

In order to characterise the high voltage driver, six external capacitors have been connected to the corresponding outputs of the driver to emulate the behavior of the piezoelectric bimorph and a current source, whose maximum output voltage can be arbitrarily limited, is used to simulate the high voltage solar cell. The sequencer is then initiated through a valid command before a measurement can be made. Figure 3-24 shows a measurement of the voltages applied to one of the capacitors at about *1kHz* and at a *VDDH* of *8V*. The top plot shows the common node voltage, which is continuously switched between *VDDH* and *VSS* so as to charge an actuator to the correct polarity. The second plot shows the output of one of the high-voltage 3-state buffer, which alternates between high and low impedance states so that the capacitor can hold its charges or be charged to *VDDH* or *–VDDH*. The difference of these two signals, which is shown on the bottom part of the plot, is the actual voltage applied to the capacitor. One can see that the switches can handle voltages twice as high as *VDDH* and of opposite polarity or *-VDDH* in a conventional *5V* technology. The maximum *VDDH* is thus limited by the breakdown voltage of the drain to bulk junction of the conventional transistors, which is approximately *10V*.

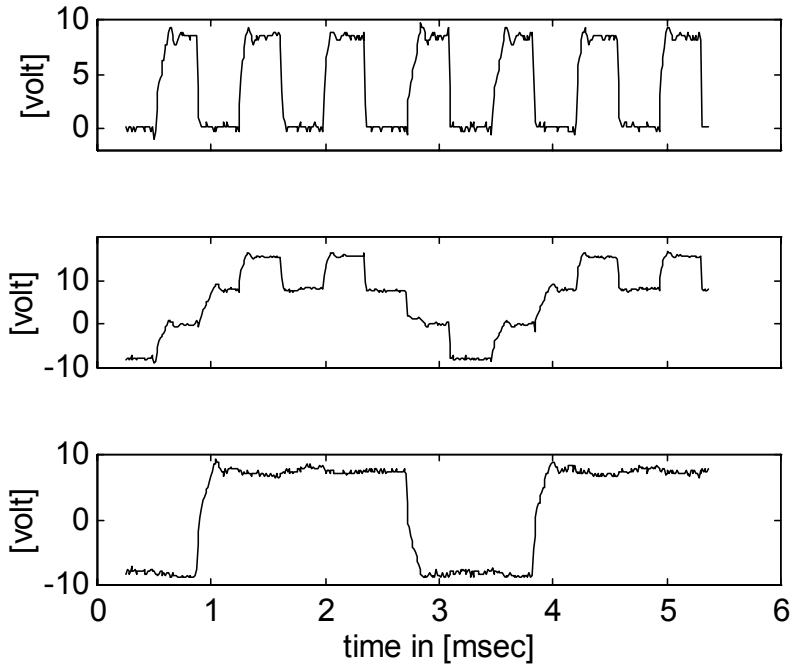

Figure 3-24. Measurements showing from top to bottom, the sequence of voltages applied to the common node, the output of one of the high voltage 3-state buffer and the voltages seen by the corresponding capacitor at 1kHz and 8V.

The complete behavior of the high voltage driver is plotted in Figure 3-25, which shows the relative phases and voltages of the six output nodes of the driver for the forward straight direction. A comparison between Figure 3-25, Figure 3-9 and Table 3-2 allows to verify the correctness of the driving sequence. The relative phase difference between these six signals will depend on the chosen direction of motion and is a very simple way to check the functionality of the decoder and sequencer circuit blocks. The phase diagram for every direction has been constructed with a similar measurement and compared with that of Table 3-2 to validate the design of these parts of the circuit.

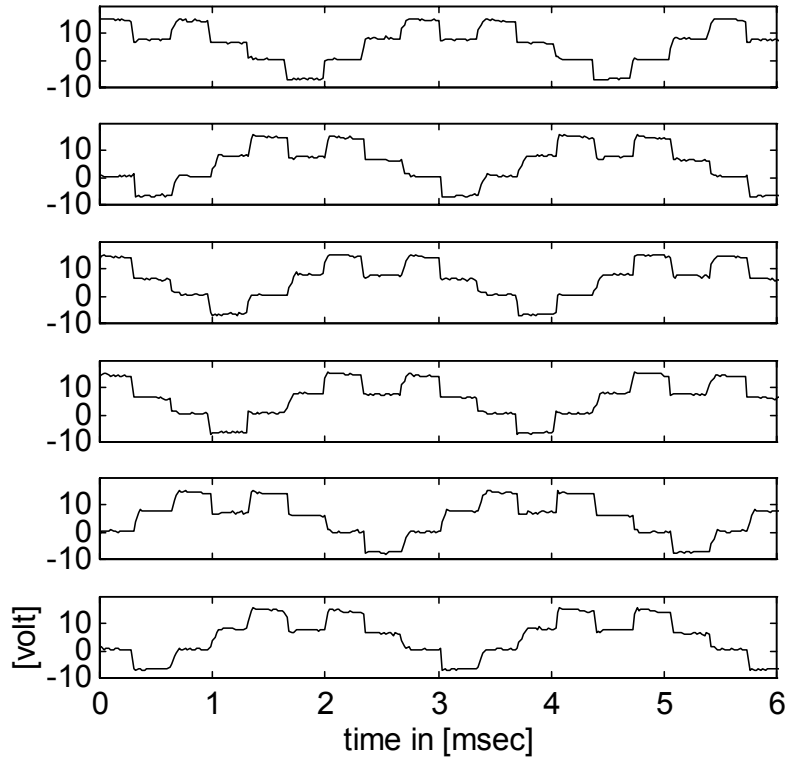

Figure 3-25. Voltages and relative phases of the driver six outputs during a few cycles in the forward front direction (output one to six from top to bottom).

3.8.5 Oscillator measurement

The pace of the current controlled oscillator can be set by a 6-bit counter/decounter that switches a R-2R network of pseudo-conductance transistors. Measurement of the oscillator pace gives steps of about 760Hz from idle to a maximum frequency of 44kHz, in good agreement with simulations. Figure 3-26 shows the oscillator frequency for the three LSBs (least significant bits) of the counter. The frequency steps

controlled by the pseudo-conductance network are fairly constant even if one increment corresponds to a *0.5nA* current difference.

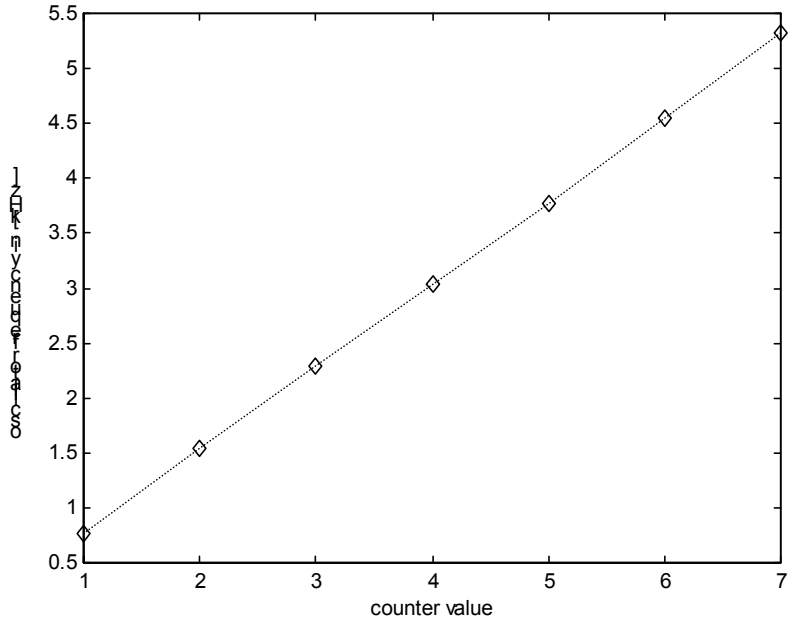

Figure 3-26. Oscillating frequency versus counter value for the 3 LSB of the counter

3.9 Power consumption

The total static power consumption of the chip in the dark remains below *1μA* at *2V*. If the IC is carefully covered with an adhesive tape outside the photodiode area, it can be operated under a strong illumination without increasing the current consumption beyond a few microamperes. The total low voltage power consumption when the IC is maximally solicited (during communication, at maximum oscillating frequency, and under strong illumination) is about *10μW*.

3.10 Conclusions

The functionality of a low-power circuit designed in a standard *5V* technology and capable of driving a piezoelectric mobile microactuator array to *±10V* in a bipolar way according to a direction and at a pace that can be IR remotely controlled was demonstrated. The circuit power consumption remains below *10μW* at *2V* under a strong background illumination when all the functions are activated simultaneously in their most power-demanding state. Infrared communication at *50kbit/s* is unaffected by the high voltage switching from *–10V to +20V* that occurs in the driver at up to *44kHz*, the maximum driver frequency. The sensitivity of the front-end, limited by noise and mismatch could not be measured due to a badly designed ASIC interface but can be obtained

from simulations. It varies from *–12dB* to *-17dB* with respect to the steady light power as it increases from 10% to 100% of one sun illumination or *1000W/m²*. The *5dB* gain in the latter case is due to strong inversion that increases the gain at higher photocurrent levels. The rejection of network induced residual light power modulation at *100Hz* is in the range of *40dB* with respect to signals in the band, indicating that filtering outperforms by far the limitations introduced by noise and mismatch. It is partly due to the trade-off that had to be made to meet the low-power low-voltage challenge but it also shows the limitation of the chosen front-end architecture.

The performances of the high voltage driver are astonishing since only a small fraction of the energy that is coupled to the actuators is lost in the level-shifter and the switches. The losses of the latter are minimised due to the choice of a current driving mode that keep the switches in conduction, rather than saturation, minimising the voltage drop.

3.11 References

[1]. E.A. Vittoz, X. Arreguit, “Linear Networks Based on Transistors”, Electronics Letters, Vol. 29, No. 3, pp. 297-298, Feb. 1993.

[2]. M.J. Declercq, M. Shubert, F. Clement, “5V-to-75V CMOS Output Interface Circuits”, IEEE Int. Solid-State Circuit Conference, 1993, pp. 162-163.

[3]. M.J. Declercq, F. Clement, M. Shubert, “Design and optimization of high voltage CMOS devices compatible with a standard 5V CMOS technology”, CICC proceedings, paper 24.6, May 1993.

4. A miniature powering solar cell

4.1 Preliminary

Powering the IC and the microactuator array is not an easy task since at least *1.8V* is needed for the IC and a high voltage of about *10V* is required to drive the actuators, which are equivalent to a capacitive load. One should recall that the weight of the power source is critical since the load that the microsystem can carry is very limited. A button battery could provide a voltage of about a volt, but the packaging would be way too heavy. Thin film accumulators are currently under development and provide an output voltage of about *2V* [1]. They might be seen as a promising candidate for this application, but their development is not yet mature enough to realise an accumulator of half a cm^2. Recent developments in amorphous silicon solar cells enable the deposition of triple NIP structures delivering an open voltage of *2V* to *2.5V* on many substrates, such as glass, inox or polyimide [2]. This solution is by far the best candidate since it offers an energy transducer and not only a limited amount of energy. Additionally the output voltage of the cell is readily compatible with the voltage required by the IC. In order to obtain the high voltage required by the actuators, not many solutions are applicable. DCDC converters usually require an external inductor for good efficiency. This inductor complicates the assembly and might be too heavy and bulky for the microsystem. On chip charge pumps require low parasitic capacitors and an output buffer capacitor much bigger than that of the actuator for efficient energy conversion. Although this solution would still be conceivable, it has not been retained since the technology that has been chosen for its high voltage compatibility has capacitors with very high substrate coupling. The solution that has finally been retained is based on lithography to put several triple junction solar cells in series.

4.2 Solar cells as miniature power supplies

The low voltage supply, powering all the logic and analog blocks, provides an open circuit voltage of about *2V* to *2.5V*. The maximum current that can be issued by the source is however limited to a few microamperes above which its voltage collapses rapidly. The power supply can be modeled with three diodes in series and a current source in parallel. To transform the solar cell into a better voltage source, a capacitor of several mm^2 (*nF* range) has been integrated on the ASIC and connected between *VDD* and *VSS* to stabilise the voltage under high peak

current consuming transients. Figure 4-1 shows the model of the low voltage power source.

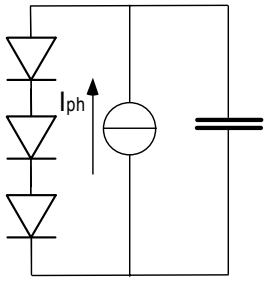

Figure 4-1. Low voltage power supply consisting of a stack of three photodiode and a decoupling capacitor.

The high voltage power source is made of four low voltage solar cells in series. Its behaviour is better described by a constant current source saturating at about *8V* to *10V* where the current starts being directly by-passed through the diodes that become forward biased.

The power that can be delivered by a photodiode strongly depends on its biasing. Under resistive load, the load has to be very carefully adapted to the level of illumination so as to maximise the solar cell efficiency as depicted in Figure 4-2. The power delivered by the photodiode is the rectangle area that can be drawn from the biasing point, where the I-V characteristic of the photodiode intersects the load conductance I-V curve. If the illumination changes, the photodiode I-V curve is simply shifted upward or downward. When the load is left unchanged, one can see that the effective power delivered to the load might be quite away from the optimum.

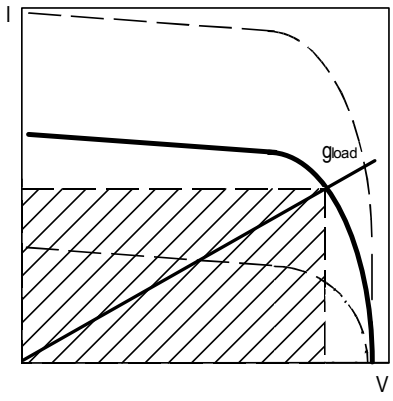

Figure 4-2. Illustration showing the influence of the illumination level on the power delivered by a solar cell to a constant resistive load.

In our case however, the load is capacitive and hence requires dynamic powering. Two distinct configurations, which are depicted in Figure 4-3,

are possible: the voltage or the current mode. In the voltage mode, a big capacitor serving as a charge tank and voltage reference ensures that the solar cell always works at a rather high voltage, close to its optimum, as long as the mean current drawn from the tank does not exceed the photogenerated current. When the tank is connected to the load, charge redistribution takes place and the load is rapidly charged nearly up to the tank voltage. It is easy to show that regardless of the switch resistivity, half of the energy that is removed from the tank is dissipated in the switch. In order to prevent this energy waste, the load should be charged by a source whose voltage increases not faster than that of the capacitor of the load so as to generate a negligible voltage drop across the switch. This condition can easily be met if the solar cell is connected directly to the load and hence works as a current source. Consequently, the load capacitor will charge almost linearly, at a rate depending on the photogenerated current until it eventually reaches *VOC*, the open voltage of the solar cell. Of course, the instantaneous power drawn from the photodiode is greatly varying during the charge, being really low at low voltage. But one can show that for a charge at constant current up to a given potential, the energy delivered by the source is half of what would be achievable if the cell were biased at the upper potential. Since half the energy is lost when connecting a capacitor to a voltage source, the overall energy needed to charge the actuator is the same. In the real case however, the charging current is not constant over the whole voltage range, being even always higher than the current at the optimum biasing point due to the non zero conductance of the solar cell. Consequently, the current source solution is more efficient and simpler since it does not require any area-consuming buffer capacitor.

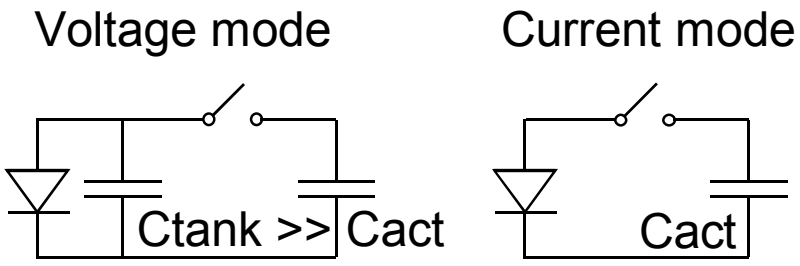

Figure 4-3. Illustration showing how a solar cell can drive a capacitive load.

4.3 Power requirement

The microactuator array needs to be powered at approximately *10V* at frequencies up to a few *kHz*. During a cycle, the six groups of actuators, each modeled by a capacitor of a few hundreds of picofarads, *Cact*, have to be charged two times at opposite polarities. Altogether, a capacitor of

12·Cact must be charged to *10V*, meaning that the required photogenerated current is

$$Iph \geq 12 \cdot Cact \cdot \Delta V \cdot f \,, \tag{4-1}$$

which is between *100μA* for ZnO and *200-300μA* for AlN at *f=10kHz*.

Additionally, the power supply of the IC should deliver a current of a few microamperes at *2V* to properly bias the analog blocks and provide sufficient transient driving current for the digital blocks and the oscillator.

4.4 Energy conversion and area limitation

Measurement of triple pin test cells realized by Fischer and al. [4] shows a power to mean current conversion of *3mA/cm²* under one sun illumination (AM 1.5). At one fourth and one eighth of this illumination, the conversion is respectively *880μA/cm²* and *450μA/cm²*, showing a slight improvement.

The total solar cell area is limited to about *0.5cm²* so as to fit on the microactuator array. Hence, about *300μA* can be generated for the high voltage supply under AM 1.5, since four cells and the IC supply have to stand on this area.

4.5 Technological and design considerations

The solar cell that has been designed and fabricated is based on a triple 'NIP' stack of amorphous silicon junction. There are numerous advantages in choosing amorphous rather than monocrystalline silicon. The first one is the required thickness of the active layers which can be reduced by about two orders of magnitude due to the higher absorption coefficient of a-Si:H. Consequently, the bulky and costly monocrystalline substrate can be replaced by numerous kind of lighter and thinner substrates, such as glass, inox or polyimide and one could even consider depositing the solar cell directly on top of the micromachined device or above IC as a post-processing step, since the deposition temperature is compatible with underlying metal films. Second, the triple pin structure produces an output voltage of about 2 volts, which is sufficient to design low power analog blocks without requiring DC-DC converters. Third, since the photodiode can be deposited on an insulating substrate, it is very easy to put lithographically several cells in series so as to generate a high voltage source, such as in [3], where a high voltage power supply for electrostatic MEMS has been demonstrated.

In our case, four cells need to be put in series in order to generate the voltage required to drive the actuators. The nominal voltage will be 8 volts under one tenth of the solar illumination and will get closer to 10V under sunny conditions. The process needed to realize such cells can be done with two masks and a YAG laser etch step. First, a metal layer is deposited by evaporation on an insulating substrate and structured to define the bottom electrodes of the four triple NIP structures. Then the different a-Si:H layers are deposited over the whole substrate in a single run. The YAG laser etches this layer where contacts between the top and bottom electrodes need to be open. The last step is the deposition and patterning of a transparent conductive oxide (TCO) that defines the top electrodes. Figure 4-4 shows a cross-section of the high voltage solar cell.

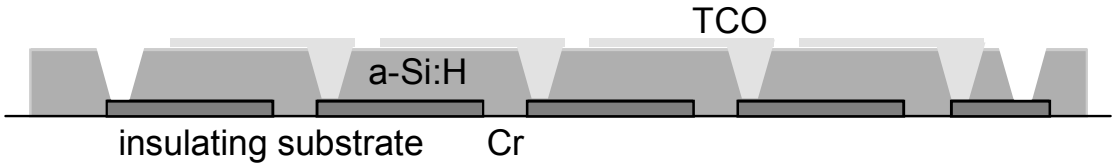

Figure 4-4. Drawing of the cross-section of a high voltage solar cell realized with junctions interconnected in series.

In order to simplify the laser etch step, all the contacts have to be made on a line. The YAG laser then removes the a-Si:H along the whole line thus easing the command of the X-Y table. Care should be taken in the design to avoid short-circuits due to misalignment between the two masks and the laser etch. Figure 4-5 shows a drawing of the top view of a possible solar cell layout.

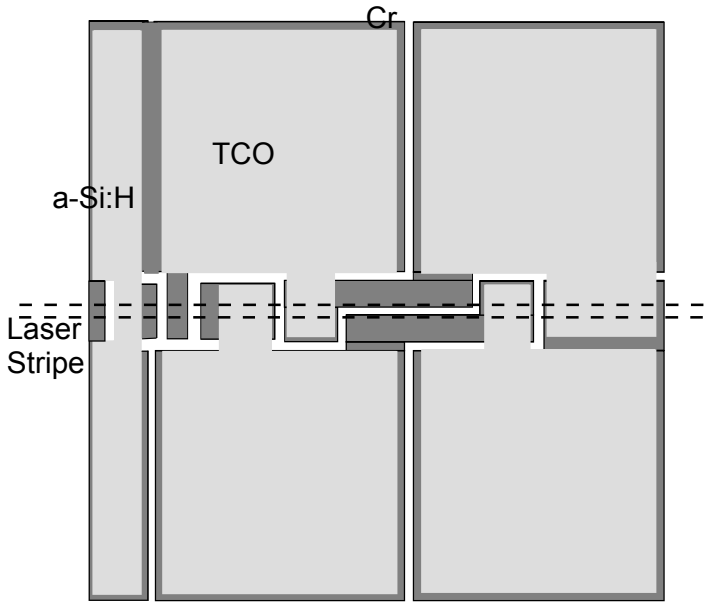

Figure 4-5. Example of solar cell layout with a single cell to power the IC and four cells interconnected in series to drive the microactuator array.

The area of the cells in series should be equal, since only a constant photocurrent can flow throughout the whole stack. In addition to the four cells in series, another single cell provides the power needed by the IC. The three bonding pads of the solar cell, -both supplies share a common ground-, should be made of about *500nm* thick metal and placed relatively close to each other to facilitate bonding.

Since the a-Si:H is left almost unetched, lateral conductance between layers at different potentials will reduce the current that can effectively be drawn from the solar cell. This is of great concern here, since the current level is really low, the voltage quite high and the process and bonding requirements favors long borders at different potentials. Spacing between any two electrodes should thus be adapted carefully according to their potential difference to ensure that the by-passed current remains negligible compared to the output current available.

4.6 Fabrication

In the first deposition run, a single NIP junction was deposited on a polyimide substrate so as to verify that the individual cells could effectively be put in series. A voltage of *2.5V* could easily be generated under the light of a microscope, corresponding to a VOC of about *0.6V* per cell. These promising results initiated the deposition of the triple NIP stack, which turned out very disappointing. The I-V curve measurement showed a device dominated by lateral conductance, since the curve was exiting the fourth quadrant -the zone where energy is produced- shortly above *2V*. Was the conductivity of the different layers of the a-Si:H fatal at such high voltage and low current levels? Maybe partially but not completely, since a similar device consisting of four cells in series and designed for credit card applications could be demonstrated shortly afterwards at the IMT. The only significant difference between the two designs is related to the laser scribe and cell geometry. In the credit card cells, the four diodes are arranged side by side and a different scribing line is used between each pair of diodes. The device reported here has a single scribing line crossing the four diodes and hence areas at different potentials. Laser induced recrystallisation of the a-Si:H layers at the border of the etched line is thus probably yielding a stripe of material with much greater conductivity. Since this stripe connects the different diodes in single scribed design, an important shunt conductance prevents the high voltage operation of the cells. The amorphous silicon layer could hopefully be etched away by using the top electrode as a mask so as to insulate completely the different diodes laterally.

The use of a polyimide substrate showed however several major drawbacks. Bonding a sample turned out to be impossible due to the lack of substrate firmness. The lithographic and deposition steps were requiring frequent gluing and ungluing of the substrate, which was complicated by the substrate curling due to the tensile stress present in the bottom electrode material. Using $50\mu m$ thick inox substrate, insulated by a CVD oxide, greatly simplified the processing since the substrate was stiff enough to withstand spinning, lithography, thick tensile metal film deposition and bonding.

Another problem which was encountered very early with the triple junction stack, was the difficulty to scribe selectively the a-Si:H layer with the YAG laser without damaging the underlying metal film. Repeated disappointing results eventually led to the replacement of the laser scribing by an additional lithographic and dry etching step.

Figure 4-6 shows a photograph of the fabricated high voltage solar cell

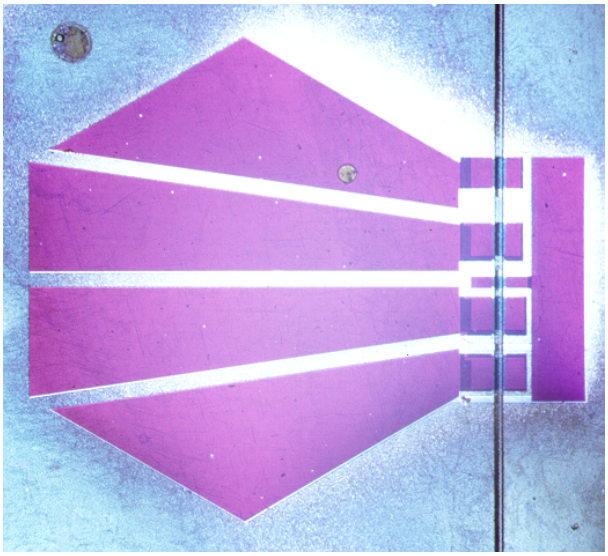

Figure 4-6. Photograph of the fabricated high voltage solar cell

4.7 Individual device separation

The separation of individual solar cell from the substrate can be done in different ways. While laser cutting, wet or dry etching should be possible depending on the substrate, careful scissors cutting proved the simplest and left working devices. This gross method was adequate to prepare a few samples for characterisation.

The most appropriate separation method however, when considering batch fabrication, would be to dry or wet etch the substrate via an additional lithographic step used to cover the cells area. An optimum

alignment could thus be achieved together with a high resolution. Taking thin silicon wafers (a few tens of microns) as a substrate seems potentially very interesting, since individual devices can be released in a few minutes with DRIE tools.

4.8 Power supply characterisation

The characterisation of the different solar cells was first made under a probe station with a semiconductor parameter analyser. I-V curves showed that about 20% of the high voltage cells had an open circuit voltage of about *9V*. In others, one, two, three or even all the junctions were shorted yielding an open circuit voltage of *6-7V, 4-5V, 2-2.5V* or *1V* respectively. The exact reason for the shorts remains unclear but they are probably due to pinholes in the a-Si:H, a consequence of the unclean deposition and processing environment or the initial inox substrate roughness. In addition, the cells were highly sensitive to manipulation, especially to mechanical contacts on the cell side, since a slight pressure (e.g. during a gluing step) resulted in new shorts. The shorts could a few times be eliminated by reverse biasing the junction with a current sufficient to vapor the pinhole, while many times no improvements could be seen. A few good samples were glued and bonded with great care on pieces of PCB to allow their characterisation under a solar simulator that can reproduce the sun illumination spectrum. Figure 4-7 shows the I-V curve of a high voltage solar cell having a single cell area of *0.08cm²* under different illumination conditions.

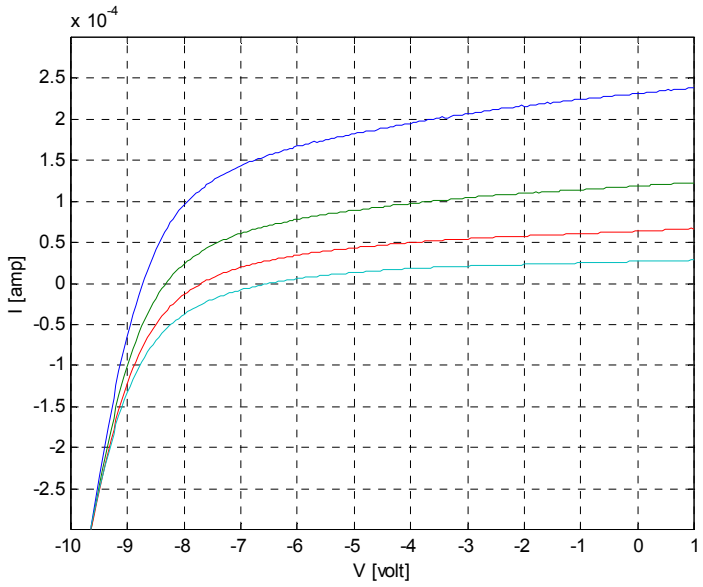

Figure 4-7. I-V measurements of a high voltage solar cell under different illumination conditions: AM1.5, one half, one fourth and one eighth of AM1.5 from top to bottom.

The abnormal decrease of VOC with decreasing light intensity is probably due to a shunt conductance. An average current density of $3mA/cm^2$ under AM1.5 comparable with previous work [3,4] was measured.

4.9 Conclusions

The high voltage solar cell could successfully be fabricated on $50\mu m$ thick inox substrates with a yield approaching 20%. Measurements showed expected performances in good agreements with earlier published work. Fabrication on polyimide foils turned out very inconvenient due to the lack of substrate firmness. The process that could be developed deviated considerably from the one that was devised initially. First, insulating laterally the different stacks from each other proved mandatory at such high voltages and low current levels, since the lateral conductance of all the doped layers was impeding the device functioning. The laser scribing also proved difficult to master with the triple junction stack and was eventually replaced by a lithographic and dry etching step. A better process would pattern the a-Si:H layer in one step, opening contact to the bottom electrode and insulating stacks from each other simultaneously. Taking individual dye separation into account, a four masks all-lithographic process done for example on very thin silicon wafers would result in an improved alignment capability, lead to a denser implementation favoring solar cell area and allow a very quick and easy separation of the individual devices via a final DRIE etch step.

4.10 References

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[2]. S. Guha et al., “A Novel Design for Amorphous Silicon Alloy Solar Cells,” in Proc. 20th IEEE Photovoltaic Specialists Conf., 1988, pp. 79-84.

[3]. J. Lee, Z. Chen, M. Allen, “A Miniaturized High-Voltage Solar Cell Array as an Electrostatic MEMS Power Supply,” in J. of Microelectromechanical Systems, Vol. 4, No. 3, Sept 95.

[4]. D. Fischer et al., Measurement of triple stack NIP junctions, IMT, University of Neuchâtel.

5. The autonomous mobile microsystem

5.1 Microsystem assembly

The assembly of the three components making up the microsystem is somewhat complicated by the fact that the resulting device is mobile. After the three components have been glued together, a temporary immobilisation of the whole structure is however necessary to realise the electrical interconnections between them. Figure 5-1 shows a schematic representation of the assembled and bonded microsystem.

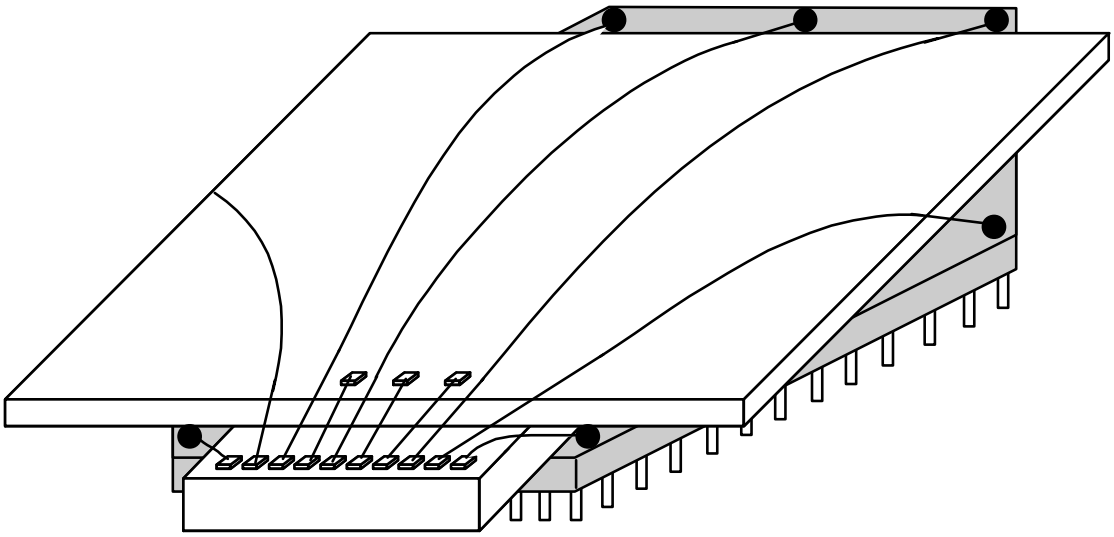

Figure 5-1. Schematic representation of the assembled microsystem consisting of a microactuator array, an integrated circuit and a high voltage solar cell interconnected electrically through wire-bonds.

A holder, capable of clamping the microactuator array mechanically has been designed to provide a platform for gluing and bonding the different components together. Figure 5-2 shows a schematic cross-section of the assembly setup where the vertical arrangement of the microactuator array (MA), the integrated circuit (IC) and the solar cell (SC) can be seen. The microactuator array is placed on top of a holder that is drilled in its center to accommodate the fragile legs and is clamped laterally between a spring structure. The piece that clamps the array on one side serves as a flat reference surface to position the IC slightly above the array and offer a stiff support for bonding. The gluing of the three components can then be performed before the different bonds between the circuit / solar cell and circuit / actuator array are done.

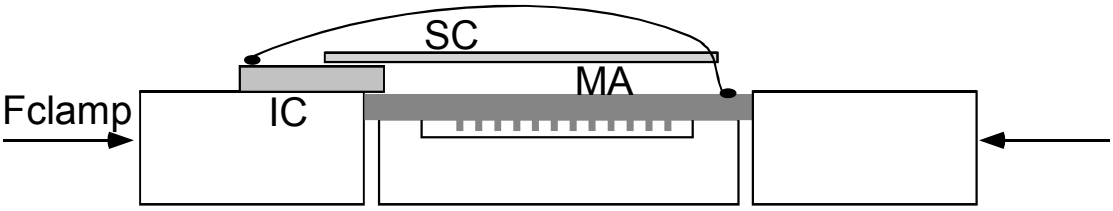

Figure 5-2. Schematic cross-section illustrating the assembly and bonding setup.

Figure 5-3 shows a picture of the assembled microsystem made with non-working components to validate the assembly approach.

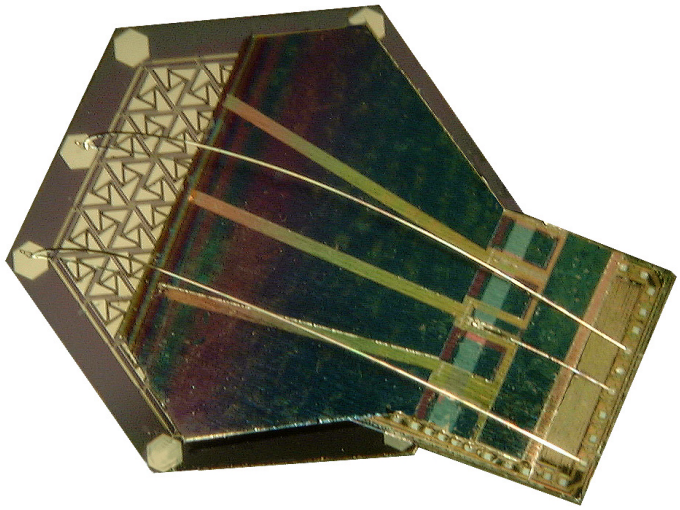

Figure 5-3. Picture of an assembled microsystem made of non-working components

5.2 Conclusions

The impossibility of getting a fully functional actuator array has so far prevented the demonstration of the autonomous millipede walking microsystem. Nevertheless, an assembly concept could successfully be validated with non-functional devices indicating the feasibility of an approach based on hybrid integration.

6. General conclusions and outlooks

6.1 Recapitulation

The work that has been achieved in the frame of this Ph.D. dissertation nearly demonstrated the possibility of realizing a remotely controlled wireless autonomous millipede microsystem capable of locomotion. The components of the microsystem consist of an application specific integrated circuit (ASIC) coordinating the energy distribution, a microfabricated piezoelectric actuator array generating the physical motion and a high voltage solar cell powering the whole system. The system is merging state of the art technologies in low power mixed-mode circuit design, in micromachining focused on deep reactive ion etching and piezoelectric thin film transducer and in the fabrication of amorphous silicon solar cell. All the three components can be batch processed and potentially produced in large quantities at low cost.

There are many innovative concepts at the system and component levels. The microsystem, having an area of about $0.5cm^2$, for a height of less than *1mm* would be the first demonstrator of a batch-fabricated autonomous microrobot that can be remotely controlled and move in different directions with an unlimited range of travel. Individual actuators have three active degrees of freedom and can achieve three-axial high amplitudes of motions (several micrometers) due to the levering effect of wafer-through etched legs. The mechanical and electrical interfaces are located on opposite sides of the wafer, greatly simplifying assembly and enabling a multiple chip approach.

The ultimate goal of this work, demonstrate the robot functioning, has so far not yet been reached due to the impossibility of getting a fully functional actuator array as a consequence of different problems encountered with the platinum bottom electrode required for highly oriented piezoelectric aluminum nitride growth. However, the characterisation of individual actuators has shown very promising results in good agreements with FEM simulations. The design of the two other components could successfully be validated after the devices were characterised.

6.2 Potential applications

The straightforward application of the mobile microsystem is an X-Y moving stage with unlimited travel range, a Z range of several micrometers and a resolution, which could reach the nanometer in the

X-Y-Z direction if the appropriate control is implemented on the ASIC. A slight modification of the ASIC and the microactuator array could lead to an additional rotating degree of freedom. If the ASIC incorporates some kind of optical local positioning system implemented e.g. with a few photodiodes and some circuitry, the microsystem would be capable of reaching accurately any position regardless of the effective step length performed at each cycle.

The fine positioning and conveying capabilities of the actuator array (the array is simply flipped upside down and immobilised) seem also very attractive. This configuration avoids the difficult problem of powering and the necessity of generating the driving signals onboard while offering most of the features of the mobile microsystem. In intelligent object positioning systems, an independent control of each actuator is desired in order to reconfigure electronically the whole conveying system in groups performing dedicated tasks, such as rotation, translation or sized-based sort. A modification of the array allowing matrix addressing would be easy to realize and multiplexing would not cause any problem since the position of a floating actuator can be maintained thanks to the charges stored on its big dielectric capacitance.

Besides its locomotion capabilities, the actuator array, which features three active degrees of freedom per actuator can generate any kind of patterns where the legs move within an ellipsoid. In particular, if the cylindrical leg is replaced by a kind of ‘Y’ extruded shape leg, local stirring in microfluidic application could probably be achieved by generating with two groups of actuators counter-rotating circular patterns in the plane of the substrate. Swinging motion alternatively introduced in a plane orthogonal to the substrate in one of the three preferential directions could simultaneously generate a flow in the liquid and thus add some valveless pumping capability to the stirring system. Applications are envisioned in biochemical analytical assay, where diffusion driven processes often require a long measuring time. Throughput of such systems might be increased if combined with such a micro stirring/pumping device.

Another potential application of the actuator array is found in telecommunication. The light emitted by an array of VCSEL (surface emitting laser) at any of the two telecommunication wavelengths could be individually coupled and guided through one leg of the actuator array since silicon is transparent at these wavelengths. Optical switching or dynamic fine positioning of an array of laser beams seems thus achievable if the actuators can be controlled independently.

By using the direct piezoelectric effect, the actuators can be changed into an array of sensors capable of sensing local pressure and shear stress. The physicochemical interactions of the leg with the texture of the sample being measured could then lead to the determination of some characteristic of the surface through an appropriate signal processing of the electrical signals generated by the piezoelectric transducers.

It would also be interesting to investigate whether the legs can be used as tactile displays for blind people.

The few examples mentioned above show the amazing application potential of the technology that has been developed for the microlocomotion project proving once again that new developments that seem weird at first hand might find numerous applications in various fields. More interestingly, the technology that has been developed is generic to a number of products that would require a robust sensing or active layer based on a bimorph structure.

6.3 Smarter powering

The device that has been realised does not make an efficient use of the energy. It has been shown in the modeling section that only about 1% of the electrical energy that is put on the actuator is transformed into mechanical one. What happens to the remaining 99%? In the current design, this energy is simply dissipated when the two ports of the actuator are shorted. This energy is however capacitive, meaning that it is a form of potential energy that deserves a better future. Coupling the actuator with an inductive component would allow the energy to oscillate between a kinetic and potential form and be reused many times. The required inductor would however be of unrealistic size for the resonance frequency of the oscillator to lie in the tens of kHz range. Why not then simply use high-Q quartz like resonators? Figure 6-1 shows a schematic of this very interesting concept based on two Colpitts oscillator.

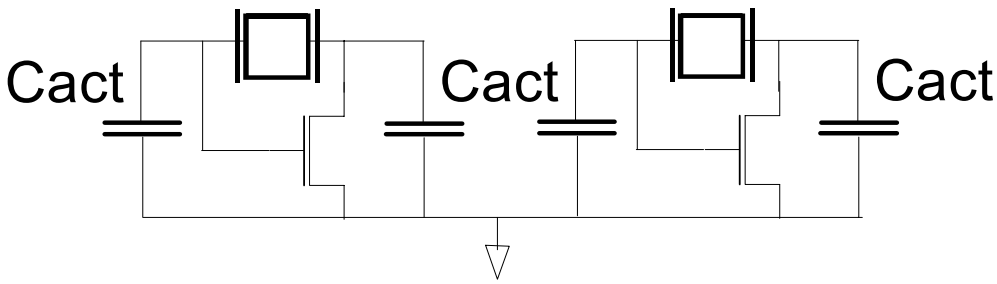

Figure 6-1. Concept level circuit for ultimate power efficiency based on two quadrature coupled Colpitts oscillators.

The actuators, represented again as capacitors, are connected through switches (not shown) to two high-Q resonators and their corresponding active element according to the selected direction of motion. The active elements provide the negative conductance that is required to compensate for the electrical and mechanical losses and ensure that the oscillations are sustained. In a Colpitts oscillator, the voltages at the two ports of the resonator fluctuate more or less in phase opposition. Consequently, the two resonators have to oscillate in quadrature so that the four signals required to produce the complementary elliptical patterns can be generated. The quadrature mode can easily be obtained with the help of little extra circuitry that is not detailed here. The power consumption of such a system should be unbeatable, since only the dissipative losses be it electrical or mechanical have to be compensated. From an integration point of view, the two resonators can ideally be fabricated directly on the microactuator array, using piezoelectric excitation.

Why not use the inductive behaviour of a mechanical resonator to implement a DC-DC voltage booster and generate the high voltage needed to drive piezoelectric actuators from a single solar cell. Figure 6-2 shows a schematic of such a circuit. If the switching transistor is driven slightly above the resonance frequency of the resonator i.e. where its behaviour is inductive, a voltage gain related to the transistor duty cycle can certainly be obtained. The low switching frequency and high resonator Q should allow for very high efficiency to be attained.

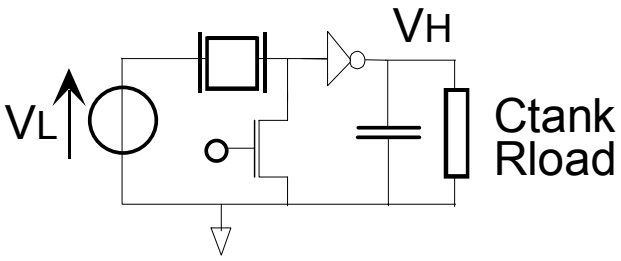

Figure 6-2. DC-DC voltage booster based on a mechanical resonator.

6.4 Single substrate integration

Why not integrate the three components on a single silicon substrate. While this idea seems truly crazy at first, it might not be that unrealistic. Aluminum nitride is the best piezoelectric material from an IC compatibility point of view and the replacement of the platinum bottom electrode would definitely enable its integration as a post-process. Could you imagine devices with embedded intelligence getting out of the etcher and starting to wander all around. Terrifying!

Publications

[1] D. Ruffieux and N.F. de Rooij, 'A 3-DOF Bimorph Actuator Array Capable of Locomotion,' In Proc. Eurosensors XIII 99, The Hague, The Netherlands, September 1999, on CD-ROM.

[2] D. Ruffieux, 'A Low Power Asic for the Control of a Mobile Microactuaor Array,' In Proc. ESSCIRC 99, Duisburg, Germany, September 1999, pp. 90-93.

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Biography

David Ruffieux was born the 12 December 1970 in Bern, Switzerland. He graduated from the Swiss Federal Institute of Technology, Lausanne, Switzerland in 1995 in microengineering after having spent a year at the Georgia Institute of Technology, Atlanta, USA. For his diploma thesis, he worked on the fabrication of a 16 by 16 vertical cavity surface emitting laser array at the Paul Scherrer Institute of Zurich, Switzerland (now CSEM Zurich). He then joined the Centre Suisse d'Electronique et de Microtechnique (CSEM SA) in Neuchâtel, Switzerland, where he worked on the conception and realisation of a bio-inspired microsystem capable of locomotion, merging state of the art technologies in low power analog circuit design, micromachining and amorphous silicon solar cell fabrication in a single system.

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Photovoltaic Group of the IMT for the fruitful collaboration in thin film solar cells. I also wish to thank Rutger Wijburg former head of CSEM's silicon service center, which managed to let me work or have some work done in the clean room between production lots. Thanks to Peter Vettiger from IBM Zurich, Arvind Shah from IMT and Eric Vittoz again, who accepted to coexamine this thesis. I also would like to thank Friedrich Heitger for his constant support and Franz Xaver Pengg for proofreading a draft version of this manuscript.

For the realisation of the microactuator array, I wish to thank Marc-Alexandre Dubois who developed the AlN process during his PhD. From IMT, special thanks to Cornel Marxer who gave me good inputs at all phases of this work, Georges-André Racine for sharing his knowledge on ZnO, Pierre André Clerc, for his help and work in DRIE and plasma etching in general, Gianni Mondin, Sabina Jenny and Sylvain Jeanneret for their help and work in thin films deposition. Thank also to all IMT PhD students and postdocs who shared technological knowledge and skills. From CSEM, I wish to thank Jean-Philippe Thiébaud, Nicolas Péclard, Karine Cormier and their operators, for their help on thin film deposition and patterning and DRIE.

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Curriculum Vitae

Name	David Ruffieux
Date of birth	12 December 1970, Bern
Nationality	Swiss
Home address	En Verdaux 22 1782 Belfaux Switzerland
Business address	CSEM SA Jaquet-Droz 7 2007 Neuchâtel Switzerland Phone: +41 32 720 56 85 Fax: +41 32 720 5763 e-mail: david.ruffieux@csem.ch
Languages	French, English, German

Education

1990-1995	Microengineering, Swiss Federal Institute of Technology, Lausanne, EPFL, Switzerland
1992-1993	Electrical engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

Degree

1995	Ing. Dipl. en Microtechnique, EPFL, Switzerland

Employment

1995-2000	PhD candidate at the Centre Suisse d'Electronique et de Microtechnique, Neuchâtel, Switzerland