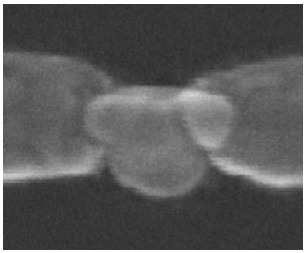
Development of an Aluminum Single Electron Transistor Scanning Probe



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par

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IMPRIMATUR POUR LA THESE

Development of an Aluminum Single Electron Transistor Scanning Probe

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FACULTE DES SCIENCES

La Faculté des sciences de l'Université de Neuchâtel,
sur le rapport des membres du jury

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Neuchâtel, le 1er septembre 2008

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Abstract

This thesis presents the development of a fabrication process for an Aluminum single electron transistor, experimental results verifying its functionality, and its integration on the tip of a scanning probe for scanning probe microscopy.

When an electron passes through a tunnel barrier, it changes the barrier's capacitance, which in turn builds up a voltage across the barrier. If the thermal activation energy is smaller than the charging energy, and the barrier resistance sufficiently suppresses quantum fluctuations, then this voltage buildup prevents any further electrons from tunneling. In other words, to be able to observe single electron charging effects in a tunnel barrier, its capacitance C must so small that the charging energy $e^2/2C$ is larger than the thermal energy k_BT and the quantum fluctuations $h/\tau = h/RC$. If those conditions are observed, then tunneling is blocked, the current is suppressed, the conductance drops, and the device is in Coulomb blockade.

A single electron transistor is a single electron charging effect based device, where two tunnel barriers are connected in series, defining a small island between them. This suppresses the quantum-mechanical uncertainty of the electron location. A gate is capacitively coupling to the island as third electrode. If the energies allow for observation of single electron charging effects, and a bias voltage is applied across the two tunnel barriers, then electrons may tunnel through both of them, resulting in a current, given that the tunnel barriers are not in Coulomb blockade. This is determined by the voltage applied to the gate electrode. A small change in the external polarization charge on the gate electrode (by fractions of the elementary charge) may move the single electron transistor from a conductive state into Coulomb blockade and *vice versa*. The current voltage characteristic of a single electron transistor is e-periodic with the gate voltage, since increasing the gate voltage allows to increase the number of electrons on the island one by one.

A process to fabricate single electron transistors was developed from scratch, employing the double angle Niemeyer-Dolan evaporation technique. A resist stack of poly(methyl-methacrylate) on top of copolymer was exposed with an electron beam lithography system. Resistively heated thermally evaporated Al was controlledly oxidized, followed by a second Al evaporation step at a different inclination angle. The overlap of the two evaporation steps defines the tunnel junction area. The device's functionality was successfully tested in a ^{4}He and a ^{3}He-^{4}He dilution cryostat for normal conductive and superconductive states.

Given that single electron transistor is very sensitive to change in charge, the scanning of a single electron transistor over a sample allows to map the change in charge, or charge distribution. The change in gate electrode polarization is measured by the change in current in the single electron transistor. In short, the current in the scanning single electron transistor changes because the capacitive coupling between the gate electrode and charges in the sample changes. Such a tool is intended to be used for local probe experiments, such as to probe the electric potentials and fields of device built in a two dimensional electron gas. A self-sensing and self-actuating quartz tuning fork based atomic force microscope probe was chosen as a platform for the implementation of the scanning single electron transistor. A monolithic Si handling chip with a notch where the proximal U-shaped end of the tuning fork can be lodged, is microfabricated with anisotropical potassium hydroxide etch. A cantilever extends from the chip body, and its end slightly exceeds the distal end of the tuning fork, and narrows down to form a tip shape, where the single electron transistor is patterned. A scanning single electron transistor probe was fabricated, and shows the same electrical room temperature behavior as the successfully a low temperature tested test structure single electron transistors. But only experimental verification will be able to show if the fabricated scanning single electron transistors probes are functional or not.

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Keywords

Aluminum single electron transistor scanning probe, single electron transistor (SET), scanning SET, tunnel junction, charging energy, Coulomb blockade, Coulomb oscillations, Coulomb diamond, single electron transport experiments, mesoscopic physics experiments, superconducting SET, SISIS structure, noncontact atomic force microscope (NC-AFM), low temperature AFM, scanning probe microscope (SPM), low temperature SPM, self-actuating self-sensing tuning fork probe, microfabrication, nanofabrication, electron beam lithography, PMMA, copolymer, Niemeyer-Dolan technique, suspended bridge dual angle shadow evaporation.

Mots clés

transistor à électron unique en Aluminium pour sonde à balayage, transistor mono-électron (SET), SET à balayage, jonction à effet tunnel, énergie de chargement, blocage de Coulomb, oscillations de Coulomb, diamants de Coulomb, expériences de transport à électron unique, expériences de physique mésoscopique, SET supraconducteur, structure SISIS, microscope à force atomique sans contact (NC-AFM), AFM à basses températures, microscope à sonde à balayage, SPM à basse températures, sonde autoactionnée et auto-captante à base de diapason, microfabrication, nanofabrication, lithographie par faisceau d'électrons, PMMA, copolymer, technique de Niemeyer-Dolan, évaporation masquée sous deux angles à travers de ponts suspendus.

Chapter 1

Introduction

1.1 Motivation

The field of mesoscopic physics[1] is bridging classical physics and quantum mechanics. Often theoretical physics predicted a fundamental effect, but it could only be verified by experiments in a mesoscopic systems only years later, simply because the fabrication and operation of such systems can be very demanding, and sometimes the tools and technologies had to be first invented. Electron beam lithography and scanning probe microscopy have made it possible to routinely fabricate devices in dimensions where charging effects can be observed experimentally, in structures that can be obtained with thin film processes.

One way to observe quantum effects is to perform electron transport experiments in low dimensional systems, such as semiconductor nanostructures kept at low temperatures to avoid thermal activation of the carriers. The design of the structures decides on what effects can be observed and

[1]The word mesoscopic, from Greek $\mu\iota\sigma o\varsigma$ (misos) "middle, intermediate" and $\sigma\kappa o\pi\varepsilon\iota\nu$ (skopein) "to see", is used to describe a certain length scale. There is no clear definition for it, but was intended to claim a space in the *middle* between *macro*scopic and *micro*scopic (atomistic) scales. This convention collides with the one inspired by SI prefixes, i.e. *micro*scopic and *nano*scopic. Where both of them agree is that this interesting field is located at length scales where quantum phenomena start to play a dominant role in electrical transport, but the physical phenomenon can be still described without discussing or analyzing the behavior of each individual electron, hole, atom or molecule involved. Some properties of a material have only a meaning when averaged over a certain amount of above individual participants, and are temperature, density, etc. . The mescoscopic scale aims to remain in the continuity by averaging over many neighboring atoms, without foraging into the discreteness of the description of a single atom. The term mesoscopic physics is being supplanted by the term nanoelectronics.

on what information can be gained. That information is obtained mostly through the structure's terminals, or through monitoring structures which are patterned so close to the investigated structure that they couple together, such as a side by side quantum point contact (QPC) monitoring a quantum dot[1], or an SET sitting on top of the Hall probe channel it monitors[2]. The location of such a monitoring detector is crucial and cannot be changed after fabrication.

An atomic force microscope (AFM) with an adequate conductive probe already can supply additional information about what locally happens elsewhere on the sample, such as in conduction channels, or along the channel's edges, where it can temporarily and locally pinch electrostatically or interrupt a channel or connect two channels together. Spin based electronics (spintronics) use the electron spin instead of its charge to store information. Recent reviews, such as ref. [3, 4] give an overview on this dynamic field. The study of charges in quantum dots can give information that helps to deduce on spin states, therefore there is a great interest and need for techniques to probe for and to manipulate spins. The local measurement of potentials, charges and magnetic fields can help to probe for spins.

A scanning probe microscope (SPM) gives information about the surface of a sample, commonly about its topography, but also about other properties as conductivity, doping, elasticity, temperature, etc. . While probing, the interaction happens locally between probe tip and sample surface, and is characterized by attractive and repulsive by force, by mechanical deformation, or by chemical reaction. An important exception is the long range force electromagnetism, which allows to probe below the surface. To observe charges below the surface, such as they occur in a buried two dimensional electron gas (2DEG), the electromagnetic fields stemming from localized charge carriers at and below the surface may be observed from above the surface. But the detector for such a minute potentials must be very sensitive.

A detector predisposed to measure electrostatic voltage (potential) difference, or electrical charge, would be an electrometer, which in the measurement instruments field is nothing more than a DC voltmeter[5] with a very high input impedance[2].

A single electron transistor is a Coulomb-blockade electrometer, which means that it does not measure directly the potential with a high input impedance, but rather the polarization charge change on its gate capacitor,

[2]In 2006, a commercial electrometer[6] compares to a voltmeter[7] in input impedance (200TΩ vs 10GΩ), burden voltage (<20μV vs <1mV), all with an input bias current of <3fA with 0.75fA p-p (peak-to-peak) noise. An electrometer attempts to put the least load possible on the circuit under test.

which moves the SET in and out of Coulomb-blockade.

A detector combining the high sensitivity of an SET with the ability of an AFM to scan over the sample would allow to chose exactly the point where the local observation for potentials and charges is done.

The goal of this thesis is to equip a tuning fork based scanning probe with special tips that feature an SET.

1.2 Scope of thesis

The scope of this thesis is the development of an Aluminum scanning single electron transistor to be used for charge detection in low temperature physics. The SET is integrated on the probe tip of a non-contact scanning probe microscope (NC-SPM). The NC-SPM provides positioning of the probe with regards to the sample topography, while the SET provides information about charge presence or charge change in the nearby substrate.

The development is done in two steps:

- Design, fabrication and testing of a process producing an SET.
- Integration of that SET on a AFM.

It is a convergence of an interesting physical effect (Coulomb blockade) piggy-backed onto a high-resolution type tool (atomic force microscopy), using miniaturisation technology (micro- and nanofabrication), to be used in a cutting edge physical research area (very low temperature physics, spin and transport observations).

Chapter 2

Scanning probe microscopy

2.1 Functional description

Microscopes allow to see what can't be seen by the naked eye[1,2]. Optical and electron microscopes collect photons and electrons, respectively, that have interacted with the sample under observation to construct an image of the sample, either in an image plane or in a data file, respectively. In contrast to that, a scanning probe microscope (SPM)[3] directly interacts with the sample to construct an image, and therefore is not bound by diffraction, reflection, and refraction, that photons and electrons are subjected to. If you touch something with you fingers, you only can sense structures down to a size which are comparable to the spacing of the pressure (or cold, heat, pain) receptors that are embedded in your dermis (or epidermis). In addition to that, you leave a sweaty, oily fingerprint. The same applies to SPM: the sharpness of the tip defines the resolution, and

[1] From the Greek words *μικρός* (micros) "small" and *σκοπείν* (skopein) "to look at, to view", simply meaning "view the small".

[2] Adding explanations of Greek or Latin word origins neither make this chapter look any smarter, nor has the author ever learnt Greek, but are given as a courteous equivalent to explaining an acronym (From Greek *άκρωνύμιν* from *άκρος* (akros) "topmost,apex; extreme,border" and *όνομα* (onoma) "the name"), when first using it. Jargon laden discussions or writings often use three letter acronyms (TLAs) without properly introducing them, leading to a feeling of isolation for non-initiated listeners, bystanders and readers.

[3] The acronym SPM is commonly used for both the tool scanning probe microscope and the technique scanning probe microscopy.

each tip-sample contact alters either tip or sample, most of the time both. These are the limiting factors for SPM.

Any new subject matter is best introduced by establishing parallels and analogies to existing and known ones. Here this will be done by means of the turntable using phonograph or gramophone records, which throughout its history has acquired an impressive level of technical complexity. It remains to date the most popular analog sound storage medium. It's review is interesting for a general overview of scanning techniques.

The invention of the phonograph using record cylinders in 1877 was followed by the introduction of competing and ultimatively dominant flat discs in 1887. The introduction in 1982 of the digital compact disc (CD) format[8] overtook market-wise the long play (LP) disc in 1988. The CD standard has been extended to accommodate not just music, but any form of digital data, up to 740 MB, only to be supplanted itself by the digital versatile disc (DVD) standard containing up to 4.7 GB, which in turn will be overtaken by – pending format wars – either HD-DVD or Blu-Ray disc (BD). Gramophone records are nowadays driven out into a small niche market, only used by audiophiles and disc jockeys (DJs), the latter add their performance to the music by speeding it up or slowing it down (scratching), by fast for- or backwarding through the music (back-cueing), fundamentally by interfering with its standard play mode. A standard play mode, or standard music scanning mechanism is described in the following. A vinyl disc contains on either side a concentric spiral groove, which starts at the disc's outer edge and ends at its inner. Some discs have two concentric spiral grooves, but this is more a technical prowess than useful feature, its prime effect being the rendering difficult of decisive (success at first attempt) access to either of the two intertwined grooves. Each side of the V-shaped groove has either of left or right sound channels topographically encoded into it. A direct-drive turntable rotates an LP disc at $33\frac{1}{3}$ revolutions per minute, which is the reason why a radial scratch across a couple of grooves, a frequent damage, is heard every 1.80 seconds. When the disc spins and a stylus is held into the groove, with a contact force of typically 10-20 mN (corresponding to an apparent weight of the stylus of 1-2 g), the cantilever holding the stylus moves according to the topography that is "read".

For a center mounted cantilever, there is on one side the stylus, on the other a magnet (moving magnet type) or a coil (moving coil type), and in the close vicinity a pair of matching fixed coils or fixed magnets, respectively. This is the core of the mechanism, sometimes the stylus movement is mechanically amplified by a longer cantilever on the magnet/coil side. The relative movements of moving magnet to fixed coils, or moving coils

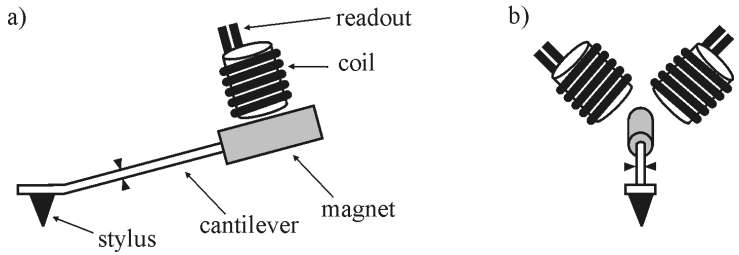

Figure 2.1: *Turntable pickup, moving magnet type cartridge, a) side and b) front view. The two at 90° mounted coils convert ("pick up") two channels of topographic information in the disc groove back to electrical signals, one coil the left flank of the groove, the other the right, yielding two channel, i.e. stereo sound.*

fixed magnets, induce voltage in the coils (fixed or moving) by electromagnetic induction. These voltages are (two coils) "read" and amplified as audio signals. The stylus, cantilever, magnet-coil assembly is called cartridge, cf. fig. 2.1, and is vertically held in position in the groove by a counterweighted tonearm, which can apply a certain range of pressures between stylus and disc groove, while the horizontal placement is given by the groove itself. Following parts of the system can by identified: turntable, disc, tonearm, stylus, cartridge, or in a general manner:

- A probe (stylus) and sample (disc).
- A scanning mechanism that provides for positioning and motion between sample and probe (turning table with grooved disc and tonearm).
- A control mechanism for the probe-sample distance (counterweighted tonearm).
- A data acquisition system (cartridge, amplifier, hifi).

The interactions between those parts follow in rough lines the connections outlined graphically in fig. 2.2. There is no image display part to the gramophone system, because it designed to give us not images of the groove's topography, but to listen to stereo sound corresponding the groove's topography. Every analogy has its breaking point. Having established those basics through a known example, the SPM *per se* is now approached. It is not without an sense of irony that one notes that in the year that the CD is introduced into the market, (bound to overtake

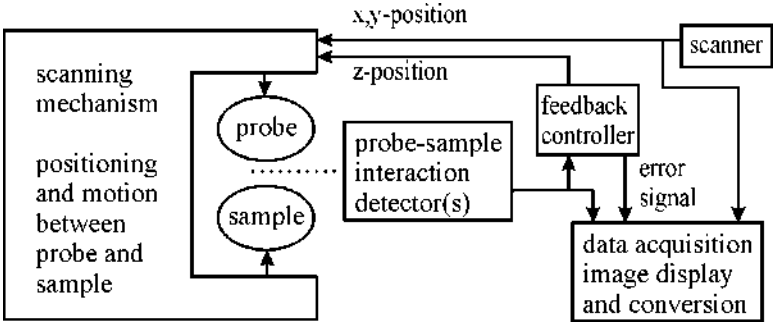

Figure 2.2: *SPM readout principle. The schematic interaction and functions can be identified in any such setup.*

the LP within six years, which effectively means that the method of a stylus picking up an analog signal is being replaced by a laser beam picking up a digital signal) the first publications for STM happen, de facto reintroducing and rebirthing the stylus concept, although not into audio reproduction, but this time into microscopy.

A scanning process is the positioning of the probe at predefined positions, such as the intersection points of a predefined grid, and the recording of the probe reading at these points. Since the probe data yielded is just data, as opposed of an intensity map such as in optical/electron microscopy, it can be used in many ways to give intuitive understanding of the reading in question, e.g. the height signal of a scan may be plotted in a three dimensional x-y-z graph, giving a wire-frame model with some depth perception of the sample observed, or the temperature reading of a scan may be plotted in an x-y graph, coloring each data point according to a color spectrum ranging from blue (cold) over yellow (warm) to red (hot). It is an art to find the most intuitive way to present the yielded data.

The positioning of the probe is the crucial part of an SPM, and requires above mentioned four basic functionalities:

The **scanning mechanism that provides positioning and motion between sample and probe**, is obtained through piezoelectric [4] actuators. The (crystalline or ceramic) structure of a piezoelectric material generates a voltage proportional to the mechanical stress applied (direct piezoelectric effect) and due to an electric field applied to a piezoelectric material, the structure is deformed proportionally to the voltage applied

[4] From Greek $\pi\iota\varepsilon\zeta\epsilon\iota\nu$ (piezein) "to squeeze, to press".

(converse piezoelectric effect). The deformation is at the crystalline level and therefore applying adequately small voltage increments theoretically allow to generate sub-atomic deformation increments. This can be used for high resolution actuation. SPM vendors calibrate each piezoelectric actuator and compensate for nonlinearities allowing to achieve sub-nm range resolution. Piezoelectric actuators are used for x, y and z actuation.

Conceptually, most microscopes share the convention that the surface being probed defines the xy-plane, while the normal vector to it, the distance probe-sample, is the z-direction. The positioning and movement can been obtained in many ways, i.e. fix the probe and xy-scan and z-control the sample, z-control the probe and xy-scan the sample, etc. . The microscope manufacturer or builder takes the decision on the scanner's layout, based on how much of the mutually interfering scanning movement effects are controllable and compensatable, by hardware design of software, i.e. when an combined xy-scanning tube does a scanning step, the voltage change to the x and y actuator cause the tube to tilt, but at the same time it also causes a minute z-distance change, which will be compensated by the z-distance feedback actuator, which will result in a bulge and deformation in the data due to the SPM design. The data may also only be compensated later on in data to image conversion.

The **control mechanism for the probe-sample distance**, is generally implemented with an electronic feedback circuit, which keeps a measured signal constant. Electronic feedback loop circuits have a maximum bandwidth, and are one of the bottlenecks limiting SPM image acquisition speed. For a constant height mode scan, the feedback needs to be significantly faster than the time spent at each point of the scanning grid. This is often achieved with third party vendor's dedicated solutions[9, 10, 11, 12].

The **probe and sample**, and the **data acquisition system**, are very specific to the task the microscopy has to perform. As an example for the intertwinedness of those functionalities a classical readout example is given. A laser beam (cf. fig. 2.4) is reflected off the cantilever holding at its end a probe, onto a two segment photodetector. The signal is constituted of the difference of the signals collected by the photodetector. If the probe on the cantilever encounters a hill on the sample, it is moved up, the cantilever deflects more, and the beam reflected off the cantilever changes position on the detector, diminishing one segment's output while increasing the other's, thereby changing the difference signal, which causes the feedback loop to diminish the z-direction actuators extension, until the reflected cantilever causes the same difference signal as before the hill was met. Different detection mechanisms require different feedback loops and different acquisitions systems.

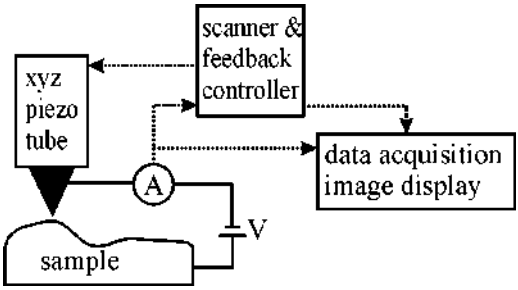

Figure 2.3: *STM readout principle. An voltage applied between probe and sample makes a current flow, which is measured. This information allows the scanner and feedback controller to regulate the probe-sample distance according to the scanning mode chosen, all while scanning the sample. The current, and xyz control signals are used in the data acquisition and image display to fabricate an image of the surface.*

Nowadays SPMs use a virtually unchanged tip-sample positioning system, but there exists a teeming field of application specific probes, application specific control mechanisms for the probe-sample distance, and application specific data acquisition system.

A rough historical overview follows.

2.2 Scanning tunneling microscope

Work on the scanning tunneling microscope (STM)[5] started in the late 1970s at IBM Rueschlikon, Switzerland. *The idea was to scan a surface, similar to a stylus profilometer, but instead of scanning a tip in mechanical contact over a surface, to maintain a small gap of a few angstroms between tip and sample and control it by the tunnel current flowing between them.*[13] First public traces appeared in a patent disclosure on STM in 1979. The first exponential dependence of tunnel current on tip-sample separation was observed in 1981, followed by public presentations and publications[14, 15], and eventually in a quarter of the 1986 Nobel Prize of Physics for both Gerd Binnig and Heinrich Rohner[13]. The tunnel current depends exponentially on the tip-sample distance, which is used for the z-feedback. A rough sketch is in fig. 2.3. Two scanning strategies are common, *constant current mode*, where the feedback loop keeps the tip-

[5]The acronym STM is commonly used for both the tool scanning tunneling microscope and the technique scanning tunnel microscopy.

sample tunnel current, and hence the distance, constant, and the *constant height mode*, where the feedback was beforehandedly used to calibrate the current against the z distance range, and the current recorded allows to deduce the z-distance during the scan.

The tip form determines directly the resolution that the scan has, and early experiments gave immediately impressive results, such as the 7×7 reconstruction of the Si(111) surface[16]. Reading of comprehensive topical reviews[17, 18] is recommended. There are many recent STM developments which shall remain untold at this place.

2.3 Atomic force microscope

A STM bases its distance feedback on a tunnel current, which limits its application to conducting samples. While performing STM, forces between the tip and sample were observed, which lead to the development of the atomic force microscope (AFM)[6] by the same team[19] as for the STM. Its first realization was an extension or enhancement of an STM. Between a conducting tip and an insulating sample, a diamond tip mounted on a lever was inserted. Once the diamond tip is in close range of the surface and is subjected to attractive or repulsive forces, the STM tip is positioned on the conductive backside of the lever. When the scanning diminishes the tip-sample distance, also the force on the lever changes, and with it its deflection, which results in a change of the tunneling current of the STM on the backside, which is used as a signal for z-direction feedback of the scanning of the sample. Although nowadays AFMs use different and/or simpler force readout mechanisms, such the laser beam reflected off cantilever system shown in fig. 2.4, the underlying tip-sample interactions remain identical. The forces are:

- Van der Waals (attractive) - dipolar atom interaction.
- Chemical or Pauli exclusion principle (repulsive) - valence bands at smaller than interatomic distances.
- Capillary forces (attractive) - adsorbed water film, surface tension.
- Electrostatic (attractive) - Coulomb forces on voltage difference (may be repulsive if both tip and sample are non-conductive).
- Magnetic - magnetic interaction (requires magnetic probe).

[6]The acronym AFM is commonly used for both the tool atomic force microscope and the technique atomic force microscopy.

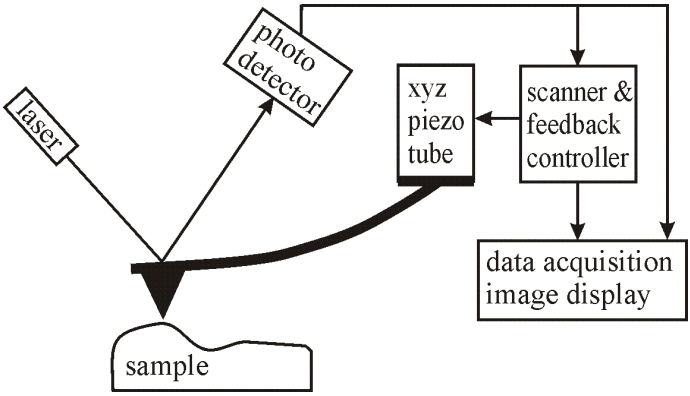

Figure 2.4: *AFM readout principle of contact mode. A laser beam is directed to the back of a cantilever near to where the probe is. When the topography changes, the cantilever bending changes, and the reflected laser beam changes the ratio of the two segment photodetector that it illuminates. The difference signal changes and is used by the feedback controller to control the tip-sample distance or pressure, through the bending of the cantilever. Difference signal, and scan xyz signals are used to form an image of the scanned surface.*

- Dissipative - friction in contact mode, damping in air, any gas or liquid.

An in depth review of the field[20] is best consumed with moderation. All forces act simultaneously and for special cases can be quite complex, but for a simple "everyday" topographic scan just involving Van der Waals, chemical, and capillary forces, the characteristic force-distance curve is schematically given in fig. 2.5. It describes the resulting force between tip and sample is changing when approaching the tip approaches the surface from far. The resulting force is increasingly attractive, up to a certain point where it drops back to zero at the moment of contact with the surface, from which point on the resulting force is repulsive.

There are many approaches on how to scan a surface. AFM manufacturers user manuals give usually good insight on their scanning strategies[21].

There are two ways to classify AFM operating modes, one based on the tip-sample distance, and one based on the tip-sample interaction or the feedback signal. The former distinguishes contact mode, non-contact mode, and intermittent contact mode, the latter static and dynamic mode.

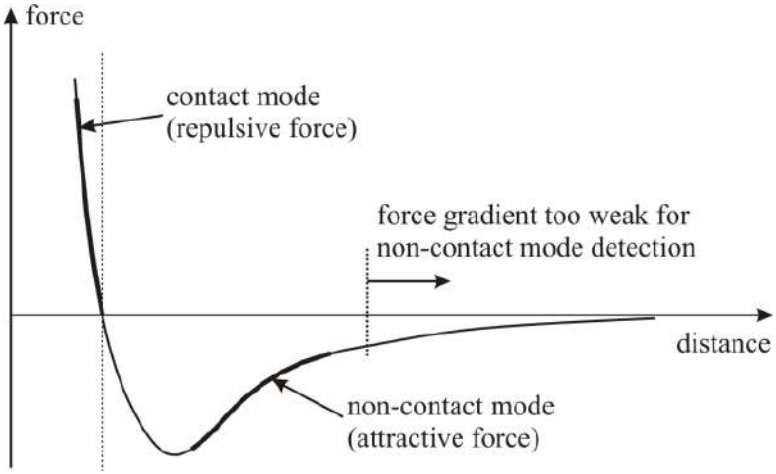

Figure 2.5: *Schematic force–distance curve of typical probe-sample interaction in an AFM. The contact mode works by definition only in the repulsive part. The non-contact mode depends on the force gradient, which is highest close to the surface. The intermittent contact mode spans the whole range from contact to non-contact mode, and has the advantage that the tip is not dragged from one point of the scanning grid to the next, but lifted off the surface, which is an advantage for fragile soft samples. This contrasts to static and dynamic mode (discussed in text).*

For the case of a topographic surface scan, with the tip in contact with the sample as described earlier, the deflection can be kept constant by the feedback loop, analogous to STM's constant current mode, while the feedback loop's signal for the z-actuator simultaneously gives the sample's height information. This is called *constant deflection contact mode*, or *constant force contact mode*. At the same time it is a static mode, because for every measurement point on the scanning grid, the tip-sample interaction is static, the signal doesn't change. If the surface is known to be flat enough to not exceed the mechanical limit of the cantilever or the detection system, it can be scanned at constant height, and the change of the deflection signal can be mapped to the height information, if it was beforehand calibrated to the z distance. This is called *constant height contact mode*, and is analogous to STM's *current image mode*. Since there is no feedback to be done for the z-axis, image acquisition is much faster than the preceding mode. In a third type of contact mode, the z-distance is increased and decreased, without ever losing contact with the sample,

effectively more or less indenting the tip into the sample, if the sample is very hard, such as Silicon, then the tip's z-position changes next to nothing, but the cantilever bends a lot, and if it is read out with a reflected laser system, gives an important cyclic feedback signal, but when the sample is moved to a less hard area, such as a polymer droplet on the sample, then the tip's z-position will change more, because the polymer is more elastic and will be indented more, while the cantilever based feedback signal diminishes. This is called *force modulation contact mode*, and is a dynamic mode.

Contact mode implies the existence of a non-contact mode, and also of an intermittent contact mode. To get any information about a surface, without getting in contact with it, the tip must get close enough to the surface to be subjected to strong interaction forces, in fig. 2.5, that is in the area in the curve where the force gradient is the highest. This is not, or at least not easily, achievable by statically placing the tip at a certain distance, because small changes in distance may immediately result in a snap into contact of tip and sample, because the feedback loop can't react rapidly enough to prevent that. That is why non-contact mode is often used synonymously with dynamic mode, where the tip is cyclically approached and retracted from the surface, traversing a certain range of the force-separation curve. It is done cyclically because it is easy to convert the tip and cantilever assembly into an oscillator, operated at or near its resonance frequency, where the energy injected into the oscillator to keep at resonance is small or neglectible, given an adequate material for the oscillator. If the tip is scanned across the surface and encounters a topographical change, then the range of the force-distance curve traversed changes. The resonance frequency of the oscillator depends on the force gradient acting on the tip. In the case of the tip getting closer to the surface and for example more or farther into the attractive part of the curve, the oscillator changes its resonance frequency, and thereby is amplitude, and phase. The oscillator driver notes these changes, and depending of what strategy was chosen – amplitude detection, phase detection, frequency detection –, creates an error signal that can be fed into the feedback loop to retract or advance the tip, to return to the frequency, amplitude or phase as before the topographical change.

The *intermittent contact mode* spans the range from contact to non-contact mode. It can be done either statically in a force spectroscopic way by lifting the tip off the surface, and moving to the next gridpoint, or dynamically, with an oscillating tip, leaving a trail of small punctual contacts. Both have the advantage that the tip is not dragged from one point of the scanning grid to the next not unlike a plough, and are used

for fragile soft samples.

2.4 Summary

Some important SPM concepts were broached here in this chapter. In the chapter *Experiments* (starting p.67) the criteria and driving forces behind the selection of the AFM type for this research are discussed. As an example to show that the last word in SPM has not been said, and that always will be space for novel approaches, the example of fiber-top cantilevers[22] is given, where a cantilever with pyramidal tip is micromachined out of the tapered end of an optical fiber by means of focused ion beam. The interference signal between injected light, and reflected light from the back of the cantilever is used for z-feedback[22].

Chapter 3

Electron transport

The goal of this thesis is to implement an SET on an AFM, which requires first a thorough understanding on what an SET is, on how it functions, and on what theoretical background it is based upon. This chapter sets out to provide for this information.

3.1 Electric conduction fundamentals

In many cases, the understanding of electrical conduction can be reduced to the concept of electrically charged particles moving through an electrical conductor. Systems can be roughly and easily described by electric and magnetic fields, potentials, currents, and impedances, and laws (Maxwell, Lorentz, Ohm, Kirchhoff, etc.) governing these sizes. The laborious path of getting from the initial discovery of the electron by Thomson[23, 24] and determination of its charge by Millikan[25, 26] and farther[1] to today's level of knowledge and understanding is often underestimated.

Electric charge is quantized in units of the elementary charge e, and electrical current is the flow of electrons per time. However, the definition of electrical current is not done by directly counting the electrons in time, but by indirectly defining the amount of constant current it takes to produce a certain attractive force between two conductors. This is because the emergent, macroscopic properties of a system are a description based

[1] Drude modeled conduction in metals with a gas of electrons, successfully applied the kinetic theory of gases to it, establishing the theory of electrical conduction. Sommerfeld replaced the Maxwell-Boltzmann velocity distribution by the quantum mechanically constructed Fermi-Dirac distribution. Today conduction is quantum mechanically fully explained[27].

on observing a large number of electrons which have a stochastic behavior. Devices such as a single electron pump or turnstile[28] are a recent development. They transfer single electrons through an array of tunnel junctions by controlling gate voltages in sequence, and permit to generate a very precise amount of electrons per time, and therefore a very precise current. They were designed based on the understanding that when the dimensions of a conductor get very small, then the observation can carry signatures of effects which have to do with the individual electron moving in, through, and out of a system. Very small means that the physical dimensions of the system are comparable to several typical and characteristic length scales of electron transport. They are its mean free path[2][l_{mfp}], its coherence length[3], its Fermi wavelength[4][λ_F], its localization length [ξ] and its system size[L]. The sizes of those length scales in relation to each other allow to classify the system according to the electron transport phenomena that will occur in such as system. For the case of this research, an Al based SET at cryogenic temperatures, with a designed island (system size W, L), of 50-100nm in diameter and 30nm thick, the value for the mean free path of 39μm (cf. footnote), exceeds the system size, $l_{mfp} \gg W, L$, which is a characteristic of a *ballistic mesoscopic system*, where the scattering of the electrons is predominantly at the edges of the system, and is far more prominent than the scattering at defects and impurities, characteristic for the diffuse transport regime. The electrons transport through such an SET will not encounter phase destroying scattering events during the transits.

As an illustration of the behavior of electrical conduction when a conductor is rendered smaller and smaller, such as by constricting it, two showcase examples are cited in the following.

The first example is the observation of a ballistic point contact, defined in a 2DEG[30]. The conductance changes in quantized steps of $e^2/\pi\hbar$ ($=2e^2/h$) when the width of the constriction is varied by changing the voltage applied to the top gate electrode, which changes the depletion of

[2]The mean free path of an electron in Al at room temperature is $l_{mfp} = \sigma m v_F/ne^2 = 14\times10^{-9}m$, with conductivity $\sigma = 35.7\times10^6\Omega^{-1}m^{-1}$ at 20°C (electrical resistivity $\rho = 2.8\times10^{-8}\Omega$m), mass of an electron at rest of m=9.1×10^{-31}kg, Fermi velocity of Al v_F=2.03×10^{6}m/s, free electron density in Al $n = 18.1\times10^{28}m^{-3}$. As temperatures decreases, the conductivity increases, and with it the mean free path. At 4K, with $\sigma = 1.0\times10^{11}\Omega^{-1}m^{-1}$ ($\rho = 9.8\times10^{-12}\Omega$m[29]) the mean free path increases to $l_{mfp} = 39.1\times10^{-6}m$.

[3]temperature dependent superconductive coherence length $\xi \approx 100nm$ indicative for the extent of a Cooper pair in metals, and phase coherence length $l_\phi \approx \mu m$, indicative for electron waves in heterostructures.

[4]The Fermi wavelength λ_F of the wavefunction of an electron in metals is short, in the order of the distance between atoms, i.e. 1nm, while in semiconductors it is longer, in the order of 100nm.

the underlying 2DEG, which narrows or widens the point contact.

The second example is a break junction setup, where a mechanically controllable pulling force is exerted on a narrow metallic wire[31]. The smallest section of the wire, called waist or constriction, decreases when the pulling force increases. This is reversible as long the elastic deformation regime of the wire is not exceeded. As the constriction is reduced, reproducible jumps in the conductance are observed, which are of the order of $2e^2/h$. This allows for study of quantum size effects on conduction in metallic constrictions.

Both examples show the quantization of ballistic electron transport[5] through a constriction. The conductance quantization is a demonstration that the conduction is not a macroscopic flow of a large cloud of electrons, but a transmission through available channels. Both cited articles use the Landauer-Büttiker (LB) formalism[32, 33], which allows to describe current as a transmission probability of an electron. Ohm's law links conductance to the macroscopic system size by $G = \sigma W/L$, where σ is the specific conductivity in $\Omega^{-1}\cdot\mathrm{m}^{-1}$, and W and L the width and length of the conducting segment. Above two experiments show that for "small" dimensions, the conductance no longer decreases linearly with the width as Ohm's law stipulates. The Landauer Formula for the conductance of a mesoscopic conductor is

$$G_{tot} = \frac{2e^2}{h} MT,$$

where M is the number of transverse modes, and T the transmission probability (and $1-T$ the reflection probability). The discrete steps of conductance reduction can each be explained by the removal or the disappearing of a transverse mode in the conductor, which is what happens in the two examples. In the former, an increase of voltage further depletes the 2DEG, and narrows down the point contact. In the latter, further pulling decreases the conductor section. For further details on the LB formalism, consider a review[34] of the field, for full immersion a book[35].

[5] Ballistic electron transport is characterized by the scattering of the electrons at the edges of the channel or system exceeding the scattering on defects inside of the channel.

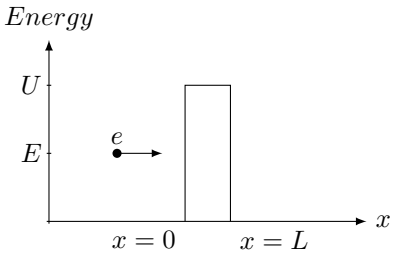

Figure 3.1: *Particle of energy E encounters a tunnel barrier of height U ranging from $x = 0$ to $x = L$.*

3.2 Transport phenomena in electronic systems

3.2.1 Quantum tunneling

Consider an electron in a conductor with energy E, on the left side of an insulating barrier of height $U > E$ and width L, as in fig. 3.1. The barrier separates the conductor into left and right electrode. By means of classical physics, there is no way for the electron to get from the left side electrode through the barrier to the right side electrode, which is one of the reasons that macroscopic objects who obey these laws, such as cars, need physical tunnels to drive through mountains. Quantum mechanics explain why for electrons this is possible (without digging tunnels) with quantum tunneling, a stochastic process. The theory is initially perplexing[36], and resides on the famous Schrödinger equations[37]. The transmission probability T for a particle to tunnel from the left electrode through the barrier to the right electrode is $T = e^{-2kL}$ where $k = \sqrt{2m(U-E)}/\hbar$. The probability depends on the width of the barrier L, the difference $U-E$ between barrier height and particle kinetic energy, and the mass m of the particle. The probability is small, but it is non-zero, and if a voltage is applied between the left and right electrode, then a current will start flowing. If the tunneling events are such that the energy of the electron does not change, the tunneling is called elastic, if it does change, and energy is dissipated, either in the barrier or at the interface, then it is inelastic. Important theory on tunneling was provided by Fowler and Nordheim[38], Simmons[39]. and with the base of BCS superconductivity[40] also on superconductive tunneling by Giaever[41, 42], and Josephson[43, 44].

Quantum tunneling happens if the particle has enough energy to tun-

nel through a barrier, either because of its average thermal energy k_BT (Boltzmann constant × temperature), or because a voltage bias is applied across the barrier.

3.2.2 Charging effects

Deliberate capacitors are electrical devices that can store energy in the electric field between a pair of closely spaced conductors. When current is applied to such a capacitor, electric charges of equal magnitude, but opposite polarity, build up on each conductor. Because of the electric accumulation, an electric field is created in the region between the conductors that is proportional to the amount of accumulated charge. The electric field E creates a potential difference ΔV (which in the case of a parallel plate capacitor is $\Delta V = Ed$). Given a capacitor charged to q and the voltage across it $V = q/C$, the energy W to add an infinitesimal charge dq is $dW = V dq = qdq/C$, and when integrated from zero charge to final charge,

$$W = \int_0^Q \frac{q}{C} dq = \frac{Q^2}{2C} \tag{3.2.1}$$

the electrical potential is obtained, or the electrostatic or Coulomb energy stored in a capacitor.

When connecting the left and right side of the tunneling barrier in fig. 3.1 to a current source it can be thought of like a capacitor which is being charged. [Each time an electron tunnels across the tunnel barrier, the energy stored in the capacitor is reduced by a well defined energy quantum of $e^2/2C$.]

3.2.3 Coulomb blockade

After a tunnel event in an electrically disconnected (isolated) tunnel junction as in fig. 3.2, the charge change results in a voltage buildup across the junction. The energy stored in the junction capacitance changes from $Q^2/2C$ to $(Q - |e|)^2/2C$ and voltage V across the junction by $\Delta V = e/C$, where C is the capacity of the junction.

Assume that the capacitor is charged to Q, which not necessarily is a multiple of the elementary charge e. An electron tunneling in either direction through the barrier, changes the charges Q and $-Q$ on the electrodes to $Q - |e|$ and $-Q - |e|$. It also changes the electrostatic energy of the junction capacity. Subtracting the charging energy *after* the tunneling

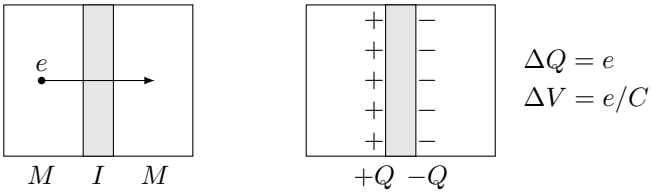

Figure 3.2: *Electrically isolated tunnel junction with a capacitance C, before (left) and after (right) a single-electron tunneling event. The charge change ΔQ results in a voltage ΔV buildup across the junction.*

event from *before* leads to

$$\Delta E = \frac{Q^2}{2C} - \frac{(Q \pm e)^2}{2C} = \frac{e}{C}(Q \pm \frac{e}{2}).$$

If the initial charge of the tunneling junction Q is within the limits $-e/2 < Q < +e/2$, then any charge change $\Delta Q = \pm e$ will yield an positive energy change, which is energetically unfavorable, hence forbidden (cf. fig. 3.3). This situation is the **Coulomb blockade of single electron tunneling**, i.e. electrostatic charge precludes tunneling, and even if there is a bias voltage applied across the junction, no tunnel current flows. If the initial charge of the tunneling junction Q lies outside of these limits any charge change $\Delta Q = \pm e$ will yield an negative energy change, which is energetically favorable, hence possible. The term *Coulomb blockade* was first used by Averin[45]. The Coulomb Blockade manifests itself on an current *vs* voltage $I - V$ curve, where the current – if not considering the Coulomb blockade – anomalously stays at zero for bias voltages of $|V| \leq e/2C$. Beyond that value, a current flows, which is first grows quadratic up to $|V| \ll e/C$, and linearly for $|V| \gg e/C$.

3.2.4 Temperature and quantum fluctuations

The Coulomb blockade always exists, but is not always observable, because other conduction phenomena may be dominant. The *temperature* of a system is a measure for the internal energy present, and a measure for the kinetic energy of the system, i.e. vibrations, particle movement or spin, etc. . The *thermal energy* is given by

$$E_T = k_B T.$$

E_T must be lower than the charging energy E_c in order to observe the Coulomb blockade. If an electron that is blocked from tunneling through

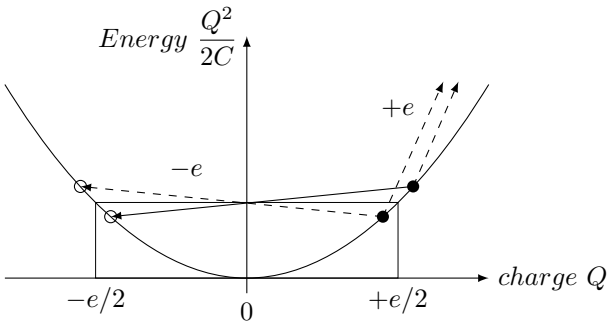

Figure 3.3: *Energy versus gate charge plot. This shows energetically the origin of the Coulomb blockade of the single electron tunneling in a current biased junction. Favorable (loss of energy) transitions are noted in continuous (—) lines, while energetically unfavorable and therefore blocked transitions are noted in dashed (- - -) lines. Circles signify ● occupied, and ○ empty positions (fig. according to[45]).*

a junction, because it is energetically disfavorable, receives enough energy from thermal fluctuations to make tunneling still favorable, or to cross over the barrier, then it is *thermally activated*, and ignores the Coulomb blockade. The Coulomb effect is smeared out or hidden. At sufficiently high temperatures ($k_B T \gg E_c$) the system is in the classical regime, Coulomb charging effects are negligible, and the system exhibits normal conductance. Solving the inequality for temperature yields the first condition that a junction must be fulfill to be in Coulomb blockade:

$$T < \frac{e^2}{k_B 2C} \ .$$

Quantum energy fluctuations, are the temporary change in the amount of energy in a point in space. The uncertainty about the energy of an electron at the barrier must be less than the barrier's charging energy, otherwise an electrons may get enough energy from a fluctuation to tunnel through a barrier that otherwise would be blocked. The Heisenberg uncertainty principle[6] reformulated for energy reads:

$$\Delta E \approx h/\tau.$$

[6]de: Unschärferelation, fr: principe d'incertitude, it: relazione di indeterminazione.

Using the typical time to charge or discharge a capacitor of $\tau = RC$, also called charge relaxation time, leads to $E_c = e^2/C \gg \Delta E \geq h/\tau = h/RC$ [7] and solving $e^2/C \gg h/RC$ for the resistance R_t or conductance G_t of the tunneling junction yields the definition of the quantum resistance R_K or the quantum conductance G_0:

$$R_t \gg R_K \equiv \frac{h}{e^2} \approx 25.8\text{k}\Omega \quad \text{or} \quad G_t \ll G_0 \equiv \frac{e^2}{h} \approx 38.7\mu\text{S}.$$

The second condition that a junction must fulfill to be in Coulomb blockade is that its resistance R_t must be higher than R_K, otherwise the quantum energy fluctuations mask the Coulomb blockade.

3.3 Electric conduction in a single electron transistor

Understanding the nature of electric conduction in an SET, and of what length scales influence it, will allow to design and fabricate it on an AFM tip. The electric conduction in an SET is done by single electron tunneling. Electron transfer across a potential barrier has a certain probability of tunneling, which is an attractive system to model with the LB formalism where transmissions between two (or more) terminals are also expressed as probabilities.

Later will be seen that the SET is fabricated using a metal, Aluminum. In metals, the Fermi wavelength λ_F is short, in the order of distance between atoms, i.e. 1nm. A quantum dot on the other hand is an island comparable in size to the Fermi wavelength λ_F, and therefore shows quantization of its electron states. The dimensions of a metallic SET are much larger, than the Fermi wavelength, therefore energy quantization cannot be observed, however other quantum-mechanical effects are not excluded. The term "quantum dot" should therefore not be used when discussing metallic SETs[46].

In a metallic island, the Coulomb blockade is a classical phenomenon since the energy spectrum of the confined region can be considered as a continuum. Furthermore, *in metallic films, the electron density is so high*

[7] While accounting for charges and energies, a tunneling event can be viewed as two sub-events, namely the removal of a charge e from one electrode, with according to eq. (3.2.1) $\Delta E_1 = e^2/2C$, and with the addition of a charge e on the other electrode, $\Delta E_2 = e^2/2C$. Hence the charging energy for transferring one electron from the left to the right of a junction or capacitor is e^2/C, cf. also fig. 3.4.

that even a film of thickness 10nm has several tens of occupied sub-bands and it is more accurate to treat it as a three-dimensional conductor[35].

Without paraphrasing: *Single electron tunneling is, like resonant tunneling*[8]*, observed in double-barrier structures. But the physical mechanism underlying the two phenomena are fundamentally different. Resonant tunneling arises from the wave nature of electrons, which gives rise to energy quantization in confined structures, while single-electron tunneling arises from the particle nature of electrons, which give rise to charge quantization. Resonant tunneling is not observed if the distance between the barriers is long enough that the spacing between the allowed energy levels is negligible compared to k_BT. But single-electron tunneling can still be observed, as long as the capacitance is small enough that the electrostatic energy of a single electron (e^2/C) exceeds k_BT. This effect would be absent if charge were not quantized, that is if e were equal to zero.* (from: Datta [35] p.247)

This work is on a metallic SET, which is in the classical or metallic Coulomb blockade regime. Semiconductors, where only few levels participate in transport, are in the quantum Coulomb blockade regime, which is not discussed here, instead the lecture of this review[47] is recommended. For the fabricated SET, the transport in the island is purely ballistic, and the island's resistance can be neglected.

The discrete levels of single electron tunneling are not due to the wave nature of the electrons (size quantization) but due to their particle nature (charge quantization).

3.4 Single electron transistor

This section shows what requirements need to be fulfilled in order to observe charging effects, and how to design simple devices based on the charging effects.

3.4.1 Junction requirements for single electron effect

In the two preceding paragraphs it was shown that the junction must fulfill following requirements: The elementary charging energy E_c of the junction must be larger than the scales of both the thermal (k_BT) and quantum ($h/\tau = h/R_tC_t$) fluctuations. The two parameters that are the easiest to be influenced are the tunnel junction resistance $R_t \gg h/e2 = 25.8\text{k}\Omega$,

[8]Resonant tunneling refers to tunneling in which the electron transmission through a structure is sharply peaked about certain energies.

which can be chosen to a certain degree by controlling the formation process of the junction, and which may be situated between the two extremes open and short circuit, and the temperature T, chosen to be low by a cryostat environment. The tunnel junction capacitance C_t, linked to it by $k_BT \ll E_c = e^2/2C_t$ can be influenced through the design or patterning, e.g. electron beam lithography, but is a less flexible parameter. In summary, **single electron charging effects are experimentally observable in high resistance junctions, with small capacitances and low temperatures.**

As an example to get an indication for the energy scales discussed, a tunnel junction formed by the crossing of two Al wires, both $50nm$ wide and defined by electron beam lithography, is made. Using the parallel plate capacitor formula $C_{pp} = \varepsilon_0\varepsilon_r\frac{A}{d}$, where $\varepsilon_\mathbf{0}$ is the free space permittivity, $\varepsilon_r = 10$ the relative permittivity of the insulator Al_2O_3, A the junction area and d=1nm the junction thickness, gives a capacitance of $C = 221$aF and yields a charging energy of $E_c = 57.9 \times 10^{-24}$J= 57.9yJ = 361$\mu$eV [9].

In 2007, electron beam lithography combined with liftoff pattern transfer cannot define junctions an order of magnitude smaller than above example, and metal evaporation (here Al) creates films with grain boundaries due to the nucleation mechanisms during the deposition which precludes easily achievable good film quality after reduction by another order of magnitude. Being at the lower end of the achievable length scales for the geometries of the structures, the remaining degree of freedom to make the single charge effects dominant is to cool down the samples to the point where the thermal activation energy is lower. Single charge effects are usually observed in cryogenic setups, and room temperature experiments[49, 50, 51] are more the exception to the rule than the rule.

The thermal activation energy of $E_T = k_BT$, which at room temperature yields $E_T = 4.41\times10^{-21}$J = 4.41zJ = 27meV, is two orders of magnitude higher than the charging energy E_c. This makes that any charging effect is masked by thermal fluctuations, and at best the *only noticeable consequence of discreteness of the electrical charge transfer through such a junction is the shot noise*[52]. In order to see any single electron charging effect, there must be $E_T < E_c$. Solving for temperature $T < e^2/k_B2C = 4.20$K. By coincidence this is the boiling temperature of

[9] Energy scales at this level are commonly expressed in electronVolts, abbreviated eV, where 1eV=1.6×10^{-19}J=160zJ, and 6.25eV=1aJ, on one hand for the convenience of having small familiar numbers, on the other hand because the Système International d'Unités (SI) prefixes necessary for such order of magnitudes were adopted by the Conférence Générale des Poids et Mesures (CGPM) only relatively recently, atto(10^{-18}) in 1964, zepto(10^{-21}) and yocto(10^{-24}) in 1991[48].

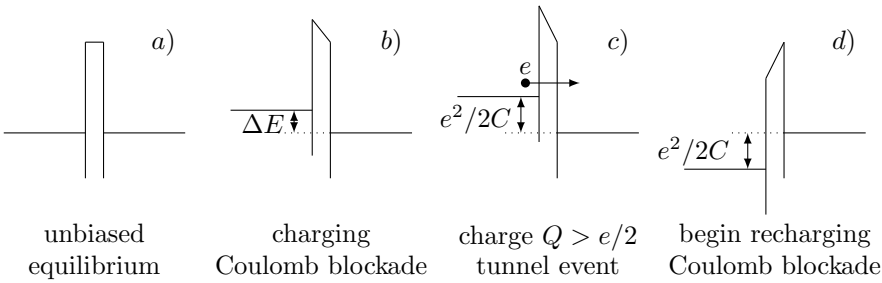

Figure 3.4: *Energy diagram of biased junction cycling through Coulomb blockade and single electron tunnel events. (a) To an unbiased junction (b) is applied a bias voltage, which slowly charges the junction. (c) When the bias voltage across the junction results to be higher than the junction's charging energy E_c, it is energetically favorable for an electron to tunnel through the junction. (d) after the tunneling, the bias voltage re-charges the junction through stage (b) until again stage (c) is reached. The cycle continues.*

liquid ^{4}He, used in low temperature refrigeration setups. The quantum energy fluctuations with above capacitance are $h/\tau = h/R_t C_t = 116 \times 10^{-24}$J = 116yJ = 725$\mu$eV, also less than the charging energy

3.4.2 Single current biased junction

Time to put this effect to use. When a tunnel barrier at equilibrium (fig. 3.4a) is connected to a constant current source, then charge will accumulate at the electrode, linearly ($I = dQ/dt$) in time (fig 3.4b) until the charge reaches and exceeds $e/2$, at which point a single tunneling event is energetically favorable and possible (fig 3.4c). If the tunneling happens, then the charge instantly diminishes by e, (fig 3.4d) the current source charges the barrier again, and the cycle restarts (fig 3.4b). The charging, reaching tunnel ability, tunneling, a recharging cycle is – as the name already suggests – cyclical and happens periodically. The current spikes observed are spaced in time by $\delta t = e/(dq/dt) = e/I$ and give a voltage oscillation in a sawtooth form across the junction with frequency

$$f_{SET} = I/e.$$

This is called *single electron tunneling oscillations*. Time or frequency are the easiest SI units to measure, because the task can be reduced to counting events instead of comparing physical units to references. In 2005,

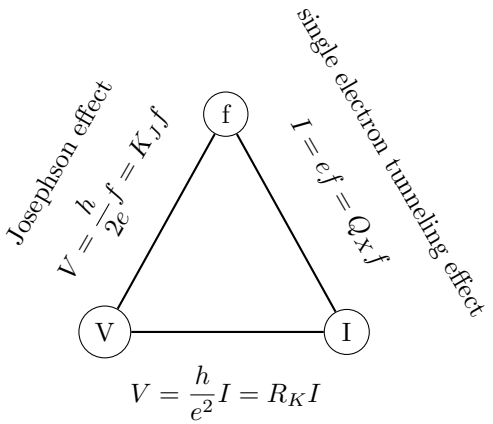

Figure 3.5: *Quantum metrology triangle, showing the SI units for voltage, current and frequency, the equations linking them together through constants, and the names of the underlying effects.*

Caesium fountain frequency standards may achieve a fractional frequency uncertainty of $\Delta f/f = 10^{-15}$[53]. Above f_{SET} equation is a very important relationship, because it links current and frequency through a simple constant, the elementary charge. It is the analog to the ac-Josephson effect: single electron tunnel events give rise to an oscillating voltage, i.e. the SET-oscillation, and whereas single flux quanta give rise to an oscillating current, i.e. the Josephson-oscillations, where the typical frequency is $f_{Bloch} = I/2e$ and describes the Bloch oscillations.

In metrology, the quantum metrological triangle (fig. 3.5) links voltage to frequency and to current through three constants which only depend on the two fundamental constants elementary charge e and Planck's constant h. In the Josephson effect, the Josephson constant $K_J = h/2e$, where the index $_J$ honors Nobel laureate Josephson[43, 44], links voltage to frequency with $V = K_J f = (h/2e)f$. In the quantum hall effect, the quantum resistance $R_K = h/e^2$, where the index $_K$ honors Nobel laureate von Klitzing[54, 55], links voltage to current with $V = R_K I = (h/e^2)I$. In the SET effect, the estimate of the elementary charge $Q_X = e$ links current to frequency with $I = Q_X f = ef$. As playful digression, the question can be asked if there will be a time when the estimate of the elementary charge will be called an constant with an eponym, such as

Thomson[23, 24] or Millikan[25] constant. The quantum metrology triangle is of course conceptually very appealing, except that in 2007 there is yet no "recommendation" by the Comité International des Poids et Mesures (CIPM) that would define the estimate of the elementary charge Q_X, a thing that has been done for both K_{J-90} and R_{J-90} in 1988[56, 57]. The "closing" of the triangle is an ultimate goal, and could be achieved by having an implementation of the complete quantum metrology triangle in a single experiment, where the three effects happen and are measured simultaneously, and the output of one effect's experiment is the input to the following effect's experiment. This would allow for the verification of coherence of the constants involved in the three quantum phenomena[58]. The uncertainties of both K_{J-90} and R_{J-90} are currently in the range of 1 part in 10^7 for open (non-closed) triangle setups.

Single tunnel junctions are difficult to measure, because apart the junction formation itself determining its charging energy, there is not much control over the experiment. Above f_{SET} can be estimated from the pA range currents that are flowing to be in the GHz range, but the current cannot be throttled or increased, it is given by the transit time of the tunnel event.

A current biased single tunnel junction is not a particularly simple system as far as single charge tunneling is concerned. It is certainly of interest for the foundations of the field, but it is not suited for practical applications, since the requirements for a clear-cut Coulomb blockade are so difficult to realize experimentally. (from: Devoret *et al.* [59])

Therefore the simple system was enhanced, adding constraints to the electrons, that helped to make the Coulomb blockade observable. This was done by introducing the idea of an island, i.e. a small isolated zone, where to or where from the electrons would tunnel through a barrier, but which would remain a dead end otherwise. An example is the single electron box: a tunneling barrier put in series with a capacitor, and the zone between them is the island. The electrons may not tunnel through the capacitor, but they may tunnel through the tunnel barrier. If the junction requirements are met (E_c, k_BT, R_T) then the voltage applied to the capacitor controls the bias through the barrier, and electrons may be added or removed one by one, allowing for observation of charge quantization[60, 61].

The double junction is the most widely used charging effect or Coulomb blockade effect device in the experimental area.

This field (of single electron tunneling) really took off when it was recognized that $R \gg R_Q = h/e^2$ ensures the localization of each electron within a particular conducting island of the system at any particular instant. This fact shows that tunnel barriers with low transparency may effectively sup-

press the quantum-mechanical uncertainty of the electron location. Notice that only this suppression makes controllable single-electron manipulation possible. (In this sense single-electronics does not fall into the much advertised category of "quantum electronic devices". Of course, single-electron devices do use quantum properties of matter, but so do semiconductor transistors. (from: Likharev [62])

For metrology application, longer island cascades are preferred, such as for single electron pumps[28, 63], because that guarantees a higher uncertainty.

Single electron transistors (N=2 junctions in series) tend to be vulnerable to quantum fluctuations (in single-electron logic circuits, each event of this kind leads to a computation). Thus, it seems more reasonable to use arrays with larger N's as basic elements of these circuits. (from: Averin and Odintsov [64])

The last section documents how overcoming the limitations of a single current based junction lead to two junctions in series.

3.4.3 Double current biased junction

Consider two tunnel junctions in series. The most important difference to a single junction is not the doubling of the junctions, but the creation of an island (fig. 3.6), an area which is completely surrounded by insulator, an important conceptual addition transport-wise. To travel from the left

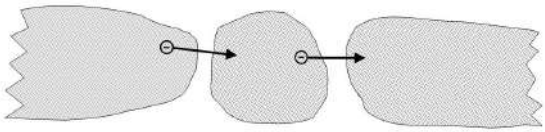

Figure 3.6: *Two junctions in series, defining between them an island, electrons have to travel across it in two tunnel events.*

electrode to the right electrode, electrons must tunnel to the island, and then off the island. A 'two single electron tunneling junctions' device has usually an additional 'normal' capacitor that couples to the island, as shown in fig. 3.7, without the possibility of quantum tunneling to and from this coupling capacitor. The names of those three device terminals are chosen – by analogy (the emotional cushion of familiarity) to the field effect transistor – drain, source and gate, respectively. The channel does not exist *per se*, but there is an island and the coupling through the gate terminal capacitor controls the transport. The name of the device is also

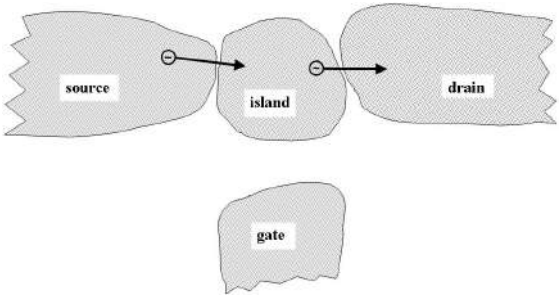

Figure 3.7: *Schematic single electron transistor, island at centre, source and drain separated by tunnel junctions, gate capacitively coupled.*

chosen by analogy: single electron tunneling transistor. Most of the time the term tunneling is omitted and single electron transistor SET is used.

An SET transistor island can be charged by tunneling across one junction and discharged by tunneling across the other junction, resulting a current through the device. The electrostatic energy of the circuit determines if transport happens or not. To determine the exact conditions, an electrical equivalent schema as in fig. 3.8 is helpful. Electrical engineers love to have an equivalent circuit of everything, because such an abstraction allows them to get a better understanding of the device. The physical island corresponds to the island on the equivalent schematic indicated by the dotted line, encompassing half of each tunnel junction, and half of the gate capacitor.

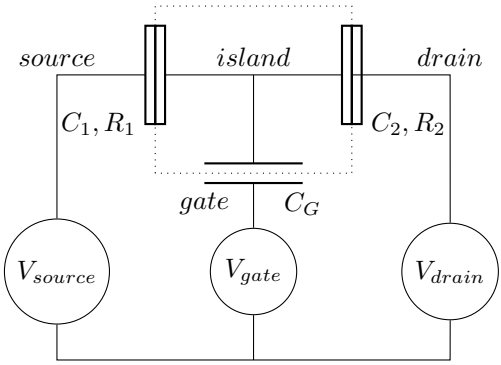

Figure 3.8: *Single electron transistor equivalent scheme*

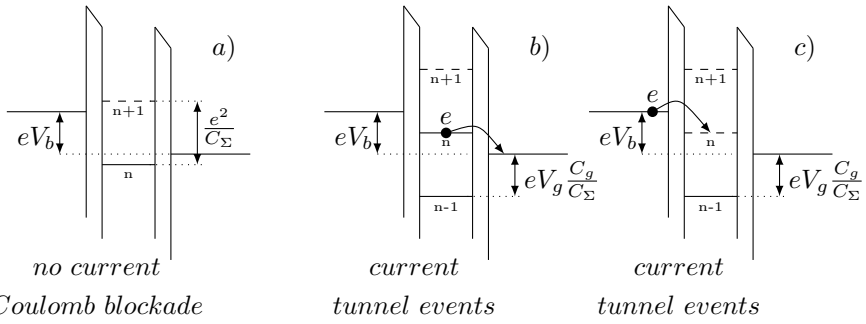

Figure 3.9: *Energy diagrams of SETs in and out of Coulomb blockade.*
a) *The island is occupied by n electrons. The energy level of the electron on the island is (due to the capacitive coupling with the gate electrode) below the conduction band of either electrode, and the charging energy guarantees that both junctions are in Coulomb blockade, i.e. tunneling through the left junction to the island would have to increase the electron's energy to reach $n+1$ charges of the island, which is energetically unfavorable and therefore not done, $n+1$ remains unoccupied.*
b) *Changing the gate voltage changes the energy level of the island. It is now energetically possible for the the n-th electron on the island to tunnel off the island through the right junction. After that, both the $n+1$ and n level are unoccupied. The island is occupied by $n-1$ electrons.*
c) *Now it is now possible for the electron on the left electrode to tunnel onto the island onto the n level, but $n+1$ remains unoccupied. The island regains an electron and is again occupied by n electrons, which would immediately tunnel off the island again if the gate bias is not lowered, and return to state b) and indiscernible from state b). The cycle of transitions b)→c) and c)→d) is established and a net current results, the SET is conductive.*

In fig. 3.9 energy diagrams of a double junction are shown. The junction is biased with V_b. In a) the double junction is shown in Coulomb blockade state, because the voltage applied to the gate sets the electrostatic energy of the island such that no tunneling can happen, while in b) and c), a current can flow (details in the caption). What happens inside the double junction is best viewed through a stability plot (fig. 3.10) and with explanation of the tunneling processes involved (fig. 3.11), but for a quantitative view, first the voltages governing the SET must be calculated.

3.4.4 Orthodox theory

The orthodox theory is a term used to refer to a set of assumptions that allow for calculation of charging effects for single electron tunneling devices. They were first formulated by Averin and Likharev[52, 65]. There is no unambiguous agreement in the literature on which assumption exactly is part and which is not. Assumptions made are:

- The dimensions and shape of the tunnel junctions are neglected.
- The duration of the electron tunneling process through the barrier is zero (or shorter than the time between two tunnel events).
- The duration of charge redistribution inside of the electrodes after tunneling is zero (or shorter than the time between two tunneling events), so that the system can get back to equilibrium.
- An electron tunnels immediately if the conditions for tunneling are favorable.
- There is no cotunneling, i.e. only one electron tunnels at the time.
- The tunneling events are correlated, i.e. if an electron enters through one junction onto the island, it will immediately exit the island by tunneling through the other junction, and if one electron moves, all the others are frozen.

The assumptions allow for a description on how a single electron tunneling device works, but it does not allow to establish a circuit model that could be easily simulated[66].

3.4.5 Energy calculation

To understand how an SET works, the electrical circuit is traditionally analyzed for the change of its energy after an electron has tunneled, and since the energy must be negative to be favorable, the conduction thresholds can be found for each junction, which allows to draw a stability plot as in fig. 3.10. This calculation has been done before in various forms[65, 67, 68, 59, 69] usually with an astringent level of terseness. A more verbal development is given here. The intermediate goal is to calculate the electrostatic energy stored in the two junctions and capacity surrounding the island. The circuit in fig 3.8 is formed of two tunnel junctions in series, defining between them the island. The island is capacitively coupled to the gate. The two tunnel junctions connect to source

and drain electrodes, the island–source junction is baptized "junction 1", and the island–drain junction is called "junction 2", and all the attributes of the respective junctions are called with those indices, i.e. capacitance, resistance, voltage, charge, number of electrons, etc. .

The total capacitance of the island is $C_\Sigma = C_1 + C_2 + C_g$. Assuming that the drain is grounded ($V_d = 0$), then a bias voltage V_b will bias the two junctions with V_1 and V_2, respectively, where $V_b = V_1 + V_2$. Instead of using V_{source} and V_{drain}, the potentials can be compound together in a voltage V_{bias} which spans across source and drain. Thus on the source $(1-f)V_{bias}$ and on the drain $-fV_{bias}$ are applied, where $0 \leq f \leq 1$, and chosen to accommodate for two standard cases of the drain grounded or asymmetrical bias ($f = 0$) (as used by Averin[45]) and antisymmetrical applied bias ($f = 0.5$) (as by Ingold[68]). For the reminder of the calculation, V_b will be used, which is the voltage applied to the source terminal, while the drain terminal remains grounded. V_b can be interpreted as V_{source} or as V_{bias} (with $f = 0$ for $(1-f)V_{bias}$).

The charge on the island q can be expressed in two ways, once from the point of view of the island, and once from the point of view of the device terminals. The charge on the island $q = -ne + q_0$ is composed of the number of electrons n present on the island, and of the background charge q_0, which accounts for any initial charge offset of the island, such as neglected capacitive coupling to the substrate or other structures, stray couplings, or random ions close to the island. The background charge q_0 can take any value, but the parts of q_0 which are an integer multiple of e can't be distinguished from additional electrons on the island, which leads to the practical limitation of $|q_0| < e$. The charge as seen by the device terminals is $q = -q_1 + q_2 + q_g$, with the number of electrons q_1 entering the island through junction 1, the number of electrons q_2 exiting the island through junction 2, and the polarization charge $q_g = C_g(V_g - V_2)$ that the island receives from the gate electrode. This yields:

$$q = -q_1 + q_2 - q_g = -ne + q_0$$

Substituting charges $q_i = C_i V_i$ by their capacity-voltage product:

$$-C_1 V_1 + C_2 V_2 - C_g(V_g - V_2) = -ne + q_0$$

Solving for V_2 yields sequentially:

$$-C_1(V_b - V_2) + C_2 V_2 = -ne + q_0 + C_g(V_g - V_2)$$

$$V_2(C_1 + C_2 + C_g) - C_1 V_b - C_g V_g = -ne + q_0$$

$$V_2 = \frac{-ne + q_0 + C_1 V_b + C_g V_g}{C_\Sigma} \tag{3.4.1}$$

and by analogy:

$$V_1 = \frac{+ne - q_0 + (C_2 + C_g)V_b - C_g V_g}{C_\Sigma} \tag{3.4.2}$$

The electrostatic energy stored on the island is the sum of the electrostatic energies stored on the two junctions and the gate capacitor.

$$E_c = \frac{q_1^2}{2C_1} + \frac{q_2^2}{2C_2} + \frac{q_g^2}{2C_g}$$

The charges are substituted through $q_i^2/2C_i = \frac{1}{2}C_i V_i^2$ and the voltage V_1 through $V_1 = V_b - V_2$. The capacitance only polarizes up to $V_g - V_2$ of the applied voltage V_g.

$$= \frac{C_1}{2}(V_b - V_2)^2 + \frac{C_2}{2}V_2^2 + \frac{C_g}{2}(V_g - V_2)^2$$

$$= \frac{C_1}{2}V_b^2 + V_2^2(\frac{C_1}{2} + \frac{C_2}{2} + \frac{C_g}{2}) + \frac{C_g}{2}V_g^2 - V_2(C_1 V_b + C_g V_g)$$

The term $C_1 V_b + C_g V_g$ exists in eq.(3.4.1), and therefore it is replaced by $V_2 C_\Sigma + ne - q_0$ to give:

$$= \frac{C_1}{2}V_b^2 + \frac{C_g}{2}V_g^2 + V_2^2(\frac{C_\Sigma}{2}) - V_2(V_2 C_\Sigma + ne - q_0)$$

This yields after shaking the tree algebraically, but determinedly:

$$E_c = \frac{C_1}{2}V_b^2 + \frac{C_g}{2}V_g^2 + \frac{(-ne + q_0)^2}{2C_\Sigma} + \frac{(C_1 V_b + C_g V_g)^2}{2C_\Sigma} \tag{3.4.3}$$

Interestingly, only the third term depends on the number of charges on the island, a convenient fact when comparing energies before and after tunneling events.

To obtain the total energy of the system, the work done by the voltage source to move electrons through the junction, i.e. $W = V_i \Delta q$ needs to be included. When an electron tunnels through a junction on to the island, then the island potential changes by e/C_Σ. The two junction's and the capacitor's charge change by eC_i/C_Σ. This polarization change must be compensated by the voltage sources. The work done by the sources attached to the junction and capacitor j to compensate the polarization

for the "receiving" of charge is $-eV_jC_j/C_\Sigma$. The work done by the source attached to the junction through which the "tunneling" is happening k, in order to compensate the polarization for the "receiving" of charge, is $eV_b(1 - C_k/C_\Sigma)$ [10].

If an electron tunnels through the first junction on to the island, then the island potential changes by e/C_Σ. The charge on the gate capacitor changes by $-eC_g/C_\Sigma$ and the gate voltage source works $W_g = -eV_gC_g/C_\Sigma$ to reestablish the polarization on the outer, off-island side of the capacitor. The drain voltage on junction 2 is assumed to be grounded, therefore no work is done there. The source biasing the tunneling junction 1 supplies to junction 2 a charge of eC_2/C_Σ and to the gate capacitor a charge of eC_g/C_Σ, totaling $e(C_2 + C_g)/C_\Sigma = e(1 - C_1/C_\Sigma)$. Therefore the work to bias junction 1 is $W_{b1} = eV_b(C_2 + C_g)/C_\Sigma = eV_b(1 - C_1)/C_\Sigma$. The work to add n_1 electrons through junction 1 is the sum of the works supplied by the voltage sources biasing junction 1 and the gate:

$$W(n_1) = W_g + W_{b1} = -n_1(\frac{e}{C_\Sigma}(-C_gV_g + (C_2 + C_g)V_b)).$$

For junction 2, the gate voltage source work remains the same. The tunneling junction 2 is grounded (no source). The source that is biasing tunnel junction 1 supplies a charge of eC_1/C_Σ and work of $W_{b2} = eV_b(C_1)/C_\Sigma$. The work to add n_2 electrons through junction 2 is

$$W(n_2) = W_g + W_{b2} = -n_2(\frac{e}{C_\Sigma}(C_gV_g + C_1V_b)).$$

The free energy of the system is the charging energy minus the work done by the voltage sources:

$$F = E_c - W$$

and after introducing the number of electrons tunneling through each junction it turns into:

$$F(n_1, n_2) = E_c - W(n_1) - W(n_2).$$

Tunneling can only happen if the energy after the tunneling is lower than before the tunneling, that means the change in free energy must negative,

$$\Delta F \leq 0 \Longleftrightarrow \Delta E \leq 0$$

[10] $C_\Sigma = C_1 + C_2 + C_g \rightarrow C_2 + C_g = C_\Sigma - C_1 \rightarrow e(C_2 + C_g)/C_\Sigma = e(C_\Sigma - C_1)/C_\Sigma = e(1 - C_1/C_\Sigma)$

When the charging energy of eq.(3.4.3) is inserted into the expression, it survives the making of the difference only in its third term, which is $(-ne+q_0)^2/2C_\Sigma$, because it is the only term carrying the dependency on number of electrons on the island. The difference of the third term of E_c,

$$\Delta E_c = \frac{[-(n+1)e+q_0]^2}{2C_\Sigma} - \frac{(-ne+q_0)^2}{2C_\Sigma}$$

reduces down to

$$= \frac{e^2+2e(ne-q_0)}{2C_\Sigma} = \frac{e}{C_\Sigma}[\frac{e}{2}+(ne-q_0)].$$

Based on the orthodox theory, only one junction has electrons tunneling through it, and therefore only one of the two work expressions $W(n_1)$ and $W(n_2)$ will change, thus only the changing one will survive the taking of the difference of ΔF. The index of free energy pertains to the junction through which the tunneling is happening, while superscripts indicate addition(+) or subtraction(-) of charge through the junction:

$$\Delta F_1^\pm = F(n_1\pm1,n_2)-F(n_1,n_2) = \frac{e}{C_\Sigma}(\frac{e}{2}\pm[+ne-q_0+(C_2+C_g)V_b-C_gV_g])$$

$$\Delta F_2^\pm = F(n_1,n_2\pm1)-F(n_1,n_2) = \frac{e}{C_\Sigma}(\frac{e}{2}\pm[-ne+q_0+C_1V_b+C_gV_g])$$

It is noticeable that the right side terms, except for a factor of C_Σ, correspond exactly to the junction voltages V_1 and V_2 derived in equations (3.4.2) and (3.4.1), i.e.

$$\Delta F_1^\pm = \frac{e}{C_\Sigma}(\frac{e}{2}\pm C_\Sigma V_1) = \frac{e^2}{2C_\Sigma}\pm eV_1 \tag{3.4.4}$$

$$\Delta F_2^\pm = \frac{e}{C_\Sigma}(\frac{e}{2}\pm C_\Sigma V_2) = \frac{e^2}{2C_\Sigma}\pm eV_2. \tag{3.4.5}$$

Electrons may tunnel if it is energetically favorable, i.e. if no energy is gained during the process. Developing for the first junction:

$$\Delta F_1^\pm < 0$$

$$\frac{e}{C_\Sigma}(\frac{e}{2}\pm[+ne-q_0+(C_2+C_g)V_b-C_gV_g]<0$$

$$\frac{e}{2} < \mp[+ne-q_0+(C_2+C_g)V_b-C_gV_g]$$

$$\frac{e}{2} \pm ne < \mp[-q_0 + (C_2 + C_g)V_b - C_g V_g]$$

$$e(n \pm \frac{1}{2}) > \pm[-q_0 + (C_2 + C_g)V_b - C_g V_g] \tag{3.4.6}$$

and by analogy:

$$\Delta F_2^{\pm} < 0$$

$$e(n \pm \frac{1}{2}) > \pm[+q_0 + C_1 V_b - C_g V_g] \tag{3.4.7}$$

which allows to construct following two inequalities as boundary conditions wherein Coulomb blockade will be observed:

$$e(n + \frac{1}{2}) > \pm[-q_0 + (C_2 + C_g)V_b - C_g V_g] > e(n - \frac{1}{2})$$

$$e(n + \frac{1}{2}) > \pm[+q_0 + C_1 V_b - C_g V_g] > e(n - \frac{1}{2}).$$

These inequalities can be observed directly when the experimental data is mapped into V_g versus V_b plots, with the I_{ds} current through the junction as third axis. The bias voltages for both junctions can be isolated, conduction onset is when:

$$V_{b1} > \pm(\frac{-q_0 - e(n \pm \frac{1}{2})}{C_2 + C_g} - \frac{C_g}{C_2 + C_g} V_g) \tag{3.4.8}$$

$$V_{b2} > \pm(\frac{q_0 - e(n \pm \frac{1}{2})}{C_1} - \frac{C_g}{C_1} V_g). \tag{3.4.9}$$

Those plots are called stability plots, as fig. 3.10, and the Coulomb blocked areas are called, due to their shape, Coulomb diamonds. It is also possible to start from equations (3.4.4) and (3.4.5), solve them for the condition "< 0", and obtain from

$$\Delta F_1^{\pm} = \frac{e}{C_\Sigma}(\frac{e}{2} \pm C_\Sigma V_1) < 0$$

$$\pm V_1 < \frac{e}{2C_\Sigma} \tag{3.4.10}$$

and by analogy

$$\pm V_2 < \frac{e}{2C_\Sigma}. \tag{3.4.11}$$

A current will flow through an SET if the voltage across one of the junctions exceeds $e/(2C_\Sigma)$, and the voltages across the tunnel junctions V_1 and V_2 depend both on bias voltage V_b and gate voltage V_g. A stability plot of

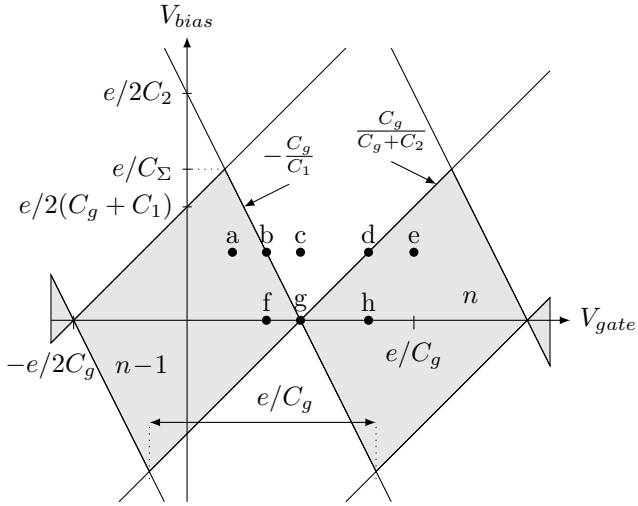

Figure 3.10: *Stability plot, V_{gate} vs V_{bias}, slopes, x and y-axis intercepts allow to extract all capacitance values of the island C_1, C_2, C_g. The two trapezoidal areas underlined with gray, delimited by the oblique lines, carrying the number of electrons n and $n+1$ are called Coulomb diamonds, the zone where the conduction is suppressed and no current flows through the island. If the junctions are not perfectly symmetrical, which is quasi always the case, then the diamond or rhomboid is deformed to a trapezoid.*

an SET such as on fig. 3.10 traces gate voltage V_{gate} sweeps against bias voltage V_{bias} sweeps, with the drain source current I_{sd} as third variable. The central diamond shaped zones on the plot, delimited by the lines of conduction start and stop, indicate the areas of Coulomb blockade, were no current flows, and they are called Coulomb diamonds. The diamonds are periodic by e/C_g along the gate voltage V_g axis, and thus allow to extract the gate capacitance C_g value. Increasing the gate voltage increases the number of electrons on the island. The edges of the Coulomb diamonds, i.e. the lines which delimit the zones where conduction is blocked, form straight lines, and their slopes, $-C_g/C_1$ for the negative, $C_g/(C_g+C_2)$ for the positives, allow to determine the values of the tunnel junction capacitors C_1 and C_2. The V_b threshold above which no more Coulomb blockade is possible has an y-axis intercept of e/C_Σ, and allow to deduce the sum of all island capacities C_Σ. An example of experimental data showing Coulomb diamonds can be found in fig. 6.14.

The schematic stability plot of fig. 3.10 contains black dots labeled **a**

through **h** which are special cases worth being discussed one by one with an energy diagram, which is done in fig. 3.11-a through 3.11-h, in order to get a good understanding of how the charging energy of the island is modulated through the gate voltage. If the double junction is in Coulomb blockade, then the static situation is given with a single energy diagram. If current is flowing, two diagrams are given, decomposing the tunneling through the island into a 'tunneling off' and a 'tunneling onto' the island step. This is the same electron tunneling, according to the orthodox theory. Energy diagrams are always an abstraction of reality, but give a good look and feel for the situation. The cases **a** through **e** have all the same bias voltage V_b but different, increasing from top to bottom gate voltages V_g. The examples start inside of the Coulomb diamond with $n-1$ electrons on the island, at location **a**, (fig. 3.11-a), with a gate voltage V_g such that the charging energy E_c defining the attainable levels on the island is aligned in a way that it blocks tunneling through the left junction. There is no current flowing through the island. By increasing the gate voltage V_g to the point where the energy level of the island with n electrons and the energy level of the left electrode align, as at location **b**, the starting point for conduction is reached. Here, the n-th state on the island can be filled from the left electrode (fig. 3.11-b right). The n-th state on the island can then tunnel off the island through the right junction (fig. 3.11-b left). The double junctions cycles between the two transports, with an electron being shuttled from the left electrode through the island to the right electrode, resulting in a current. Increasing the gate voltage V_g more as in **c** pushes the energy level down (fig. 3.11-c), until the threshold where conduction is about to stop as in **d** (fig. 3.11-d) is reached. Further increasing the gate voltage V_g move the SET back into Coulomb blockade as in **e**, with no current flowing (fig. 3.11-e).

The cases **f** through **h** (fig. 3.11-f through 3.11-h) have all zero bias voltage $V_b = 0$ but different, increasing gate voltages V_g. Locations **f** and **g** are both in Coulomb blockade, while location **g** is conducting, but because of zero bias voltage V_b, the tunneling may be in either direction, and the net current is zero. The flattening in the I-V characteristic is the first signature that a structure sees charging effects, and a good indicator that Coulomb blockade is happening. The example of an SET with symmetrical junctions, i.e. identical R_i and C_i (simpler special case), is given in fig. 3.12. It's caption describes how the two I-V plots correspond each to the data in a single vertical line of fig. 3.10.

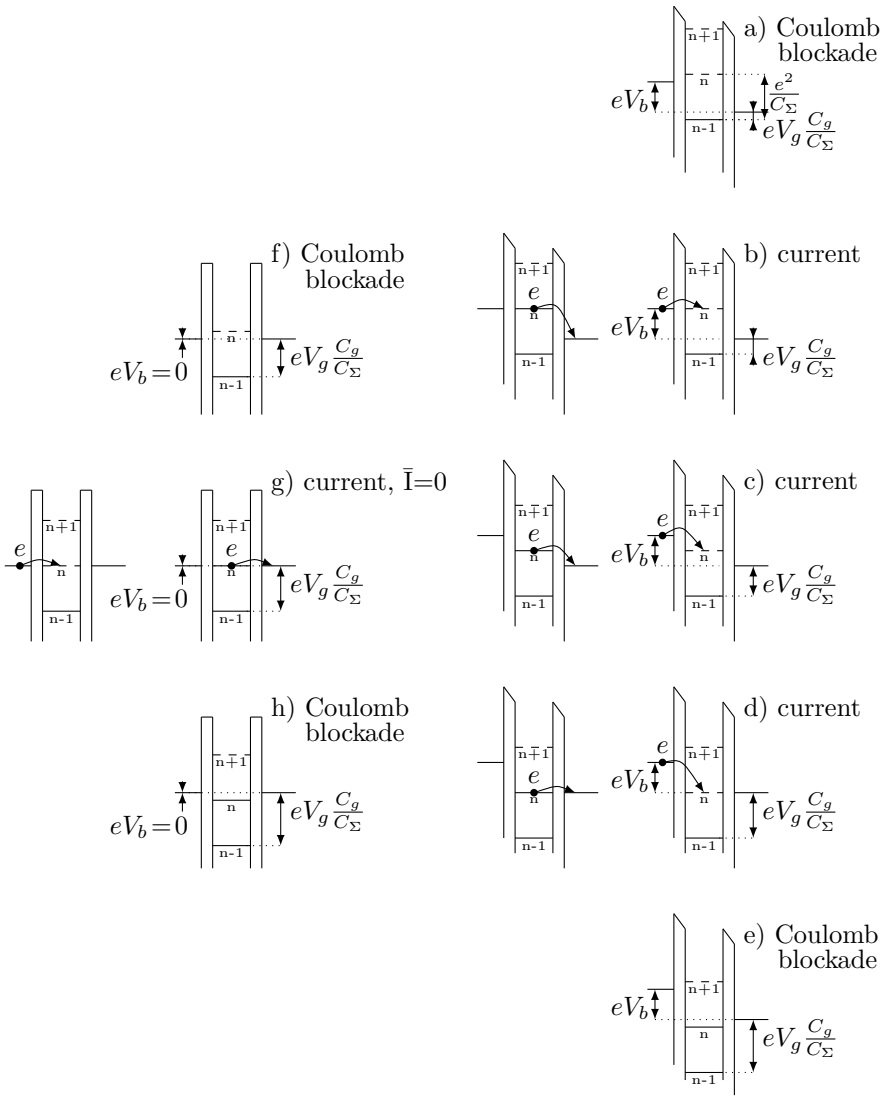

Figure 3.11: *Selected processes in the stability plot. Dashed lines indicate unoccupied levels on the island. Detailed explanation in the body of text.*

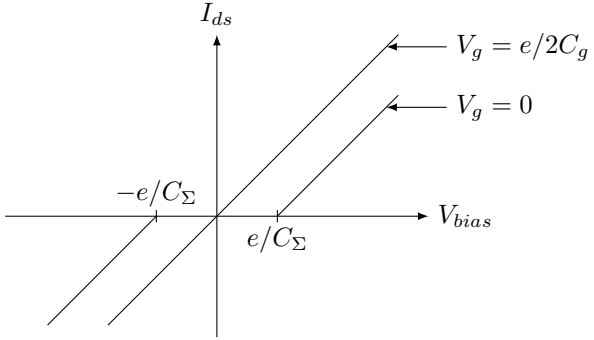

Figure 3.12: *$I_{ds}-V_b$ characteristic for an SET with symmetrical junctions, i.e. $R_1 = R_2$ and $C_1 = C_2$. When the gate voltage is $V_g = 0$, then the current is blocked for $|V_b| < e/C_\Sigma$. This I-V characteristic is periodic every $V_g = ne/C_g$ and corresponds in fig. 3.10 to traces passing along vertical lines through the centers of the diamonds. When the gate voltage is $V_g = e/2C_g$, then the current is flowing for any V_b. This I-V characteristic is periodic every $V_g = e/2C_g + ne/C_g$ and corresponds in fig. 3.10 to traces passing along vertical lines through point **g** and following x-axis intersects.*

3.4.6 Other tunneling processes

The orthodox theory (subsect. 3.4.4) makes a set of assumptions. The processes coming into existence by removing those hypothesis are cotunneling, i.e. more than one electron may tunnel at the time, and non-correlation, i.e. an electron may enter through one junction and does not have to immediately exit the island by tunneling through the other junction, but may be part of a tunneling cycle containing several states. When one electron enters through one junction, and a different electron leaves the island through the other junction, then this is *co-tunneling of two electrons* (term describing the phenomenon), or *macroscopic quantum tunneling of charge*, abbreviated q-mqt (term describing the elementary process)[70]; the terms are used synonymously. In elastic cotunneling, the electron is transported through a virtual charged state of the island, and temporarily violating the energy conservation, and after tunneling the island is again in its initial ground state. When the dot is left in an excited state, then this is called inelastic cotunneling, which requires a second tunnel process which initiates at this excited state to bring the island back to the initial ground state. Cotunneling is a high interest area[71], but in the case of the measurements done with the structures fabricated during this thesis, such as fig. 6.12, no

tunneling processes other than simple Coulomb blockade ones can be distinguished, mostly due to the noise in the measurement. When cooling to lower temperatures to reduce the "smearing out" of the charging effect due to thermal activation, as in fig. 6.16, at 403mK, a magnetic field of 0.5T was applied to suppress the superconductivity of Al ($T_c = 1.18$K), which is known to suppress inelastic cotunneling processes[72], which makes that they cannot be observed, again. Consequentially, higher order tunneling processes were not further investigated.

3.5 Superconductivity

Superconductivity is the absence of electrical resistance and the exclusion of interior magnetic field, and occurs in some materials at low temperatures (considering only type I superconductors). A free electron in a normal conducting metal behaves as a quasiparticle. For electrical transport this signifies that electrons may collide with the lattice, and this manifests itself macroscopically as resistivity. The lattice itself oscillates due to the thermal energy, propagating vibrations are phonons. At low temperatures, a Cooper pair[73] is formed by electron-phonon interaction. While electrons repel each other due to their identical charge, an electron attracts the positive ions of the lattice. A moving electron deforms the crystal lattice around it by this attractive force, and creates an area of greater positive charge, which in its turn is attractive for other electrons. Two electrons may get bound together and become a Cooper pair by this mechanism, called electron-phonon interaction. Only electrons close to the Fermi level may be paired into Cooper pairs. A bound Cooper pair in a superconductive metal has a lower energy compared to the Fermi level of the metal in normal conductive state. The difference is called the superconductive energy gap Δ. To break up a Cooper pair, an energy of 2Δ is needed, and as long as the lattice cannot supply this energy, a Cooper pair moves through the lattice without any resistance[11]. Superconductive electron tunneling effects are an ideal experimental verification and illustration of the phenomenonical description of the density of states dependence of the energy gap predicted by the Bardeen-Cooper-Schrieffer (BCS) theory of superconductivity[40].

[11] Subatomic particles fall into two classes, based on their statistical behavior. Those particles to which the Pauli exclusion principle applies are called fermions and follow Fermi-Dirac statistics; those that do not obey this principle are called bosons and follow Bose-Einstein statistics. Free electrons are fermions, and Cooper pairs are bosons.

3.5.1 Energy scales

In a superconducting SET the **charging energy** E_C is no longer the only energy scale important for transport, rather it is one in three, the two other being the **Josephson energy** E_J, and the **energy gap** Δ, which are discussed in the following one after the other.

The Josephson energy is related through $E_J = \hbar I_c/2e$ to the junction's (dc Josephson effect) critical current I_c, the maximum current of the zero voltage supercurrent $I_s = I_c \sin \Delta\phi$, where $\Delta\phi$ is the phase difference of the Cooper pair wave-function between the electrodes. The Ambegaokar-Baratoff formula for superconducting tunnel junctions[74, 75] allows to estimate the critical current I_c with $I_c R_n = (\pi\Delta/2e)\tanh(\Delta/2kT)$[76] where R_n is the normal state resistance. For $T = 0$ it reduces to $I_c R_n = \pi\Delta_{Al}/2e$, where Δ_{Al} is the energy gap of Aluminum, and combines to the Josephson energy estimation formula of

$$E_J = \hbar/2e \cdot \pi\Delta_{Al}/2eR_n = h\Delta_{Al}/8e^2R_n. \tag{3.5.1}$$

For large area junctions, i.e. much larger than thousands of nm^2, the Josephson energy exceeds the charging energy, $E_J \gg E_C$, and transport is dominated by the supercurrent, the double junction is in the Josephson regime. For small junctions[12], the situation is reversed, $E_J \ll E_C$, the supercurrent is suppressed, and the tunneling of single electrons is limited by charging effects, i.e. sequential tunneling of quasiparticles, a behavior identical in phenomena to the normal or non-superconductive SET.

The energy gap Δ was introduced above with the Cooper pairs. At the critical temperature, where the onset for superconductivity is, it opens up around the Fermi energy level, then widens to be fully open at $T = 0$K. Energy diagrams are the tool of bandgap engineering. Junctions involving normal and superconductors can be equally intuitively understood with density of state diagrams, however, the information is for the junction interface, and not valid for the junction depth as it is with a semiconductor model.

When the temperature is $T > 0$, then thermally excited phonons with energy comparable to twice the energy gap Δ can unbind the bound electrons of a Cooper pair into two normal electrons (scattering and destroying the pair). One of the two freshly unbound electrons goes above the gap as quasiparticle, the other one remains energetically below the gap, where it continues to be part of the superconducting state, and very rapidly is

[12] Letter and review titles use the terms *small tunnel junction*[45] and *ultra small tunnel junction*[77] to indicate junction size as distinguishing feature of their work.

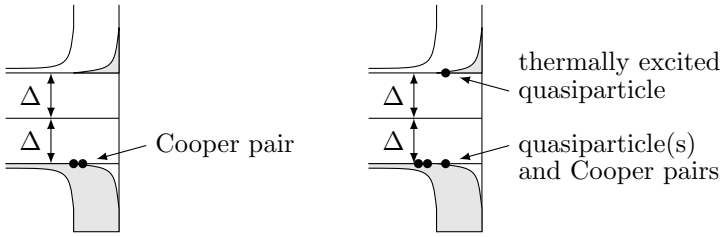

Figure 3.13: *Density of state diagram, Cooper pair and quasiparticle.*

bound and again unbound to other electrons. In a density of states diagram, as in fig. 3.13, the electrons in states above the energy gap of height 2Δ, are referred to as normal electrons or quasiparticles.

In the states below the energy gap, the electrons are paired, and referred to as Cooper pairs or as superconducting electrons. This means that for conduction processes involving quasiparticles, only top electrons above the gap are available. As soon as "normal" states on the other side of the tunnel barrier become available, also the Cooper paired superconducting electrons contribute to the tunneling current. To break up a Cooper pair, an energy 2Δ is needed, and in the density of state diagram, this is represented by the energy gap extending on either side of the Fermi Energy. The energy gap depends on the temperature with $\Delta(T)/\Delta(0) \approx 1.74(1 - T/T_c)^{1/2}$ [76], and the approximation $\Delta(0) = 1.76 k_B T_c$ can be used.

3.5.2 Superconductive transport

In a superconductor, electron transport is no longer exclusively done by quasiparticles, but also by Cooper pairs. To understand transport in a superconductive SET, first quasiparticles transport is discussed, because of the analogy with transport in a normal conductive SET. Then transport implicating also Cooper pairs is discussed.

3.5.2.1 Superconductive tunneling characteristic

In fig. 3.14, three types of junctions, namely normal–insulator–normal (NIN), normal–insulator–superconductor (NIS) and superconductor–insulator–superconductor junctions (SIS), are considered. On the left hand side, for all three cases, first the tunneling current through the junction is plotted against the bias voltage at $T = 0$. As temperature raises, normal

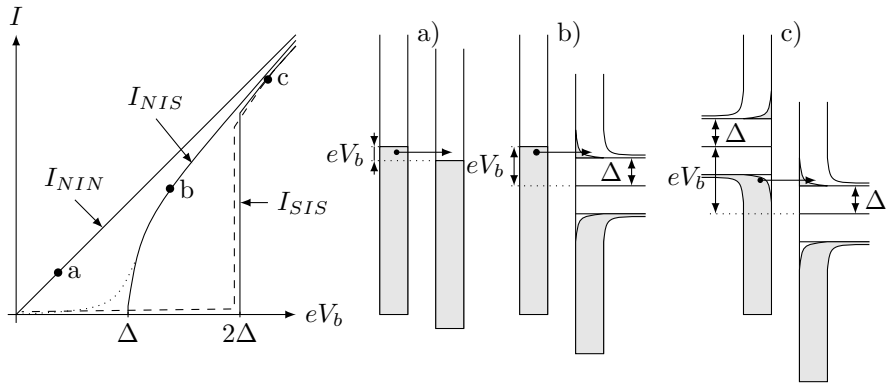

Figure 3.14: *Tunnel junction I-eV plot, with density of state diagrams. The currents in the I-eV plot are labeled I_{NIN} for a normal-insulator-normal junction (NIN), I_{NIS} for a normal-insulator-superconductor junction (NIS), and I_{SIS} for a superconductor-insulator-superconductor junction (SIS). The dotted line indicates I_{NIS} for $T > 0$, and the dashed line indicates I_{SIS} for $T > 0$. Dots labeled a, b and c in the I-eV plot are examined in density of state diagrams, each of them shortly after the onsets of conduction, which are at $V_b > 0$ for (NIN), at $V_b > \Delta/e$ for (NIS) and at $V_b > 2\Delta/e$ for (SIS). Below those bias voltages, no tunneling occurs, because there is either no bias (NIN) or because the energy gap impedes the tunneling (NIS & SIS). NB: Charging effects neglected, which is only correct for large junctions, i.e. $E_J \gg E_C$.*

states can be excited and contribute to the tunneling current for SIS tunneling in the same way as in NIS tunneling. This is shown as dashed and dotted lines. On the right side, the density of state diagrams are given, for all three cases shortly before a further reducing of the bias voltage V_b would render the electron tunneling impossible. Those limits are at $V_b = 0$ for NIN, at $V_b = \Delta/e$ for NIS and at $V_b = 2\Delta/e$ for SIS. Below those threshold voltages, there is not absence of tunneling, but tunneling is not exclusively based on quasiparticles, and it is orders of magnitude lower than quasiparticle tunneling.

3.5.2.2 Superconductive quasiparticle transport

To have electrons tunnel, and to move away from the zero bias current, the junction must be voltage biased. The device fabricated during this thesis is a SISIS-SET, and therefore the junction type of most interest here is the

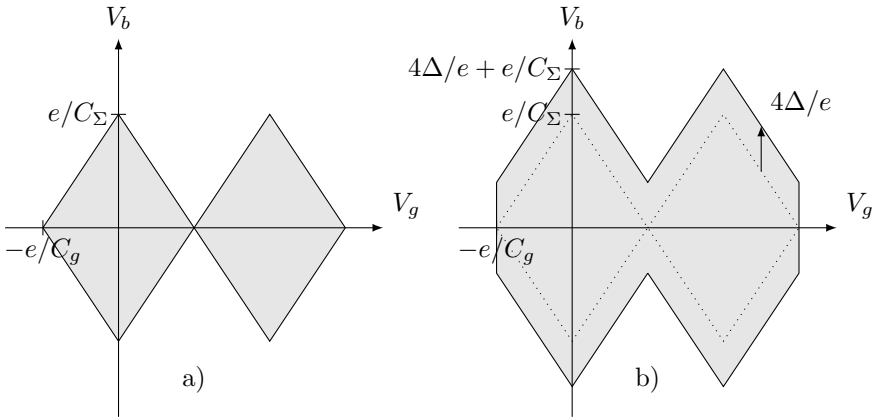

Figure 3.15: *Stability diagram superconductive SSET. The areas in gray tone are in Coulomb blockade. Diagram cropped to V_g ranging from $-e/C_g$ to $3e/C_g$, a) Coulomb blockade for normal conducting SET. b) Coulomb blockade for superconducting SET, the conduction threshold is offset by $4\Delta/e$.*

SIS junction, where due to the energy gap that opens around the Fermi energy level when superconductive, the bias needs to be at least $2\Delta/e$ to make tunneling through the insulator possible. The change in energy is 2Δ, because there are no quasiparticle states possible inside of the energy gap.

For two junctions in series, such as it is the case in an SET, this adds up to a necessary bias voltage of $4\Delta/e$. The direct consequence is that to have any electrons available for charging effects, the energy 4Δ must be supplied, before even single charge effects can start to happen. This results in the Coulomb blockade limit being increased by $4\Delta/e$ on either side of the voltage bias V_b axis, as shown in fig. 3.15. The bias must offset first the superconducting energy gaps of the two superconductive (SIS) junctions, and the charging energy caused by the island charge, which can be modulated by the gate voltage. The bias of $V_b > 4\Delta/e$ only allows for Cooper pairs to be broken up and to tunnel as quasiparticle through one of the junctions. Other than that offset, the single electron tunneling has the same behavior as a normal conductor.

Taking the bias voltage current onset inequalities from equations (3.4.8) and (3.4.9), and adding an offset corresponding for the bias of $V_b > 4\Delta/e$,

the following inequalities are obtained:

$$V_{b1s} > 4\Delta/e \pm (-q_0 - e(n \pm \frac{1}{2}) - C_g V_g)/(C_2 + C_g) \tag{3.5.2}$$

$$V_{b2s} > 4\Delta/e \pm (+q_0 - e(n \pm \frac{1}{2}) - C_g V_g)/C_1. \tag{3.5.3}$$

Considering junction 2, and starting with no background charge q_0, an empty ($n = 0$) island, and a gate voltage $V_g = e/2C_g$, one finds the $V_b = 4\Delta/e$ offset, while for a gate voltage of $V_g = 0$, the condition for the bias $V_b = 4\Delta/e + e/2C_1$ is found. $e/2C_1$ is the y-intersect of the junction 2 line, and when the SET is symmetric, then this reduces to e/C_Σ.

Above formulation is equivalent to the more general formulation for the threshold value for sequential tunneling in a (symmetric) superconducting SET given in ref. [78], where the sequential tunneling of quasiparticles conduction threshold is the smallest value of

$$V_{seq} = \frac{4\Delta}{e} + \frac{4E_c}{e}(\frac{1}{2} + n \pm \frac{Q_0}{e}), \tag{3.5.4}$$

where the island polarization charge $Q_0 = C_g(V_g - V_b)$ can be chosen by the gate voltage V_g.

In an attempt to graphically illustrate quasiparticle transport in a SISIS structure when limited by the Coulomb blockade, the diagram of states was drawn in fig. 3.16. This warning is included: only quasiparticle tunneling is considered, the Cooper pair contribution to transport is neglected. The diagram shows that a small divergence from the shown situation will cut off electron tunneling, because the graphic is just at the onset of conduction, when for each junction the $2\Delta/e$ bias is applied. By its nature, this only shows conducting beyond the 4Δ energy threshold of Coulomb blockade.

The illustrating graphics for the case where the bias is further increased, up to almost the $4\Delta/e + 2E_c/e$ limit, is given in fig. 3.17, although is does no longer satisfyingly cut off all quasiparticles transport.

3.5.2.3 Josephson quasiparticle cycle and Singularity matching

As long as the bias voltage remains below the threshold voltage formulated for sequential tunneling in eq. (3.5.4), the superconductive SET is in Coulomb blockade, the sequential tunneling of quasiparticles is suppressed by the combination of the Coulomb blockade and the superconducting energy gap impeding the tunneling. But unlike as it is the case in the normal conductive state, there is still current flowing, although at a lower magnitude, and because of different transport types.

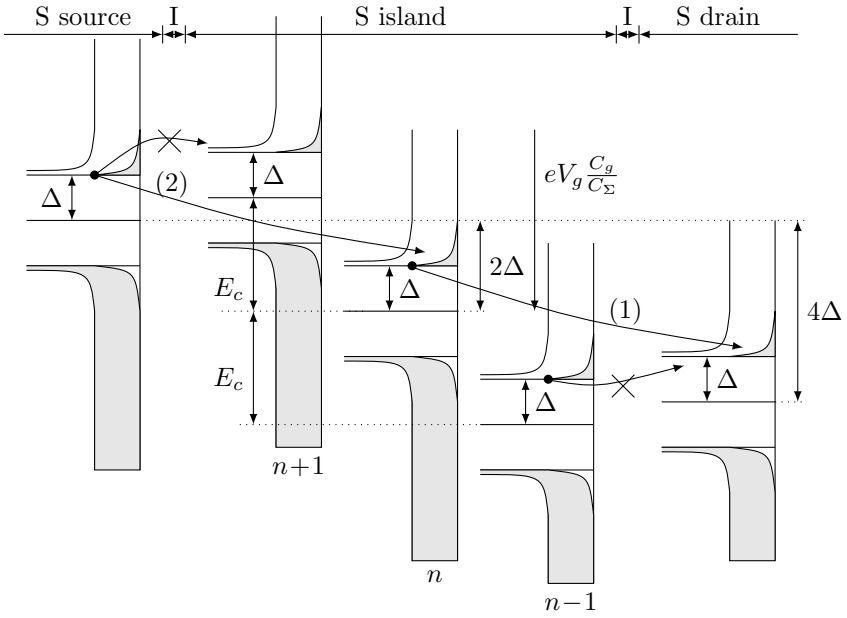

Figure 3.16: *SISIS* 4Δ *single electron tunneling density of states. The affiliation of each DOS diagram is indicated in the top. The island zone features three DOS diagrams, because the number of electrons on the island changes the energy offset to the left electrode.*
On the island state occupied with $n-1$ *electrons (right), the thermally excited quasiparticles above the energy gap cannot tunnel off the island to the drain electrode, because energetically unfavorable. On the source electrode, the thermally excited quasiparticles above the energy gap cannot tunnel to the unoccupied island state with* $n+1$ *electrons (meaning that the island has* n *electrons) because it would be energetically unfavorable.*
On the occupied island state with n *electrons (center), the thermally excited quasiparticles above the energy gap can tunnel off the island to the drain electrode, indicated by (1), because the sufficient bias* $2\Delta/e$ *is applied to tunnel through the barrier. On the source electrode, the thermally excited quasiparticles above the energy gap can tunnel to the unoccupied island state with* n *electrons (meaning that the island has* $n-1$ *electrons) indicated by (2), because the sufficient bias* $2\Delta/e$ *is applied to tunnel through the barrier. Starting with an occupied island state* n*, first (1) then (2) can happen, which leads to a cycle with current, where quasiparticles flow from source to drain. N.B.: Electron trajectories are arched for visibility, and do not imply temporary energy gain during tunneling. N.B.: Only quasiparticle tunneling is considered, the Cooper pair contribution to transport is ignored.*

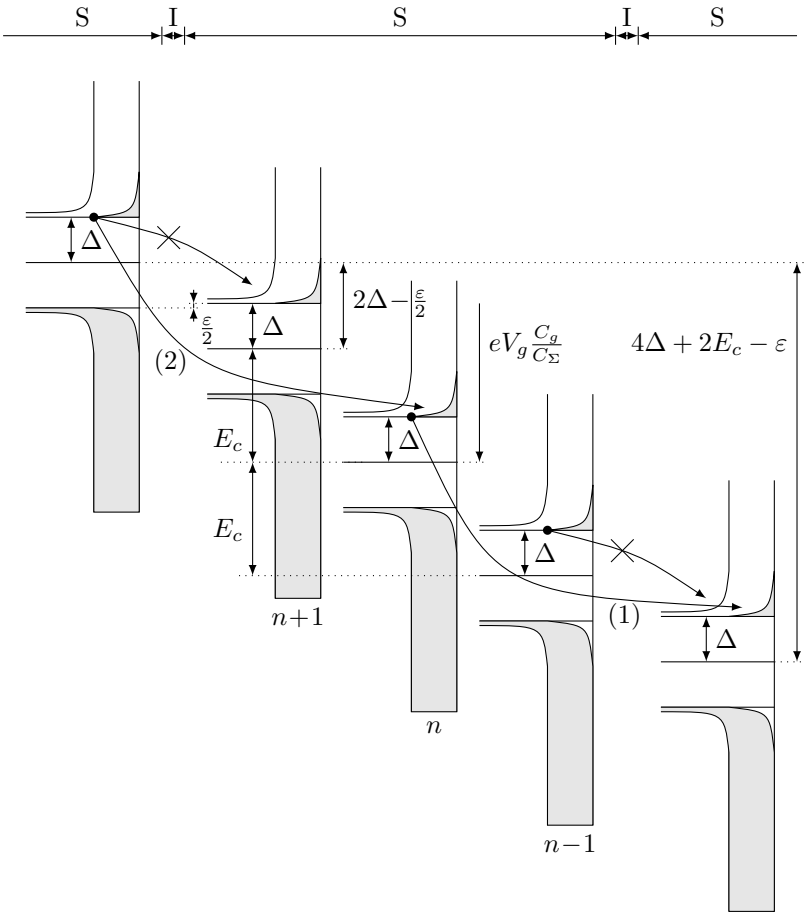

Figure 3.17: *SISIS $4\Delta+2E_C-\varepsilon$ single electron tunneling density of states. Similar situation as fig. 3.16, but with higher bias across source drain, but just ε below onset of conduction for any gate voltage. This makes that the $n-1$ island cannot empty to drain, and $n+1$ island cannot fill from source. But the n island can emptied through drain (process 1), then filled through source (process 2), which establishes a cycle. If voltage is increased by ε, then all island state can contribute to conduction.*

Two other threshold voltages are cited along with above sequential tunneling of quasiparticles [from [78] and [79, 80]]: The singularity matching (SM) peak predicted by Korotkov[81], where the density of state diagrams of one junction are aligned and thermally excited quasiparticles of empty states both above and below the energy gap may tunnel into the above and below states in the island, respectively. The bias voltage threshold is expected at

$$V_{SM} = \frac{4E_c}{e}(\frac{1}{2} + n \pm \frac{Q_0}{e})$$

and most pronounced between $2\Delta < V < 2\Delta + e/C_\Sigma$[81]. The Josephson quasiparticle (JQP) process first described by Fulton *et al.*[82] has first a Cooper pair tunnel through one junction either on or off the island, then two quasiparticles tunneling separately through the other junction off or on the island, with a threshold voltage of

$$V_{JQP} = \frac{4E_c}{e}(n \pm \frac{Q_0}{e}),$$

and a condition of being efficient between $2\Delta + e/2C_\Sigma < V_{JQP} < 2\Delta + 3e/2C_\Sigma$. Quasiparticle tunneling is blocked for both SM and JQP situations. But since the transport mechanism is not due to quasiparticles tunneling but based on Cooper pairs, there is a current. After tunneling onto the island, a Cooper pair may split up, and the electrons are in a state on the island, where it is energetically favorable for the quasiparticle to tunnel off the island. For zero bias tunneling, and for SM, the fig. 3.18 graphically explains the functioning through density of state diagrams.

Interestingly, there are currents observed at bias voltages below the Coulomb blockade, therefore not due to single electron tunneling effects, but due to other transport mechanisms.

In an SET of type superconductor-insulator-superconductor-insulator-superconductor (SISIS), pure Cooper pair tunneling (dc Josephson effect) near and at zero bias voltage is possible, a supercurrent [76] of Cooper pairs may flow coherently through the SET.

Furtherleading discussion of transport in SISIS type SET are done in papers by following authors: Fulton[82], Maassen van den Brink[83, 84], Hergenrother[85], Haviland[86], Nakamura[79, 80], Korotkov[81], Siewert[87, 88], Fitzgerald[89], Hadley[69], Manninen[78], Hadley[69], and their lecture is recommended.

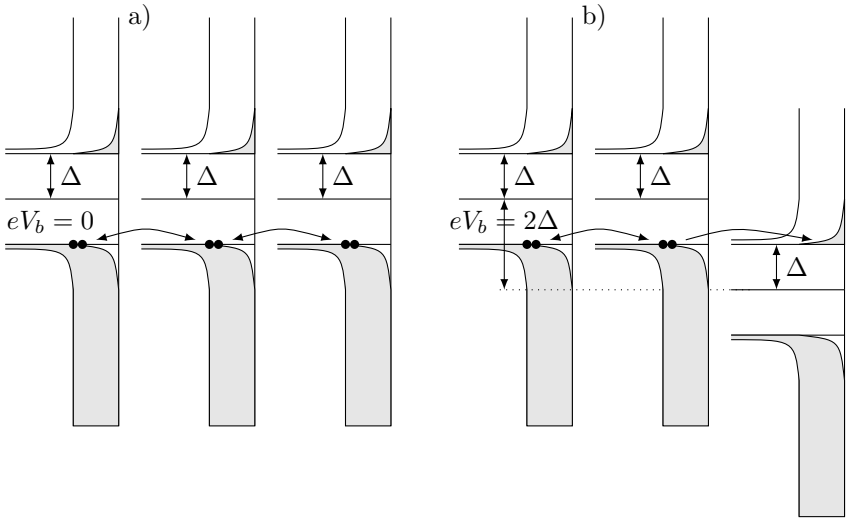

Figure 3.18: *SISIS zero bias CP, singularity matching (SM) density of states.*
a) Cooper pair zero bias tunneling by Josephson dc effect (CP) The states below the energy gap of the island are aligned with the states below the energy gap of ***both*** *electrodes. i.e. their Fermi levels are aligned, there is no bias applied.*
b) The states below the energy gap of the island are aligned with the states below the energy gap on the left electrode, i.e. their Fermi levels are aligned. Quasiparticles may tunnel on and off the island through the right electrode. Quasiparticles may tunnel off the island on to right electrode. The continuous removal through the right junction will result in a current. (Also called quasiparticle extraction in the case of non-equal gap superconductors[76].)
N.B.: Electron trajectories are arched for visibility, and do not imply temporary energy gain during tunneling.

3.5.3 Even-odd number parity effect with superconducting island

When the charging energy is plotted against the island charge it yields fig. 3.3. When the charge induced by the gate polarization $Q_g = C_G V_G$ is written as explicit term, then the the charging energy $E_c = Q^2/2C_\Sigma = (ne + Q_g)^2/2C_\Sigma$ e-periodic with Q_g, defining a family of overlapping parabola with e-periodicity. Every number of electrons on the island permit tunneling, when the charging energy is attained. However, if the system is superconductive, then single-e tunneling events ($n \longrightarrow n \pm 1$) are rare, and only $2e$ (Cooper pair) tunneling events ($n \longrightarrow n \pm 2$) occur[90]. If the number of electrons on the island is even, then the tunneling process happens, but if the number of electrons on the island is uneven, then a quasi-particle, a single electron, must be found, which is only possible above the energy gap Δ[76]. This is equivalent to raising the parabolas at the locations of uneven island occupation to a higher level, which results that the current is no longer e-periodic but $2e$-periodic with the gate voltage. This will not be seen in our experiments, because the temperatures reached are not low enough.

3.6 Summary

This chapter introduced the charging effects that the device should exhibit in order to be used as a charge detector, and what the conditions are to be able to observe Coulomb blockade (CB). Initially, this chapter was slated to cover transport aspects based on the charging effects of an SET in and out of Coulomb blockade. But when the structure was cooled down below the critical temperature for superconductivity, the interesting transport phenomena that were observed called for an explanation of charging effects that included the superconductive context, too, to be able to understand and interpret the results.

Chapter 4

Single electron transistor fabrication strategies

In the preceding chapter, single charge effects and single electron transistor theory were explored. This chapter aims to show a cross section through fabrication strategies and techniques that various groups have developed and pursued to obtain functional SETs. The strategies are discussed following a rough classification by the medium wherein the electrons transport happens, i.e. first metallic ones, then semiconductor ones. Then the state of the art of scanning SETs is reviewed.

4.1 Metallic

The first successfully fabricated SETs were metallic, evaporated with a technique using two distinct evaporations. Two publications which were important for developing this technique one by Niemeyer, one by Dolan, are reviewed. Then the structuring of metal by local anodic oxidation (LAO), in contrast to its evaporation, is reviewed. Two further, uncommon techniques are discussed, illustrating that the introduction of new processing steps such as chemical mechanical polishing (CMP) can be an opportunity to fabricate new types of SET devices.

4.1.1 Dual angle shadow evaporation

A very widespread and popular SET fabrication method is the Niemeyer-Dolan technique, also called *suspended bridge dual angle shadow evapora-*

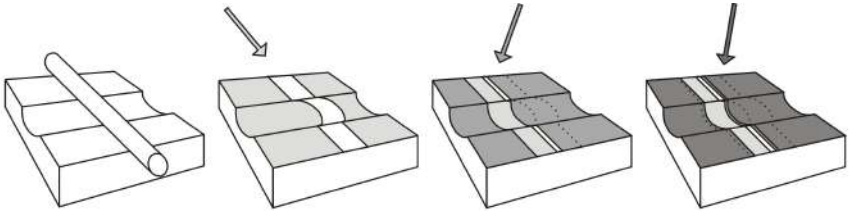

Figure 4.1: *Original Niemeyer technique, for clarity shown with fiber removed after each evaporation step (according to fig. 1 in ref. [91]).*

tion. The first steps for this technique were pioneered by Niemeyer[91], who aimed for *"allowing for the fabrication of SNS-type (superconductor – normal metal – superconductor) and SIS-type (superconductor – insulator – superconductor) Josephson junctions with areas ranging from smaller than* $1\mu m^2$ *up to* $500\mu m^2$*"*. A glass fiber is laid across a groove in a substrate (fig. 4.1 left). The shadow that the fiber casts during the evaporation divides the substrate surface into two electrically unconnected evaporant coated halves (fig. 4.1 center left). If the evaporation is inclined away from the normal, rotated by a certain angle around an imaginary axis through the fiber, then the shadow of the fiber in the groove will be offset with respect to the evaporant shadow on the substrate surface. The offset will be away from the evaporant source with regards to the fiber, extending some distance into the groove underneath the normal projection of the glass fiber. A second evaporation, inclined in the opposite direction results in an extension underneath the fiber, too, overlapping and contacting the previous evaporation only in that area (fig. 4.1 center right). A third evaporation, at a slightly steeper inclination than the second to avoid any spillover that would establish electrical contact between first and third evaporation (fig. 4.1 right), completes the formation of a junction of type "first evaporant – second evaporant – third evaporant" such as an SNS junction. The groove width defines the junction width, while the inclinations of the evaporations and the fiber diameter define the junction length.

With the Niemeyer technique only, it would be difficult to realize an SET. This is so because it is difficult to obtain multiple, sequential junctions when their definition is done by the manual placement of a fiber on a groove. Furthermore, there is no simple way to get a small island other than by two neighboring fibers spaced by a short distance. This is why later, when the theory of single charging effects proposed the SET device, nobody tried to realize one using this technique.

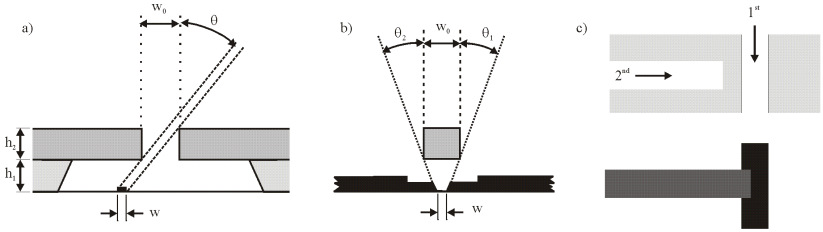

Figure 4.2: *An inclined evaporation yields narrower structures than by the employed mask is wide. a) An evaporation inclined by an angle θ through a mask pattern opening of width w_0 yields a narrower width of the evaporated pattern of $w = w_0 - h_2 \tan\theta$. b) A suspended bridge of width w_0 yields a narrower spacing between two lines of $w = w_0 - h_2(\tan\theta_1 + \tan\theta_2)$. c) Beyond a critical angle $\theta_c = atg(w_0/h_2)$, no evaporant gets past the mask. A line of w_0 width will be patterned as a line if parallel to the evaporation direction, and not pattern at all if at 90°. This can be exploited to create junctions between lines patterned in two distinct evaporation steps (according to fig. 1 in ref. [92]).*

The technique was further developed with Dolan[92] not using "suspended glass fibers" but "suspended resist": *"... a procedure recently developed for 'lift-off' processing of thin-film circuits allows for the suspension of reasonably large segments of a resist mask a known distance from a substrate ... and provides a simple means of making small-area Josephson junctions and varying-thickness superconducting bridges"*. An opening in the suspended resist mask has a certain thickness, and if the evaporation happens at an angle greater than the critical angle θ_c — where the upper edge of the nearer side of the mask opening projects to the lower edge of the farther side of the mask opening — then there is no line of sight between evaporant source and substrate, and the evaporation is inhibited by the mask edges' self-obturation. Fig. 4.2 a) shows how the angle θ controls the width w of a line through a mask opening w_0 wide, fig. 4.2 b) shows how the two angles θ_1 and θ_2 control the line separation w for a suspended mask w_0 wide. and fig. 4.2 c) shows how an overlap is created using two distinct evaporations, both beyond the critical angle. The importance of this publication is that patterning of the suspended masks is done by electron beam lithography, and not by fiber placement as with the Niemeyer technique. This allows for almost any shape, anywhere.

The theoretical prediction of *Coulomb Blockade of Single-Electron Tunneling, and Coherent Oscillations in Small Tunnel Junctions* in 1986 by

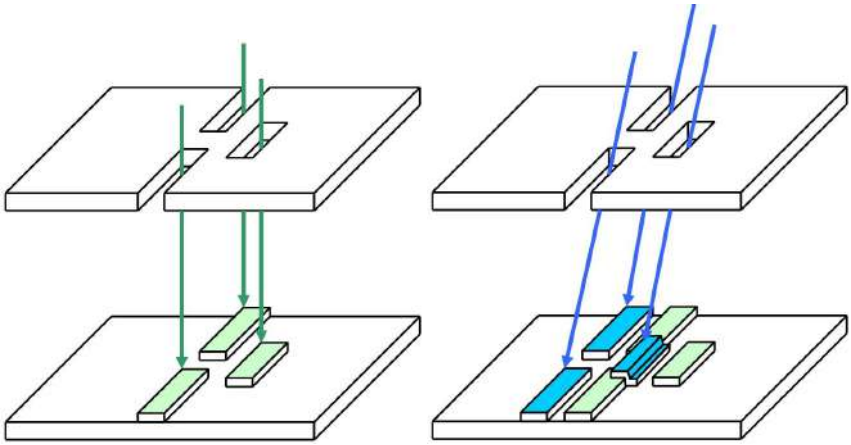

Figure 4.3: *Illustration of the Niemeyer-Dolan technique. The first evaporation step (left) is followed by an in-situ oxidation step, then by the second evaporation step (right).*

Averin and Likharev[45] was first experimentally verified in 1987 by Fulton and Dolan[93], using the technique, which nowadays is commonly called Niemeyer-Dolan technique, as shown in fig. 4.3. The technique has drawbacks due to the resist employed (if resist is employed). During the metal evaporation step, the resists heats up and outgasses, causing contamination of the film, which is bad for the quality of the evaporant film, and bad for the adherence of the second evaporant. But conceptually speaking, this technique is simple, smart and appealing. The key to SET fabrication is that the technique allows for the formation of tunnel barriers between two evaporations. The barriers can be formed without breaking the vacuum by an *in situ* oxidation step. The end result of an example using Al and its oxide as tunnel barrier is shown in fig. 4.4.

4.1.2 Local anodic oxidation

Instead of evaporating the metallic conductors through an electron beam lithography defined masks, scanning probe microscopy can be used as a tool to define per local anodic oxidation devices in a thin metal film.

A conductive tip that is negatively biased above a certain threshold voltage in humid air and that is moved in close proximity to or in contact across a thin metal film locally oxidizes the substrate[94]. The effect is mediated by the humidity in the air that is spontaneously adsorbed to

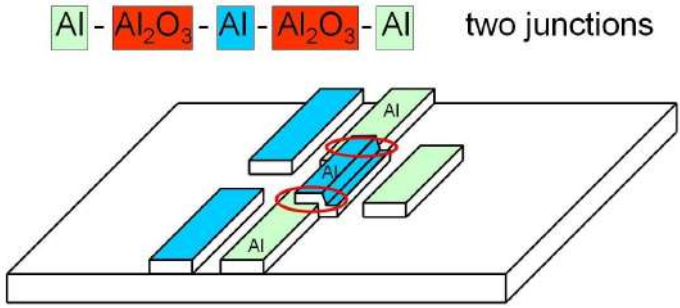

Figure 4.4: *Result of the steps evaporation, oxidation, evaporation: the created in the center the sequence Al–Al$_2$O$_3$–Al–Al$_2$O$_3$–Al defining the sought after source–junction–island–junction–source structure. The two unconnected electrode duplicates on the left, and the single unconnected island duplicate on the right are not used, they are "supernumerary".*

the substrate and tip to form a water film. A common explanation for this phenomenon is that at the moment the voltage biased tip reaches the water film on the metal film, an electrical current is established from the tip through the water through the oxidized metal region (native or built up) to the thin metal film. The water is hydrolyzed. The hydroxyl ions move through the already formed oxidized metal film towards the thin metal to react there. They move because of the applied electrical field, which is defined by the voltage bias applied to the tip. After a certain time, there is a buildup of space charge in the formed oxide because of the H^+ ions formed during the oxidation of the metal, which can lead to the OH^- ions being intercepted to form H_2O before they can reach the oxide-metal interface. This limits the oxidation reaction. The negative charge carriers move to the positive electrode and this gives the process the name LAO.

The first device that was constructed using AFM-induced LAO was a metal-oxide-metal junction[95], fabricated by interrupting a narrow Ti conductor. The current-voltage characteristic showed Coulomb blockade, a signature of single electron effects.

The first SET defined by STM-induced LAO was patterned into a Ti film, and was operable up to room temperature[49].

The LAO technique can be applied to any type of device that can be defined by patterning a thin film.

4.1.3 Chemical mechanical polishing of Ti filled trench

A trench is fabricated in an insulating substrate. A Ti line is patterned across it, thicker than the trench is deep. The line is controlledly oxidized, this oxide will be the tunnel barrier. The entire area is covered with another Ti layer. Using CMP, the wafer is ground down until the initial substrate appears. The only place where Ti remains is inside the trench[96]. The first evaporation that crossed it forms the island. On either side in direction of the trench, there are the remains of the oxidation step, and they form the tunnel barriers. They are followed by Ti layer of the second evaporation which form the source and drain electrodes. The device characterization showed Coulomb blockade up to 433K.

4.1.4 Step junction, step edge cut-off

A groove with an undercut sidewall profile is fabricated in an insulating substrate. A thin metallic nanowire is patterned across it, thinner than the groove is deep. At the sharp edges of the groove, the wire is discontinuous, and the open gaps on either side of the groove act as tunnel junctions. The combination of groove depth and wire thickness determines the tunnel gap. In ref. [97], using this method, Coulomb blockade could be observed in an SET structure up to 77K.

In a similar strategy, called step edge cut-off (SECO), evaporating metal on a step of previously evaporated barrier material resulted in an interruption of the metal strip at the edge of the step. The fabrication by evaporation of a step with a height in the range of 10nm creates the gap used as the tunneling barrier. Defining the gap interruption of the metal stripes is much less effort compared to the fabrication of a tunnel junction defined by overlaps of two evaporation using masks defined by electron beam lithography with linewidths in the range of 50nm. As evaporant Cr/Cr_2O_3 was chosen, which because of its low tunnel barrier height allowed to use a larger electrode separation, and a step of 10nm. Coulomb blockade could be observed at 10K[98], and an SET signature could be measured[99].

4.2 Semiconductor

To observe electron transport in semiconductors, either bandgap engineering can create a layer of free electrons (2DEG), which then can be shaped by local selective depletion into an SET, or a heavily doped semiconduc-

tor can be physically microfabricated into a nanowire exhibiting quantum effects.

4.2.1 Shaped two dimensional electron gas

The surface of a semiconductor heterostructure (2DEG), is covered with a thin Ti layer. Using AFM-induced LAO, gate and channel structures are fabricated in the Ti layer. By applying potentials to the shaping electrodes, the 2DEG underneath them is depleted, and the remaining, undepleted channel regions form a semiconductor quantum point contact[100] adequate for transport experiments.

It is possible to directly pattern the capping layer of a AlGaAs/GaAs semiconductor heterostructure by AFM-induced LAO. This forms the same type of in-plane gates and nanostructures as above experiments by locally depleting the 2DEG[101], although not temporarily but permanently.

The two examples show how versatile shaping of 2DEG by AFM-induced LAO can be.

4.2.2 Microfabricated MOSFET and nanowires

Silicon based devices dominate microelectronics. An SET can potentially be smaller than a metal-oxide-semiconductor field-effect transistor (MOSFET), which if used as a memory cell allows for denser integration. Creating a fabrication technique for an SET that can be integrated into an existing complementary metal-oxide-semiconductor (CMOS) process flow, or that can be seamlessly added to it, is a very interesting perspective. Which is why there is a lot of effort in this field. Two publications discussing modified MOSFET structures are reviewed, then two using doping modulation, then three using geometric constrictions.

4.2.3 Modified MOSFET, gate modulation

In a MOSFET, the gate creates an inversion layer which forms the conduction channel. In a modified MOSFET approach, an additional gate is introduced, which via local, additional modulation of the inversion layer forms the tunnel barriers.

On top of the gate of a Si metal-oxide-semiconductor field-effect transistor a second gate electrode is patterned[102]. It is electrically isolated from the lower gate, and composed of lines and spaces forming seven crossbars across the lower gate. A one-dimensional inversion layer channel is

formed by applying a potential to the lower gate. By gradually increasing the potential on the upper gate, the inversion layer channel is gradually transformed into a quantum wire with coupled quantum dots. The signature of Coulomb blockade was observed in the source drain current.

Fabricated with a standard MOSFET technology, a Si nanowire forms the channel of the structure[103]. The upper gate creates an inversion layer along the entire nanowire. Three small isolated lower gates between channel oxide and an upper gate are used as tunable barriers to cut the channel into multiple zones, such as a long island, two islands, or a short island. The tunable gate-induced electrostatic barriers allow to control Coulomb blockade in the silicon nanowire.

4.2.4 Doping modulation

The doping based approach uses the modulation of doping to form tunnel barriers.

Two silicon nitride spacers are deposited on each side of the gate of a gated nanowire. Then the whole sample is heavily doped. The nanowire is protected underneath silicon nitride spacers and gate. This creates a modulation of doping along the nanowire channel, which, if carefully chosen, creates tunnel barriers[104]. The island can be put in inversion by the gate potential. The gated nanowire is transformed into an SET.

Using ion implantation, phosphorus doped (Si:P) conductive zones are created within silicon to form island and reservoirs of single electron devices[105]. This approach is limited to cryogenic temperatures due to the small ionization energy of the phosphorus donors.

4.2.5 Geometry based

If the tunnel barriers are obtained by reducing the number of transmission channels in a conductor by geometrically constricting it, then this is typically done with some or all of the following steps. An electron beam or photolithographical pattern transfer step is done, then an etching or oxidation step reduces the geometries and dimension of the pattern to attain dimensions where mesoscopic phenomena appear.

Silicon nanowires can be fabricated taking advantage of the anisotropy of potassium hydroxide (KOH) etching[106].

Using electron beam lithography, a silicon wire is patterned in a SOI wafer. Where the island of the final device will be, the covering mask is connected through narrower connection to the devices leads. With an anisotropic KOH etching step, all but the mask protected wire is removed.

At the narrower connection, the underetch further reduces the section of the connection between island and electrodes. A final, time controlled oxidation step reduces the channel dimensions, creating the tunnel barrier by reducing the available transmission channels. The substrate is used as backgate[107].

A SET was fabricated on silicon on insulator (SOI)[108, 109], Using electron beam lithography and liftoff, a Cr mask is defined, which then is used for a pattern transfer in an anisotropic dry etching step. Subsequent thermal oxidation reduces the dimensions of the device further, leaving a small island connected through two silicon tunnel barriers to the electrodes. Clear Coulomb blockade could be observed at 4.2K.

4.3 State of the art

4.3.1 State of the art SSET at beginning of thesis

Some possible strategies to fabricate an SET have been presented in the preceding sections. Given that an SET is a device very sensitive to charges, how can it be brought close enough to a device to be able to measure it?

A straightforward solution is to pattern an SET directly on top of the device of interest, such as the transport channel [2, 110] to be investigated, where an SET was patterned on top of a Hall bar defined in a 2DEG.

In 1997, M.J. Yoo *et al.* reported in Science [111, 112]: *"A single-electron transistor fabricated at the end of a sharp glass tip, is scanned in close proximity across the sample surface. Images of the surface electric fields of a $GaAs/Al_xGa_{1-x}As$ heterostructure sample show individual photo-ionized charge sites and fluctuations in the dopant and surface-charge distribution on a length scale of 100 nanometers".*

The classical approach for SET fabrication is shadow evaporation on a flat substrate using electron beam lithography, but a flat substrate is difficult to bring within nanometers of a surface to be scanned.

Yoo's elegant approach is to sidestep the problem by forming an SET on a glass fiber with a three angle Al evaporation, an elegant exercise in self-shadowing evaporation, see fig. 4.5 where a) shows the tapered fiber side and front view. The first Al evaporation b) covers half a side of the fiber, but the nominal evaporation thickness is only obtained perpendicular to the evaporation source, on the sides of the fiber, the thickness is evanescent. If the fiber is now taken out of the evaporator, then immediately a native Al oxide forms. On the sides, where the Al is thin, the film completely oxidizes through, forming an electrically insulating Al_2O_3 layer. On the top, where

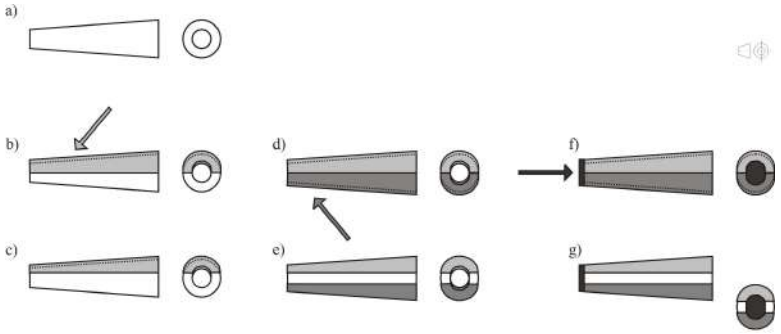

Figure 4.5: *Yoo et al's SET on tapered fiber, three angle evaporation*

the Al film is thicker, the native oxide is only on the surface, with the rest of the film electrically conductive. What would remain of conductive Al is shown schematically in c). The second evaporation step d) and what would remain after native oxide formation e) is analogous to b) and c). Up to here, two evaporations b) and d) were done. Now, a controlled deliberate oxidation of the Al forms the Al_2O_3 tunnel junctions. The island is evaporated from the front side of the fiber in f). The evaporant forms the island, but also spills over to the body of the fiber. This is no problem, because it arrives on thin tunnel oxide formed in the previous step, and it arrives at a very steep angle close to the parallel of the surface, giving a very thin film. Then the fiber is taken out of the evaporator. This time the native oxide is really formed, just as anticipated in steps c), e) and g). The final structure is an SET (with no gate electrode). This is not a Niemeyer-Dolan technique as on p.58, but a three angle self masking evaporation. Their fabrication technique does not allow for batch processing, the probe is not a standard AFM formfactor, etc., but the important fact is that they succeeded to make a SSET and to gather nice data. This paper was one of the inspirations for this thesis' objective, implementing an SET on an AFM probe.

4.3.2 State of the art SSET today

Attempts by other groups to implement an SET on an AFM had been unfruitful at the beginning of this thesis (2002). But as progressively was learned, several other groups were working towards that same scanning single electron transistor (SSET) goal.

In his thesis of 2000, Canali[113] notes: *"Although we could fabricate*

an SET at the end of a sharp cantilever, ... the device was not working properly because the source and drain junctions were blown up probably by the dry etching step".

In 2003, Steinman *et al*[114] report that they work on a SSET AFM probe, and use ICP RIE dry release etch to form free-standing silicon AFM cantilevers. *"At present, no junctions that have exhibited suitable tunneling characteristics have been measured on released cantilevers".*

SET are used as charge detectors because they are extremely charge sensitive, and the two reports were a confirmation that any fabrication process had to be designed very aware of this fact. See also the later discussion on the antenna effect on p.148.

There must be other groups who have been or still are working on an SSET AFM but decided not to report yet non-functional implementations.

In 2004, Brenni *et al* stated their intentions in an introduction to their article[115]: *"While thermal noise is reduced at cryogenic temperatures for an advantage in reaching the quantum limit, there are many experiments that would gain in feasibility by using higher operating temperatures. An example of such a project is the scanning-SET microscope, which would be difficult to place in a mK temperature cryostat".*

It is not a coincidence that the first successful SSET on AFM was reported by the same group in 2006 by Brennig *et al*[116]: *"We report fabrication as well as proof-of-concept experiments of a noninvasive sensor of weak nanoscale electric fields. The sensor is a single electron transistor (SET) placed at the tip of a noncontact atomic force microscope (AFM)".*

4.4 Summary

An overview over existing single electron transistor fabrication strategies and techniques was given in this chapter. There is not one strategy which is best, every single one depends on the available fabrication technology, on the desired target application, and on the ability to dream up new solutions. In the next chapter, we present the fabrication process for an SSET that was developed during this thesis.

Chapter 5

Experiments

In this chapter, the fabrication of a scanning single electron transistor (SSET) is discussed. First, a seemingly out of place overview on micromachining techniques pertinent to the subsequent fabrication steps is given. Then, the development of the fabrication process for an SET on a flat substrate is presented. Then, to understand why what choices were made, the planned operating environment of the probe is explained, with its directly deriving set of SSET design constraints. Some existing atomic force microscope (AFM) functionalizations with their strategies are presented. Then, Pandora's toolbox is opened and the steps to fabricate an SSET on an AFM are shown.

5.1 Microfabrication techniques

Microfabrication techniques relevant to this thesis are briefly explained and illustrated in the following, but for an in-depth overview of the field please consult reference books, currently[117, 118, 119, 120] are counted among them. Before transferring a pattern, it must first be established. Two patterning techniques are discussed, and then various transfer techniques.

5.1.1 Lithography

The word lithography[1] stood for the printing technique developed by Alois Senefelder in 1796, based on the repulsion of oil and water, and important

[1]The word lithography is coined from the greek word $\lambda\iota\theta o\varsigma$ (lithos) "stone", and $\gamma\rho\alpha\varphi\epsilon\iota\nu$ (graphein) "to draw".

in the historical context because it introduces chemistry into printing, as opposed to Johannes Gutenberg's printing press of 1436, which was based on a purely mechanical principle (but nevertheless groundbreaking because it made document reproduction possible without a room full of monks). It involves a pattern drawn with a hydrophobic medium such as a grease crayon on a hydrophilic support such as limestone, an acid etching step to render the non-patterned area of the stone hydrophilic, removal of the hydrophobic pattern, wetting of the surface, applying of a hydrophobic ink. Since the water is attracted to the hydrophilic etched areas, the hydrophobic ink is repelled to the areas where originally the pattern was drawn. The ink is transferred in a press to paper, hence the name pattern transfer. Lithography is nowadays synonymously used for any pattern transfer technique.

5.1.2 Photolithography

Photography, uses "light"[2] to draw, in place of the "stone" in the previous technique. It is the next important step towards photolithography. Silver halide crystals in gelatin based film emulsions are used. The compounds are light sensitive, and under photon exposure change back to metallic silver, and store a spatial image of the photon intensity. The silver halide grains which contain silver "freed" from the halide by photon interaction are faster developed by an oxidizing agent than the unexposed grains, which implies that the reaction has to be time controlled, otherwise everything is developed to black. The fixing process removes the unexposed and undeveloped silver halide from the emulsion. The result is called a negative because the highest light intensity results in the darkest areas, which is the inverse of our perception, where high intensity is bright. One more step — image reversal (and incidentally enlargement) — is needed to obtain a photograph, the desired positive black and white image.

Photography is optimized to provide shades of transparency, but microfabrication needs binary masking capability, to selectively mask or unmask substrates for additive of subtractive process steps. Photolithography masks use photosensitive organic materials, called photoresists. As one further digression please take note that the name is no longer created by switching out the stone of lithography, but by prefixing it by "photo", which shows the acceptance of the term as generic for pattern transfer.

Photoresists come in two forms, positive and negative resists. A positive resist's solubility in a developer increases with exposure to light, while

[2]From Greek $\phi\omega\varsigma$ (phos), light.

for a negative one it decreases.

In positive photoresists common in microfabrication, a small amount of diazonaphthoquinone (DNQ) is dissolved in novolak resin, a low molecular weight pheno-formaldehyde condensation polymer[121, 122]. When exposed to light, the DNQ changes and produces a carboxylic acid group, which increases the solubility in a base (developer) of the exposed resist areas by orders of magnitude compared to the unexposed resin. Negative photoresists rely on free-radical-initiated photocross-linking or photopolymerization[123], which decreases their solubility compared to the unexposed areas. Resists are actively researched and developed, and new solutions are introduced into micromachining, such as chemically amplified negative resist, or high aspect ratio negative resist such as SU-8[124].

The wavelengths of the light sources used in photolithography are historically linked the to spectrum of Hg gas discharge lamps, filtered for certain peaks in the ultraviolet (UV) range, i.e. G-line (436 nm), H-line (405 nm), I-line (365 nm). The minimal feature size W in optical projection lithography is given by the Rayleigh diffraction limit $W = k\lambda/NA$, where k is process specific (around 0.5), NA the numerical aperture of the optics and λ the exposure wavelength. To reduce the minimal feature size, the sources continue their decrease in wavelength into deep ultraviolet (DUV) with KrF laser (248 nm), ArF eximer laser (193 nm) and F_2 eximer laser (157 nm). Immersion lithography, increasing NA, buy time to decrease the wavelength, time needed to work out source complexity and optics absorption for extreme ultra violet (EUV) such as with laser pulsed Xe gas plasma (13.5 nm).

The light is projected onto the photoresist through a photomask , typically out of quartz, borosilicate or soda lime (only quartz is transparent from UV to infrared (IR), the other have narrower transparency windows but are at a third of the cost). An obturating (occluding) layer, typically Cr, defines by its absence where the light is allowed to pass to reach the photoresist. The Cr in its turn is patterned by etching it through a resist layer which was exposed with an electron beam or laser system. Photolithography exposes a whole area (an entire wafer or just a stepping field) simultaneously, or in parallel. The following instrument does it sequentially.

5.1.3 Electron beam lithography

Electron beam (e-beam) lithography uses a beam of electrons to pattern the resist. When the electrons reach and penetrate the sample, they interact with its constituents by transferring energy to it. In re-

sists of widespread use, this results in a change of solubility by either the scission of chemical bonds of polymers (positive electron beam resist) or the cross linking of monomers (negative electron beam resists). Not to forget are electron beam induced desposition (EBID) where residual carbon molecules are redeposited as masks[125, 126, 127, 128], or as structures[129, 130] or traces of introduced metal-organic gases are cracked to form electrical connections.

An electron beam lithography system is extremely versatile, because the beam can be deflected to whatever spot the driving software decides to. The pattern data can be modified up to a very short moment before the pattern is written. However, this comes at a speed disadvantage, because every spot has to be addressed individually and sequentially, which is acceptable in R&D settings, or in low number prototype or production series.

One distinguishes inelastic and elastic electron–solid interactions. In an inelastic one, also called forward scattering because of its little angular influence on the electron trajectory, the electron interacts with the atom's electrons, resulting in little change of its momentum, and loss of energy. The energy is found in the excited secondary electrons that the atom emits. In an elastic one, also called backward scattering, the interaction is with the atom nucleus, and results in a large angular deflection (large momentum change), but no energy change. Forward scattering causes little beam broadening. Backward scattering may interact with the substrate far away from where the initial beam was directed. This can be used for a benefit, such as for creating a negative or overhanging profile, which is beneficial for a liftoff process.

An incident electron beam creates an energy deposition profile in the sample which is the combined contribution of forward and backward scattered electrons. The influence of both forward and backward scattered electrons can be modeled as a sum of two Gaussian distributions[131]. This scattering phenomena is the origin of what is called proximity effect[132], which is the fact that the exposure dose in a given point is influenced by the scattering of the exposure of other nearby points.

The resists used in electron beam lithography are formulated to change their solubility due to interaction with electrons instead of photons, otherwise (handling and functionality) they are very comparable to those used with photolithography. Popular are poly(methyl-methacrylate) (PMMA) [133, 134], or poly(methyl-α-chloroacrylate-co-α-methylstyrene) (ZEP), which both are chain scission type positive tone resists, and hydrogen silsesquioxane (HSQ)[135] or calixarene hexaacetate p-methylcalix[6]arene (calixarene)[136, 137], which both are negative tone resists. Reviews on electron beam

resists[138] contain further leading information.

The resolution in electron beam lithography is limited by scattering, whereas in photolithography it is limited by diffraction.

5.1.4 Additive and subtractive steps

Resists come in positive and negative flavors, the exposed areas become solvable and unsolvable, respectively, and after the development step, the underlying substrate is locally unmasked. This is used for two processes: additive and subtractive ones.

For generality, the term "resist" to is briefly broadened to "masking layer". In an additive process a material is added. The material is added using any thin film process (evaporation, sputtering, plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), etc. ...). After this addition, the masking layer is dissolved and removed. The areas where the added material is is sitting on the masking layer is lifted off with it, hence the name *liftoff processing*; only the unmasked areas retain the added material.

In subtractive processes, etchants attack, react and remove material. Two major groups are distinguished, wet and dry. In wet etching, the etchants are liquid, such as KOH for anisotropic Si etch, buffered hydrofluoric acid (BHF) for isotropic SiO_2 etch, phosphoric acid (H_3PO_4) for isotropic SiN etch, etc. . They are each chosen because they selectively etch one material, while leaving others intact (or seemingly intact, etched at a much lower rate). Dry etching uses a plasma to ionize gas molecules, which are then driven by an electrical field to the surface to be etched, where they react with the material on the surface of the sample, and are called RIE, inductively coupled plasma RIE, deep reactive ion etching (DRIE)(Bosch process with passivation cycles), cf. ref. [139, 140, 141, 142]. Only the unmasked areas are attacked by the etchant. Dry processes tend to have an anisotropic etch profile, because the electrical field which conveys the ions arrives perpendicularly to the surface. The masking layer is preferably etched at a lower rate than the substrate, often by orders of magnitude, or even not at all.

A profile view of positive and negative, additive and subtractive processing is given on fig. 5.1 for comparison. Resists are the most versatile masking layer, but any thin film can be used, especially if temperature excursions are not an issue. A SiO_2 layer may be wet etched with BHF, or dry etched with RIE, both through an exposed and developed resist layer. This SiO_2 layer can then be used as a masking layer for wet anisotrop-

ically KOH etching Si. Resists have an upper temperature limit. They can be mildly heated, such as in a wet etching bath to increase the etching rate, or in a dry reactive ion etcher because of heating through the plasma, but they need to stay clear of their vitreous transition temperature, which most of the time is below the 100°C mark. Otherwise they start to flow, which initially degrades the resist flank profiles, then the resist pattern definition itself. At higher temperatures, resists simply burn. Most thin film processes for additive processing, such as chemical vapor desposition (CVD), operate in temperature ranges too high for resists. Therefore an additive step is used without any mask, followed by masked subtractive patterning step to remove the unwanted areas. subtractive techniques, most of the time called etching, that were used were wet etching and dry etching. The wet ones contain the etchant dissolved, usually in water, and include KOH for anisotropic Si etching, BHF for isotropic SiO_2 etching, H_3PO_4 for isotropic SiN etching, Aluminum etchant (mixture of $H_3PO_4/HNO_3/CH_3COOH$) (Al-etch) for Aluminum, etc. . The dry ones work in a vacuum environment filled with little gas, and when a high electric field is applied then a plasma forms. The plasma ionizes the present gas and dissociates it into the reactive species, who either diffuse or are field driven to the surface to be etched, react there, desorb and diffuse away either pumped off or redeposit on the chamber walls. The etch recipes are specific for material to be etched, such as Si, SiO_2, SiN, specify the reactant chemistry (SF_6, CF_4) and their flow quantities, ancillary gases to avoid chamber redeposition (O_2) or etching uniformity (He), polymers for sidewall protection (C_4H_8), the source power, the plasma pressure, the bias voltage, etc. . They are often kept secret, because their derivation is not straightforward, but boundary to artistic.

5.1.5 Pattern transfer summary

The various pattern transfer techniques are summarized in fig. 5.2 to give a graphical idea of where they are identical, similar or different.

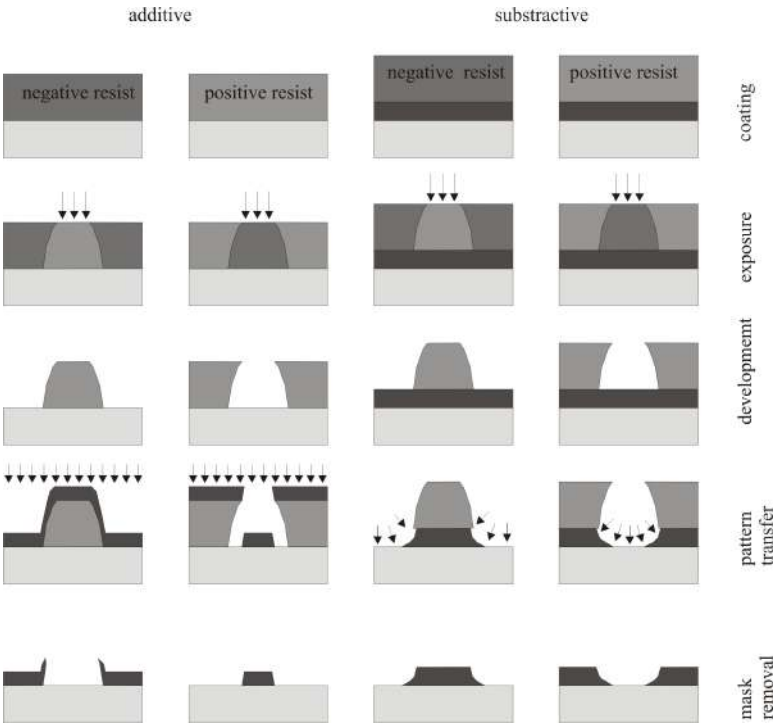

Figure 5.1: *Additive and subtractive pattern transfers using positive and negative resists. The left-most column is avoided, because the liftoff can be difficult or impossible. The overcut profile is uniformly coated with the added layer, giving the solvent no point of entry to dissolve the resist (and lift off the added layer). For thin layers, manual or ultrasonic agitation may rip off the nevertheless thinner raising parts, leaving raising fragments behind. All this is not an issue in the second row, where the undercut caused by exposure and development guarantees a discontinuity in the added layer film. The subtractive steps on the two right columns does not have this restriction. It is isotropic for wet etching, and close to anisotropic for dry etching.*

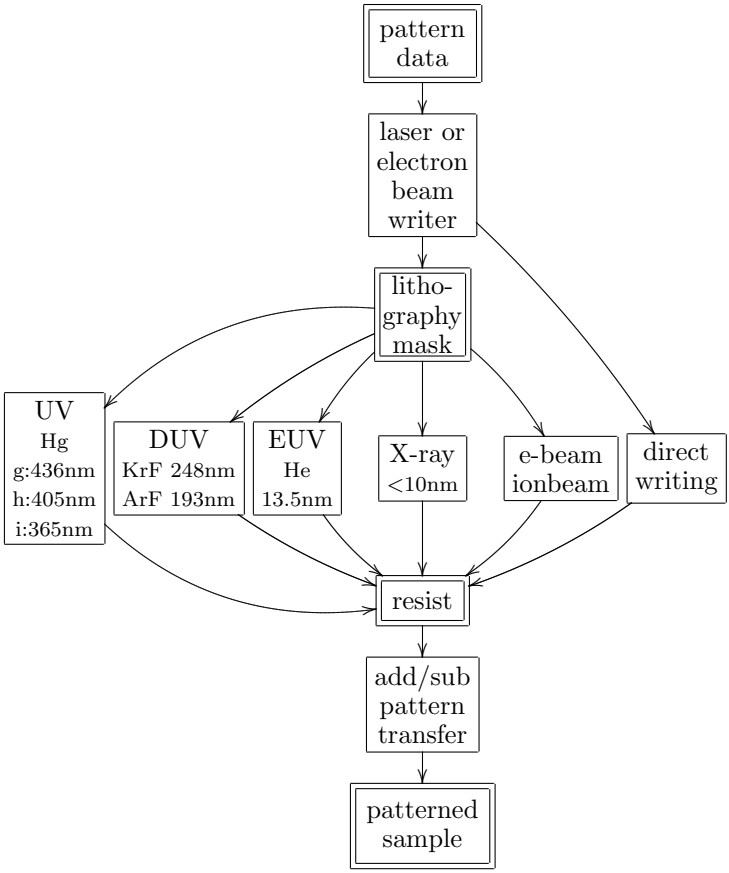

Figure 5.2: *Common pattern transfer techniques.*

5.2 Requirements for operation in cryostat

It is essential to study first how a scanning SET probe would be operated. This will give an understanding of what boundary conditions are important, and of what factors are to be considered from the start on of the design. To do so, one more step back is taken to understand what transport phenomena are to be observed.

5.2.1 Electrons in two dimensional electron gas

In a two dimensional electron gas (2DEG), electrons are free to move in two dimensions, but confined in the third dimension. Such structures are commonly fabricated using molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD), where layers are controlledly, sequentially and flatly deposited. In the case of a 2DEG with modulation doping, typically are present: a base layer, a spacer layer, a doping layer and a capping layer. The base and spacer layer are made from two materials chosen to have very similar lattice constants but different band gaps. They form a heterojunction. The doping layer's donors get ionized, and diffuse into the base layer with lower conduction band until stopped by the resulting electric field. In the base layer, at the heterojunction, the seeked 2DEG can now be found, with electrons free to move in the x and y, but not in the z axis (direction of deposition of layers). Furtherleading reading on 2DEG, such as Tsuneya Ando's[143] succinct (236 pages) review give in-depth insight into this field.

To create a structure or device that can be investigated, the freedom of the electron along both x and y axis must be limited, because in a 2DEG, it is only restricted in the z axis. The basic method is to physically shape the material or to modify the potential landscape for the charge carrier by means of electric fields. This can be done in various ways. Through an etch mask, the layers forming the heterostucture of the 2DEG are etched away, and the remaining stack forms the device. A gate electrode is added on top of the stack, and by applying a voltage, the 2DEG is depleted locally, i.e. underneath the electrode, which shapes the device. An elegant way to structure these gate electrodes is LAO, where the electrodes can be defined directly in the capping layer, or a metal top layer, or both as shown in[144].

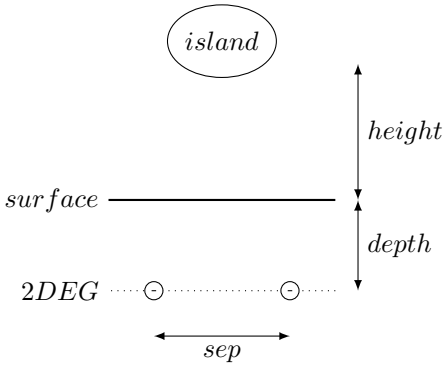

Figure 5.3: *Schema for potential induced by two point charges.*

5.2.2 Lateral resolution

A 2DEG forms in the baselayer very close to the heterojunction, and electron transport will therefore happen noticeable below the surface of the capping layer, in depths ranging from 50nm to 200nm, a decision taken by the bandgap-engineer. The depth of the 2DEG is the first factor influencing the lateral resolution of a scanning probe, because on one hand the field diminishes with the square of the distance, on the other hand the lateral resolution, i.e. the angle under which two features are seen and can be discerned decreases with increasing distance.

As a Gedankenexperiment (fig. 5.3), we consider two point charges located at a certain depth in a 2DEG, and look at the potential they induce in an island of an SET that is scanning at a certain height above the sample surface. For the scope of this coarse overview, we assume that the 2DEG is situated at a depth of 100nm below the surface. One point charge causes a potential of 1 arbitrary units (a.u.) at the surface. We calculate the potential seen by the island by adding the potentials of the two charges which are $\propto ((sep/2)^2 + (depth + height)^2)^{-1/2}$, and plot it along an axis going through both charges.

The potential plots are organized as follows: The potential at the indicated height 0nm, 50nm and 100nm (cf. title) is shown in the top left as a 3D-view, varying the charge separation from 0 to 1000nm and the observer position x=-3 to $+3\mu m$. In the bottom left is a topview, in the bottom center an zoom-in into the heart of the topview, and the column to the right gives potential-separation curves for select separations of 0nm, 100nm, 200nm, and 400nm. The plots are for 0nm (fig. 5.4), 50nm (top

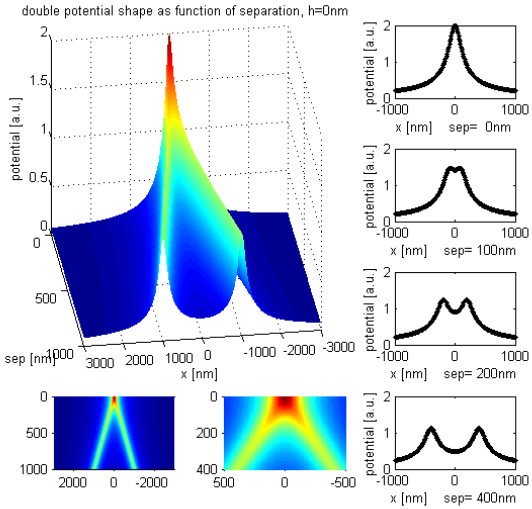

Figure 5.4: *Potential of two point charges, height=0nm.*

fig. 5.5), and 100nm (bottom fig. 5.5). A summarizing table of potential-separation curves is show in fig. 5.6. The conclusion is that if the island is at up to a height of 50nm above the surface, then charges separated by 200nm are possible to be resolved, while if the island is much higher, the separation between the point charges needs to be bigger, and the drop of the potential if measurable will be quite small.

This gives a rough idea of what order of magnitude the lateral resolution of an SSET may reach.

A scanning probe tip is by nature fragile, and this is even more the case if a device is integrated at its tip, even if there is a mechanical feature present to protect it. Therefore contact or intermittent contact mode AFM are not recommended. For non-contact AFM, a few nm of scanning height can be achieved, and the probe will be able to follow the surface topography tightly. For a 2DEG buried below 50nm and 200nm, another 5nm added by the hovering tip signifies maximally 10% more distance, which is not a significant loss in signal or resolution.

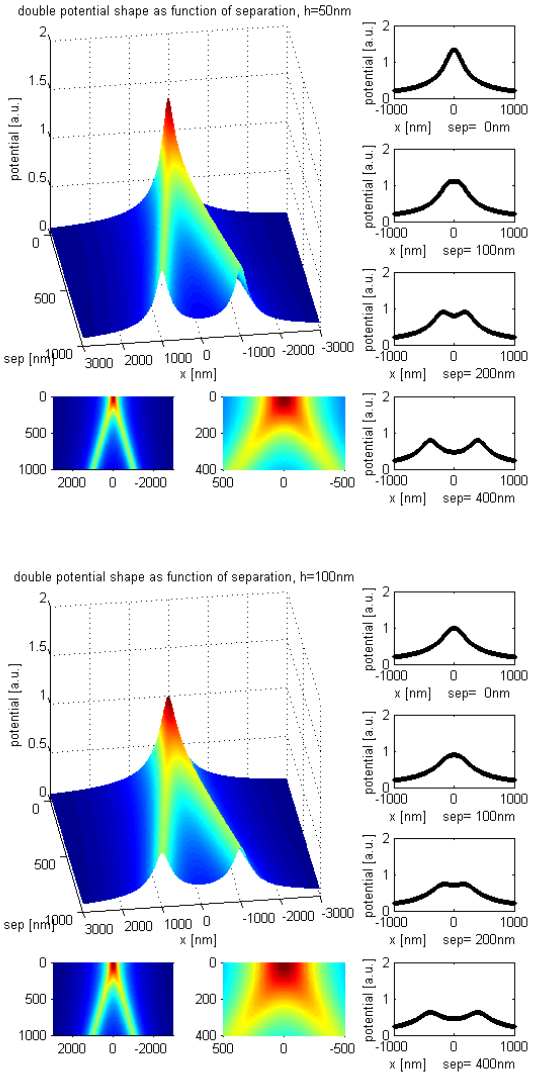

Figure 5.5: *Potential of two point charges, height=50nm,100nm.*

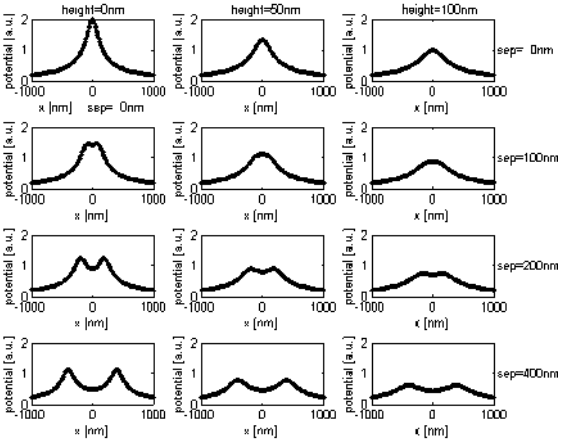

Figure 5.6: *Summary for potential of two point charges.*

5.2.3 Probe actuation and sensing

In commercial AFMs, the workhorse for cantilever deflection measurement is laser light reflection detection. The confined space of a cryostat environment, combined with the light sensitivity of semiconductor samples, any "reflected off cantilever laser beam" based readout system must be encapsulated to be optically isolated from the rest of the system.

This potentially complex endeavor lead to the consideration of an alternate systems. The development of the tuning fork cantilever based AFM[145], had already been undertaken in Neuchâtel. For a historical view of the field "quartz tuning fork as force sensor", cf. subsection 5.8.2 on p.135. The tuning fork (TF) provides the base for a self-actuating and self-sensing probe, and can be easily customized. Therefore it was close at hand to use it as a platform to base the solution for the SSET on it.

In summary:

- The buried 2DEG requires scanning close to the surface to not further decrease the lateral resolution and signal to measure.

- The use of non-contact mode is necessary to avoid wear and tear of fragile tip and devices.

- The light sensitivity of 2DEG samples and the confined space in a cryostat, encourage the use of a system that has the self-actuating and self-sensing nature of a tuning fork base probe.

5.2.4 Requirements

Section 3.4.1 briefly discussed the junction requirements for an SET. Here they are restated.

Tunnel junction capacitance. The charging energy $E_c = e^2/2C_\Sigma$, is the important parameter. C_Σ is the total capacitance of the island. The gate and substrate coupling are much smaller than the contribution from the junction capacitances. To have a small charging energy, the tunnel junctions are made as small as possible to get small capacities.

Gate and stray capacitance. Preceding paragraph mentions that the capacitance emanating from gate and substrate coupling are smaller than the junction capacitances. This must be done deliberately by reasonable choice of parameters, i.e. a gate electrode leads comparable the junction leads will have much lower capacitance because of much wider dielectric, but still coupling to the SET, and patterning the SET on a sufficiently thick isolator, such as SiN or SiO_2, reduces as much as possible the island to substrate capacitance.

Tunnel junction resistance. As seen in subsection 3.2.4, the minimal value for a junction resistance is $R_T = h/e^2 \approx 25.8\text{k}\Omega$. This resistance is proportional to the junction area, and exponentially dependent on the junction thickness.

To be able to observe CB above milliKelvin temperatures, the charging energy must be raised. This is done by reducing the junction areas, which lowers the junction capacitance. Smaller junctions result also in higher junction resistances, which diminishes the overall current through the SET, and thereby the observable signal, which makes that the junctions should not be too small, neither. While very small junctions are possible to fabricate, the granularity of the Al film often is a source of problems. In an idealized oxidation step, the perfectly flat surface of Al is oxidized. After a second evaporation step, this oxidized layer acts as a junction. When this idealized layer gives way to a realistic thin film composed of Al grains, some of the inter grain boundaries will oxidize and turn in to junctions themselves. This is not a significative problem for bigger junctions, where the film as a whole will remain conductive up to the junction, but for very small junctions, this may result in the case where so many grains were isolated, that there is no more an electrical path all the way up to the junction, with the end result that the oxidation step caused

an open circuit instead of a tunnel junction.

5.3 Attempts with novel processes

One of the nanotools' group competencies is the microfabrication of AFM probe chips with special tips. An initial idea was to photolithographically define an SET. It is clear that the minimum feature size obtainable with the equipment available in the local cleanroom are probably around 1μm, which is at least an order of magnitude above what would be required. But that does not mean that it cannot be achieved with supplementary steps, i.e. the combination of a pattern transfer and a dimension reducing etching or oxidation step to create a structure or a proxy structure which ultimately defines an SET. Some of the explored ways to obtain an SET structure are shown in the following subsection.

5.3.1 Tip effects

An AFM probe tip can be fabricated and guaranteed to have a tip curvature radius of couple of tens of nm. It should be possible to exploit a yet to be found process specific peculiarity to create a structure which could be suitable to form an SET, either directly, or indirectly. The example of a step junction, as discussed in subsection 4.1.4, is taken, where a step in the substrate layer causes a gap in the conducting film laid across it, and if chosen well, that gap can act as a tunnel junction. A double step, caused by a groove in the substrate, can yield an SET, as demonstrated in ref. [97, 99]. It would be highly interesting to use a minute micromachining effect that manifests itself at a tip apex to create such a special topographic feature. For example the use of a deliberate knife-edge[3] shaped tip defining an island structure. Another idea is a micro-molded pyramid structure out of two materials. The electrical field used in RIE is higher near sharp tip apexes than on the flat substrate. The higher electrical field drives more reactants to the tip apexes, which makes that they are preferentially etched, at least as long as the tips are very sharp. This can be used in a timed etch to cap the tips, leaving the body of the tips mostly intact. The capped tip gives a selective wet etchant access to the second material used in the tip molding process. Initially just a hole, it will gradually open up

[3]Pyramid Si mold tips are based on four {111} KOH etch defined planes meeting in one point. Asymmetric mask openings, non-uniformities during pattern transfer, etch rate variation due to up/down left/right orientation or H_2 bubble flow cause that ideal point to widen to a real line, often called knife-edge.

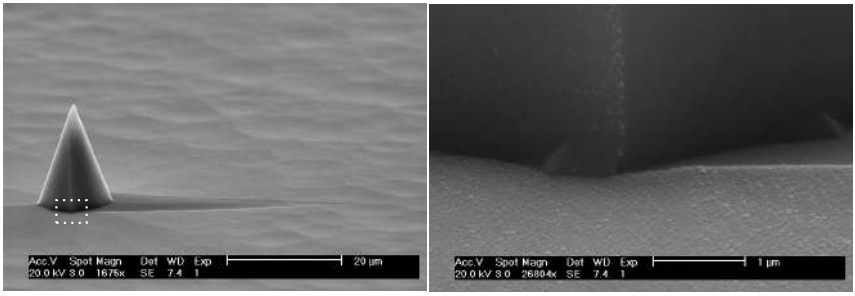

Figure 5.7: *Evaporation shadow cast by pyramid (left), detail of facing pyramid corner (right).*

to a wider volume, all protected by a surrounding wall of the first material used in the tip molding process. An evaporation step could create a Spindt-tip[146, 147] like metallic island at the top of the tip. The challenge to electrically connect it remains.

Another idea is to use a tip to cast a shadow onto a nearby structure. Oblique evaporation and shadow capability was ascertained. Fig. 5.7 shows an anisotropically etched tip, after an oblique angle evaporation, with an off-plane angle of 20°, of 100nm thick Aluminum. The shadowed zone has clearly delimited edges.

5.3.2 Backside trans-illumination

The following technique (fig. 5.8) was to create a thin, metallic (Al) wire on the edge of a micromachined pyramid, which would connect to a structure at the tip apex.

Two of four sides of a pyramid were covered with Al using oblique evaporation (cf. fig. 5.8-a overview, 5.8-b SEM picture, 5.8-d section). Then negative photoresist was spun on the pyramid's side of the wafer, completely immersing them (fig. 5.8-e). The photoresist was exposed from the backside of the wafer through the pyramids. Because the pyramids are made out of Ta_2O_5, they transmit well the exposing UV light. They light of the exposure will bend slightly around the corner due to diffraction, making that a thin line of Aluminum on the ridge will remain protected by the photoresist (PR), if the etch is timed correctly. The exposed photoresist is developed (fig. 5.8-f). The Al is etched using the somehow overlapping PR as etch mask (fig. 5.8-g). The PR is removed (fig. 5.8-h section, 5.8-c overview). The ingenious technique did not work, because the Al was

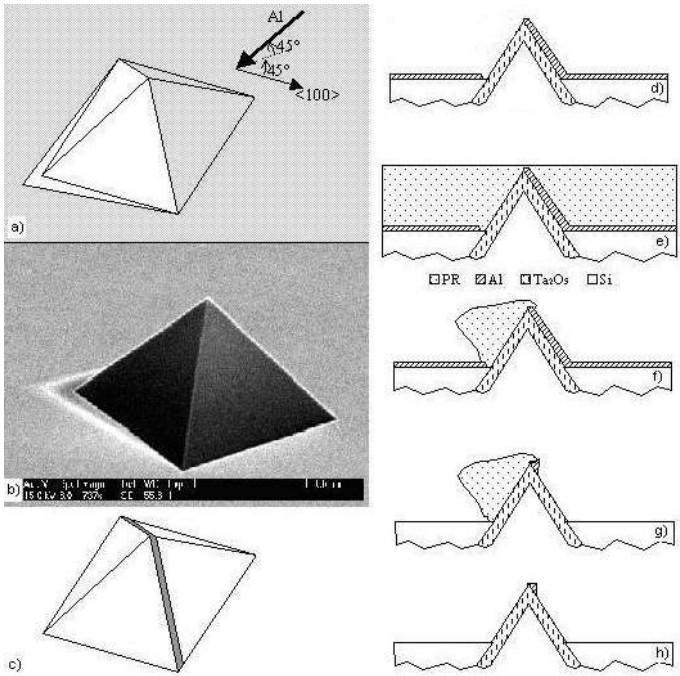

Figure 5.8: *Principle of the "shadow on pyramid" technique. Oblique evaporation coats two of the four sides of a micromachined Ta_2O_5 pyramid. After coating with photoresist, the wafer is exposed from the backside, the UV light passes through the pyramid, but not through the Al coating. The photoresist exposed due to diffraction at the edge of the Al protects the Al during the subsequent etching step. This technique did not work.*

never covered sufficiently by the PR, and even got attacked by the NaOH based developer. But some interesting traces of where the UV light passed are shown here. The top is flat, because that is how high the PR was spun. The remaining PR features cones, almost Gaussian shapes, that extend in the direction of the plane and not parallel to the transmitted light. They are due to the reflection of the UV light off the adjacent Al covered pyramid walls. The illumination of non-coated pyramid (fig. 5.9 right) exposed the PR on all four sides. Knife edge type tip of pyramid permits to determine its orientation.

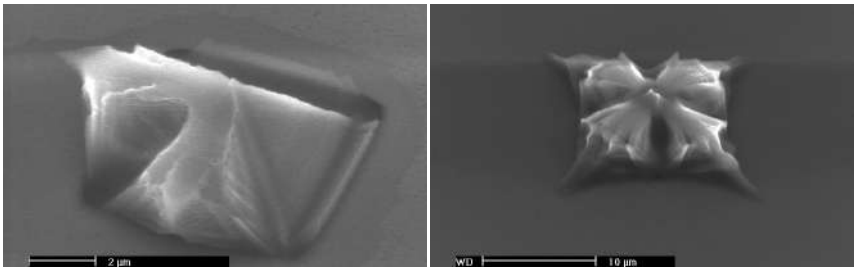

Figure 5.9: *Exposed negative photoresist vanes on pyramids. Pyramids protected on two sides with Al (left) and unprotected (right). Where unprotected, the exposure and development of the negative photoresist yields the unusually shaped resist structures. Scalebars 2µm (left), 10µm (right).*

5.3.3 Single shot shadow evaporation

5.3.3.1 Projection on structure

This approach intended to metallize a narrow structure, and use a shadow casting structure to interrupt the metallization somewhere, either to create an airgap junction on the narrow structure, or a jump from the narrow structure to the shadow caster and back (cf. step junction on p.60). The principle is shown in fig. 5.10. There are many things to solve, and they

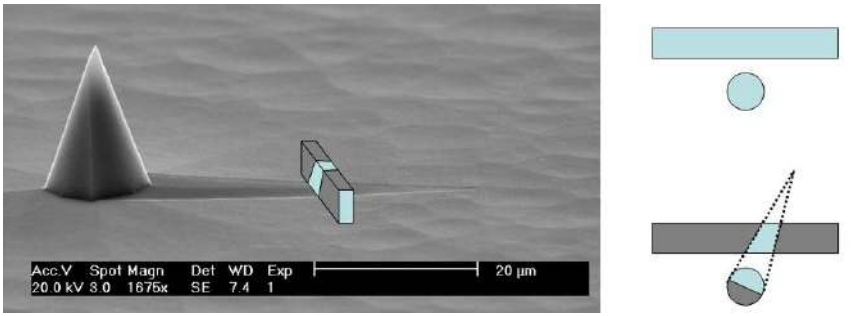

Figure 5.10: *Oblique evaporation principle. The shadow the pyramid casts on the wall creates an evaporant interruption in the top of the ridge*

are looked at here in sequence. A tetrahedral[148] type tip can be obtained as shown in fig. 5.11. The result in the SEM picture (right) is obtained as follows: A Si structure is enveloped by an etch KOH resistant layer, here SiO_2, surrounding it like a wall (left), and anisotropic etching of Si

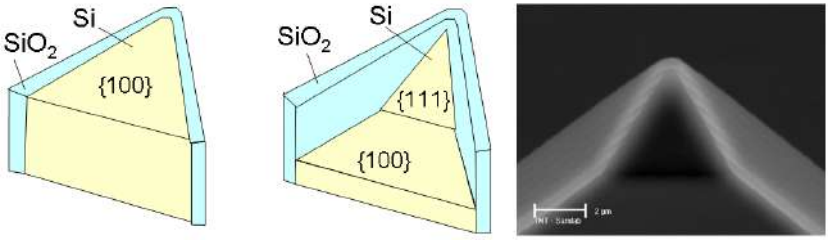

Figure 5.11: *Anisotropic etch defined tetrahedron. The SiO_2 wall protects the Si from etching, and while in the bulk the {100} plane steadily advances, in the corner the slower {111} appears. Scalebar=2µm.*

in KOH defines the tetrahedral shape by a {111} crystalline plane and the shape of the envelope wall (center).

The top ridge of the surrounding wall could be metal coated to play the role of the narrow conductor. Any evaporation done in the situation of fig. 5.11 would short circuit tip and conductor together, (cf. left on fig. 5.12), therefore a spacer is needed. An Si_xNy layer added to the exterior of the wall, allows to selectively etch and remove the SiO_2 layer with BHF, to end up with the situation where a thin gap separates Si_xN_y and Si tip (cf. right on fig. 5.12).

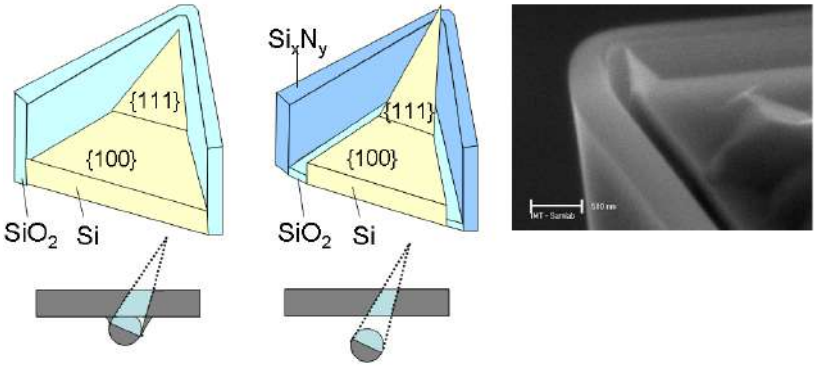

Figure 5.12: *Spacer layer to avoid tip-wall contact. The SiO_2 layer which initially was the wall on which the evaporant was projected, changes its role to spacer. Once the Si is etched down to reveal the tip, the space is removed.*

The oblique evaporation has the tip cast a shadow on the wall, but

also covers the whole tip, which is not good because it is that tip which should be the small island of an SET (fig. 5.13-left). The addition of a retracted plane casts a shadow on the tip. (fig. 5.13-center), thereby creating a small island, defined by the shadow of the retracted plane from the bottom, and by the edges of the tip for the rest. The scanning electron microscope (SEM) pictures (fig. 5.13-right) show an almost 2μm wide step across which the shadow is cast. The closeups of the tip show a good

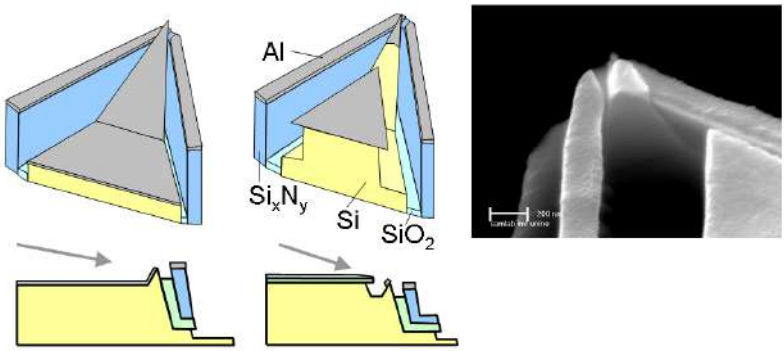

Figure 5.13: *Tip protected through shadow mask during evaporation. A retreated masking plateau protects the lower lying parts of the tip from evaporation. Scalebar=200nm.*

definition of the source–island–drain structure (fig. 5.14).

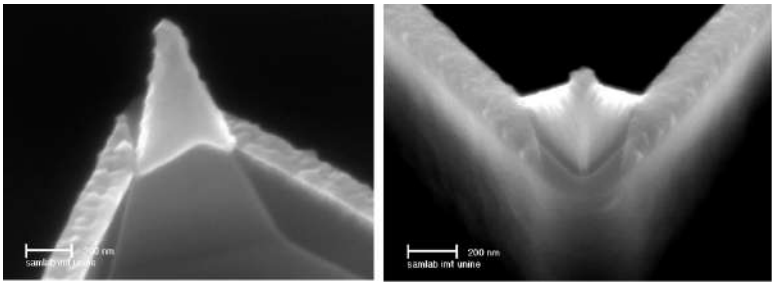

Figure 5.14: *Front and back view of shadow evaporation. The interruption of the metal lines can clearly be seen, as well as the sharp island bottom line shadow cast by the retreated mask. Scalebar=200nm.*

5.3.3.2 Fabrication process detail

The process starts with a Si <100> wafer with thermally grown SiO_2. A cantilever sized rectangle is pattern transferred (positive photoresist, BHF wet etching) into the SiO2 (fig. 5.15-a). The underetching of the SiO_2 mask layer defines via crystal planes the cantilever tip (fig. 5.15-b). Half of the SiO_2 mask thickness is wet etched in BHF (fig. 5.15-c). The overhanging part of the mask is etched from both sides and therefore disappears. The remaining part is used later as an evaporation mask. Three additive steps follow. First a thermal oxidation to grow a Si_2 layer, then a layer of LPCVD SiN, then a layer of LPCVD polySi (cf. fig. 5.15-d). In a carefully

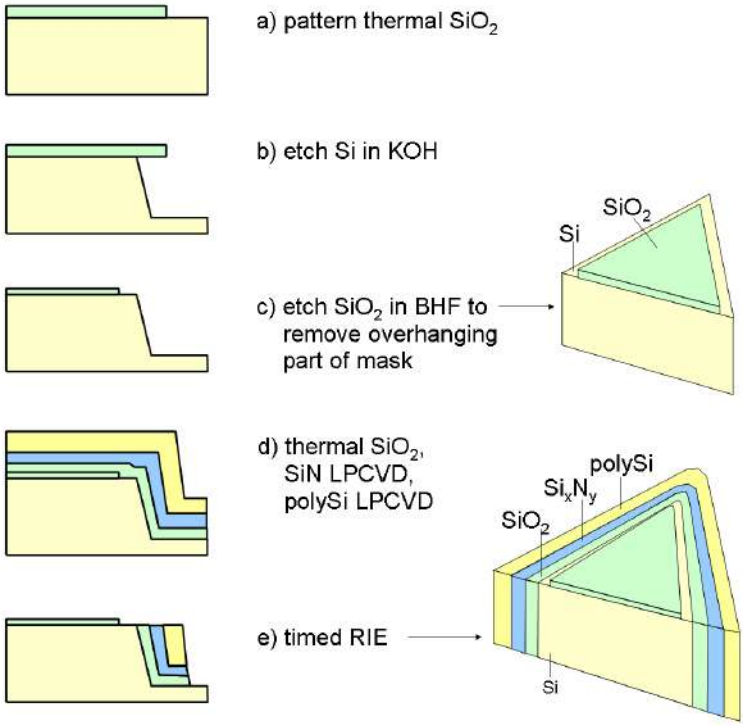

Figure 5.15: *Process, steps a) through e). See body text for details.*

timed RIE step, the polySi, the SiN and SiO_2 are removed, but only as little as possible of the initial mask SiO_2 (fig. 5.15-e). Because the RIE is very directional, the etch rate is much higher on the flat top surface

than on the sidewall, therefore the sidewall is still polySi at the end of the etching, while on the top side the layers are gone. This step is very time critical. The SEM pictures (fig. 5.16) show that an additional 20 seconds change the situation from a covered protected structure to an open and accessible and etchable layer. The SiN layer is the one whereon the tip will

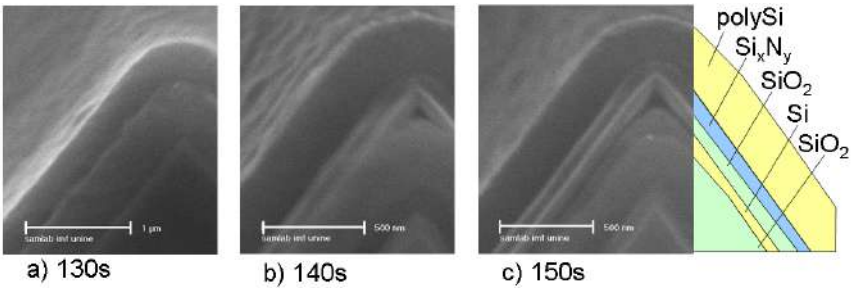

Figure 5.16: *The time criticality of the RIE step shown through SEM pictures at three points of time during the etching: a) SiN still covering the entire ridge, b) SiO_2 beak visible c) SiO_2 open and ready for next process step. The right half gives the stratigraphic sequence.*

project its shadow during evaporation. Therefore it must be lower than the tip, and the SiN layer is etched down (fig. 5.17-f). The tip is formed by KOH etch of the Si layer (fig. 5.17-g). The SiO_2 layer between tip and wall is removed (fig. 5.17-h). The oblique evaporation step can now pattern the metal lines on the ridge of the SiN wall to be source and drain, as well as the island on the Si tip all being protected towards the bottom by the SiO_2 masking layer rear view (fig. 5.18) and side view (fig. 5.19). Although the two final SEM pictures look conceptually promising and appealing, the electrical connection of the SET candidate structure revealed to be impossible to realize, even with the help of FIB. Test structures brought to low temperatures never showed any SET signatures. Therefore this approach was abandoned and buried.

But not without learning something: Don't develop an SET on an AFM-tip, first develop an SET, then transfer it to a AFM-tip. The potential for a global failure is lower.

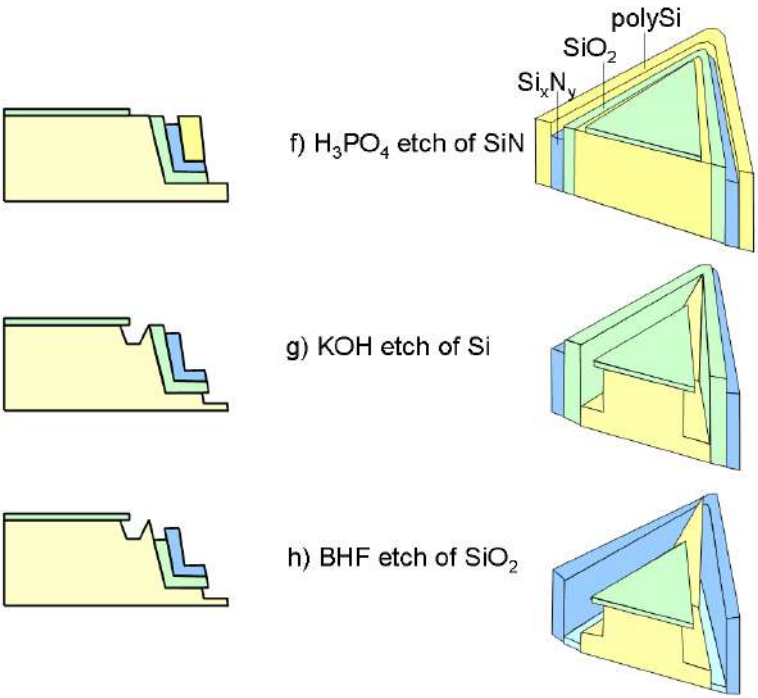

Figure 5.17: *Process, steps f) through h). See body text for details.*

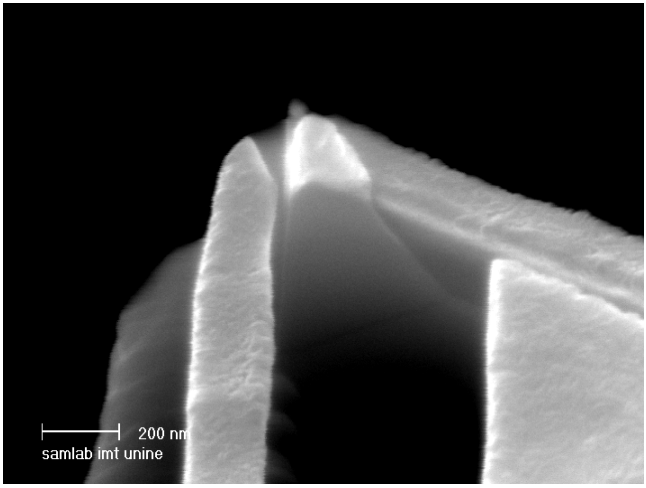

Figure 5.18: *Postevaporation, view angle left from the evaporation source.*

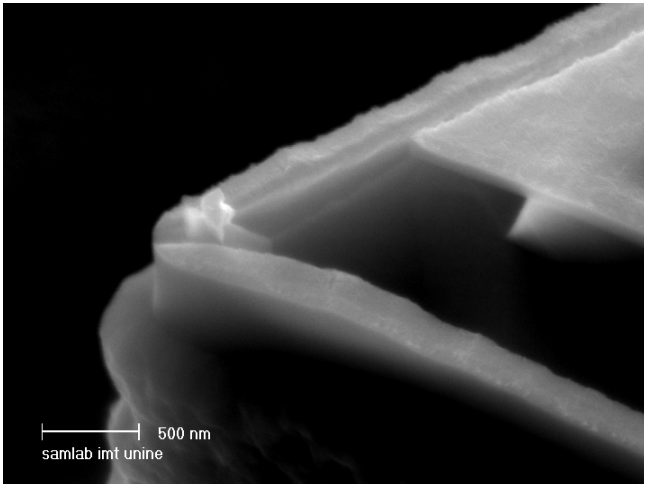

Figure 5.19: *Postevaporation, side view perpendicular to evaporation.*

5.3.4 Electron beam induced deposition

Inside of the electron beam's sample chamber, the vacuum is such that it is sufficient for good electron beam patterning, which does not mean that it is perfect. In fact, there are residual hydrocarbons inside of the chamber, which can come from the sample, the used resist or the oil of the roughing pump. The electron beam activates those molecules and they end up where the beam hits the substrate as a crosslinked hydrocarbon deposit[149]. This is useful for focusing, because if the electron beam is perfectly focused in one spot, the scanning is turned off for a short period, such as three seconds, then the hydrocarbon deposit will be a fine circular dot, also called *contamination spot*. If it is not a spot, then more adjusting of focus, astigmatism, aperture or gun align is needed.

But can also be used for structuring: a contamination resist pattern written by electron beam induced deposition was used to protect a Au-Pd layer during ion etching[125], or a high aspect ratio STM tip was be deposited[150] on top of an existing blunter tip. The EBID technique looked promising, since the dimensions of the structures would be finer than anything patterned using an intermediate resist step could possibly be. Trials performed to generate patterns are shown in fig. 5.20. While the control of the beam is manual (compared to automated resist pattern exposure) but possible, the exposure leaves a parasitic "halo sheet" of contamination resist at the area where the write field supposedly is, despite the fact that not a single SEM picture was acquired of the area before the Al etch. The source of this could not be isolated, and this technique was abandoned.

5.4 Process development for single electron transistor

From the preceding unsuccessful trials, a reason was inferred for why the three techniques, firstly SETs defined by electron beam direct write combined with Nieymeyer-Dolan type evaporation (fig. 4.1), secondly etch or oxidization narrowed Si-wire techniques, and thirdly structured 2DEG, are so popular: those methods have proven over and over to work well.

With an electron beam lithography system available, the Niemeyer-Dolan technique was chosen for the next attempt.

This was also compatible with the ability of fabricating a working SET. being a prerequisite for placing an SET onto an AFM probe, to fabricate a working SET. First, SETs were to be realized on a flat substrate, which

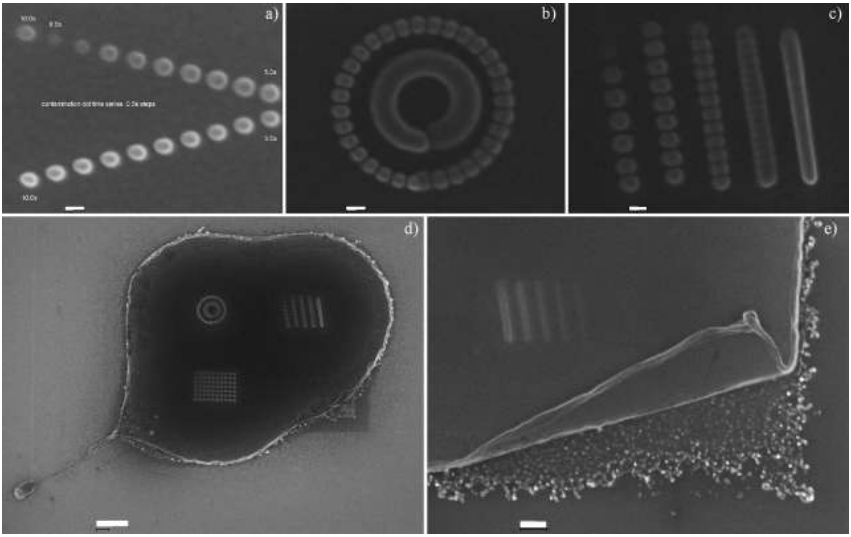

Figure 5.20: *Electron beam induced contamination spots. a) Dots with increasing dwell time, first top left dot: 10s for reference, then starting with 0.5s in 0.5s increments to the right, then back left. b) Concentric circular pattern, the inner ring's dots have collapsed into one structure. Note the discontinuity at the junction. c) Line patterns, diminishing spacing from left to right. d) Three patterns exposed on bare Al, then exposed to Al etch. Despite that never a scanning electron microscope picture of the field was taken, just the mere positioning of blanked beam on the writefield where the pattern had to be written, created such a contamination halo, that the Al etch could not do its work. e) Edge of the "contamination halo sheet", peeled back after Al etch. The slightly attacked grainy Al layer is revealed, and distinguishes well against the Si substrate. Scalebars: a)-c): 50nm, d): 200nm, e): 500nm.*

would be assembled into a sample holder adequate for a cryostat setting, a 32pin ceramic chip holder, and prove that it works. Then this precious piece of fabrication knowhow would be used to integrated the SET onto a tip of a cantilever of an AFM-chip.

5.4.1 Constraints of the Niemeyer-Dolan technique

The suspended bridge dual evaporation technique by Niemeyer-Dolan, discussed already in fig. 4.3, was selected, and the process had to be developed from scratch. In the Comlab, the joint cleanroom of the University of Neuchâtel (UniNE) and the Swiss Center for Electronics and Microtechnology (CSEM), there was no evaporator where the sample inclination could be changed without breaking the vacuum, nor could the chamber be flushed with a special gas, such as oxygen for barrier formation, all with control on the pressure inside, two requirements for Niemeyer-Dolan technique. The development of the process was started, and an evaporator fulfilling these requirements was received on loan from the Nanophysics group of the Swiss Institute of Technology Zurich (ETHZ).

5.4.2 Substrate for chip carrier

The sample holder chosen by the Nanophysics group of ETHZ for their cryostats is a industry standard 32-pad ceramic leadless chip carrier. At its core, surrounded by the bonding pads, lies an area of about 7.5mm $\times$ 8.8mm, where the sample can be placed, then bonded to the chip carrier's bonding pads. A chip size of 7mm $\times$ 7mm was chosen as test vehicle (fig. 5.21). The Nanophysics group usually has one or few samples per chip, therefore they feed 12 signals through the cryostat insert from sample holder to the exterior, leaving the remaining 24 pads of the chip carrier unconnected. Their samples are usually done by LAO of or on 2DEG samples, where one or few electrical structure per sample are obtained, therefore 12 signals are certainly sufficient. As samples and experiments grow more complex, their more recent cryostat inserts have more signals wired through. SETs are patterned by electron beam lithography and easily obtained in quantities of tens or hundreds. The practically implication of this meant that 8 SETs were patterned per chip, their room temperature I-V characteristic was measured, and the best three candidates selected and bonded, one line needed for the sample ground, and the two remaining used for test structures, such as single junctions or reference resistors.

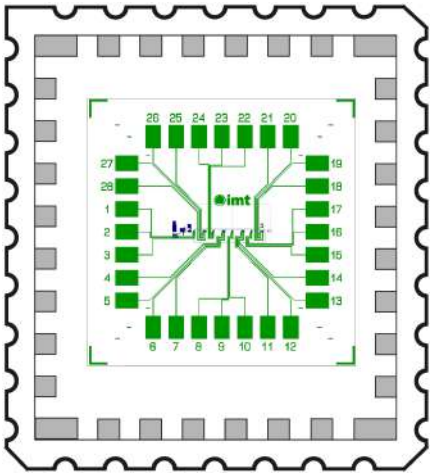

Figure 5.21: *Chip carrier 32 pads (11.5mm×14mm outline), with SET test vehicle at center (7mm×7mm)*

5.4.3 Electron beam lithography system

The available and used electron lithography system is a Raith 150, with a LEO column at its core. Its electron source is a thermionic field emission cathode of Schottky emitter type. An etched <100> oriented W monocrystal with a sintered reservoir of ZrO_2 in the shaft is heated with a small current. The ZrO_2 diffusing to the filament lowers the W work function for emission of electrons. This combined with an electric field extracts the electrons from the tip to the extractor electrode. The LEO column lacks an internal beam crossover, which would cause beam broadening due to Coulomb repulsion between the electrons when their trajectories meet at the crossover points. This contributes to obtain a sharper beam spot. Beam energies up to 30keV can be reached. The interferometric stage is driven by three motors on x,y,z axis, and piezoelectric actuators, and its position repeatability is within 1nm. The stage carries a holder, which is passed with a robot arm conveyor system from airlock to chamber and back. There are special task holders, one allowing for sample rotation and tilt, one clamping the sample electrostatically.

5.4.4 Spin-coating

The electron beam resists processes that were available and characterized were based on 100nm and 200nm thick layers of PMMA, molecular weight 950kDa, from Microchem Corp[151].

A typical approach to create suspended bridge structures is to take two resist of different sensitivities. The top layer, which will be the mask, is less sensitive, and it is the one which is patterned. The bottom layer is more sensitive, and the exposure will yield a hopelessly beyond recovery overexposed pattern, which is also intentionally. The development step will remove all exposed resist, and the perfectly well defined openings in the top layer will find themselves floating over the same pattern in the bottom layer, however in a considerably enlarged version. This is because of the higher sensitivity of the bottom layer resist, makes appear the resulting double Gaussian energy distribution of the scattered electron beam (cf. subsection 5.1.3 on p. 69). is larger, and exposes a larger volume of resist. A halo surrounds the original pattern, and creates the desired undercut. Two exposed lines next to each other will define a suspended bridge between them. If the bridge is too long, then it may stick to the surface after development, it may deform during evaporation, it may not lift off at all, factors to be considered during design.

Publications frequently mention the use of copolymer as bottom layer, and so does the standard PMMA's product leaflet[151], which is why in the end a copolymer was purchased to develop a sandwich structure. The resist sandwich relies much on strictly repeatable layer thicknesses of the two constituents. The layers are applied using spin-coating, therefore exact copolymer and PMMA spin curves were established. Spinning curves link coating rotation speeds ω to target resist thicknesses t, $\log(t)$ vs $\log(\omega)$ is linear, with $t = k\omega^{-\alpha}$, where α varies from 0.4 to 0.7, and k a fudge factor compounding various effects, such as cinematic viscosity, volume fraction of solids, volumetric flow rate, etc.[152]. The process can be viewed as being composed of two limiting steps: Initially, the film thickness variation is due to radial flow, also called radial convection, and the variation due to solvent loss can be ignored. At a certain critical point, there is a transition to where the thickness loss due to solvent evaporation is dominant[153]. Analytical solutions were numerically solved and compared to experiments[154]. As the solvent evaporates from the resist during spinning, its viscosity changes, a concentration gradient is established from the outer edge down to the substrate, alike a solid crust floating on the remaining liquid, until all dilute solution is gone, for each phase[155]. Recent articles perform AFM on spun and postbaked PMMA, fresh and

day old ones, to detect and explain pin-hole formation due to remanent solvent evaporation[156]. They show that for the very thin layers employed (thickness 8nm), the postbake was not sufficient to remove all solvent, the layer remained wet, and became solid after being in vacuum for a day, with tensile stress buildup forming pinholes. This behavior confirms the common strategy of spinning resist only just before using it. Resist is not something static.

5.4.5 Resist system

First the electron resist PMMA was reviewed, with commercial name plexiglas[4]. The product is distributed under the name of PMMA 950k 11% solids in Anisole, meaning that 11% solids of PMMA, of molecular weight 950 kDa [5] are dissolved in solvent Anisole. To be able to spin thinner films, the original solution was diluted down to 4% solids in Anisole.

The energy of the exposure causes *main chain scission*[134] turning the developer insoluble long polymer chains into low molecular weight monomers and oligomers(few monomers), which are soluble in developers.

The copolymer used is a resists based on a mixture of PMMA and methyacrylic acid (MAA). Their respective monomers are[133, 157]:

```
MMA:          CH3                    MAA:          CH3
              |                                    |
    ...[-CH2-C-]...                        ...[-CH2-C-]...
              |                                    |
              COOCH3                               COOH
```

Two varieties are distributed, MMA(8.5)MAA and MMA(17.5)MAA, which differ in the amount of MAA used, 8.5% and 17.5% solids, respectively. They have lower molecular weight and higher dissolution rates in developers, comparable to PMMA 50kDa and PMMA 100kDa, respectively. The lower the molecular weight, the shorter the polymer chains, the easier for electron beam to scission chains into small chunks which are solvable by the developer. The selected copolymer MMA(8.5)MAA 11% solids in ethyl lactate contains 8.5% MAA in MMA (therefore 91.5% MMA), which are dissolved by 11% solids in safer solvent ethyl lactate. The molecular

[4]Inspired from Latin plectere - to weave, an inspiration from the fact that PMMA crosslinks.

[5]kDa = kiloDalton, one Dalton equals the atomic mass and is approximately the mass of a H atom (1.66×10^{-24}g). PMMA consists of many MMA or ($C_5O_2H_8$) units, which each weigh $5\times12+2\times16+8\times1=100$ Da = 0.1kDa, therefore the mean length of the PMMA chains is 9500 monomers.

weight is in the 50kDa range[6]. The spin curves for the copolymer were not available, therefore they were established for three dilutions, cf. fig. 5.22, aiming to cover the thickness range from 50 to 400nm.

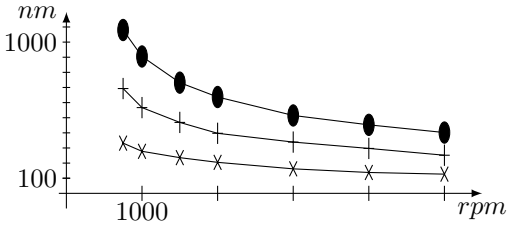

Figure 5.22: *Spin curve for copolymer, ×:6%, +:9%, ●:12% percent solids in ethyllactate.*

The double layer structure called for sanity checks before proceeding, such as a guarantee that the copolymer bottom layer is sufficiently dry after softbake, before the PMMA top layer is spun, and that the PMMA solvent does not significantly dissolve or attack the baked copolymer layer, and that the softbake intended for the PMMA does not induce peeling between copolymer and PMMA . Those preoccupations proved to be unfounded.

Early test exposures patterned everything on the test vehicle by electron beam, but bonding pads, and lines reaching to the SET structures are large surfaces and therefore very time intensive to pattern. Therefore, an approach using a prepatterned substrate, containing bonding pads and connector lines, reduced the electron beam patterning to very short times, since only the SET and maximally 20μm long lines had to be exposed.

The resist sandwich is applied using spin coating, which is not uniform towards the edges of the substrate, especially if the substrate is square and not circular, as shown in fig. 5.23. To get the same constant resist thickness for all exposed structures, then they need to be centered on the chip.

5.4.6 Electron trajectories in resist

The existing processes had been characterized for 200nm thick PMMA. The initial idea was to add the copolymer underneath it, and use identical exposure and development parameters. Since the copolymer is much more sensitive, it should just dissolve a bit more, and yield the perfect undercut.

[6]Private communication, Rob Hardman, MicroChem Corp.

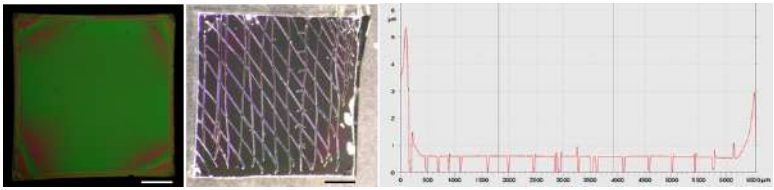

Figure 5.23: *Resist thickness variation on sample. 200nm PMMA ontop of 400nm copolymer. Optical microscope (1mm scalebars) shows fringes(left) in corners, indicating resist thickness variation. Scalpel scratches(center) in the resist are measured with a profilometer(right), showing very regular 600nm thickness, except for the 0.5mm close to the edges (scale ticks horizontal 500nm, vertical 1µm).*

It was not clear if the electron trajectories would be little or much affected by the longer path through the resist, given that the copolymer addition of 400nm copolymer would result in a threefold of the path through the resist. Analytic solutions are rather laborious not to say difficult, which is the reason of Monte Carlo type simulation of electron trajectories in solids being popular[158]. A Monte Carlo simulation of the resist—substrate stack intended to be used for an electron beam lithography can give a coarse overview of where the parameter space should be searched for a viable solution, i.e. acceleration voltage. The distribution of the electron trajectories indicates which part of the resist will receive sufficient dose to be removed by the development step. A freely available university-developed Monte Carlo simulator [159, 160, 161, 162] was used to investigate.

The final SET realization was done with 100nm of PMMA on top of 200nm of copolymer (cf. fig. 5.37 for explanation) sitting on 400nm of SiN on bulk Si. The initial resist thickness (200nm PMMA on 400nm copolymer) and the final ones are given on fig. 5.24 for comparison for 10kV acceleration voltage. The result of the standard 10kV acceleration voltage is sufficient for the 600nm thick resist stack (and better for the 300nm stack), and that if one wanted to avoid charging the substrate and shoot right through it, the substrate would have to be less than a micrometer thick, which was difficult but not impracticable. Again, Monte Carlo simulations used this way are an indicator, not a result *per se*. The pictures illustrate electron trajectories in an attractive way. The results for the whole acceleration voltage range possible on the electron beam lithography equipment are given, first for energies ranging from 1 to 9keV in higher resolution pictures, then for energies ranging from 1 to 30keV.

This gives an indication of electron trajectories. To simulate the expo-

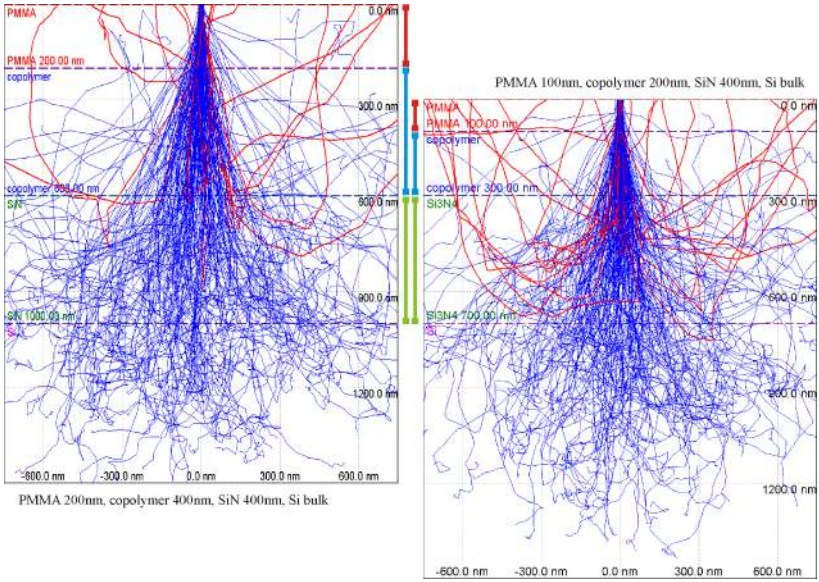

Figure 5.24: *Monte Carlo simulations for thick and thin resist stacks, aligned vertically at the SiN-copolymer interface for comparison, grid 300nm × 300nm, electron trajectories in blue, backscattered electrons trajectories red. Layer bars in center between the two simulations are green for SiN, blue for copolymer, and red for PMMA.*

sure, which translates to which part of the resist received a sufficient energy dose from those electrons in order to be modified to dissolve in or resist to the developer (positive or negative tone), the development process must be included in the model. In addition to single point energy distribution, proximity effects, resist sensitivity change due to local heating, absorbed energy change due to proximity effects and resist heating eventual postexposure bake influences on acid diffusion in resist, developer resolution and rates. The quality of a simulation will lay in how well it will manage to reconcile the difference between exposure profiles and developed pattern shapes[163].

5.4.7 Exposure tests

The 10kV acceleration voltage can possibly be a sweet spot for exposure permitting for easy development. Dose determination tests were done, and the created undercuts are looked at. The datasheet for PMMA resist[151]

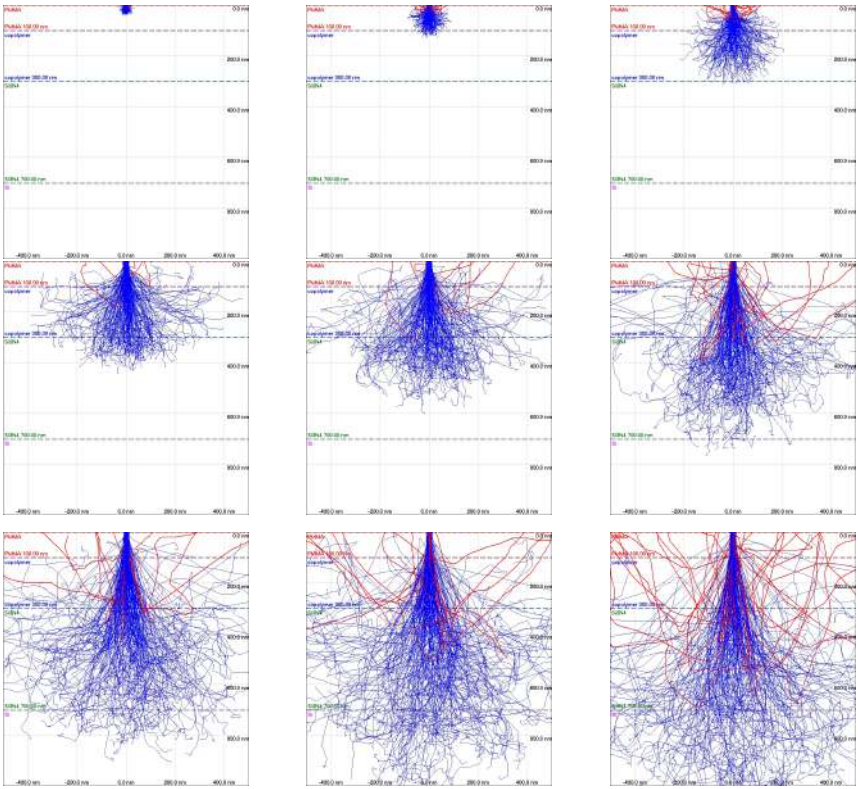

Figure 5.25: *Monte Carlo electron trajectories simulation for acceleration voltages ranging from 1kV to 9kV, closeup. (left to right) top row 1,2,3kV, mid 4,5,6kV, bottom 7,8,9kV*

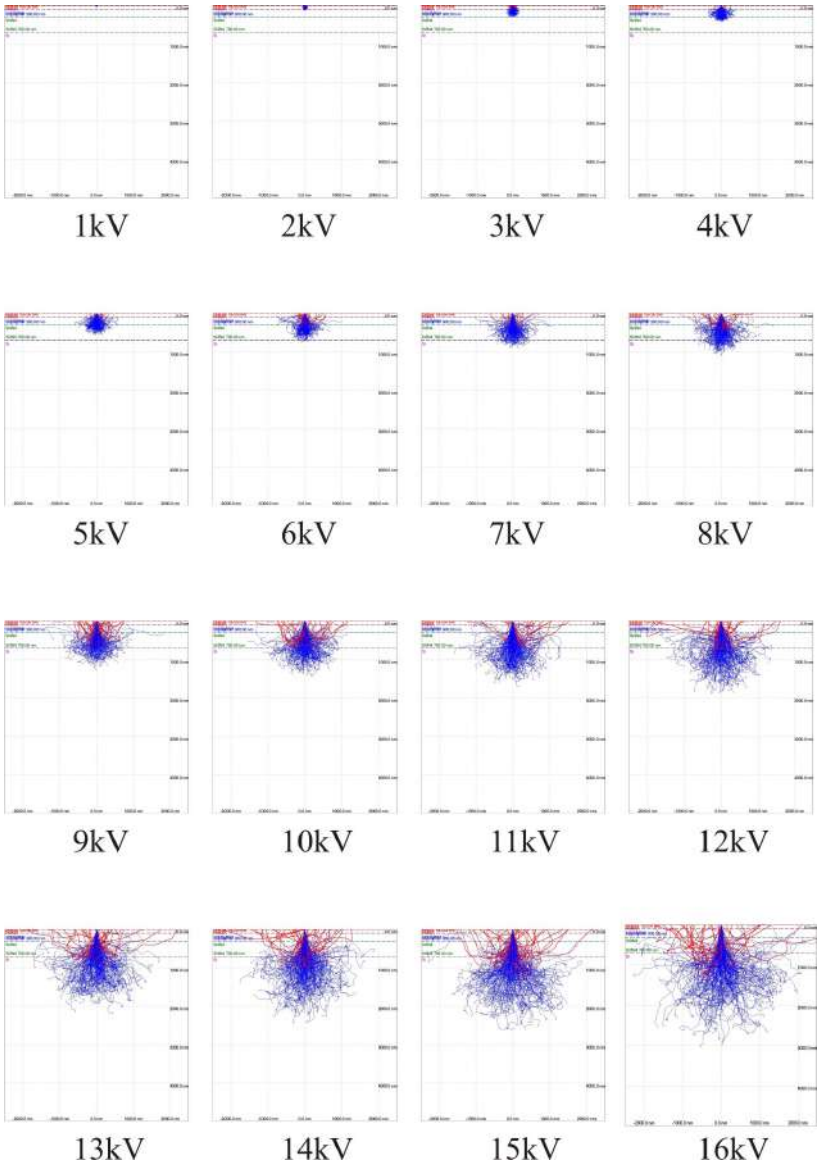

Figure 5.26: *Monte Carlo electron trajectories simulation, overview for acceleration voltages from 1 to 16kV.*

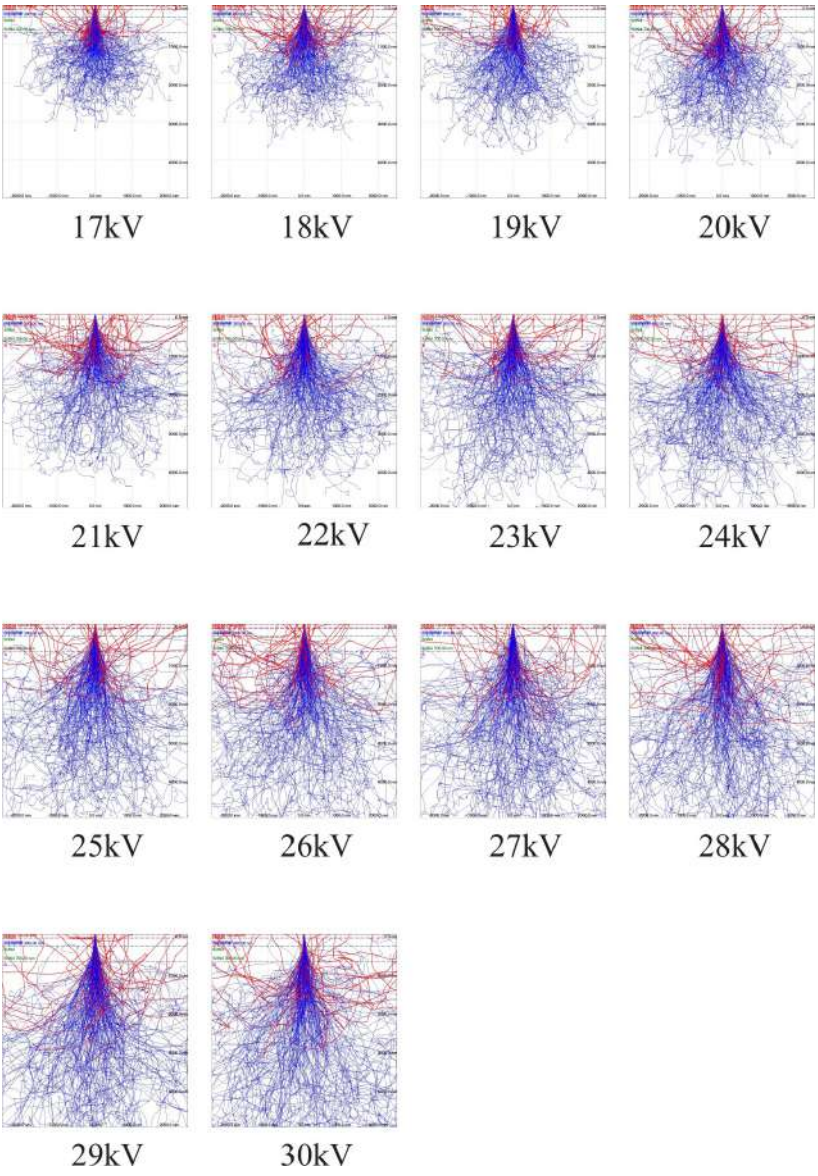

Figure 5.27: *Monte Carlo electron trajectories simulation, overview for acceleration voltages from 17 to 30kV.*

sets the expectation for electron beam exposure dose in the range from 50 to 500 μC/cm^2. When focusing the beam, the finest contamination spot diameters obtainable range from 20 to 50nm. The beam itself is supposedly able to be as fine as $\leq$2nm at 20keV beam energy[164]. By multiplying the area exposure dose by the assumed spot diameter of 20nm, which corresponds to the width of an imaginary exposed single pixel line, the single pixel line dose ranging from 20000 to 50000pC/cm is obtained. The important and influencing factors, other than the coated resist thickness, are exposure dose, developer and developing time. The reference values for exposure were given by the electron beam manufacturer with as developer mixtures of methyl isobytil ketone (MIBK) and isopropanol (IPA), area dose 100μC/cm^2, and single pixel line dose 1000μC/cm, development in MIBK+IPA=1+3 for 45s, stop in IPA for 30s, then rinse in deionized water (DI) water for 30s. For various thickness combinations, from 200nm PMMA layer on top of 200, 300, 400, 500nm copolymer, down to 150nm copolymer with 100nm PMMA, were exposed with wide dose ranges to find good PMMA mask definition and good copolymer undercut, cf. fig. 5.28. The parameters for exposure doses of the supplier were carried forward.

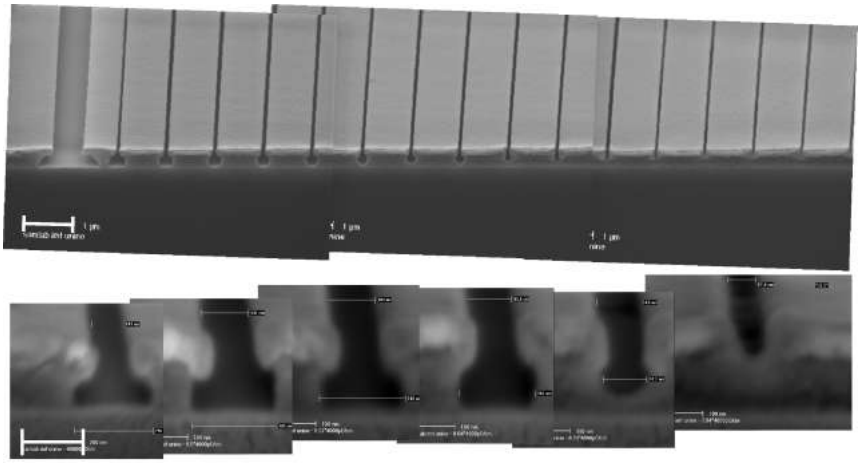

Figure 5.28: *Single pixel lines (SPL) patterned next to an area exposure (to be able to find the SPLs), SPLs with decreasing dose (top, scalebar 1μm) and selected exposure profiles (bottom, scalebar 200nm). As the SPL dose diminishes, the undercut disappears, until towards the end of the series the point is reached where the copolymer doesn't receive any significant dose anymore.*

5.4.8 Standard and non-standard developers

The developer has two tasks. Dissolve the exposed PMMA to create openings in the mask layer according to the exposure pattern, and dissolve the underlying exposed copolymer and create thereby the undercut which allows for two inclined evaporations. Three examples of different strategies are given.

Some use a developer in combination with a selective solvent. after developing the top layer, an additional step removes the copolymer – exposed or not – with a solvent propylene glycol monomethyl ether acetate ($C_6H_{12}O_3$) (PGMEA), timed to create the desired undercut[165, 166].

Others, after the spinning of the copolymer, flash expose with UV light the whole wafer, with a dose below the copolymer exposure threshold. Then the top PMMA layer is spun. The electron beam exposure follows as usually, then development. The copolymer will create more undercut with less dose, because it is already partially pre-exposed[165].

Another method is to electron beam expose a wide strip with a low dose, chosen to be above the clearance threshold for the copolymer, but below the clearance threshold for PMMA. In a second step with high doses the fine mask pattern is exposed. The doses of both exposures together sum up to the clearance dose of the fine mask pattern in PMMA, and creates a wide undercut in the copolymer[166].

In the initial stages of selecting a resist system that would produce a significant undercut of copolymer under PMMA, the performance of MIBK+IPA=1+3 as developer was not producing satisfactory results. Later on in the project, this revealed to be influenced by the spin-coating process, and was solved. Nevertheless, other developers and developing strategies were investigated, in particular the use of PGMEA to increase the undercut in a second development step, for it selectively etches copolymer and not PMMA, and the use of alcohol-water (IPA-H_2O) cosolvent systems as alternate developer.

To visualize the undercuts created by the development step in an exposed pattern, the samples are first scratched with a diamond tip, then cleaved. The practicable minimal length of a pattern necessary to be able to cleave across it with relative ease is ≈3mm. To be able to locate the exposed pattern on the wafer by the naked eye, the pattern was bordered with two reference rectangles of width 200nm, spaced 5μm from each other. A continuous single pixel line, spaced 100nm from an adjacent dashed (100nm dash - 100nm no dash) single pixel line, in order to create floating structures, was placed for four times, every 1μm, between the two above reference rectangles. Fig. 5.29, 5.30 and 5.31 show the exposure

of the pattern with single, double and triple of the standard dose, respectively, where the unit dose is $100\mu C/cm^2$ for area and $1000\mu C/cm$ for single pixel lines, then developed (top rows) with standard MIBK+IPA=1+3 development, MIBK+IPA=1+3 for 45s, stop in IPA for 30s, then rinse in DI water for 30s, and compared with alcohol-water based development, IPA+H_2O=9+1 for n seconds, stop and rinse in DI water for 30s, where n equals to 15s (second row), 30s (third row), 45s (fourth row), and 60s (fifth row) of development time. One can see that the single pixel line unit dose is insufficient for MIBK development, and gives a better result when doubled. Further, the alcohol-water based development gives very similar development profiles compared to the MIBK ones, a surprise given the simple and cheap composition of the developer. A comparison of profiles is given fig. 5.32. For further leading information on the influential parameters for developers, development conditions and development process, such as developer dilutions, temperature[167], agitation effect on contrast curves, line edge roughness, sensitivity, resolution, refer to[168, 169, 170]. Alcohol-water cosolvent systems[171, 172, 173, 174] are interesting because they only act as a solvent when mixed together, separately taken, both isopropanol and water, are non-solvents for PMMA . The decision was taken to increase the single pixel line dose, and to use MIBK+IPA developer.

The final recipe was that the copolymer was spun on a oxygen plasma cleaned surface, without adhesion promoter, softbaked for 90s on a hotplate at 180°C, cooled on a cold surface, then the PMMA was spun, softbaked for 10 minutes on a hotplate at 180°C. After exposure, the development was done in MIBK+IPA=1+3 for 45s, then stopped in IPA for 30s, then rinsed in DI water for 120s, then blow dried with N_2. If the duration of the second softbake, i.e. after the top layer PMMA spinning, is significantly lower than the arbitrarily chosen 10 minutes, then a long time later in the fabrication process, notably during liftoff of the evaporated metal, the adhesion of the evaporated metal in the areas freed of resist, would be very bad, and very often the whole evaporated SET would peel off. A hypothesis is that after an insufficient softbake, the solvent ethyl lactate remaining in the unsufficiently baked copolymer bottom layer would during electron beam exposure be transformed in a way that would form a residue on the substrate, and preclude the evaporant from adhering properly.

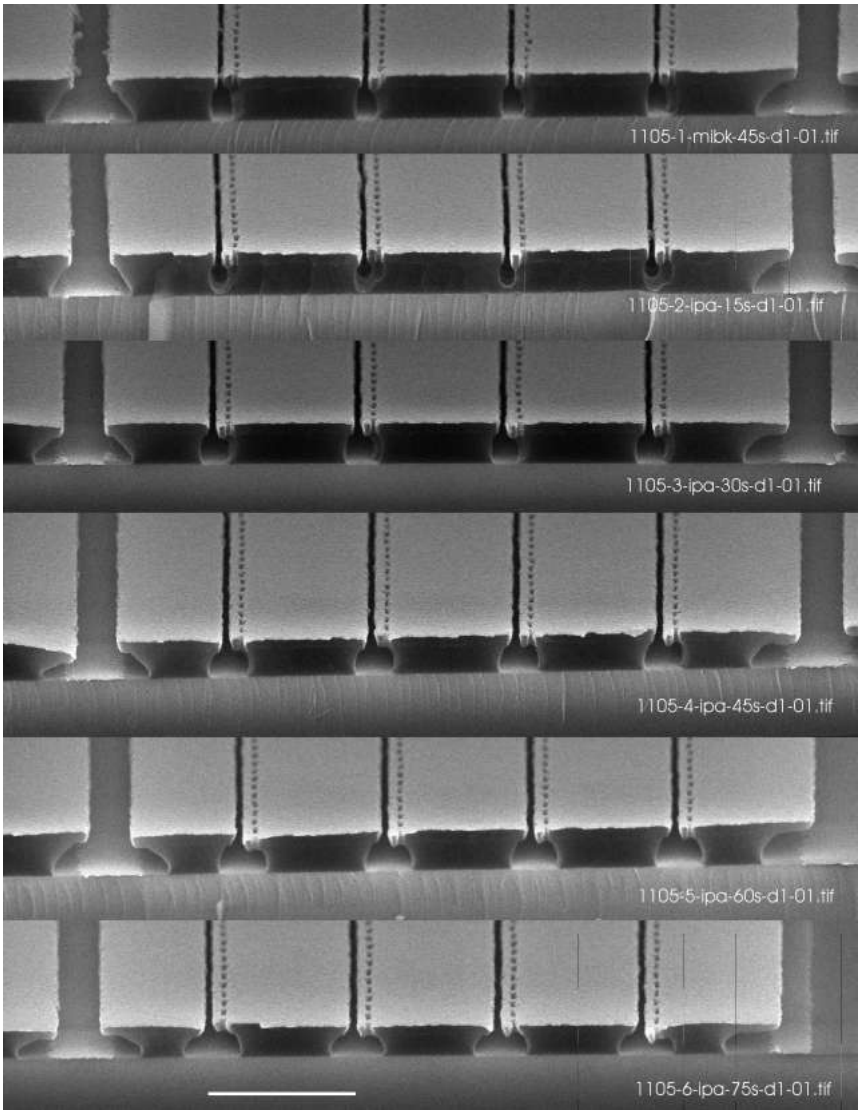

Figure 5.29: *Single pixel line profiles, dose 1000$\mu C/cm$, top row developed for 45s in MIBK+IPA=1+3, others (top down) in IPA+H_2O=9+1 for 15s, 30s, 45s, 60s, 75s. Scalebar=1μm.*

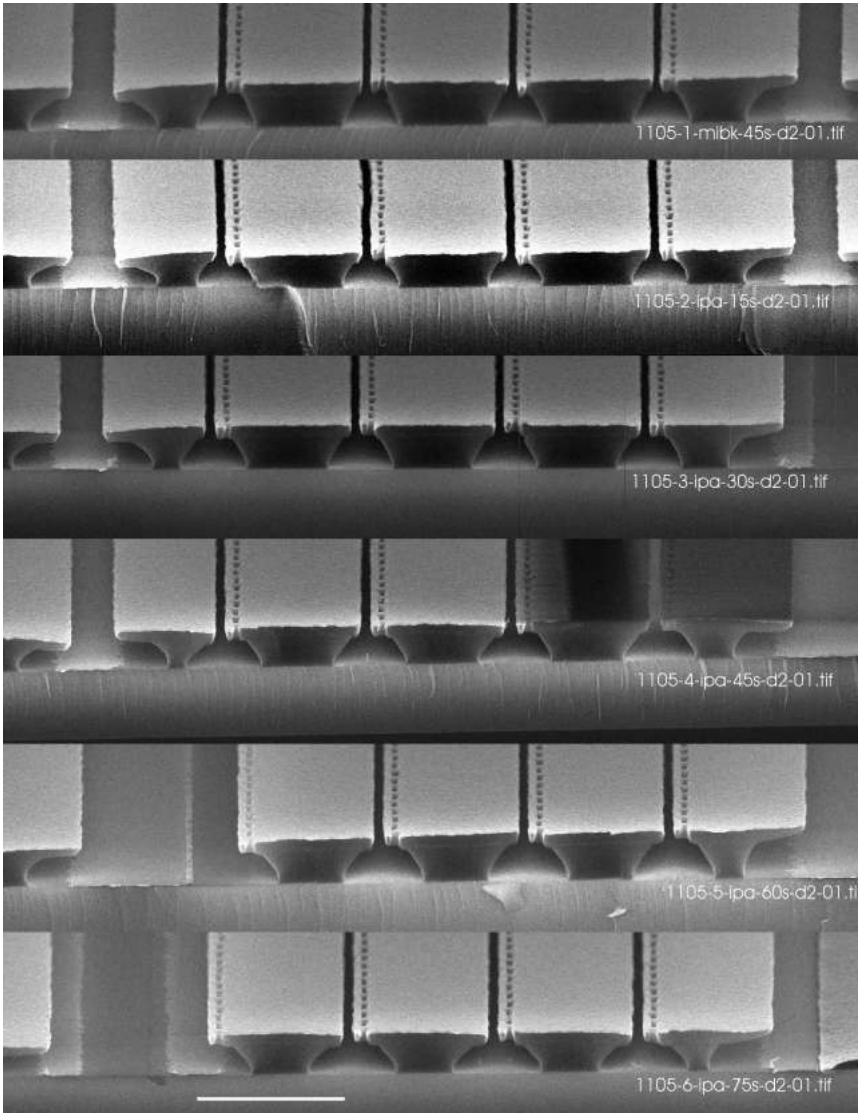

Figure 5.30: *Single pixel line profiles, dose 2000$\mu C/cm$, top row developed for 45s in MIBK+IPA=1+3, others (top down) in IPA+H_2O=9+1 for 15s, 30s, 45s, 60s, 75s. Scalebar=1μm.*

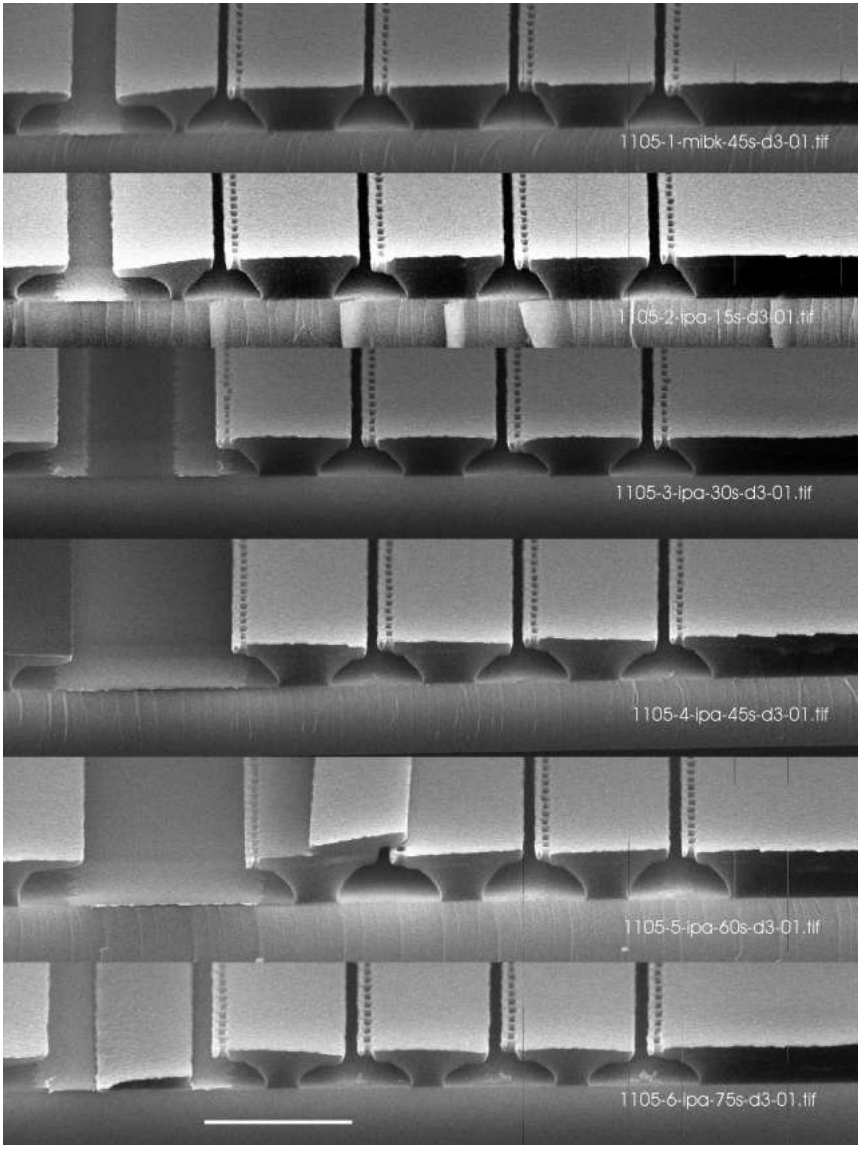

Figure 5.31: *Single pixel line profiles, dose 3000$\mu C/cm$, top row developed for 45s in MIBK+IPA=1+3, others (top down) in IPA+H_2O=9+1 for 15s, 30s, 45s, 60s, 75s. Scalebar=1μm.*

Figure 5.32: *Undercut profile function of dose and developer. SPL dose 1000 through 3000 $\mu C/cm$, top MIBK+IPA=1+3, others IPA+H_2O=9+1. The lower right side SEM pictures show a* ***cave in*** *effect of the resist bridges. This is not a mechanical issue, it is due to the interaction of the scanning electron beam acquiring the picture with the sample, and cumulative, i.e. getting the worse the more images are captured. Scalebar=100nm.*

5.4.9 Layout design

The gdsii design constraints are simple:

- Two inclined evaporations through a mask must be able to produce an island connected to drain and source through two junctions with drain and source, and possibly a gate electrode nearby.

- Because the design will ultimately go onto a probe tip, which is traditionally wedge shaped, the SET and the connections leading to it were positioned inside of a imaginary wedge shaped area.

- The structures should be as small as possible with the technology, making them bigger if required remains possible.

- The junction capacity and resistance are defined by the overlap of two evaporations steps. Incident angle variations can result in significant overlap variation, however this is more pronounced for perpendicular than for parallel movement with regards to the axis of angular rotation. To avoid that kind of variation all SETs were aligned on an equatorial plane on the test chip aiming to have all evaporation inclination angles the same.

The first constraint is only bound by imagination. Some sketches done to get spatial feeling of the situation are rendered in fig. 5.33. They are by no way an exhaustive catalog of solutions, but an indication that the chosen design is not the only one possible. When two structures are patterned close to each other, then the development undercut makes that the remaining mask layer between them is no longer supported by the copolymer layer. This has to be kept in mind, because the bridges can be of a certain length, beyond which they easily break during development or sample manipulation, or collapse under tensile stress or melt under heat during the evaporation step.

The second constraint is already respected in those sketches (except for the right top one), it just needs to be kept in mind.

The third constraint became clear after the first couple of single pixel line exposures. With the chosen process, the smallest obtainable line width turned out to be 60-70nm sometimes going up to 100nm, depending on development and evaporation variations, as seen in fig. 5.32.

The forth constraint is of importance in the whole chip floorplan only, and the equatorial plane can be guessed by the crowding of lines in the center of fig. 5.21 on p.94.

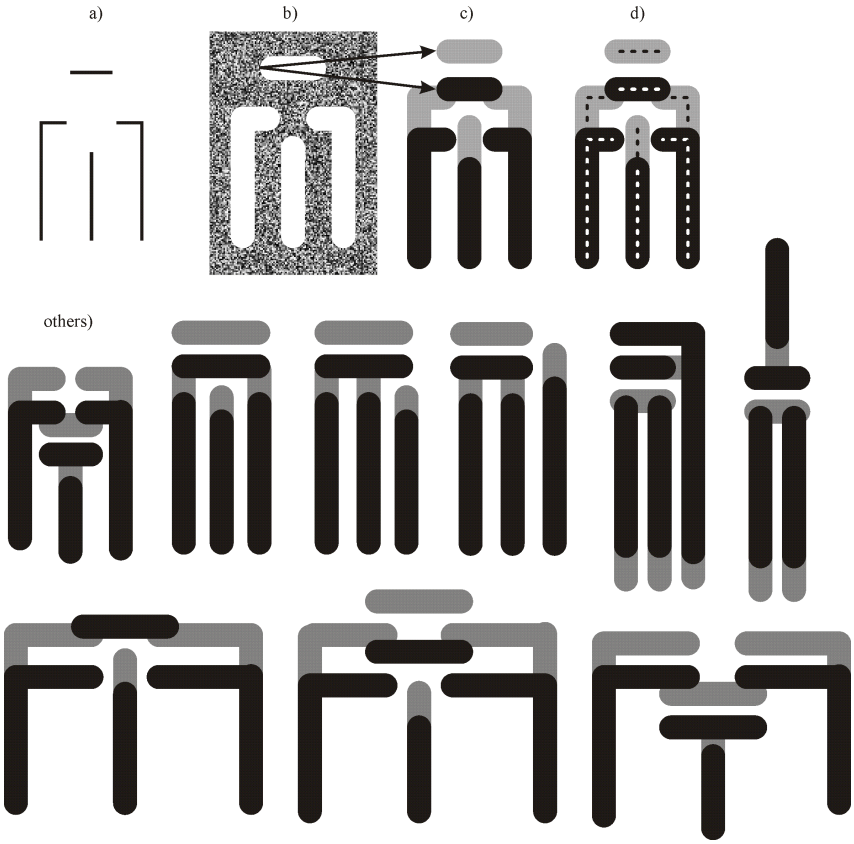

Figure 5.33: *Double angle mask fabrication sequence and mask proposals. a) gdsii mask data as used for exposure, b) resist (dithered) with developed zone (white) removed, c) two evaporations at two angles(arrows) define two shadows (first grey, second black), d) shadows with superimposed original gdsii mask data projection. others) shows variations of possible structures.*

5.4.10 Exposure dose

5.4.10.1 Dose ranges for dots, lines and areas

The used electron beam lithography equipment[7] distinguishes three regimes of exposure, namely dots, lines and areas. **Dots** are exposed directing the beam to a specific location. Then a controlled opening and closing of the beam blanker allows for the specified dose of charge to be deposited. Given that the beam current is constant, the parameter available is the time the blanker is open, or *dot dwell time*. In this case, the limitation is the "shutter speed" of the beam blanker. The default electromagnetic beam blanker of a SEM is considered to be too slow for this purpose by the electron beam lithography equipment manufacturer, therefore they added their own electrostatic beam blanker. The pattern generator, which ultimately controls the blanker, runs at 10MHz, and the software allows for minimal dwell times of 0.1μs to be achieved, which is short.

Before continuing, a closer look to "directing the beam to a specific location" is given. The electron beam column has towards its end the "scan coils" which deflect the beam in x and y direction, within the "write field". The deflection signals are calculated based on the fractured data of the gdsii design data in a digital pattern generator. For a given writefield, the pattern generator can resolve single deflection steps with a resolution which is determined by its A/D converters capacity, in this case 16 bits, which yields for a 50μm$\times$50μm writefield a minimal deflection step of $50\mu m/2^{16}$=0.763nm. This is the minimal grid to which any design data must be clipped to or rasterized upon. **Lines**, also called *single pixel lines (SPL)* because the beam only passes a single time on the picture element (pixel) when drawing the line, are created by moving the electron beam along the path defined by its start and end coordinates. The exposure starts at the beginning of the line where a determined dose is deposited. Then without blanking, the beam is moved to the next position along the path, a position defined by the increment of *line step size*, where another dose is deposited, and so on until the end of the path is reached. The *line step size* is generally small compared to the electron beam diameter, therefore the deposited doses, if assimilated to a circle viewed from the top, overlap enough for them to be no longer individually distinguishable. With constant beam current, the parameters available for SPL exposure are the *line dwell time* and the *line step size*.

Areas are exposed as a non-interrupted series of lines that are "cadenced" internally, and spaced from each other by the *area step size*. The

[7] Raith 150 Gaussian beam vectorscan, details in subsection 5.4.3 on p.94.

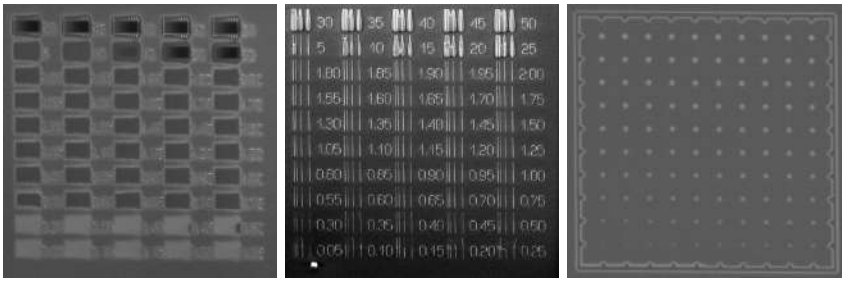

Figure 5.34: *Dose grid exposure on a 50µm×50µm write field. Doses range from 0.05 to 50× nominal dose. (left) area dose (1 =100µC/cm^2), (center) single pixel line dose (1 = 1000pC/cm), (right) dot dose (1 = 0.1pC).*

pattern generator and the fracturing software decide on the strategy on how to fill an area. With constant beam current, the parameters available for area exposure are the *area dwell time* and the *area step size*.

The exposure doses are given for each of those three cases separately, and they have to be determined for each new resist system. Following grids on fig. 5.34 were used for their determination, and later on in each single exposure, because in case there were unexpected behaviors, the exposure could immediately be checked solely based on the simple dose patterns which would take 2-3 minutes to expose. An interesting effect happens at high doses, where PMMA is known to re-crosslink. It starts with a slight shadow around 15× the nominal dose, grows to full contrast reversal around 30× nominal dose. The pattern remains in PMMA, as if it were a negative electron beam resist, surrounded by a halo of developed and removed resist, which received even far away from the pattern its clearing dose due to the backscattering of the very overexposed pattern. Indirectly, this is an observation of the zone that backscattered electrons can reach, the β backward scattering parameter of proximity correction.

5.4.10.2 Dose determination

Dose determination is a starting point, it gives the information on how much energy must be deposited by the electron beam to make the resist solvable to the developer. But the energy may not only come from the electron beam that is drawing the pattern, but also from an adjacent pattern in form of forward or backwards scattered electrons, more commonly known under the name proximity effect, with well described models[132], and

methods to extract the model parameters from test exposures[131]. Parameters determined in a student course for 100nm PMMA on Si extracted forward and backward scattering constants of α=50nm and β=600nm. There are an additional 200nm of copolymer and 400nm of SiN for the SET samples, but the values clearly indicate that the scattering range is similar to or farther than the entire SET structure. See also in the appendix B on p.189.

In an ideal world, the exposure tool allows to simulate an exposure including proximity correction. The used electron beam litho system has this capability, but only for polygons, i.e. areas, but not for single pixel lines and dots. This capability was only introduced in 2007[175], and therefore not available in the early days of dose determination. With the ability to simulate ruled out, matrix exposures, such as in fig. 5.35 were done to figure the interplay of minimal spacings and sufficient doses.

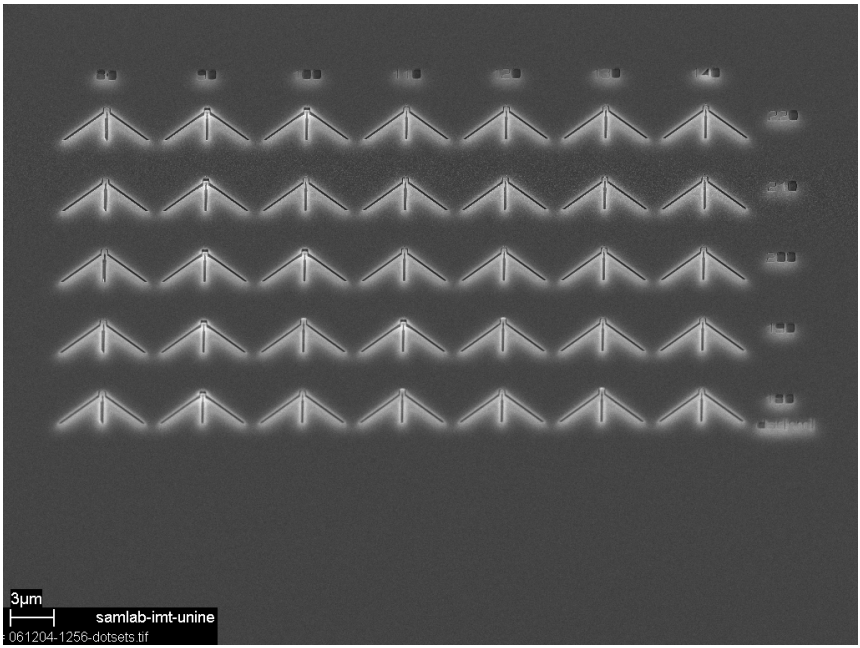

Figure 5.35: *Typical matrix exposure, varying source-drain spacing (horizontally) and gate offset to source-drain baseline (vertically). Scalebar 3µm.*

5.4.11 PMMA-copolymer layer thickness change

Line edge roughness of the final Al lines continued to be an issue. After some reflection, it was realized that the evaporant had a long trajectory ahead of it after passing through the mask opening, i.e. after the 200nm PMMA mask, there were still 400nm flight path to go before hitting the substrate, which is not a long distance considering how far a distance was traveled since the source, but a lot comparing the feature size desired as shown in fig. 5.36. Furthermore, the 200nm thickness of a mask defining

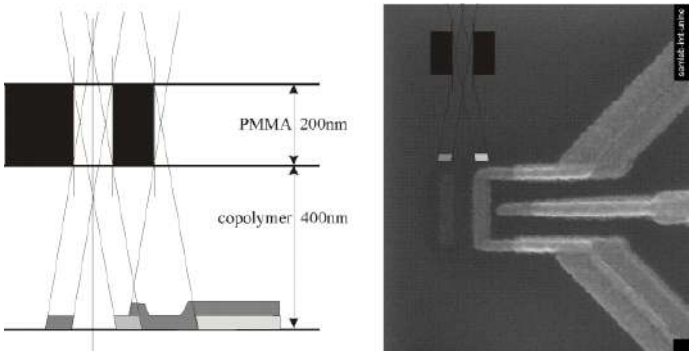

Figure 5.36: *Resist sandwich PMMA 200nm, copolymer 400nm*

60-100nm wide structure required the use of deposition angles close to the normal, only to be able to pass through the mask, while thinner mask layer would have allowed for flatter evaporation inclination angles, allowing for single pixel lines spaced farther away from each other. Even though the passing from a PMMA-copolymer resist sandwich of 200nm-400nm to 100nm-200nm required small dose adjustments, the immediate result was a sharper definition, as can be contemplated in fig. 5.37.

5.4.12 Undercut versus bridge stability

The undercut, which for the suspended bridges translates to lack of support through the copolymer layer, renders them fragile. At the same time it is necessary to permit two inclined evaporation steps to overlap. The undercut must be at least half of the spacing of the exposed single pixel lines, since two adjacent halves contribute equally to join together. In fig. 5.38, the undercut reaches about 200nm behind the edge, more than sufficient to create a free-standing, non-supported PMMA zone between

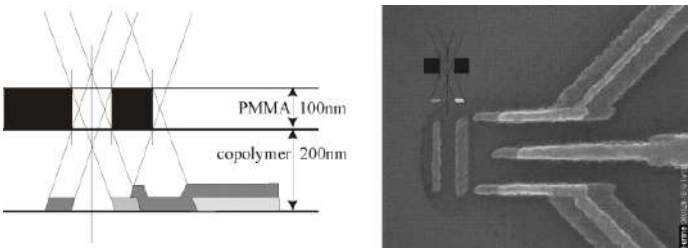

Figure 5.37: *Resist sandwich PMMA 100nm, copolymer 200nm*

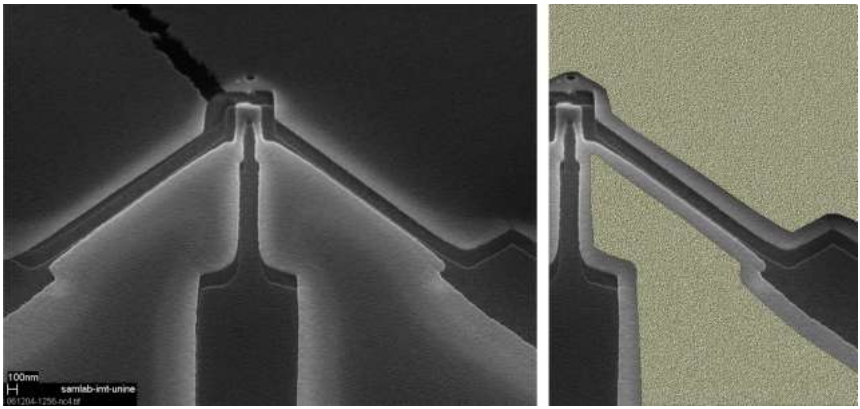

Figure 5.38: *SEM picture (45° tilt) after one metal evaporation step. Undercut, freestanding areas of PMMA charge up more (brighter) than areas supported by copolymer (darker). The grey outline on the half-figure on the right retraces supported PMMA. The chargeup gradient between freestanding and supported areas blurs the exact line. The crack leading from the SET zone towards the back of the image formed during SEM observation due to stress induced by heating of the resist. Scalebar=100nm.*

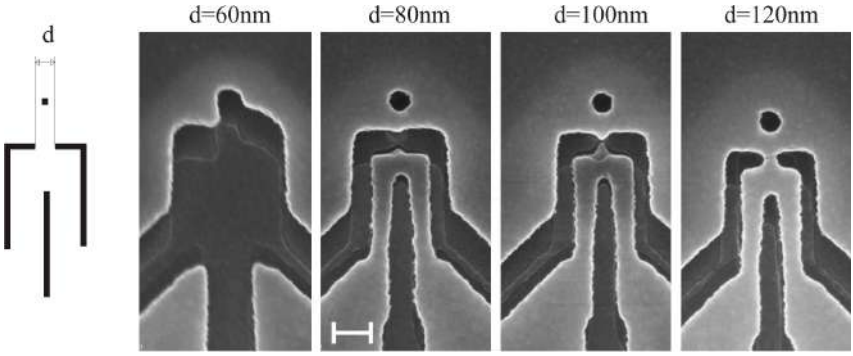

Figure 5.39: *Double angle mask variations. The gdsii on the left shows the SET structure, with the source-drain spacing d as the parameter being varied. SEM pictures after one metal evaporation step. Due to the inclined observation, the metal layer contours can be seen underneath the mask. d=60nm: resist bridge breaks away during development. d=80nm: pinch on opening visible (scalebar=200nm, valid for all). d=100nm: bridge formed, but torn open due to tensile stress induced by Al film evaporated. d=120nm: bridge formed, and stable. Scalebar=200nm.*

two lines spaced by 200nm in the SET area. The balance between getting an undercut and having a bridge sagging because not enough supporting structures are around is a balance sometimes difficult to find. As shown in fig. 5.39(left to right), minute changes to the spacing d between the ends of the lines intended to be the source and drain electrodes may yield results ranging from the whole structure being torn off, to perfect spacing, allowing to contact the island of the other evaporation with two small tunnel junctions, but also obtain a spacing where the island remains unconnected.

5.4.13 Low order sacrificial alignment mark

At one time, the gdsii was changed when the connectors where pushed from a flat layout into a hierarchical subcell. That day, not a single SET was patterned. After several exposures, and intensive old *versus* new comparisons, because the contents of the gdsii were unchanged, except for the rendering hierarchical, the following analysis was made. Sometimes, especially after stage movements done with the x-y motors, that span more than just one or two writefields, the stage or the electron beam does not settle immediately or correctly, and the first few polygons of an exposure

are blurry, out of shape, or not patterned at all. The order in which shapes are patterned depends on their chronological order of creation in the gdsii. Unless a different cardinal order is assigned to them in the gdsii with the gdsii editor's command "order", this sequence is not modified. The blurring effect was hidden at first, because the big area structures of the connectors were drawn in the very beginning, and because they are large structures, the couple of missing or blurred meandering lines at some random polygon edge went always unnoticed. Those connectors remained fixed and unchanged, meanwhile the SET cells changed and had several major revisions. The day the connectors were pushed down into a subcell to make editing and selecting the remaining polygons easier, the SET cells became to be the most ancient ones in the gdsii, and therefore were moved from late in the exposure order of shapes to the initial positions. During the exposure, nothing was there to protect them from being the first structures to be exposed and therefore they were blurred out. This behavior could be reproduced by other users of the local systems, but not by the electron beam lithography system vendor, and might be related to our model of pattern generator, although already replaced twice for different reasons. To work around this strange effect or rather to avoid the fact, low order sacrificial alignment crosses were inserted in every writefield, and manually forced to have the lowest order number in the exposure, hence the name low order sacrificial alignment mark. As fig. 5.40 top left shows, the alignment mark is the first structure to be written (detail bottom left) and because of that it is blurry, while the rest of the structure is fine. The alignment marks are written in this order: first the large rectangles: west(1), south(2), east(3), north(4), then the central fine cross(5,6), finally the thin bars(7-14) forming the surrounding square, counter clockwise, starting from the west. The only lines patterned correctly are the last three fine lines of the surrounding square, west to top-left(14), north to top-left(13), and north to top-right(12).

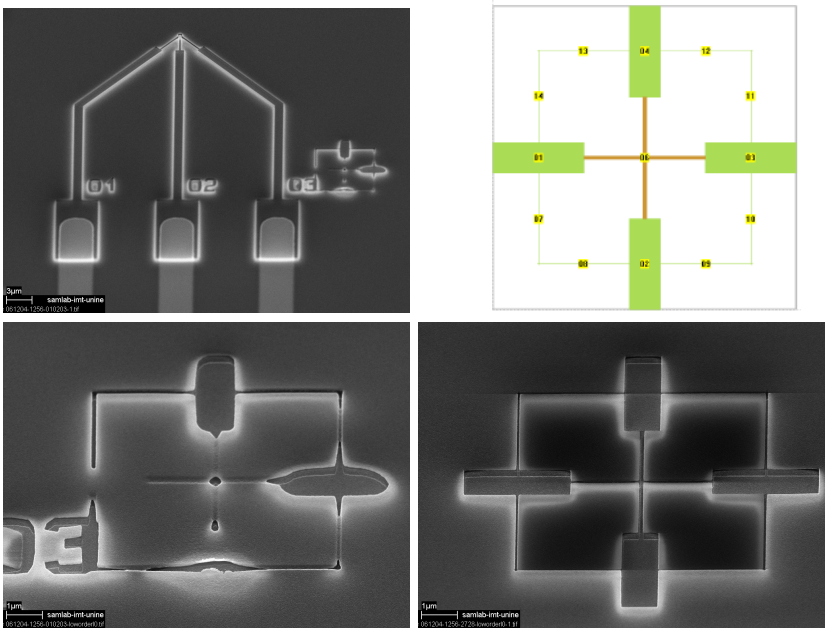

Figure 5.40: *Low order sacrificial structure to avoid feature loss. Top left: correctly and sharply patterned SET with connection lines. To the right of ID number "03", a blurry sacrificial alignment mark can be seen. Every writefield with critical structures (single pixel lines, dots) required such sacrificial structures. Top right: the gdsii with the order numbers of the shape on bright background, Bottom left: close up of the blurred sacrificial alignment mark, where big rectangles 1(west) and 2(south) are missing, and 3(east) and 4(north) are patterned but have blurry corners. Bottom right: sharp sacrificial alignment mark, written immediately after another one was written. No blur, sharp corners. All scalebar=1µm, except top left where scalebar=3µm.*

5.4.14 Layout design data

Since the process development was an iterative process, the gdsii is only given here in the end, in fig. 5.41 as overview of the whole writefield, including the low order sacrificial alignment mark, which is sharp because the previous writefield was 50μm below, and therefore stage movement was minimal, and stabilized within time for this writefield. The gdsii layout data for the SET itself is given in detail view in fig. 5.42, with the corresponding SEM picture.

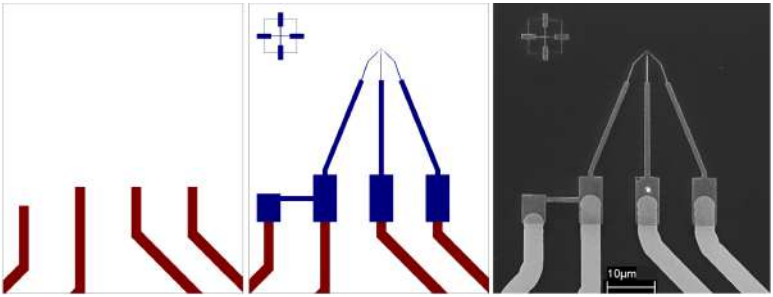

Figure 5.41: *Layout of Pt connectors (left), the structures written by electron beam lithography added (center) and the corresponding SEM picture (right). Scalebar=10μm for all.*

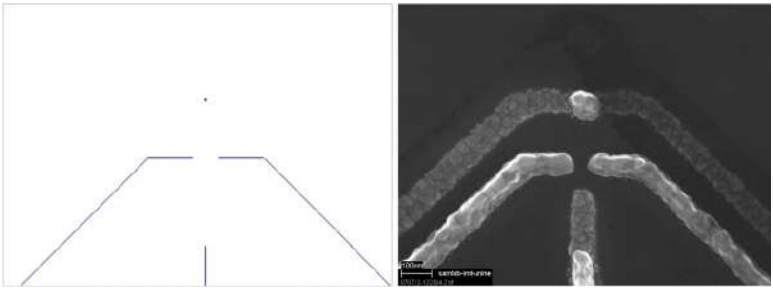

Figure 5.42: *Gdsii layout of SET (left), composed of single pixel lines and a dot, with the corresponding SEM picture (right). Scalebar=100μm.*

5.5 Evaporation

5.5.1 Note on barriers and tunnel junctions

The evaporation steps to deposit source, drain and island are the crucial part the of metallic SET fabrication, because it is here that the tunnel junctions are defined, and the they must have just the right capacitance and resistance to allow for single electron charging effects.

All publications on metallic SET use tunnel junctions as barriers, except one. Nazarov established that tunnel junctions are not needed to provide single electron effects in a metallic island, but may be replaced by an arbitrary scatterer, which however must be providing for sufficient isolation between the island and the source and drain electrodes[176]. This concept was proven in the experiment by Krupenin[177, 178] using highly resistive Cr thin-film strips to connect an Al island to its Al source drain, fabricating an functional SET. Between the Al and Cr evaporation, the vacuum was not broken, and no oxidation step was done to form an Al_2O_3 tunnel junction between Al and Cr, the Cr lines are the arbitrary scatterer. Processing-wise this has the additional advantage that no oxidation step is required.

5.5.2 Melting temperature

Resist is not inert during the evaporation of the electrode material. The glass transition temperature (T_g) of the used PMMA is approximately 95–106°C. If the temperature gets higher, then the pattern is no longer guaranteed, because the resist starts flowing. The high temperatures cause a thermal load on the resist, which combined with ultra high vacuum leads to outgassing of the organic polymers, and this gas is readily reintegrated in the metal film being deposited, deteriorating or annulling its superconducting properties. This is especially a problem when superconductive or ferromagnetic metals with high melting points are used. Direct IR-radiation from the source heats the resist and the evaporation chamber and is a major concern. The heat-up of the resist can be mitigated by evacuating the heat to the substrate it is sitting on, ideally one with high thermal inertia, and then further to a substrate holder, ideally one which is actively cooled. The heat up of the evaporation chamber itself does not get anywhere near the melting points of the used materials, such as Nb(2468°C), Ta(2996°C), Fe(1535°C), Co(1495°C), Cr(1857°C), Ti(1660°C), which are used by researchers interested in fabricating special junction sequences involving supraconductivity, rather than in SET behavior. Nevertheless, the

temperature of the chamber may get close to the limits allowable for the resist.

One solution to steer clear from resists during evaporation steps is to use only non-organic masks. Two examples are given.

On a Si substrate, a SiO_2 layer is grown as spacer layer for the undercut, and a Si_3N_4 layer for the masking. A PMMA layer on top is patterned by electron beam lithography, then the pattern is transferred into the Si_3N_4 by RIE, and finally, the SiO_2 is etched by BHF to provide an undercut. The mask is ready for a two/three step oblique evaporation[179, 180].

A PMMA layer on top of an SOI wafer is patterned by electron beam lithography. RIE transfers the pattern into the Si layer, then the BOX layer is BHF etched to provide the necessary undercut[181].

Those techniques can create very fine SET, with close to perfect electrical behavior. But the suspended structures remain there after evaporation, which is no problem if you want to characterize the SET, but which is a problem if you want to use the SET as a probe. To remove the SiO_2 supporting layer alike a "liftoff" process, BHF can be used as an etchant, but it also etches many metals, and the SiO_2 of the natively oxidized Si substrate, making adhesion a tricky business, tricky to the point that it is not done.

But to avoid such elaborate schemes, many SETs are realized using low melting point metals, one of the reasons for Al(T_f =660°C) being so popular. An even more important reason for selecting Al is of course its stability and quickly formed oxide.

5.5.3 Critical temperature for superconductivity

Another attribute rendering Al attractive for the investigation of superconductivity, is that it is superconductive below T_c=1.18K , and an all Al SET will become a SISIS structure if cooled enough (where S stands for superconductor, I for insulator, and N normal conductor). The fabrication of SNS and SIS Josephson junctions was the motivation for developing the two angle shadow evaporation technique[91], and Josephson devices remain a researched area[182, 183].

Other low melting point metals such as Cu(1083°C), Pb(327°C) and Sn(232°C) play minor roles, and are used because Cu remains normal conductor and Pb(T_c=7.20K) and Sn(T_c=3.72K) are superconductive before Al(T_c=1.18K). A superconductor-insulator-normal conductor-insulator--superconductor (SINIS) structure based on an island in Al and on source and drain in Pb or Sn, can be rendered SISIS and back SINIS, merely

by adjusting the cryostat temperature. This works for any adequately designed Josephson junction structure using those metals.

5.5.4 Metal layer formation

Metal evaporation is a standard cleanroom technique, and rarely intricacies such as film granularity need to be considered. Later in fig. 5.43 it will be shown to be an issue.

Metal evaporation is a form of physical vapor deposition (PVD), where enough energy is provided to the source material to permit its particles to be emitted. This can be done by resistively heating the source material, or by electron beam bombardment heating it, or by sputtering, where ions (e.g. Ar) are smashed into the surface to break free source atoms. The mean free path is the distance traveled between two similar events, such as elastic collisions of molecules in a gas. In PVD the goal is to guarantee that the freed particles of the source material are hitting the substrate and are not interacting with anything in between. The mean free path must be bigger than the distance source to target. Using the hard sphere gas model, the mean free path is given by $l_{mfp} = k_B/\sqrt{2}\pi d^2 \cdot T/p$ and using values obtained for the Al evaporator d_{Al}=0.26nm, T=300K, p=10^{-5}mbar=10^{-3}Pa, one finds l_{mfp}=13.8m, sufficient by a large margin for the 40cm "throw distance" in the evaporator used. A side effect of long throw distances is the collimation of the vapor, avoiding that an SET on the left of the substrate looks very different than the one on the right.

When the travelling atoms in vapor phase hit the substrate, they undergo a phase transition to solid. This is not a uniform process, and depends on nucleation, which is *the surface and interfacial energetics of the substrate and the condensing atoms*[184]. Three growth regimes are distinguished, namely *monolayer formation*, where the atoms are more strongly bound to the substrate than to each other, *island growth*, where the interaction between atoms is greater than with the substrate forming three dimensional nuclei, and the mix of it *layer plus island growth*. The substrate temperature will remain low, low enough to preclude it from allowing for bulk diffusion of atoms. Therefore the *film microstructure is composed of tapered columns with domed tops and the columns are separated by voids*[184]. These insights were not verified, but they set the strategy for evaporation, which was to have high rates of deposition to not switch from one growth regime to another in the process.

Another indication comes from the observations[185] that a more uniform film quality, judged by the roughness of its topography, is yielded by using highest possible evaporation rates, lowest possible chamber pressure,

and baking out the chamber prior to evaporation to eliminate background oxygen and water.

5.5.5 Al native oxide growth kinetics

Metal oxide barriers are very popular because they are easy to form by just exposing the metals to oxygen. But the phenomenon must first be explained before it can be controlled.

Al exposed to air forms within a few seconds a 2-3nm thick native oxide film at room temperatures. The oxidation is initially extremely rapid, but after short time drops to very low or negligible values, as a stable film is formed, which impedes further growth[186, 187, 188].

The first oxygen atoms arriving at the unoxidized Al surface react there and form immediately an oxide film. The solid reaction product Al_2O_3 separates the two reactants Al(solid) and O_2(gas). The Al–O_2 interfaces turns into two interfaces Al–Al_2O_3 and Al_2O_3–O_2. Any further reaction requires that one of the two reactant crosses through the formed oxide. Free metal electrons pass from the metal through the oxide film to adsorbed oxygen on the oxide film by tunnel effect or thermionic emission, while the latter is neglectable at room temperature, as well as concentration driven diffusion. Some of the adsorbed oxygen atoms become anions O^- or O^{2-}. An electric field is established across the oxide layer, between the Al surface and the O anions. When the oxide layer is thin, that field is very strong, and every Al^{3+} that escapes from the metal is pulled by the field across the oxide layer to the anions, to form more Al_2O_3, and the film thickness increases. The limiting condition is where the film is too thick to allow for electrons tunneling through it. The behavior of holes and O^- O^{2-} anions is reverse but analogous.

The core message of these paragraphs is that the limiting factor for oxide growth is the electrons no longer being able to tunnel through the oxide barrier. To form a tunnel junction adequate for an SET, the oxidation must stop before the reaction is self limiting, otherwise no electron tunneling and no charging effects will ever happen. To stop the oxidation, the reactant oxygen must be removed. The oxide layer must be protected from further oxidation, which would immediately occur should the Al_2O_3 covered Al ever see oxygen again. Conveniently enough, adding the second Al electrode of an SET, provides both defining of the junction area and protecting it against further oxidation. All other areas of the Al electrodes can oxidize up to their final native thickness without interfering with the charging effects of the defined junction.

5.5.6 Al oxide tunnel junction formation

An Al film is evaporated, and *in situ* oxidized, forming out of the top layers of Al film a layer of Al_2O_3, then the second metal is evaporated, and the couple of atoms thick Al_2O_3 layer between the initial Al and the second metal forms a high quality tunnel junction. If no Al is planned as conductor, a very thin Al layer can be evaporated and completely oxidized, furnishing the tunnel barrier.

As example for the former are the transport experiments in ferromagnetic – nonmagnetic – ferromagnetic SETs based on Co-Al-Co[189], or based on NiFe-Al-NiFe[190]. The magnetoresistance studies are done with the Al island in the superconducting state.

As example for the latter are the junctions in ferromagnet-insulator-ferromagnet (FMIFM) trilayers that have been realized by first evaporating a 1nm thin Al film, then performing in a lightly pressurized loadlock a complete *in situ* oxidation[191]. The authors have estimated the final AlO_x thickness, based on bulk values for Al and Al_2O_3, to be 30% larger due to the incorporation of oxygen in the Al lattice. From the ratio $\frac{molecular\ weight\ Al/density\ Al}{\frac{1}{2}(molecular\ weight\ Al_2O_3/density\ Al_2O_3)} = \frac{26.98/2.70}{\frac{1}{2}(101.93/3.97)} = 0.78$ where $\rho_{Al_2O_3} = 2 \times 26.98 + 3 \times 15.99$, and $\frac{1}{2}$ adjust to a 1:1 Al atoms ratio, it can be estimated that in the growth of 1nm of Al_2O_3, 0.78nm of Al is consumed, and in the growth of 1.28nm of Al_2O_3, 1nm of Al is consumed.

Aluminum is often used for metallic SET transistor, because a tunnel barrier can easily be created by a controlled oxidation, giving a good junction. Because Al is superconductive, at low temperatures a magnetic field must be used to extinct the superconductivity. Or a normal (non-superconductive) metal can be used.

Chromium differs from Aluminum in that it does not oxidize as willingly. The time necessary is much longer, such as 15h at $2{\times}10^4$ Pa at room temperature[192]. This could be reduced to 30s or minutes by exposing the Chromium to oxygen plasma at 0.5 torr (66.5 Pa)[193]. Exposing Aluminum at room temperature to room pressure would result in a native oxide film that is too thick to exhibit any charging effects.

There is no method or consensus on how to fabricate tunnel junctions of a certain resistance in the literature other than varying oxidation time and pressure until the required range is found. Furthermore this is challenging to repeat with the local setup, because minute changes in evaporation rates and inclination angles can cause (on that scale) big geometric changes of the junction section, which directly changes the resistance. Resistance tests on single junctions (each measurement is the mean of 4 junctions), identically patterned and developed, 1^{st} evapora-

oxidation time[min]	0	1	2	3	5
resistance[kΩ]	0.92	57.0	243	171	149

Table 5.1: *Junction resistance vs oxidation time at 1mbar*

tion, oxidized varying time, but with comparable pressure and process, 2^{nd} evaporation, yielded results with some trend, but were difficult at best to interpret. Table 5.1 shows that oxidation increases the tunnel resistance. But the conditions in the evaporator varied more from one evaporation to the other than from one oxidation time length to the other. However, oxidation had an effect as the 0 minute oxidation sample confirms. To be sure that the resistance was over the minimally required resistance quantum $R_T = \frac{h}{e^2} \approx 25.8k\Omega$, oxidation had to be at least a minute, and was set to two minutes to have a margin, given the imprecise nature of the measurements.

An attempt of explanation is to be found in the nature of the evaporator. Oxidation was done in a "dynamic vacuum" as opposed a "static vacuum", i.e. the chamber could not be isolated from pumps and flooded with oxygen to a certain pressure, then be left to itself for two minutes. The turbomolecular pump could be put in a standby mode with reduced pumping power. Then oxygen could be introduced through a needle valve, and the control of the influx of oxygen, compensated by volume removed by the pump would create the pressure inside of the chamber.

How much oxygen is there available on the surface of the Al? In surface chemistry, when a surface is exposed to a gas, the dose of the gas deposited on the surface is expressed in Langmuir, i.e. a monolayer deposition of the adsorbate, 1 Langmuir, is deposited at 10^{-6} Torr in a second. $dose = pressure \times time$. This is if every gas molecule sticks to the surface. At 1.33mbar(1Torr) it happens in a μs, therefore the oxidation reaction is not oxygen limited under these conditions. This thesis is not about oxide growth kinetics, but its understanding is key, for it allows for educated guesses of appropriate processing conditions. Therefore the oxidation time 1-2 minute range at 1mbar was carried forward, because those parameters produce a usable resistivity value and a junction which is not affected by the graininess of the producible Al films.

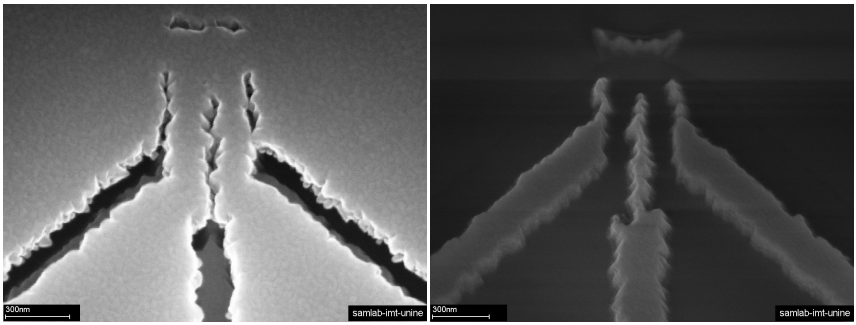

Figure 5.43: *Al film quality before and after liftoff. SEM picture (tilt=45°) of Al evaporation 100nm thick on resist stack before (left) and after liftoff(right). The granularity of the Al film precludes the use of this evaporator, at least with its current process parameters. Scalebar=300nm.*

5.5.7 Existing evaporator

The first evaporation result with the cleanroom's standard Al evaporator had a major problem with the grain size, to the point where it was not possible to conceivably use it, as clearly is demonstrated by fig. 5.43. Furthermore, the evaporator could not change the sample inclination without breaking the vacuum, nor could the chamber be flushed with oxygen to grow tunnel junctions.

5.5.8 Dedicated evaporator

A thin film deposition system from tectra GmbH. was received on loan from the Nanophysics group at ETHZ. It is a modular general purpose system, with bell jar, fitted with thermal evaporator, an electron beam evaporator, a quartz microbalance. And most importantly: the sample holder can be inclined any angle (all 360°). A so called feed through collar with free ports allowed for the addition of following three items, connected by means of standard CF flange components.

Highly pure oxygen gas was fed through a needle valve. An N_2 gas line was added to flush the chamber when at ambient pressure, to reduce water film adsorption on internal surfaces. A thermocouple (Chromel-Alumel) was installed at close vicinity ($< 1cm$) of the sample holder and the readout was done through a general purpose multimeter. This was done to be able to observe the sample temperature evolution during evaporation.

The Al foil which was fitted initially to protect the evaporator walls

against Al deposition from the resistive "all directions" heater, was replaced by stainless steel sheets (0.5mm thick), with half centimeter clearance from their bottom to the chamber floor, to avoid cut off volumes. The folded Al foil had created trapped and stagnant volumes, which increased the pumpdown time by at least a factor of two, a fact noticed and appreciated only once the change was done.

A quartz crystal microbalance based thickness monitor[194] was programmed for Al and the evaporation geometrical offset tooling factor, and calibrated successfully. The thickness indications were of a resolution of 0.1nm. The frequency change caused by a mass addition on the surface of a shearmode thickness oscillator is used to determine the thickness change, with the formula $\delta f/f = -\delta m/\rho_Q At$, where f is the quartz oscillation frequency, ρ_Q the density of quartz, and A the shear surface area and t the thickness of the quartz.

5.5.9 Evaporation sources

The evaporation source must provide the evaporant with sufficient energy to be emitted from the solid evaporant. This is usually done by heating the evaporant. The evaporator is equipped with a thermal evaporator, and an electron beam evaporator. The few evaporations done with the electron beam based evaporator proved unstable at best. Its small crucible led to situation where not enough thermal inertia would lead to thermal runaway conditions, where within a short time laps a very slow rate evaporation could exponentially grow out of control to a very high rate, the whole crucible would overheat, simultaneously the chamber pressure would raise to the point where the pressure interlock would turn of the power supply of the evaporator, all this before an operator had the time to reduce the filament current. Therefore the thermal evaporation was preferred. The best way to hold an evaporant during evaporation is to contain it within itself, e.g. an electron beam heating a small zone in a larger pill/coin of evaporant. Thermal evaporators directly touch the evaporant, such as a twisted W wire, which has the evaporant sitting on it, and when reaching latter's fusion temperature, it will through wetting adhere the W twisted wire. Evaporation is straightforward, unless you do something special, such as more than one evaporation in the same run. In the case of Al rods melted on a W wire, the two of them form an alloy, which firstly makes that the evaporant is no longer pure Al, and secondly renders the W wire very brittle, so brittle that the thermal cycle for the second evaporation step would sometimes induce sufficiently stress in the W wire to rupture it. The direct contact between source and evaporant was avoided by using

a BN crucible, heated with a W wire basket.

5.5.10 Illustration of the two evaporation steps

The result of a double angle evaporation of Niemeyer-Dolan type evaporation is shown in fig. 5.44.

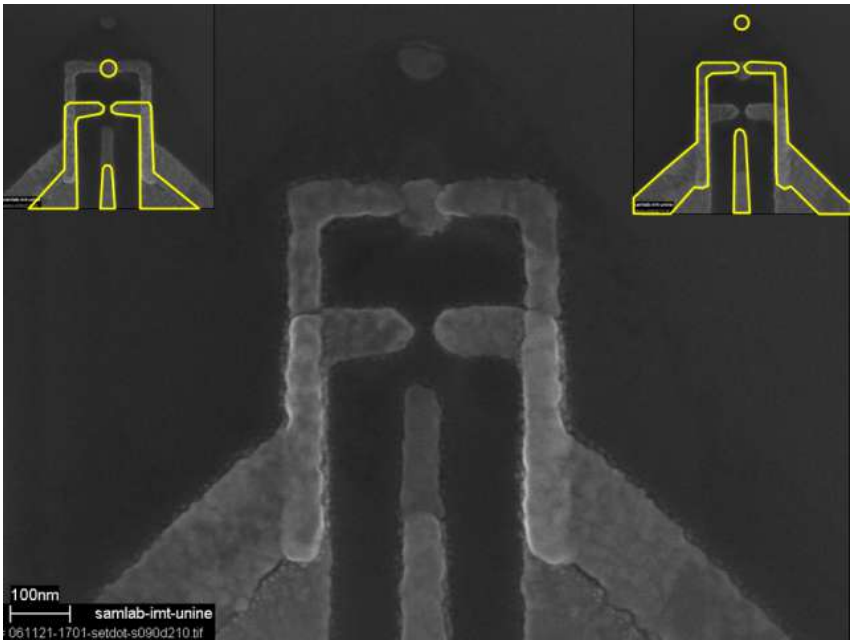

Figure 5.44: *Double angle evaporation with schematic overlaid insets. The insets (top left) and (top right) each have outlined one of the two evaporation steps visible in the main picture (scalebar=100nm).*

5.5.11 Mask clogging

When evaporating a material through a mask, mask clogging is generally speaking not an issue because the evaporated thickness is not comparable in size to the mask opening, except for techniques as Spindt tips[146, 147], where clogging is the core requirement of the process.

In this process, however, the evaporation of a 30nm thick Al film will have some evaporant stick at the mask edges and the effect will be seen because the mask opening is only 80-100nm wide, this is the mask clogging

effect. The clogging is amplified by the two angle evaporation, because the first evaporation under angle clogs not just the top edge of the mask opening, but its whole exposed (at glancing angle) side. In fig. 5.45 the measured diameter and width are measured for first and second evaporation, and the changes are from 100nm to 70nm, and 86nm to 44nm, respectively. This effect is very hard to model, and depends a lot on the evaporation steps, which have their small built-in variations, which is one of the reasons why part of the fabrication process is based on trial and error as in fig. 5.39. Evaporation is not a trivial task, and time was spent

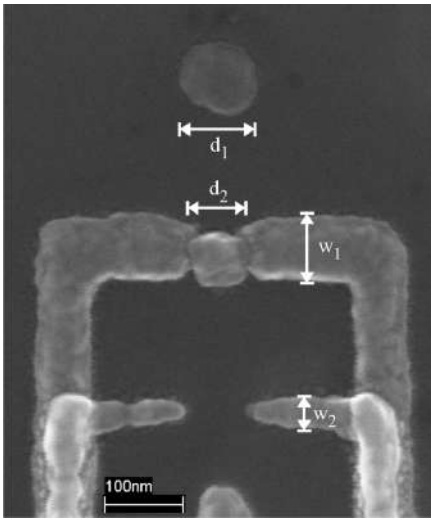

Figure 5.45: *SEM picture of line width narrowing due to mask clogging. Evaporant deposits on mask edge and reduces opening. Diameter of island d_i and width of source/drain w_i are smaller for 2nd (i=2) than for 1st (i=1) evaporation.*

trying to understand and render double evaporation possible.

5.5.12 Liftoff

Liftoff relies on the solvent removing the resist underneath, and the evaporant itself. For very thin PMMA and large surface, it can take half an hour and more, and is best done assisted by ultrasonic agitation (1MHz), to avoid that released metal redeposits on the substrate.

Liftoff is also the step which revealed adhesion problems of previous

steps, when entire patterned areas also peel off. In the current process, a post development bake, below vitreous transition temperature, i.e. at 90°C for 90s had to be introduced, in order to dry the resist from the developing step, followed by a 10s oxygen plasma treatment, to clean the freshly exposed substrate, without destroying the fine surrounding mask structure. The combination of those two steps made that during evaporation, the resist did not outgas anymore to the point to no longer permit the evaporated layer to stick.

5.6 Scanning probes

The scanning probe itself is one of the four important items that were isolated in subsection 2.1 on p.7. The initial research direction was to microfabricate the sharpest tip apexes possible, to obtain high lateral resolution, then to batch microfabricate them[148, 195, 196].

Current AFM probes are fabricated following a *de facto* industry standard size as shown in fig. 5.46: from a handling part, also called chip or probe body, of about 3400μm×1600μm×525μm [8], a cantilever extends and carries the tip. The cantilever's dimensions determine its spring con-

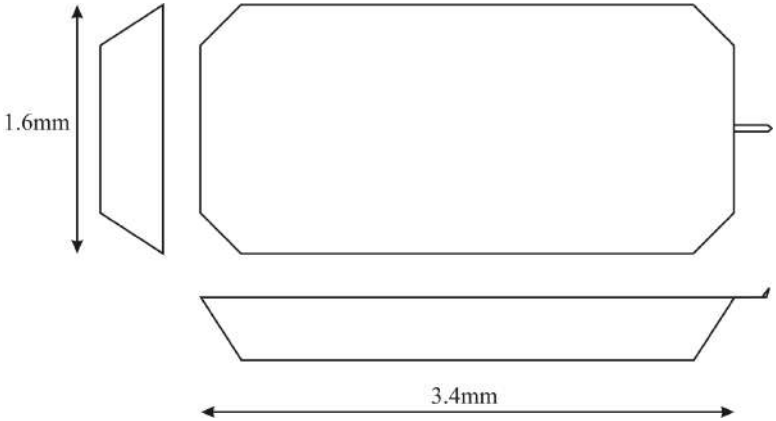

Figure 5.46: *AFM chip dimensions. The trapezoidal cross-sections are due to wet anisotropic etching, and are at an angle of 54.78° corresponding to the inclination of the <111> plane with regards to <100> plane. Dimensions 3.5mm×1.6mm×390μm or 525μm.*

[8]The thickness depends on the substrate: 4 inch wafers, single or double side polished, are 525 and 390μm thick, respectively.

stant, $k = Et^3w/4L^3$ where E is Young's modulus, t is the thickness, w is the width, L is the length of cantilever, and resonance frequency $f_0 = 0.162\sqrt{E/\rho} \cdot t/L^2$ and thereby its application to hard or soft samples, to contact or non-contact mode, etc. . Tips are commonly bought from AFM probe tip manufacturers, such as from one of today's market leaders, nanoworld.ch.

5.7 Tip functionalization

It has not been long until these tips were functionalized, i.e. rendered more apt for specific applications. Microcast SiN tips molded in Si tip molds formed by KOH etch are rendered sharper by low temperature thermal oxidation[197] of the Si forming the mold. The oxide grows ununiformly towards the mold's "pit apex".

Coating a tip with diamond (vapor phase deposition) makes a tip harder and more wear resistant[198, 199].

Coating a tip with magnetic material allows for magnetic force imaging, requiring a two pass approach: First the surface is scanned in contact/tapping mode to obtain the topography. Then the tip is lifted off the surface and scanned in non-contact mode, using topographical information collected beforehand, in constant height over the surface. The magnetic tip now translates any magnetic force gradient into a resonance frequency shift.

Using highly doped semiconductors or coating it with metal renders a tip conductive, opening the door for applying a voltage between an tip and the sample, apt for scanning gate applications or STM type spectroscopy, and performing electrostatic force microscopy, revealing material properties such as capacitance, surface potential, charge or dopant distribution, dielectric properties.

But it can be made even more complex, versatile and interesting, by integrating complete devices on tips. Semiconductor manufacturing steps are two dimensional, planar processes. Their technological transfer to three dimensional environment of a scanning probe tip is not straightforward. Just the application of resist alone to a tip, all while guaranteeing constant thickness, at least for the to be patterned area, can be a major obstacle to overcome. Solutions to conformally coat three dimensional structures are found in "direct spray coating"[200], where resist is dispensed through an atomizing nozzle on a rotating wafer, or in "float coating"[201], where the structure is immersed in water, the resist is dripped on the water to form a film after the solvent has evaporated, and it deposits upon draining of

the water on the structure, or "droplet on demand coating"[202], where resist is deposited not unlike an inkjet printer.

If the problems inherent to techniques for transferring patterns to three dimensional structures are solved, it allows for all devices, that were possible to be realized planarly beforehand, to be realized on scanning probes, either on tips, flattened tips or pyramidal tips, or just on the probe edge.

Examples are a scanned thermocouple[203], detecting magnetic fields with a scanning Hall probe[204] or a scanning superconducting quantum interference device (SQUID)[205]. detecting electric fields with a scanning QPC[206].

5.8 Tuning fork based scanning probe microscope

5.8.1 Tuning forks as frequency standard

In non-contact or dynamic mode, when the interaction force between tip and sample changes e.g. due to a topography change during scanning, it causes a shift of the resonance frequency of the cantilever which is used to determine the z-distance (or any seeked image information). The frequency shift is due to the gradient of the tip-sample interaction force, whereas contact mode force microscopy is directly sensitive to the force. This is only true for small oscillation amplitudes[207], because for bigger amplitudes, the range swept in the frequency shift-distance curve, analogous to the force-distance curve of the static mode, is too large and cannot be linearized. Therefore, a robust solution must have small oscillation amplitudes.

The easiest mode of operation is to excite the oscillator and when interacting with the sample topology, observe the shift in resonance frequency, amplitude change and phase change. Both amplitude and phase signal are a mix of the tip-sample distance and the resonator quality factor, and they cannot be separately observed[11]. When the phase is kept constant at 90° using variable excitation frequency and the sensor's amplitude is controlled, then the resonance frequency can be used as a measure of the tip sample distance.

For non-contact modes the oscillators themselves are the limiting factor. The amount of energy dissipated to maintain the oscillation should be as small as possible, or in different terms, the quality factor should be high. This yields higher sensitivity, with the drawback of decreased bandwidth, i.e. slower scanning speed.

Quartz (crystalline SiO_2) is piezoelectric, which allows it to be actuated just by applying an electrical field across it, and at the same time allowing for detection by observing the current signal. It has almost no internal mechanical losses, meaning little dissipation. This is why it has been chosen long ago in the watch industry, where energy consumption directly limits the battery life. While newer watch crystals run in length/width extension or shear mode, or even at higher frequencies for increased stability, early and initial developments and today's standard and mass market products use the tuning fork based oscillating cantilever or prong design at 32768 Hz, a frequency, which is easily divided by a chain of 15 D-flip-flops (delay flip flops), to 1 Hz, ideal to pace a step motor driving the seconds hand of a watch.

A two prong, U-shaped quartz tuning fork, electrically connected in a way that when oscillating, the prong ends move in counter phase, i.e. one prong mirrors the other with regards to an imaginary mirror plane through center of the U, i.e. both prong ends move away from the imaginary centerline, and move towards it simultaneously. This has the additional advantage that the tuning fork barycentre (center of mass) stays at rest, and no resultant force or momentum is perceived by the overall structure.

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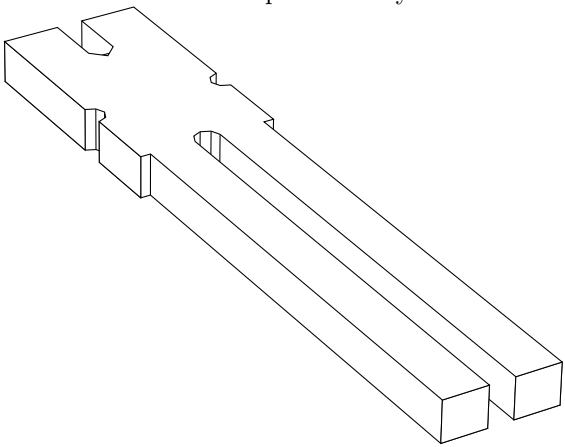

Figure 5.47: *Wireframe model of a tuning fork*

The resonance frequency of such a tuning fork can obtained by measuring the prongs and calculating the bending of a cantilever with quadratic

cross-section, which is

$$f_{0_n} = \frac{(k_n l)^2}{2\pi\sqrt{12}} \sqrt{\frac{E}{\rho}} \frac{t}{l^2}$$

where f is for frequency [Hz], with Young's modulus $E = 78.308$ GPa [9], density of quartz $\rho = 2650$ kg/m^3, prong length $l = 2370$ μm, prong thickness $t = 220$ μm. The term $(k_n l)$ is the n-th solution to what remains after solving the equation of movement for flexural vibration of a cantilever clamped on one side and free on the other, i.e.

$$\cos k_n l \cosh k_n l = -1,$$

and the first three modes are

$$(k_0 l) = 1.875, \quad (k_1 l) = 4.694, \quad (k_2 l) = 7.855.$$

The value $(k_0 l)^2$ is sometimes also called fundamental frequency f_0=3.516 . Introducing this solution into the equation gives the zero-th solution $f_{0_0} = 34386$ Hz, a value which will decrease due to the additional mass deposited on the prongs when metalized to establish electric connection, and then further will decrease when laser trimming removes material in the center of the U structure, making the prongs longer, or increase when laser trimming evaporates and removes electrode material near the prong ends, all to arrive at the final frequency of 32768 Hz, the 2^{15} frequency standard.

5.8.2 Tuning forks as force sensor

The first reported use of a quartz tuning fork as force sensor was for scanning near-field acoustic microscopy[208], where the bare prong corner was used to scan a grating, resulting in μm resolution, an achievement for a unpretentious prong corner. Any oscillator can be used, such as a rod-shaped 1 MHz length extension quartz resonator[209], but the higher stiffness gives lower sensitivity, and the higher frequency a faster response.

A huge benefit of tuning fork is that they are self-actuating and self-sensing, i.e. no additional readout mechanism is required, an advantage which was rapidly understood by many, and taken as an invitation for exploring a new field.

To remedy the poor lateral resolution of bare prongs sharper tips were used. Electrochemically sharpened W, Fe[210] and PtIr[211] wires, cantilevers broken off AFM probes[212, 213], microfabricated tips[214], tips

[9] Private communication, Silvio Dalla Piazza, Microcrystal, Grenchen, Switzerland

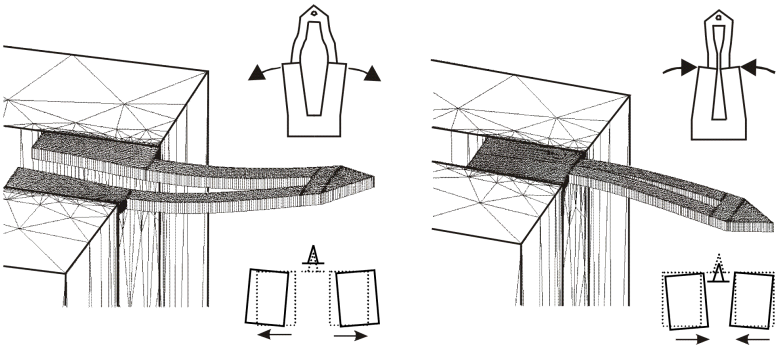

Figure 5.48: *FEM analysis of prong, cantilever and tip movement. The front and top view insets of the concept show how x-y plane movement of the prongs is transformed via the cantilevers into a z-axis movement of the tip. (Image courtesy Terunobu Akiyama).*

broken off the cantilever of an AFM probe[215], were epoxy-glued to one prong end, allowing to achieve lateral resolution orders of magnitude higher than just with a prong corner, and the ability to do more than just topography, such a scanning gate or magnetic force measurements. The major drawback is that each probe is assembled manually, one by one. The first batch fabrication process targeting to turn tuning forks as into oscillatory force sensors was defining of polymer tips[216] with an inclined lithography.

Important contributions for the understanding of the frequency-modulation non-contact AFM technique[217, 218, 219] and in using quartz tuning forks as force sensors[220, 221, 222] were made by Giessibl *et al.* The asymmetrical addition of weight on only one prong has the disadvantage that the tuning fork becomes slightly unbalanced and its quality factor diminishes. This can be overcome by blocking one of the prongs as done in the Qplus sensor[220].

Or it can be solve by inventing a new class of devices[145, 223, 224]. A tuning fork is used to drive and sense a cantilever probe. A micromachined cantilever, exhibiting a monolithic, sharp tip, is glued to the side of both prongs, adding the same amount of weight to both, maintaining the mechanical oscillatory symmetry, and creating an out of plane cantilever and tip movement. The spring constant of the probe can be chosen by designing the cantilever. In some applications, like for imaging with atomic resolution in high vacuum, it is preferable to directly use the stiff prong of the quartz tuning fork as lever, which has compliance in the order of a few kN/m. For other applications like imaging biological samples, bet-

ter results will be achieve if the spring constant of the probe is less than 0.1 N/m. By changing length and section of the cantilever, the desired spring constant can be achieved.

Batch fabrication and assembly are possible[225]. As the cantilever is

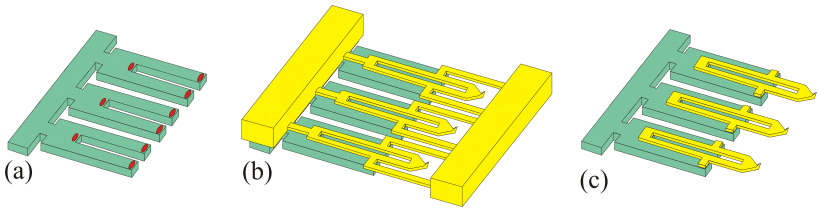

Figure 5.49: *TF to AFM-chip assembly process: (a) Epoxy resin is applied to the TF in three locations. (b) The cantilevers are aligned with the TF and assembled. (c) The TF with cantilevers are separated from the cantilever holding wafer.*

microfabricated, all techniques in the arsenal can be used to functionalize surfaces or design devices, similarly to what was exposed for the functionalization of AFM tips, cf. fig. 5.7. This lead to conductive probes[226], and electrically shielded probes.

5.8.3 Microfabricated AFM-chip-cantilever with tip

Most AFMs are built to accommodate a *de facto* industry standard size chip that has a small protruding cantilever carrying the tip (cf. fig. 5.46, while tuning fork based approaches considered the tips to be an add-on to the tuning fork. In order to become a drop in replacement for existing probes, above form factor had to be emulated. All silicon parts (cantilever, interconnecting beams and base) were monolithically microfabricated as a single chip. The TF was subsequentially assembled onto this chip[227]. The four straightforward ways to accomplish this are shown for TF on top side (non bulk micromachined) placement in fig. 5.50, and for TF on back side (bulk micromachined) placement in fig. 5.51. A vertically inserted TF causes a weight balance dissymmetry on the tuning fork prongs and therefore a worse quality factor than the horizontally inserted TF, which applies (ideally) the same weight. The driving factor for choosing one of the approaches is the mechanical clearance of the tip. The length of the cantilever defines the probe's stiffness, which is why the TF is better not placed on the same side of the cantilever where the tip is pointing out, otherwise the handling chip must be held almost perpendicularly to

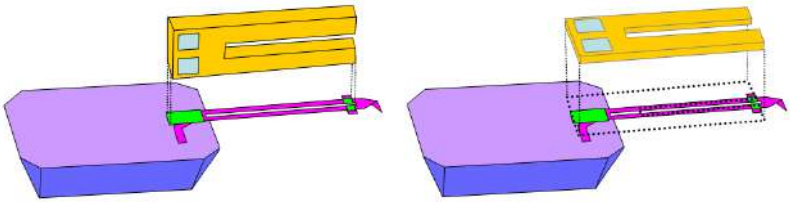

Figure 5.50: *AFM-cantilever-probe chips, TF inserted from top side, vertically(left) and horizontally(right) oriented.*

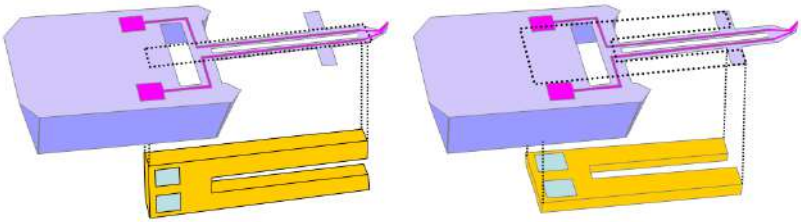

Figure 5.51: *AFM-cantilever-probe chips, TF inserted from bottom side, vertically(left) and horizontally(right) oriented.*

the surface to allow the tip to see the surface and the TF not hitting simultaneously. For top side inserted TF with tips on the opposite side, this mechanical clearance problem is reduced to a couple of degrees of tilt of the chip and therefore also the tip with regards to the surface. This is not an issue for bottom side inserted TF, reason for why it was chosen. The electrical connections to the sensor will add some tilt in this situation as well, but this is another problem.

5.9 Scanning probe single electron transistor

Blatantly generalizing, the surface of a 2DEG sample is perfectly flat, with the notable exception of the lines defining the electrical devices fabricated by locally anodically oxidized GaAs or Ti layer, which bulge out up to 10nm high[228, 144].

This topological predictability allows for simplification because the z-range excursions of the scanner will be small, and a very stiff cantilever can be chosen. This favored the use of a bottom inserted vertically oriented TF as in fig. 5.51(left).

Therefore, a AFM handling chip with protruding cantilever with SET at the tip will be designed.

5.9.1 Microfabricated AFM-chip-cantilever with single electron transistor

The body of the chip is done by wet anisotropic etching, one of the core Si microfabrication techniques. The anisotropy expresses itself in different etch rates for what appears to be different crystalline planes. The term *appears* is chosen because — like many other fundamental manufacturing techniques — it is heavily used, at the level of the phenomenon well observed and described[229, 230, 231, 232, 233, 234, 235, 236, 237, 238], but at the physico-chemical level, it is still not well understood, although promising theoretical work[239, 240] assimilates the etching process to a "peeling off" of the crystal planes of lowest apparent etching rate, which is the {111} plane. There is a general consensus on that those planes appear during etching along edges parallel or perpendicular to the <110> direction on a {100} wafer. But what exactly happens in a convex corner, where two <110> edges meet, is unclear, especially because it heavily depends on the etchant, e.g. concentration, temperature, usage or age, dilution with alcohols or other additives, batch circulation, orientation in the bath, etc. .

As an illustrative example of a subtractive pattern transfer the KOH etching step is now given in great detail. In fig. 5.52(top), the photomask is shown. The layout shapes in blue are found as opaque zones on the photomask (this pattern transfer is done externally at a mask shop). The Si wafer has a 400nm thick thermally grown SiO_2 layer, whereupon a positive photoresist (AZ-1518 by MicroChemicals) is spin coated, then exposed with above pattern. After the development step, the exposed areas are wet etched away with BHF or dry etched with an RIE. The wafer is put into KOH etchant for a determined time, until about 10μm of Si are left (of an initially 390μm thick wafer). In fig. 5.52(bottom) one can distinguish the bare Si (bright, yellow tone), also called the "etch bottom" with a characteristic irregularity reminding of bubbles. The untouched Si (fair, red-brown tone) shows the areas which were protected by the SiO_2 mask. The dark (almost black) areas are the {111} planes which at 54.78° do not reflect light of the optical microscope illumination. Notable are the corner compensation structures on the layout. On the left side the two big rectangle-form extensions at 45°, on right of the center two pairs of fine top-bottom lines protecting each one of the two thick arms extending to the right from the body of the chip, and finally two top-bottom lines

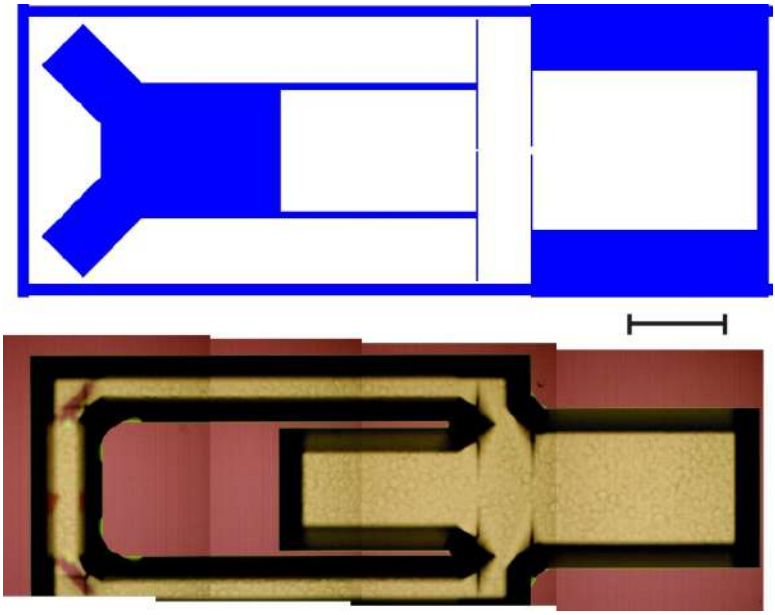

Figure 5.52: *Layout mask for the KOH etch step (top), and patchwork optical microscope picture of etch result (bottom). Scalebar=1mm.*

reducing the receding of the convex corners of the large membrane area. The lines protect because they are based on edges parallel to the <100> direction, and the etchant has to nibble away the undercuts at the end of the lines, which is much slower than perpendicular to the chip surface. A nice detail on the photo are the bright areas (green) where the corner compensation structures used to be. Those areas are the remanents of the SiO_2 etch masks. KOH etches SiO_2 at a much lower rate compared to Si (50:1), but the end effect is that they are removed with some time lag.

5.9.2 Metal lines prepatterning with lift off resist

The future cantilevers are prepatterned with the metallic connectors. This is done with a LOR[241] resist process. LOR liftoff resists are PMGI (polydimethylglutarimide) based and are used in combination with conventional positive resists for lift-off processes. Its function is analog to the copolymer in the liftoff used to define the SET. LOR develops isotropically and faster than a top layer resist, creating a reentrant sidewall profile, i.e. an

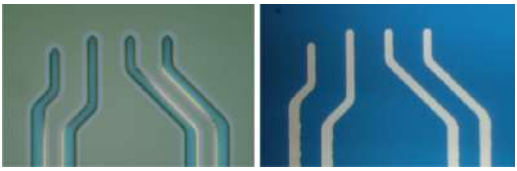

Figure 5.53: *LOR process. Left: Resist with developed (removed) lines showing in blue (dark tone) with undercut (bright tone). Right: Metal lines after liftoff, line width=2μm, line pitch=10μm.*

undercut, which ensures that a deposited film has a discontinuity, at the exposure edge, which facilitates liftoff. A Pt layer was deposited with a Ti adhesion layer, then liftoff was done.

5.9.3 Single electron transistor patterning on AFM-chip

This step was designed to be identical to patterning on the testvehicle. The only increased difficulty was the resist spinning on substrates which already were backside etched. The traditional vacuum chuck to hold the samples during spinning would have broken the nominally 10μm thick SiN/Si membranes, therefore a solution using low adherence Silicone films (gelpak) attached to the vacuum chuck for the two spinning cycles had to be worked out. The same technique was used to pattern the resist for the RIE release down the road in the process.

5.9.4 RIE release

The SET had to be patterned on the cantilevers before the cantilevers were fabricated, because otherwise it would have been impossible to obtain an uniform electron beam resist layer, given that the structure has to be at the edge of said cantilever. Therefore, a technologically and electrically challenging RIE etch step had to be done.

It was technologically challenging, because the masking layer for the RIE etching was to be defined by photolithography, and photoresist developers are usually NaOH based, which dissolves also Al, the material that the SET is made of. Therefore the structures had to be covered entirely in resist at all cost, and mask alignment was very critical. If the SET is too close to the edge of the protecting mask, then the developer dissolves it, if the SET is too far from the edge, the spatial resolution during scanning

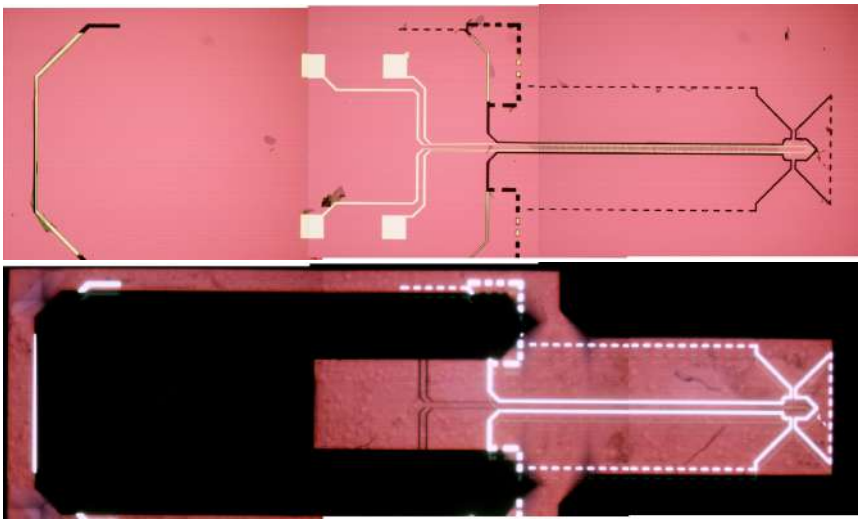

Figure 5.54: *AFM chip after RIE for release perforations. Both upper and lower optical microscope pictures are top views of the chip (patchworked together). The illumination is from the topside (top=incident light) and backside (bottom=transmitted light). The perforated lines allow the attached flaps to be broken out. Consider the pads sized 200μm×200μm as scalebars.*

will be bad.

It was electrically challenging, because the SET's tunnel barriers may be destroyed by electrostatic discharges in the process of fabrication, an effect known in CMOS process technology as the antenna effect, and which is discussed in more detail in subsection 5.9.6 on p.148. Fig. 5.54 shows the four pads with metal lines leading from the body of the AFM-chip through the fine cantilever to the tip area, with the two sideways leading designated rupture points. The transmitted (shine through) illumination shows where the membrane is supported by thick silicon (dark) and where it freestanding (bright). The through-illuminated lines (white) show where the RIE has etched through the membrane.

5.9.5 Tuning fork insertion

The TF has now to be glued into place. The recess in the AFM-chip body is not very accessible, and electrical connections can be established only with higher order dexterity. Therefore a shark fin, cf. fig. 5.55, was

glued with isolating epoxy to the proximal end of the TF, and with electrically conductive epoxy lines were drawn from the TF pads on to the fin, allowing for electrical connection at a more accessible place, once the TF would be glued into place. In fig. 5.56, the result of the anisotropical KOH etch from this side, and the through holes etched by RIE from the opposite side can be admired. The central body of standard AFM-chip dimensions is supported only by the 10μm thick surrounding Si membranes, and respectful handling of the samples is recommended, because any inadvertedly supplied shock may prematurely release, as seen in fig. 5.59, an AFM-chip-cantilever-SET without any easy or practicable way to add-on the required TF. Before the sharkfinned TF can be assembled to the holding chip, the three 0.5μm wide flaps, already free on three sides, but still holding on to the membrane through their forth perforated one, have to be broken out, as hinted on fig. 5.58. Their role is to protect the Si cantilever extending to the distal end of the sensor, where the SET is located, during processing. In an alternate processing flow, its role was to create a flat surface around the SET, to allow for resist spinning with a chance of getting an uniform coating, a result possible to obtain, given that the gap is very narrow.

The tip area where the SET is situated, as shown in fig. 5.57, is still fully supported by the membrane, and mechanically connected through two bridges. and are labeled "bridge" in fig. 5.57. where the distal flap can be guessed by its perforation towards the top of picture, and the two flaps on the right and left of the extending cantilever which itself can be identified by the patterned four metal connection lines, coming from bottom of the picture. The crosses are alignment marks, the numbers the timestamp of the electron beam patterning.

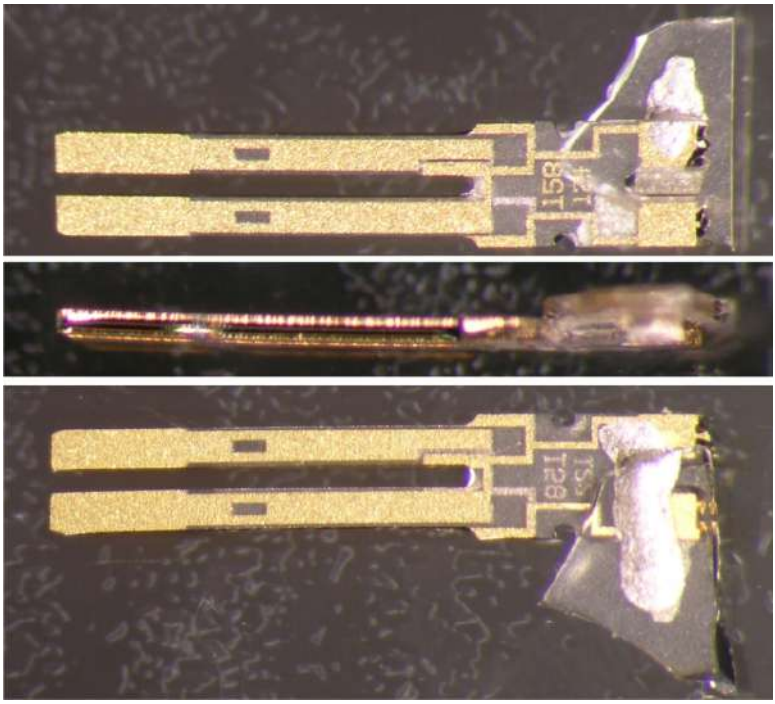

Figure 5.55: *Tuning fork with connector sharkfins. The fin is glued with insulating epoxy on to the TF, covering on one side the upper TF pad. Then two lines are drawn with conductive epoxy. The first line starts at the lower TF contact pad on the finned side of the TF, and it leads on to the fin, then to the upper third of the fin. The second line starts at the upper TF contact pad on the not finned side of the TF, and it leads across the top part of the TF onto the fin, then continues to the upper third of the fin. The second line is on the other side of the fin than the first line. That way, both TF contact pads are equally well accessible from the fin, despite the TF being lodged in the AFM-chip notch, where the TF pads are difficult to access. The TF is 3.63mm long, 0.69mm wide, and 0.13mm thick.*

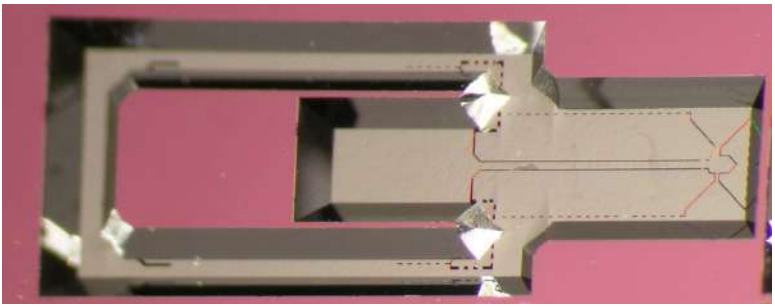

Figure 5.56: *Backside after RIE release. The photograph shows nicely the anisotropically etched crystal planes. The darker dashed lines are the RIE etched holes in the membrane, and are the release perforations. The darker continuous lines outline the cantilever extending from the probe body.*

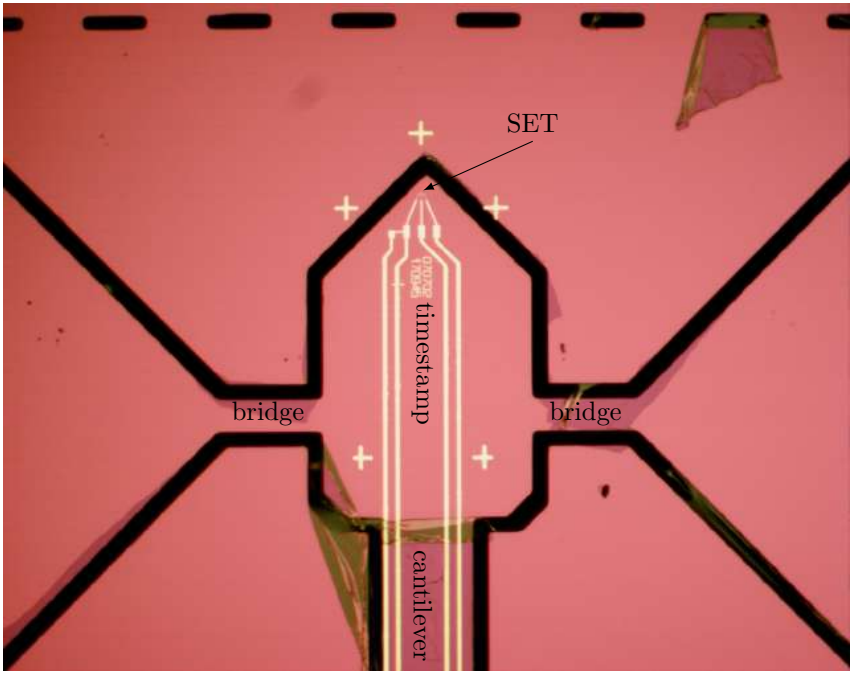

Figure 5.57: *Tip area of the SSET and the distal end of the cantilever coming from the bottom into the picture (75µm wide). The bridges attaching the tip area to the membrane are 30µm wide. The exposure timestamp can be distinguished in the center between the connectors.*

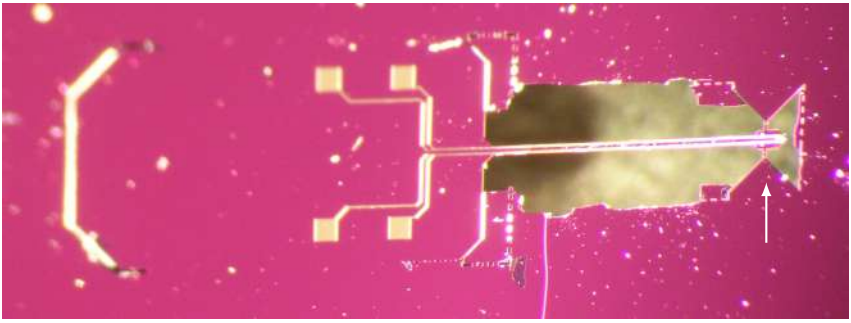

Figure 5.58: *Broken out flaps preparing for the gluing of TF. The tip area with an SET discussed in fig. 5.57 can be identified above the indicative white arrow, albeit the zone appears rotated clockwise by 90°, i.e. the two bridges run top–bottom, and no longer left–right. Consider the pads sized 200μm×200μm as scalebars.*

The breaking out of the flaps is done manually, and the insertion of the TF that has glue at the distal end of its prong and at its base, will only attach it to the tip area, and not to the surround flaps. The breaking does not need to be precise as shown in fig. 5.58.

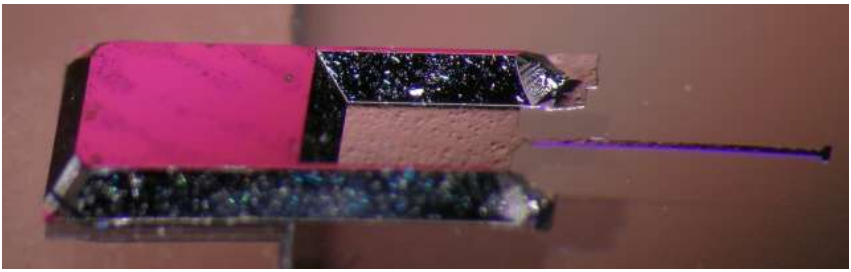

Figure 5.59: *AFM-chip-cantilever-SET released by accidentally dropping it, surprisingly the cantilever was not severed.*

A completely assembled AFM-chip-cantilever-SET with TF is shown in fig. 5.60 and 5.61.

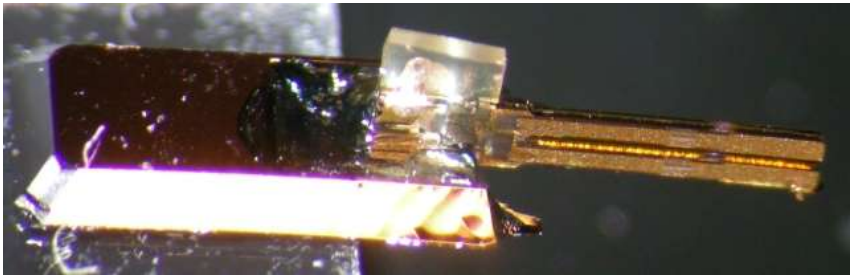

Figure 5.60: *SSET after final assembly, bottom side view*

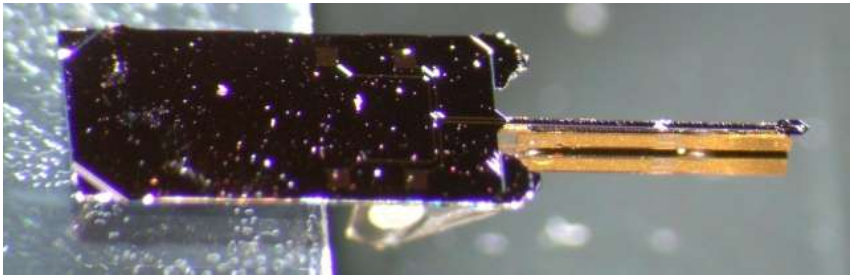

Figure 5.61: *SSET after final assembly, top side view*

5.9.6 Antenna effect analogy prevention

A major preoccupation for the last DRIE release step was the anticipated antenna effect, known in the CMOS part of the semiconductor industry as plasma induced gate oxide damage [242, 243, 244, 245, 246]. The effect can be described as follows: reactive ion etching (RIE) employs RF fields to ionize atoms and chemically very reactive radicals, and an electrically induced DC field to convey them to the substrate to be etched. Those ions, and radicals, will chemically react with the substrate, but some of them or some of their charge will partially end up in the material being structured, in the case interesting us, in the conductors such as metal or poly. The charge will distribute equally in the metal, then through vias and contacts to the polysilicon lines. Where it gets interesting is the transistor gate area, where the polysilicon line crosses the transistor diffusion. The gate oxide is very thin, optimized for transistor operating with a few volts applied to the gate, and not for the voltage induced by the charge being accumulated during a RIE step. Eventually, the charge accumulated is high enough to bias the gate oxide with a voltage which makes it break down, literally with a ionizing lightning, with the result that the transistor is shot and set to gate voltage. This charge accumulation effect can be prevented by respecting foundry rules, which are more rule of thumbs fitted to empirical data than a true understanding of the effect. The tools used to flag such rule violations are optimized for design rule checking (DRC), which historically evolved from checking intra and inter polygon dimensions, therefore antenna rules are formulated in a way that can be checked by them, i.e. keeping perimeter and/or area of metal to gate ratios within certain limits, including higher metal layers, and/or keeping via to gate area ratios within certain limits, or active countermeasures such as reverse biased diode insertion, which turns conductive at a voltage lower than the estimated gate breakdown, providing a path to evacuate the charges to the substrate.

An SET does not have a thin gate oxide, but two even thinner tunnel junctions. No experiments were carried out to determine the breakdown voltage, given that it was already challenging to obtain working devices. Some devices withstood accidental 10V gate bias without showing any degradation.

But the fabrication process was established to have the SET formation step as late as possible, to avoid damage to it during further process steps.

Three factors were especially considered:

- RIE/DRIE was permitted, if it was not possible for the ions to reach the metal layer, such as in the case where metal lines are protected

by photoresist.

- Oxygen plasma stripping, also called ashing, typically used to remove organic photoresists from wafer, was forbidden after SET formation.

- Countermeasures were tested, i.e. the drain, gate and source were shorted together with extra patterned lines, which were laid over the break-out perforation, so that they would disconnected from each other upon the breaking out of the device.

5.9.7 Considerations on electrostatic discharge

Without looking at charge paths, human body model (HBM), charged device model (CDM) or field induced charge device model (FCDM) for the handling of the devices in cleanroom, test, assembly, and operation, one is aware that any electrostatic charge buildup, and eventually electrostatic discharge (ESD) will be a fatal problem for a device electrically as sensitive as an SET. From the moment on that the devices were evaporated, they were considered hot and handling was only done with a grounded operator. Under our cleanroom conditions, this is illusionary, and limits itself to touching grounded parts of the benches or machines before interacting with the samples, grounding pliers before touching the samples, using conductive handling boxes, etc. .

It cannot be determined which was the single critical step which made that entire lots were lost or rather zapped, with metal evaporated and redistributed over the surface, or metal connectors molten and recrystallized, as in fig. 5.62, but by rigorously applying above guidelines, the failure mechanisms were no longer visible as molten or sputtered metals.

5.10 Cryostat measurements

The cryostat measurements were performed at ETHZ in a variety of equipment ranging from Dewar type liquid ^{4}He baths (down to 4.2K), over pumped ^{4}He (1.3K–4.2K) cryostats, down to ^{3}He-^{4}He dilution refrigeration type cryostats (400mK). The temperatures indicated are the ones that the samples were measured at, the Ensslin group has equipment that reaches even lower temperatures. For more details on how to attain those low temperatures regimes, on design and operations principles of cryostats, the lecture of reference books like Pobell's[247] is highly recommended.

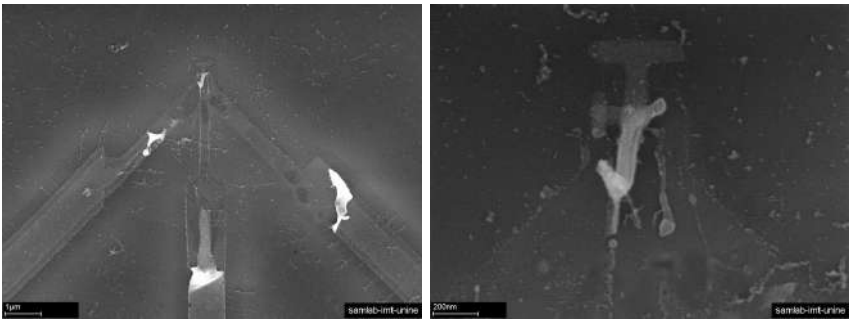

Figure 5.62: *ESD damage on samples. Left: The metal is missing on the finer tracks, and peeled back on the wider tracks. The "T" structure in the test structure survived, the rest of the material was ejected into the surroundings. Right: closeup of the central device area. The metal left is no longer composed of many grains, which indicates re-melting during the ESD event.*

5.11 Summary

This chapter documented and explained the microfabrication steps necessary to obtain a scanning probe single electron transistor according to the goals set for this thesis. It is a complex process, because it combines together a process for a single electron transistor with a process for a tuning fork based scanning probe for an atomic force microscope. The results of measuring the SET in a cryostat are presented in the next chapter.

Chapter 6

Results and discussion

The experimental chapter described the how the fabrication process of an SET and an SSET were developed. This chapter presents low temperature measurements which show that the fabricated structures function as SET structures, and discusses the gathered data, such as how junction parameters can be deduced, and what transport phenomena could be observed.

6.1 First sample, chip mounted

Among the irrefutable proofs that an SET is functioning as intended is the stability diagram, with its Coulomb diamonds. But already signatures of single electron charging effects, are nice to have, such as the Coulomb oscillations.

There are several preliminary checks that an SET goes through before it is cooled down in a cryostat to get beyond the limit where the charging energy E_c is dominant over the thermal activation energy $k_B T$.

Optical inspection is done post liftoff to make sure that the structures are freestanding, i.e. that all of the Al film that was not deposited onto the substrate, but on the resist, was removed, and that the Al film on the substrate adheres correctly. Then follows SEM inspection, which reveals if the evaporation was successful, i.e. if the inclinations of each of the two evaporation steps were chosen correctly and produced overlapping areas, defining source-island and drain-island junctions. After these inspection steps, a room temperature measurement assessed if the SET showed a current-voltage (I-V) characteristic compatible with expected resistance of two junctions connected in series, i.e. $2 \times R_H \approx 51.6\text{k}\Omega$.

With lower temperature, the electrical resistivity of Aluminum[248, 29] and metals in general decreases. Literature does not talk about the temperature dependence of the electrical resistance of Al_2O_3. It does not seem to be part of the ceramics that might be high-temperature superconductive, therefore it was assumed that it will have a behavior of an insulating material with high resistivity that decreases with increasing temperature, with an electrical resistivity at room temperature about $1\times10^{14}\Omega$cm . Al drops fom 2.3Ωcm at 293K to $9.83\times10^{-12}\Omega$cm at 4.2K. When at very low temperatures, the remaining resistivity of the two junctions will be attributable essentially to Al_2O_3. Looking at above values, this is already the case at room temperature, where Al is not yet superconductor. Given the sensitivity to charge of the device, elementary ESD protection was used at all times (conductive containers, tweezers with conductive tips, conductive mat on workplace, grounding wrist strap). But also for the resistance measurements, very low current had to be used. A semiconductor parameter analyzer[1] in source voltage and measure current mode was used, limited to a maximum current 10uA. Resisitive lines patterned as reference next to the SET candidates had 800Ω to 4kΩ resistance values, and in principle could have been used for on-sample thermometry during cooldown. The junctions measured yielded resistances of either lower than about 5kΩ, or above 100kΩ ranging up to 10MΩ, the former being malformed or shorted junctions, the latter the interesting structures. Chips with candidate structures were glued with conductive epoxy (Epotek H20E) into the chip carriers, then the candidate SETs were bonded with Al wire of 45μm diameter to the Au pads of the chip carrier. The test vehicle mounted in a chip carrier as in fig. 5.21 was first remeasured in the semiconductor parameter analyzer to make sure that no ESD event destroyed any structures during handling and bonding. Then cooldown started to verify for single charge effects.

For the cooldown, a commercial cryostat (Oxford systems) of type continuously pumped liquid ^{4}He was used, which allowed to reach the temperature range of 1.3K $\leq T \leq$4.2K. Details about performing experiments at low temperatures, from techniques to physics of cryogenics can be found e.g. in ref.[247].

[1]The HP4155A semiconductor parameter analyzer measures currents as low as 10fA. Quasi-static measurements were performed using voltage sweeps that were started at negative values, increased to maximum positive values, with the chuck and bulk Si of the wafer grounded.

6.2 First measured single charging signature

The first device which was measured and exhibited Coulomb blockade is shown in fig. 6.1.

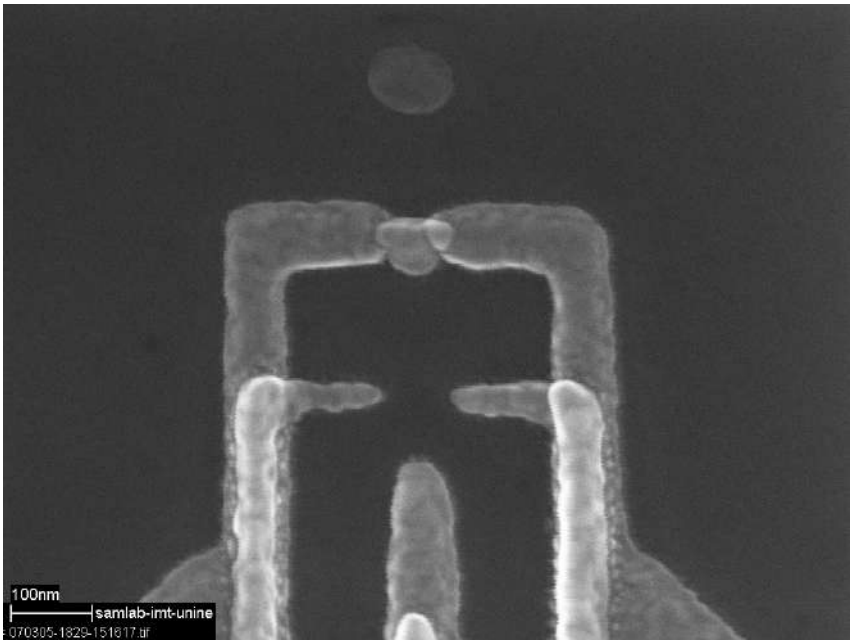

Figure 6.1: *SEM picture of first functional SET structure. The two evaporation steps were explained in fig. 5.44.*

The I-V curve in fig. 6.2, plots drain current against source drain bias, with gate grounded, for the sample at 1.7K. It shows the first recorded data of a nonlinearity around zero drain source bias, which is indicative of Coulomb blockade in a SET. When the temperature is raised to 3K, then the curve straightens out, it approaches the linear I-V dependency, characteristic for resistors, because the electrons receive sufficiently energy from thermally activation to hop over the junction, ignoring the Coulomb blockade. The Coulomb blockade is barely visible here in the curve, but it was an important result, because it was the first measurement which showed the typical signature of the physical effect that the device was built for to exhibit, and this ultimately indicated a successful device fabrication.

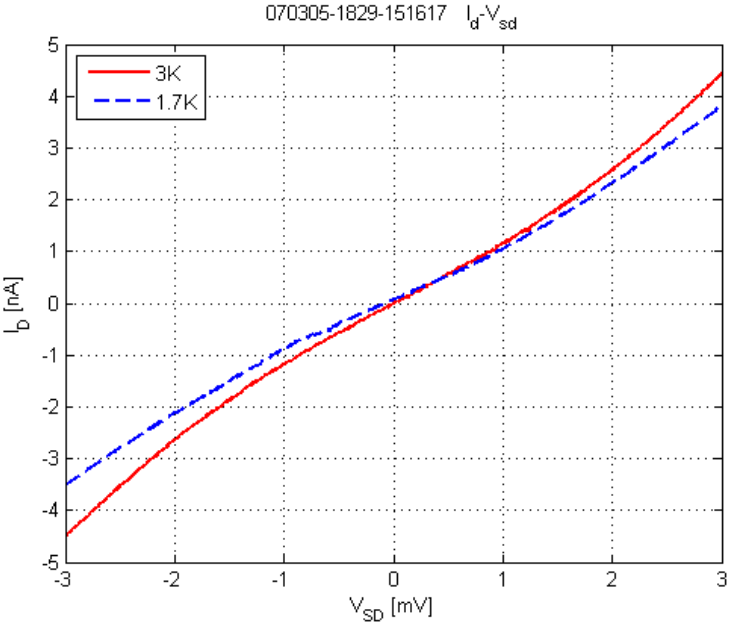

Figure 6.2: *First I_d-V_sd measurement which showed nonlinearity around the origin, indicator for Coulomb blockade. When the temperature is lowered from 3K to 1.7K, the effect becomes more pronounced, because less electrons are thermally activated, and therefore to a lesser degre "smear out" the Coulomb blockade. This was an important measurement, because it was the first confirmation that the functional device was fabricated.*

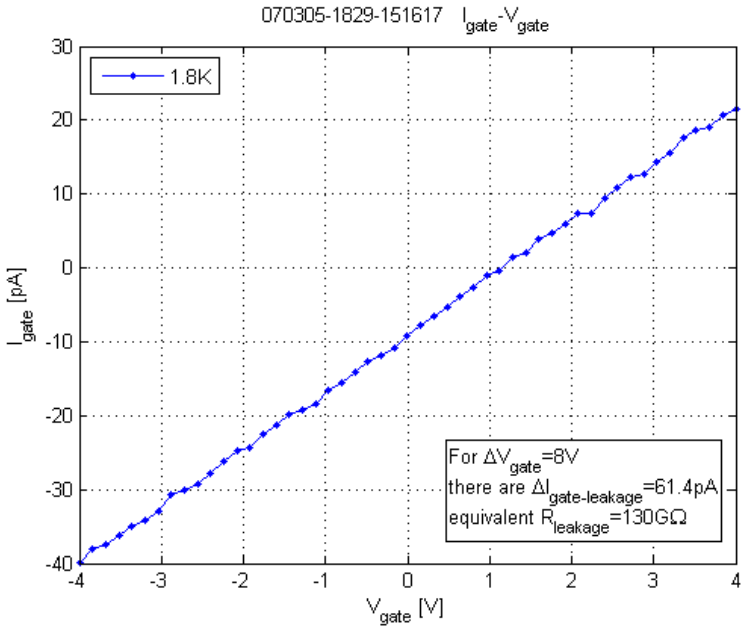

Figure 6.3: *Gate leakage I_g-V_g.*

For an SET defined by LAO in a 2DEG, a technique used by the Nanophysics group where the cryostat measurements were done, one important indicator for the quality of the device is the electrical isolation between the different electrodes. For metallic SETs defined by electron beam and liftoff, this is in theory not a problem, because the isolation is not done by suppressing an existing conducting layer, but by depositing conducting electrodes, mechanically separated from each other by an airgap. However the gate leakage current must be known to judge if the 700nm thick SiO_2 layer sufficiently isolates the SET from the Si substrate. The I-V plot in fig. 6.3 shows the gate current as function of the gate voltage, and measuring yields an isolation resistance of $R_{gate-bulk}$=130GΩ, which is three orders of magnitude above the tunneling junction resistance of this device ($R_{source-drain}$=380kΩ through the island, measured postbonding).

The Coulomb oscillations in fig. 6.4 are the first ones observable in a fabricated structure. The plot shows the differential conductance in function of the gate voltage, with a small signal applied across source and drain, i.e. V_{sd-dc}=0V and V_{sd-ac}=1mV_{rms}. The ac signal is small enough

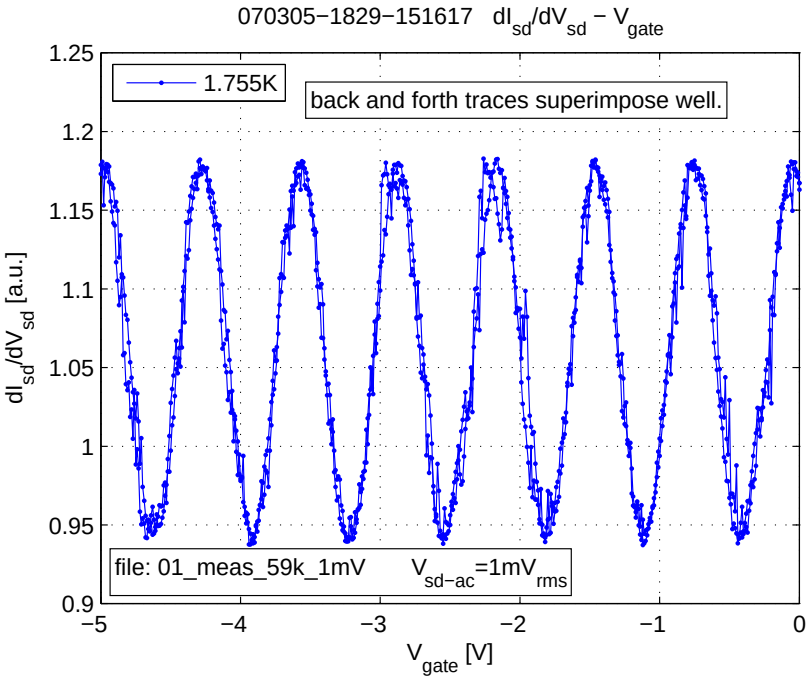

Figure 6.4: *Coulomb oscillations — $dI_{sd}/dV_{sd} - V_g$. The periodicity of the oscillations allows to extract the gate capacitance, $\Delta V_g = e/C_g$ which is C_g=225zF. The traces superimpose well, which is a sign for well formed junctions, were no charge rearrangement under current happens. T=1.755K*
.

to not move the junction out of Coulomb blockade, but big enough to allow for a lock-in amplifier measurement setup. A valley indicates the current was suppressed, and a peak that the current was unaltered. In fig. 3.10, this corresponds to a sweep along V_{gate} (x-axis), with a maximum of current for each $V_g = e/2C_g + ne/C_g$ and a minimum of current for each $V_g = ne/C_g$. The Coulomb oscillations are periodic with V_g and spaced by e/C_g. A coarse measure of the spacing of 0.7V yields C_g=225zF. The first peak (other than the one close to zero) that can be well distinguished on the plot is at gate voltage -0.75V, and if compensated with the 0.7V periodicity yields -0.05V, which set the initial island charge offset to $q_0 = -0.070e$.

The next point of interest is to fix the gate voltage at a valley (peak)

of the Coulomb oscillation, and then sweep the bias voltage V_{sd}, which for a valley (peak) will yield a current-voltage plot corresponding to the case outlined in fig. 3.12 with $V_g = e/2C_g$ ($V_g = 0$). In fig. 6.5 the two cases can be seen, although not as conductance, but as differential conductance. The valley case at $V_g = -0.30V$ has a huge drop and rise of the differential conductance, which corresponds to the strong change in current slope when the junction enters Coulomb blockade, and then exits it again. In the theoretical stability diagram of fig. 3.10, this can be understood as a sweep of V_b along the y-axis through the origin or through $V_g = e/C_g$. The peak case at $V_g = -0.65V$ has very little change of the differential conductance, which corresponds to the small change in current slope, because Coulomb blockade is avoided. In the theoretical stability diagram of fig. 3.10, this can be understood as a sweep of V_b along the y-axis through $V_g = e/2C_g$

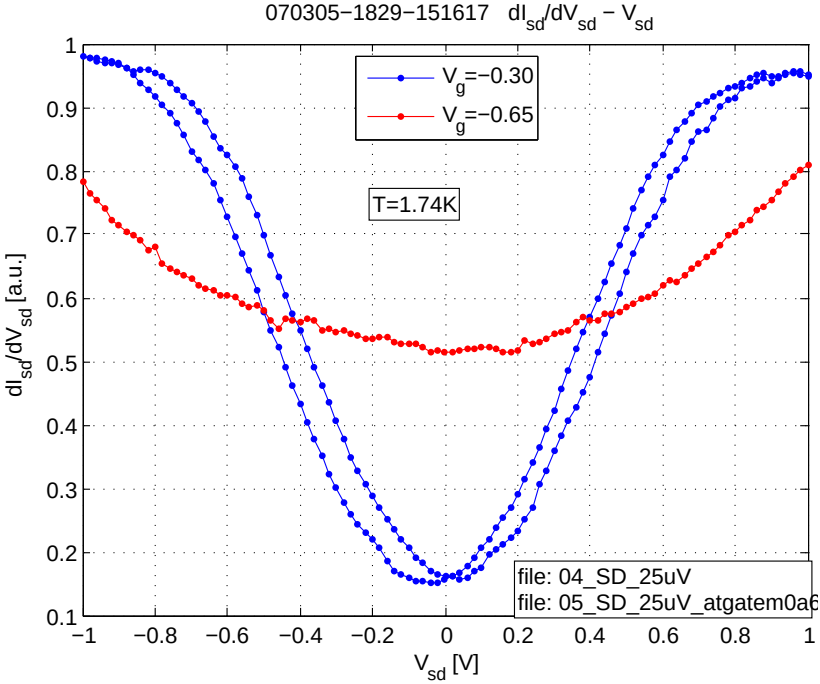

Figure 6.5: *Coulomb oscillations — $dI_{sd}/dV_{sd} - V_{sd} - V_g$. Sweep through a Coulomb blocked part ($V_g = -0.30V$) and nonblocked ($V_g = -0.65V$) part of Coulomb diamond. T=1.74K .*

Graphically the most appealing are the stability plots, plotting bias *versus* gate voltage, with the current in the z-axis. Fig. 6.6 shows Coulomb diamonds.

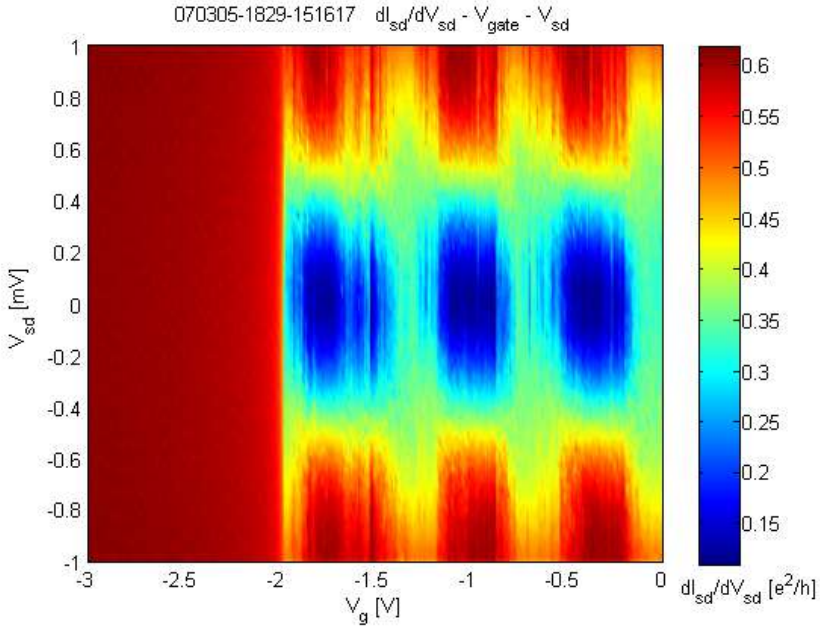

Figure 6.6: *Coulomb diamonds 2D — $dI_{sd}/dV_{sd} - V_{sd} - V_g$. On the left side, from V_g=-2V to -3V, the current is high at all time, because during the overnight measurement, all the ^4He in the cryostat was consumed, and without any further cooling, the temperature rose, above the level where the thermal activation allowed electrons transport to ignore the charging energy. It is an indirect proof, that when the sample was cooled enough, the observed transport was really bound by charging effects. The shape of the diamonds at this temperature reminds more of circles, this is because the limit of the thermal activation is not a threshold with an on/off behavior, but rather a gradual smearing out of a sharp threshold. T=1.708K .*

Fig. 6.7 presents the same data as in fig. 6.6 but in three dimensional plot, because relative current magnitudes are easier perceived as depth than as shades of color, especially on a monochrome reproduction. The flat representation is useful to extract the junction parameters from the stability diagram, as indicated in fig. 3.10. However, this is not done with this figure, because of the noisy picture, but with fig. 6.14, which was

cooled down to lower temperatures.

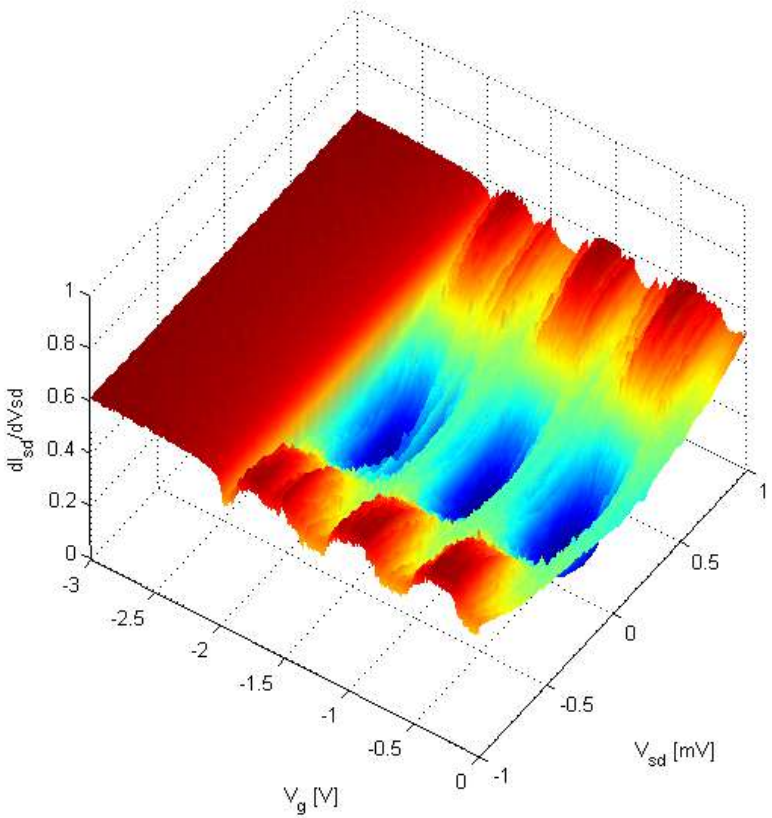

Figure 6.7: *Coulomb diamonds 3D — $dI_{sd}/dV_{sd} - V_{sd} - V_g$.*

In fig. 6.8, I_{sd} vs V_{sd} plots were taken during cooling down, to get the temperature, below which the Coulomb oscillation starts. This is not a sharp line, but nevertheless indicative.

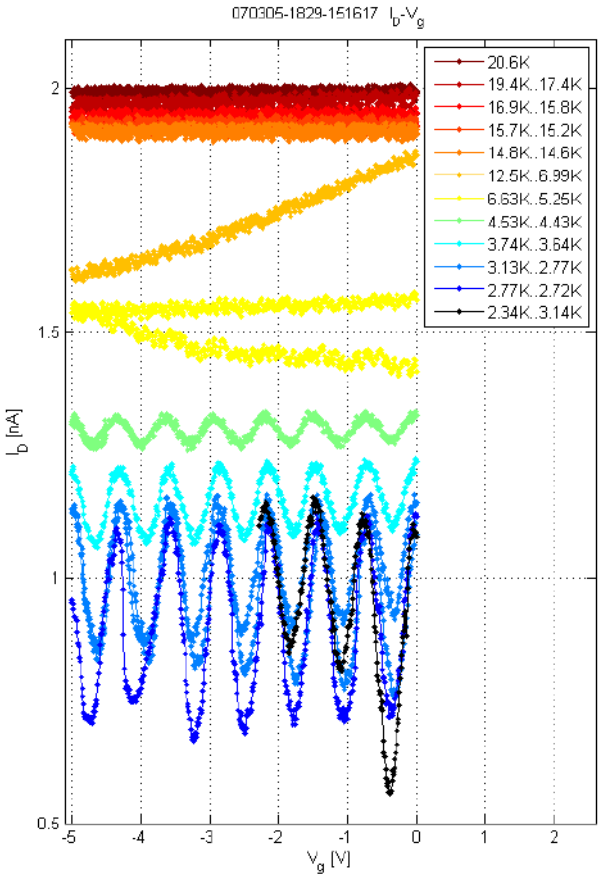

Figure 6.8: *Temperature dependence — dI_{sd}/dV_g vs V_g. Sweeps done during cooldown. The first oscillations appear in the sweep spanning 4.53K to 4.43K.*

6.3 Second sample, chip mounted

Measuring the Coulomb blockade in a first sample is an important step. But is the working SET a typical result of this fabrication process, or just a single random occurrence? Two more SET on the same test chip were measured and they both exhibited Coulomb blockade aswell, which was proof that the Niemeyer-Dolan technique was implemented in a way which repeatably produces working devices. What about the tunnel junctions? Was it just one lucky evaporation, oxidation, evaporation cycle, where through a concurrence of lucky circumstances the conditions were reunited to create a working double junction?

A different test chip was measured. Its SEM picture is shown in fig. 6.9. Its junctions were formed in an evaporation cycle distinct from the first sample.

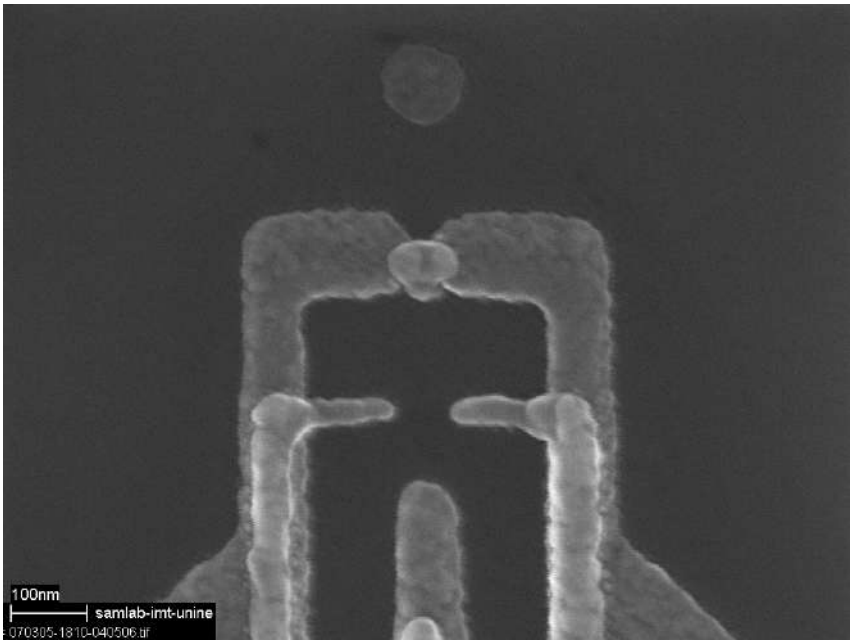

Figure 6.9: *SEM picture of second functioning SET. This structure and the one in fig. 6.1 were formed in two different evaporation-oxidation-evaporation cycles, and show that the fabrication process is repeatable.*

During the initial cooldown, bias voltage sweeps were made regularly to see how the Coulomb oscillations of the current evolve. The first trace in

fig. 6.10-top was taken at 3.27K, swept from V_g=0V to -3V shows small oscillations, back and forth sweep superimpose. The second trace in fig. 6.10-center was taken at 3.07K and from V_g=0V to -3V. The sweep starts a 0V, goes to -3V, then returns to 0V. On the return trace, around -2.75V, the current has a jump, which results for the rest of the back sweep to be in an opposing phase compared to the forth sweep. This is attributed to a charge rearrangement, i.e. the voltage sweep has caused a change of the background charge q_0 of the island. It is possible to see that it happened, but it is impossible to say what exactly happened, or where it happened, if it is an trapped ion, an injected charge, an intermediate state in the tunnel barrier, etc. . The third trace in fig. 6.10-bottom was taken at 2.52K, swept from V_g=0V to -3V. The current oscillation starts with a valley, at the same location as the center(3.07K) sweep, and not with a peak as the top(3.27K) sweep. The charge rearrangement is therefore permanent, at least until the next charge rearrangement.

The forth trace in fig. 6.11-top was taken at 2.41K, swept from V_g=0V to -4V. The current oscillation still starts with a valley, at the same location as the previous figure's center(3.07K) sweep. The fifth trace in fig. 6.11-center was taken at 2.29K, swept from V_g=0V to -4V. There are multiple charge rearrangements, on both back and forth trace.

With decreasing temperature, the modulation of the current increases. For 3.27K, the decrease was to ∼94%, for 3.07K ∼88%, for 2.52K ∼83% for 2.41K ∼77%, for 2.29K ∼73%. The modulation values are approximate, because the minima and maxima are not sharply defined on the sweeps. In addition to that, the temperature was not stabilized during a measurement, but was done during the cooldown. When in the variable temperature cryostat the ^{4}He needle valve is opened and closed, the temperature decreases sharply, then the decrease flattens out, and at this moment the measurement sweeps were taken. This is by no means a stable state, but gives a quantitative information. The sixth trace in fig. 6.11-bottom superimposes in color the five preceding traces.

After the cooling down measurements, the second sample also showed Coulomb blockade, as shown in fig. 6.12, taken at 1.88K . and three dimensionally in fig. 6.13.

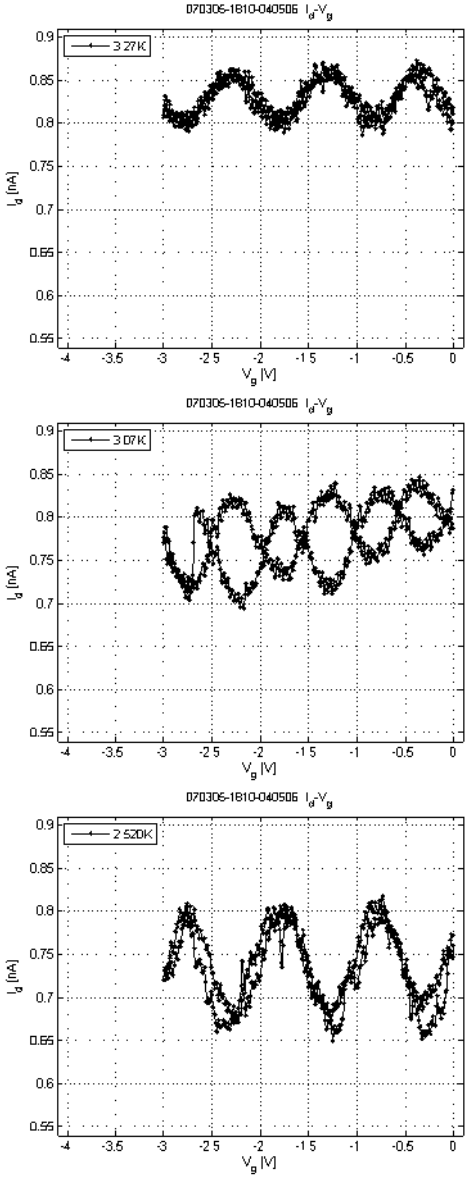

Figure 6.10: *Coulomb oscillations, temperature dependence — for 3.27K(top), 3.07K(center) and 2.52K(bottom). Charge rearrangement for 3.07K . See description in body of text.*

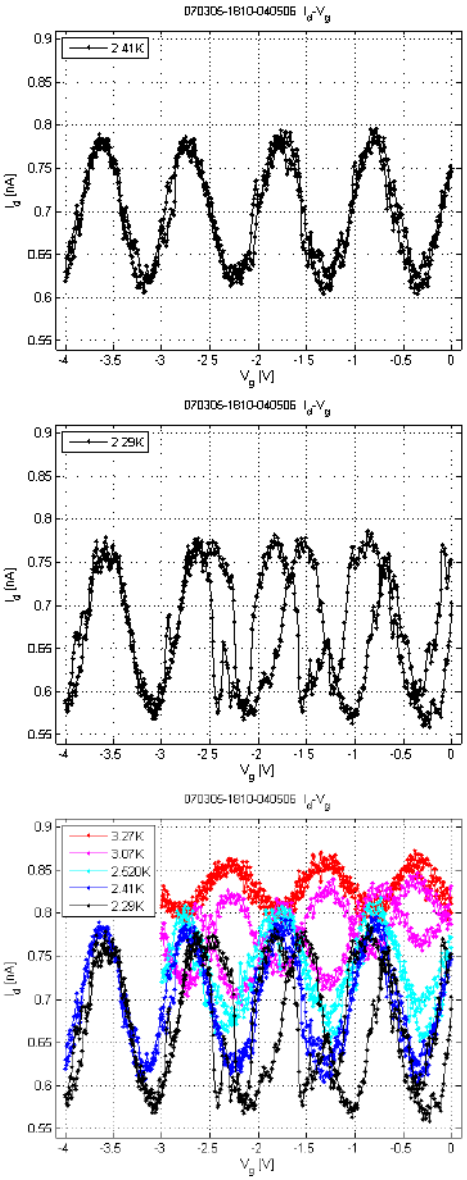

Figure 6.11: *Coulomb oscillation, temperature dependence — for 2.41K(top), 2.29K(center) and all five temperatures superimposed(bottom). Charge rearrangement for 2.29K . See description in body of text.*

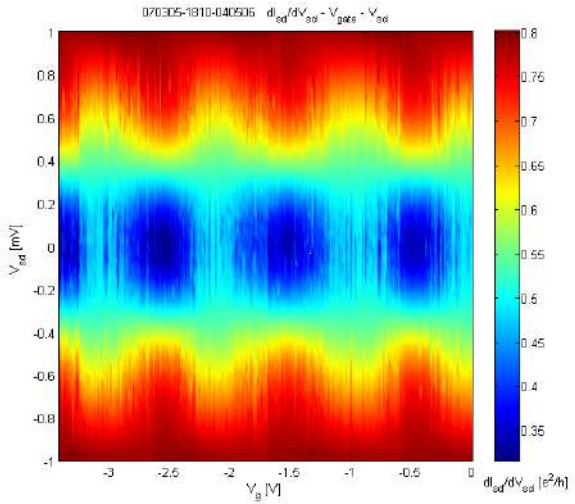

Figure 6.12: *Coulomb diamonds 2nd sample 2D — $dI_{sd}/dV_{sd} - V_{sd} - V_g$*

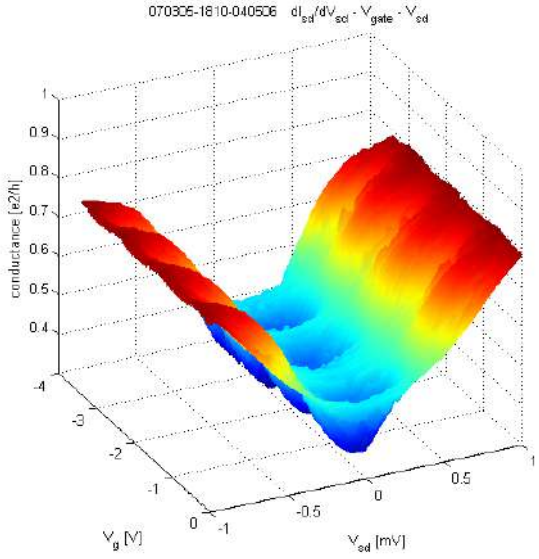

Figure 6.13: *Coulomb diamonds 2nd sample 3D — $dI_{sd}/dV_{sd} - V_{sd} - V_g$*

6.4 Results at 400mK, normal conductor

The Coulomb diamonds at 1.8K have blurry at best boundaries. To extract junction parameters with less uncertainty, the boundaries need to be better defined and sharper. For this, the temperature needed to be lower than the ∼1.8K range achievable in pumped ^{4}He variable temperature cryostats. A ^{3}He–^{4}He dilution refrigerator type cryostat was used to reach temperatures of 400mK.

At the time of design of the SET, no thought was given to superconductivity. After the decision to use a dilution refrigerator, the materials used were surveyed for their critical temperatures T_c, to understand when which part of the setup would turn superconductive. The Al(T_c=1.175K) SET is connected to prepatterned Pt(T_c=0.019K) connectors on a Ti(T_c=0.40K) adhesion layer. The lowest temperature at which a measurement was done was 400mK. If the Ti adhesion layer was superconductive under this conditions, then no sign of it was visible in the measurements, the Al showed very clear superconductivity.

The first set of measurements was done with an magnetic field of B=0.5T applied. The critical magnetic field of Al at 0K is 10.5mT. With increasing temperature it decreases to zero for the critical temperature for superconductivity, which means the applied magnetic field is largely sufficient to preclude the phase change of Al to the superconducting state.

Based on the indications in the theoretical stability diagram in fig. 3.10, the junction parameters for fig. 6.14 were calculated. For e/C_g, the voltage extracted is 471mV, which yields C_g=339zF. For e/C_Σ, the voltage extracted is 926μV, which yields C_Σ=173aF. The slope $-Cg/C_1$ extracted is -1838μV/471mV=3.9×10^{-3}, which with above C_g yields C_1=86.9aF. From $C_\Sigma = C_1 + C_2 + C_g$ the value of C_2=86.1aF is obtained, which is quasi the same size as C_1, given the uncertain nature of the graphic measurement. The charging energy is $E_c = e^2/2C_\Sigma = 74 \times 10^{-24}$J=74.0yJ. At 402mK, the thermal activation energy is k_BT=5.55yJ . This means that Coulomb blockade is observable by a margin of an order of magnitude, and that the threshold condition $E_c = k_BT$ will be reached at T =5.36K .

The two pronounced cases of varying the bias voltage V_b with the gate voltage V_g fixed at the maximum Coulomb blockade with $V_g = e/C_g + ne/C_g$ and at the minimum Coulomb blockade with $V_g = e/2C_g + ne/C_g$ are given in fig. 6.15. The would be location of their vertical trace across fig. 6.14 is indicated by arrows.

The stability diagram of fig. 6.14 is given in a three dimensional representation is given in fig. 6.16 .

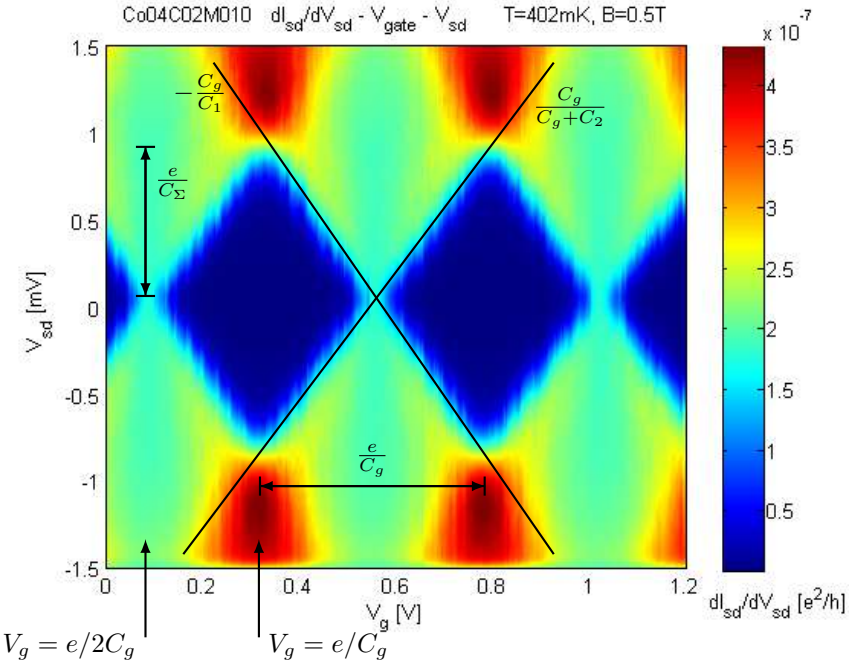

Figure 6.14: *Coulomb diamonds, 404mK, normal conductor, annotation permitting to extract junction parameters, see body text.*

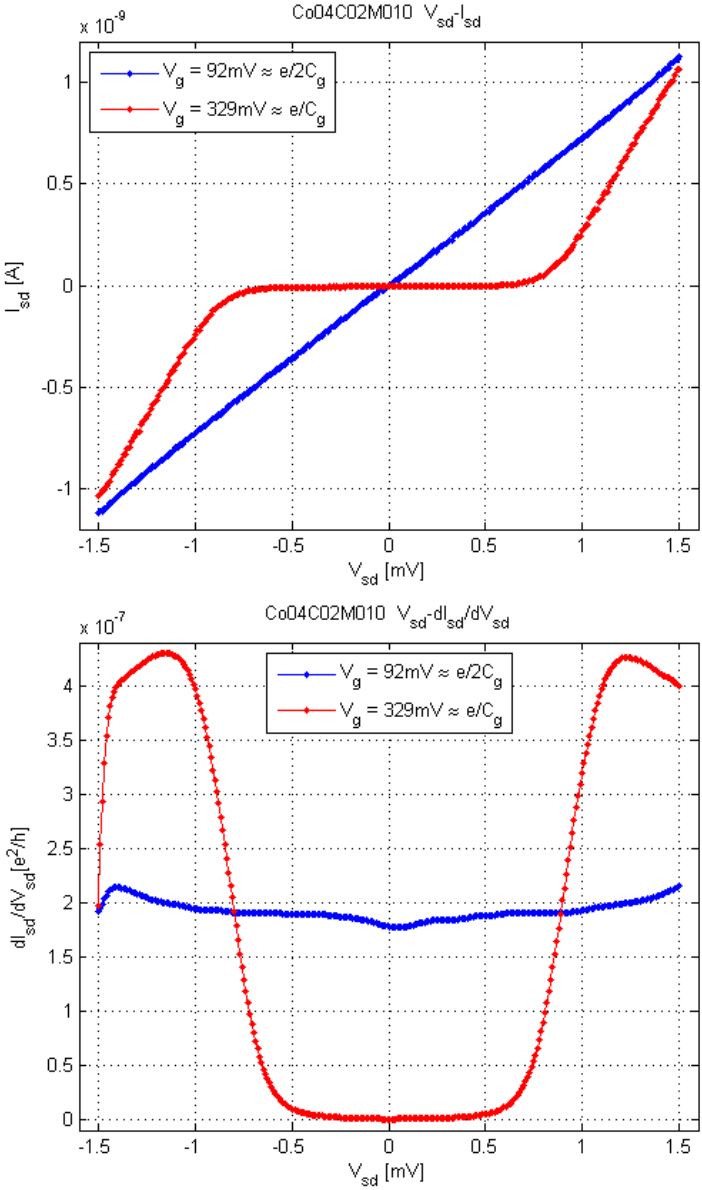

Figure 6.15: *Coulomb blockade for $V_g = e/C_g$ with a big differential conductance change (u-shape) and for $V_g = e/2C_g$ with very shallow change. Peak vs valley $dI_{sd}/dV_{sd} - V_{sd}$.*

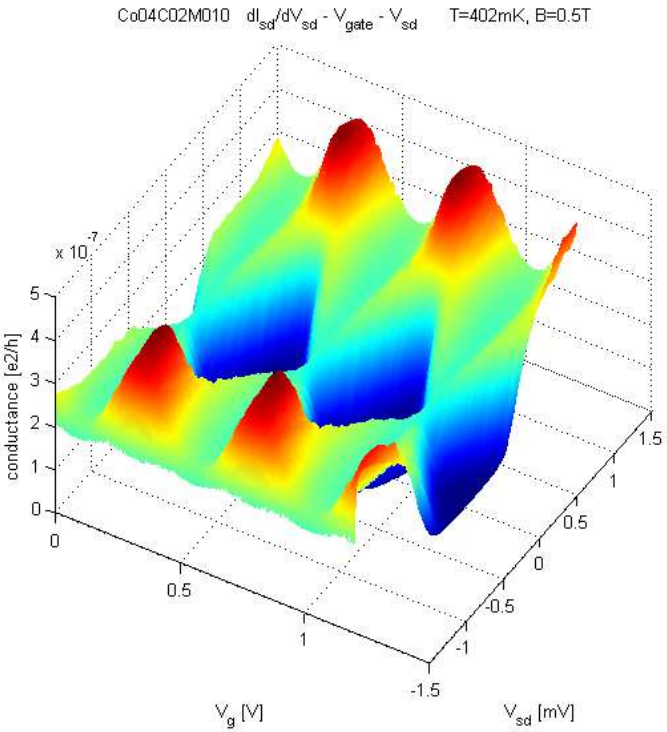

Figure 6.16: *Coulomb diamonds 3D, 402mK, 0.5T, $dI_{sd}/dV_{sd} - V_{sd} - V_g$*

6.5 Results at 440mK, superconductive

In fig. 6.17 the Coulomb diamonds can be seen, but also signatures of many other processes happening. The most striking feature is the offset of the Coulomb diamond body along the y-axis, the $4\Delta/e$ shift of the quasiparticle conduction onset. The currents inside of the Coulomb blockade diamonds, which are signatures of transport not due to pure quasiparticle conduction, are orders of magnitudes smaller. They are not well visible, because the measurement aimed for the Coulomb blockade measurement, and not for subgap transport phenomena. The colormap was flattened for all but the smallest currents reveal the transport inside of the Coulomb blockade diamonds.

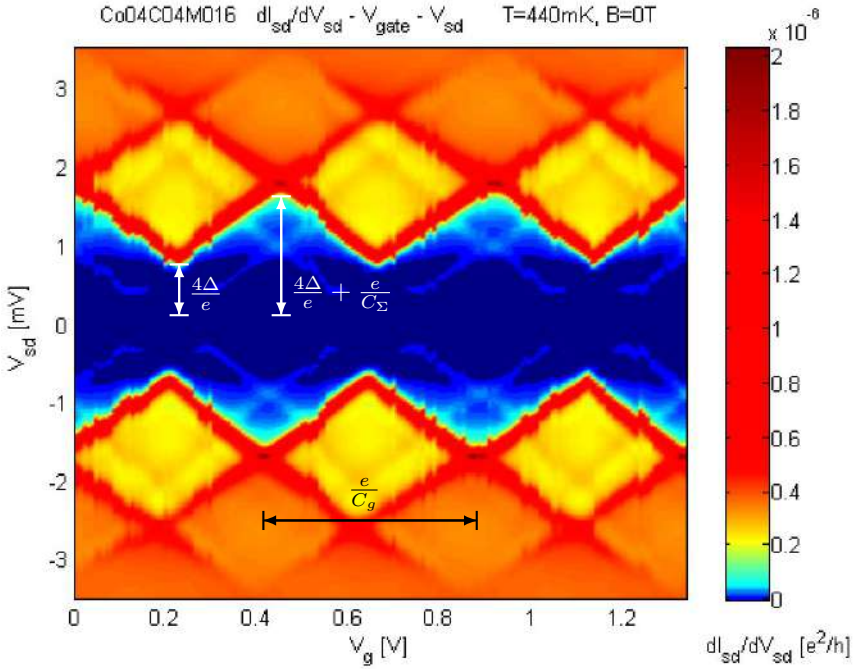

Figure 6.17: *Coulomb diamonds 440mK — $dI_{sd}/dV_{sd} - V_{sd} - V_g$*

There are better ways to enhance the poorly visible data than to manipulate the colormap. A subset of the data in stability diagram was taken to yield the six figures in fig. 6.18, where stability diagram and three dimensional image live side by side. The top row shows the original current

data, the center row shows the logarithmic current, the bottom row shows the logarithmic current clipped to show only low currents.

From the linear current stability diagram excerpt in fig. 6.19, the energy gap Δ and the charging energy E_c could be reconfirmed.

From the logarithmic current stability diagram excerpt in fig. 6.20, The slopes of the subgap transport cones could be determined. Then they were copied to the following image, because the major currents can not be read anymore from the clipped data.

From the clipped logarithmic current stability diagram excerpt in fig. 6.21, the subgap transport signatures could be identified.

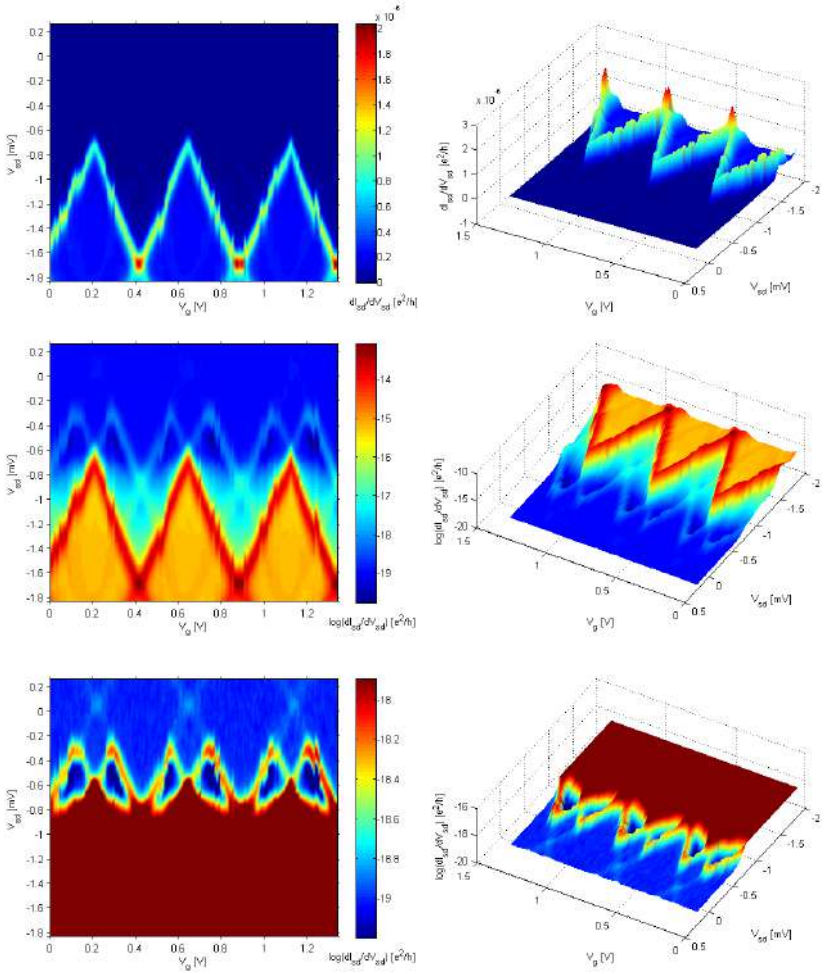

Figure 6.18: *Coulomb diamonds 440mK data, current linear (top row), current logarithmic (center row), subgap transport appears, current logarithmic, clipped (bottom row) to show small currents in subgap transport.*

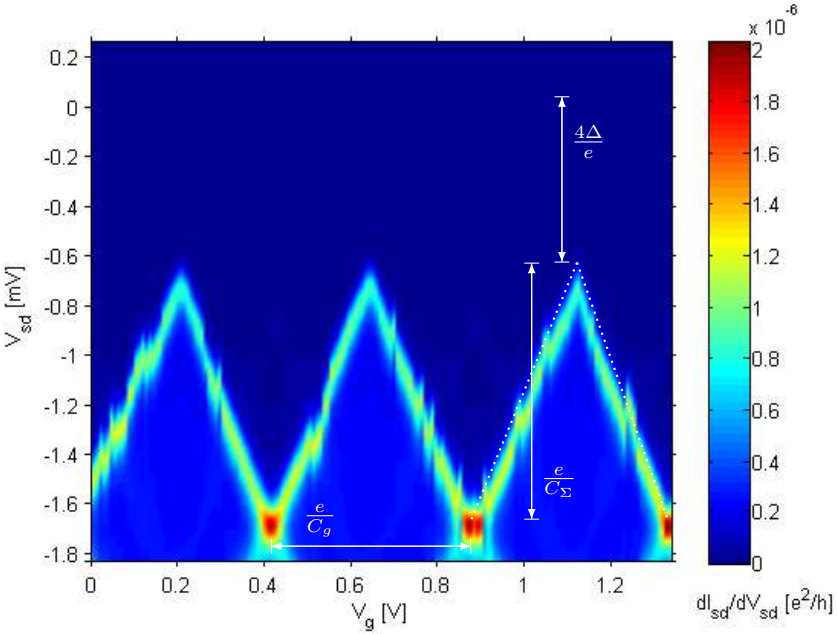

Figure 6.19: *Coulomb diamonds 440mK 2D lin — $dI_{sd}/dV_{sd} - V_{sd} - V_g$. because of the linear current scale, almost no subgap transport can be seen.*

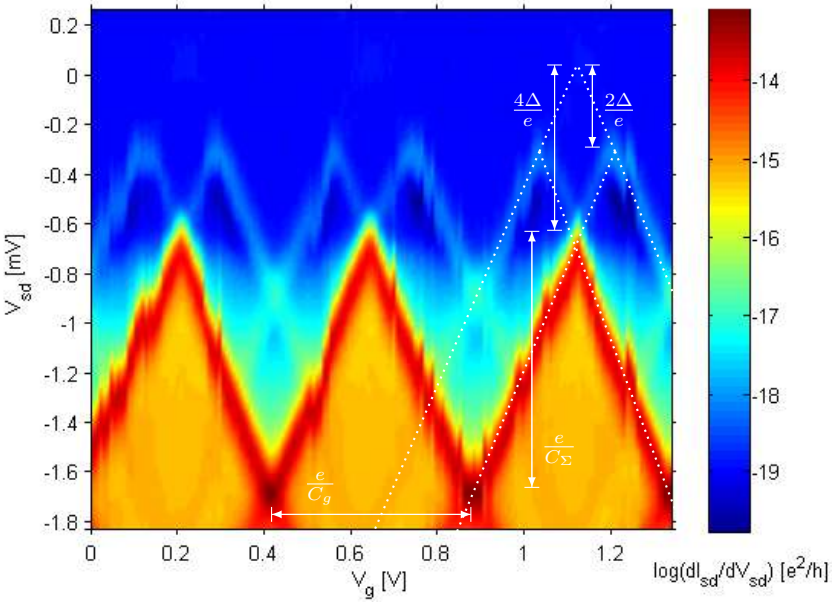

Figure 6.20: *Coulomb diamonds 440mK 2D log*

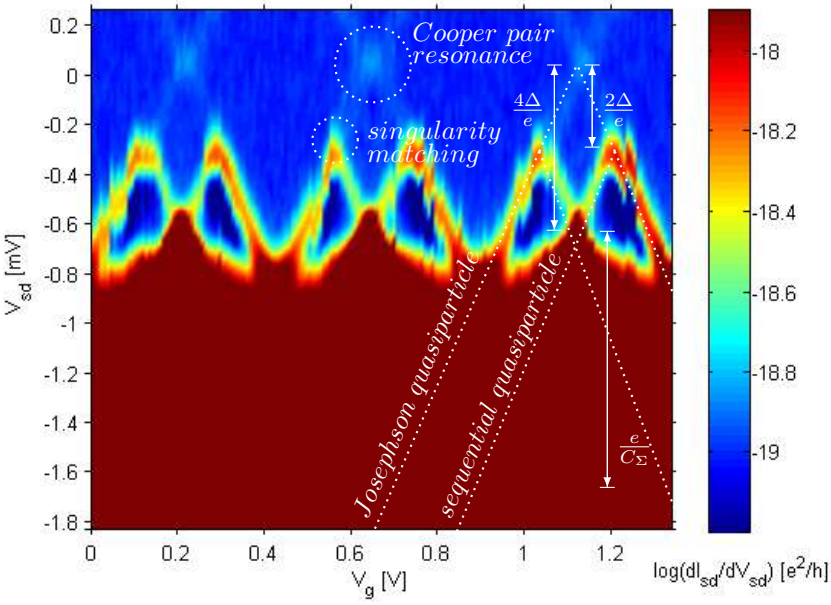

Figure 6.21: *Coulomb diamonds 440mK 2D log clip*

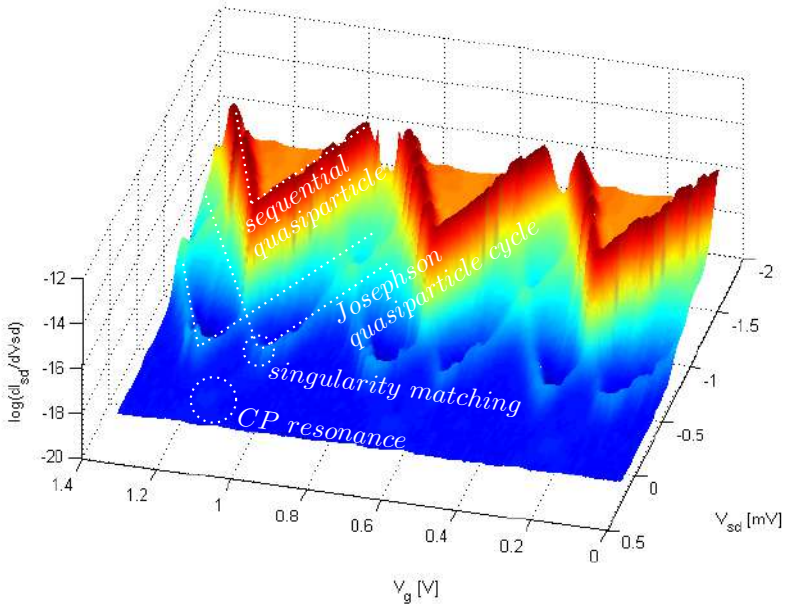

Figure 6.22: *Coulomb diamonds 402mK 3D log B=0.5T — $dI_{sd}/dV_{sd} - V_{sd} - V_g$*

6.6 Summary

The superconductive SET have three typical energy scales that govern them, besides the thermal energy $E_{th} = k_B T$:

the charging energy $E_c = e^2/2C_\Sigma$,

the energy gap Δ,

the Josephson coupling energy $E_{Ji} = h\Delta/8e^2R_i$.

For the sample discussed here, the data was gathered from the stability plots, and using the Ambegaokar-Baratoff relation developed in section 3.5.1 on p.44, $E_J = h\Delta/8e^2R_n$, the Josephson energy of each junction are estimated, i.e. E_J=2.36 μeV (symmetrical junctions assumed). The values are summarized in a table, and compared with other values gathered form publications discussing SISIS type SETs.

paper	C_1 [aF]	C_2 [aF]	C_g [aF]	C_Σ [aF]	R_1 [kΩ]	R_2 [kΩ]	R_{tot} [kΩ]	E_C [eV]	Δ [eV]	E_J [eV]
thesis	87	87	0.3	174	275	275	550	460μ	201μ	2.36μ
Hadley[69]	178	210	1.07	389	-	-	1800	206μ	203μ	-
Manninen[78]	110	110	14	234	210	210	420	350μ	210μ	-
Visscher[249]	57	96	7	160	88	397	485	0.5m	0.2m	4.5m
Nakamura[79]	115	115	5.9	236	485	485	970	340μ	215μ	1.4μ

Table 6.1: *Parameters of SISIS SETs*

The measured sample was in the $E_J \ll \Delta < E_c$ regime. This means that the effects due to the Josephson energy, i.e. the supercurrent, will be either unobservable or very faint.

Above the superconducting gap, the dominant mechanism is the sequential tunneling of quasiparticles. Despite the Coulomb blockade, charge can be transported by thermally excited quasiparticles or by a combination involving both Cooper pair and quasiparticles, and may only happen if energetically favorable. The threshold voltages were discussed in section 3.5.2.3 on p.48, and were for singularity matching

$$V_{SM} = \frac{4E_c}{e}(\frac{1}{2} + n \pm \frac{Q_0}{e})$$

and for Josephson quasiparticle cycle

$$V_{JQP} = \frac{4E_c}{e}(n \pm \frac{Q_0}{e})$$

and as reminder for the sequential quasiparticle tunneling

$$V_{seq} = \frac{4\Delta}{e} + \frac{4E_c}{e}(\frac{1}{2} + n \pm \frac{Q_0}{e}).$$

The Coulomb diamonds for the superconducting SET were recorded using their quasiparticle tunneling thresholds as a reference for the current axis. However, inside the Coulomb blockade, in the so called sub-gap transport zone, the current is very small in comparison to outside of the Coulomb blockade. This is why if there the Coulomb diamond measurement were to be redone, the dynamic range for current should be fixed to cover the inside of the gap, and the range of the measurement instruments should be adapted to better resolve the small currents.

At the time of this writing, the device characterization and the scanning operation testing of the assembled SSET through the Nanophysics group has not been concluded, which is why there is yet no result for this core goal.

Chapter 7

Conclusion and outlook

This thesis presents a fabrication process which aims to integrate a single electron transistor on the tip of an atomic force microscope probe to be used as a scanning single electron transistor (SSET).

The theory of Coulomb blockade is elaborated, existing fabrication strategies and techniques are reviewed, and then a fabrication process is established from scratch.

Devices patterned standalone on a test vehicle and devices patterned on a chip-cantilever assembly of a tuning fork based self-actuating self-sensing AFM sensor were fabricated with the developed process.

The single electron transistor was proven to work at low temperatures standalone. The single electron transistor was patterned on a scanning probe tip, and assembled into tuning fork based probes. Those probes exhibit comparable electrical properties at room temperature as do the non-integrated, standalone ones which were successfully measured at low temperatures. This is an indicator that the probes might be functional at low temperatures.

However, since the probes have not yet been characterized in a cryostat environment, there is no proof that the devices on the probes are functional and will show single electron charging effects.

If the integrated devices show the desired effects, and Coulomb blockade can be observed, then there still remains a lot of work ahead. A scanning single electron transistor has an enormous potential as a tool to investigate mesoscopic systems and for nanoelectronics, but there will be many factors to be investigated with regards to the scanning strategy to be used. How near or how far from the surface must the SSET be operated for best charge resolution? The tuning fork cannot be operated while

the SET is measuring, because the current needed for actuation would disturb the SET too much. It may be turned off for each measurement point. Or the sample topology may be acquired in a first pass, and then using this information, a second pass without tuning fork (no z-feedback) is performed, while the SET measures continuously, or just when the probe stops at each grid points of the scanning field. The SSET must be immobile while measuring for charges, but what kind of measurement and also result would it obtain if it were to continuously scan the surface? Is there a better structure than just an SET to observe charges?

Since other groups are also still working on SSET, there will certainly be a continued interest in such a technology, and further research answering this mostly practical questions.

Acknowledgements

This dissertation reports my research and findings and carries my name. It was possible to be accomplished with the help of many others, who helped me scientifically and in real life with explanations, suggestions, advice, structure and friendship. I would like to thank them here[250].

First and foremost, I thank my wife. We met during this research. When during the second half of this project, despite my intensest efforts, my devices refused to cooperate and remained for a long time non functional structures, she has been an important source of strength, solace and comfort well described by this succinct quote: *'Success is the ability to go from one failure to another with no loss of enthusiasm.'*, attributed to Winston Churchill (1874–1965). Not only she has been patient and understanding when what was anticipated to be a three to four year process stretched out to more than five years, but also she wrote her own thesis in parallel. Our son was born during this time. His – mildly put – unforgiving requirement for our full mental attention and physical presence during his waking hours was a good counterweight to our work, his increasingly perplexing questions stimulating, giving us great joy and happiness when engaging with him.

I thank my thesis advisor, Professor Urs Staufer. He provided structure, when the great independence, that he allowed, had to be contained. He encouraged exploration, permitted to do research in many areas.

I thank Professor Nico F. de Rooij, for giving me the opportunity to work in his research group.

I thank my *sempai* Terunobu Akiyama for indulging my *kōhai* youthful excesses and errors, and for his inspiring mastery of and rule over microfabrication techniques, which were incentive and stimulus to beat my process into the limits of my control.

I thank the Nanophysics group of Professor Klaus Ensslin, Laboratory for Solid State Physics, ETH Zürich, Switzerland, who characterized the devices at low temperature in their laboratory's cryostats with great

competence.

In Switzerland, not unlike many other countries, the federal government executive branch promotes scientific research with federal money. This is done through the Swiss National Science Foundation (SNSF), which has National Research Programs (NRP) and National Centres of Competence in Research (NCCR)[1]. Within the NCCR Nanoscale Science, there is the module 'quantum computing and quantum coherence', with the project 'manipulation of single spins', wherein this thesis is located as a subproject. I thankfully acknowledge financial support from the NCCR 'Nanoscale Science' of the SNSF, and the République et Canton de Neuchâtel.

The working environment at Samlab is a very stimulating one, and it has been a good experience, both personally and professionally.

Many thanks to everyone.

Neuchâtel, November 2007
Kaspar Suter

[1] **fr:** Fonds National Suisse (FNS), Programmes nationaux de recherche (PNR), Pôles de recherche nationaux (PRN). **de:** Schweizer Nationalfonds (SNF), Nationale Forschungsprogramme (NFP), Nationale Forschungsschwerpunkte (NFS).

Appendices

Appendix A

Process recipies

The process recipie is compiled from the labbook entries for the fabrication for a working SET. The process starts with an already processed substrate. It is a Si <100> wafer, that was standard cleaned, then had 700nm of thermal oxide grown, and received the connector lines out of Pt 100nm on a Ti 50nm adhesion layer which were patterend using a liftoff process with a resist system composed of LOR-3B as bottom and S-1813 as top layer, AZ-400K as developer.

```
__2007-03-05-Mon_____________________________________________________________
   IMPORTANT: did Oxygen Plasma strip 30min, before spinning, no dehydrate/HMDS
  botlayer: 200nm-2000rpm.copolymer-EL6%
    5s@500rpm acc5 / 45s@2000rpm acc5 / 90s@HP180degC [180target]
  toplayer: 100nm-1500rpm.pmma950k-Anisole2%
    5s@500rpm acc5 / 45s@1500rpm acc5 / 600sec@HP180degC [600target]

070305-1800-1810-1820-1829 [using 061206-spun-071] exposure
  exposed design J:\AFM\KSu\exp\070305\top.gds
  includes 25/25 u/v writefield offset stitch field compensations on all 4 chips
  Column parameters
  Voltage:  10 kV  Aperture:  30 um  Beam current:  140.4 pA
  Magnification:  2000 x  Working distance:  6.091 mm
  Exposure parameters
  -- Areas --  Step size:  9.6 nm  Dwell time:  0.656 usec
  nominal Dose:  100 uC/cm^2  calculated Dose:  99.938 uC/cm^2
  -- Single Pixel Lines --  Step size:  1.6 nm  Dwell time:  1.139 usec
  nominal Dose:  1000 pC/cm  calculated Dose:  999.473 pC/cm
  -- Single Dots --  Dwell time:  712.251 usec  calculated Dose:  0.1 pC

__2007-03-06-Tue_____________________________________________________________
070305-1800-1810-1820-1829 develop
  develop MIBK+IPA=1+3 45s, IPA-30s, H2O rinse 120s, N2 dry
```

```
  post development bake hotplate 90s@90degC
070305-1800-1810-1820-1829 plasma oxidation descum
  (tepla 300 plasma processor)
  oxygen plasma, tepla, 10s of program2, 200ml/min, 700W, backgroundTemp=31degC

__2007-03-07-Wed_____________________________________________________________
070305-1820-1829 evaporation
  evaporation resistive tectra delta 45deg screw side
  morning: melt new Al rods, evap 22.5nm onto nothing to get rate going.
  afternoon: base pressure 2.2E-7mbar, T0=22degC
  1st: 27.7nm (-25deg 14h) tectra, thermal, W-wire-BN-basket, Al rods
    base pressure 2.5E-6mbar @ 30degC
      rampup: 10s-20%@7V
              10s-40%@7V
              20s-60%@7V 1.9E-6mbar 27degC
              30s-80%@7V 2.2E-6mbar 30degC
              10s-90%@7V 4.6E-6mbar ...
      (check for pressure increase at 80%@7V, wait 5-30s for stable pressure
       or pressure above 1.0E-5mbar, then open shutter)
  evap rate start 4.6E-6mbar, end temp 56degC
  oxidation 2min TMP=standby=666Hz, 1.0E+0mbar [8.6E-1mbar .. 1.6E+0mbar]
    vernier 4.3, temp evolution xxdegC -> xxdegC
  2nd: 43.7nm (+20deg 10h) tectra, thermal, W-wire-BN-basket, Al rods
    NotaBene: process runaway, some Al spilled into W-basket,
    base pressure 4.0E-6mbar @ 38degC
      rampup: 10s 40%
              10s 60% 8.6E-6
              20s 80% 1.4E-5
                  90% 1.6E-5
    evap rate start 1.6E-5mbar, end temp 63degC

070305-1820-1829 liftoff
  acetone@ultrasonic1MHz/isopropanol/di liftoff 30min

__2007-03-09-Fri_____________________________________________________________
070305-1829 measurement[hp4155a semiconductor parameter analyzer]
  070305-1829-010203   (dotSet D1-G1-S1)
  070305-1829-0103     (dotSetDS) 2mV/(-745+659)nA= 1.43 MOhm       BOND
  070305-1829-252627   (dotSet D1-G1-S1)
  070305-1829-2527     (dotSetDS) 2mV/(-1.85+1.90)nA = 533 kOhm     BOND 252627
              2527     (dotSetDS) 2mV/(-1.19+1.24)uA = 823 Ohm      postbond
  070305-1829-2728     (1jct)     2mV/(-9.50+10.25)nA= 101 kOhm     BOND 28
              2728     (1jct)     2mV/(-1.18+1.24)uA=  826 Ohm      postbond
  070305-1829-222324   (dotSet D1-G1-S1)
  070305-1829-2224     (dotSetDS) 2mV/(-1.75+1.81)nA= 562 kOhm      BOND 222324
              2224     (dotSetDS) 2mV/(-1.16+1.21)nA= 844 kOhm      postbond
  070305-1829-040506   (dotSet D1-G1-S1)
  070305-1829-0406     (dotSetDS) 2mV/(-743+767)pA= 1.33 MOhm       BOND
  070305-1829-0607     (1jct)     2mV/(-1.10+1.15)uA= 889 Ohm
  070305-1829-080910   (dotSet D1-G1-S1)
  070305-1829-0810     (dotSetDS) 2mV/(-2.11+2.18)nA= 466 kOhm      BOND
```

```
  070305-1829-111213   (dotSet D1-G1-S1)
  070305-1829-1113     (dotSetDS) 2mV/(-2.03+2.10)nA= 2.7MOhm       BOND
  070305-1829-1314     (1res)     2mV/(-1.18+1.23)uA= 829 Ohm
  070305-1829-151616   (dotSet D1-G1-S1)
  070305-1829-1517     (dotSetDS) 2mV/(-2.25+2.33)nA= 437 kOhm      BOND 151617
              1517     (dotSetDS) 2mV/(-2.56+2.69)nA= 381 kOhm      postbond
  070305-1829-18192021 (4pointRes Rl1-Rl2-Rr1-Rr2)
  070305-1829-1819     (Rl1-Rl2-lineres) 2mV/(-1.56+1.63)uA= 627 Ohm
  070305-1829-2021     (Rr1-Rr2-lineres) 2mV/(-1.31+1.36)uA= 749 Ohm
  070305-1829-1821     (1res)            2mV/(-1.09+1.15)uA= 1120 Ohm

__2007-03-12-Mon_____________________________________________________________
H20E h20e epotek glue for bonding
  http://www.epotek.com/SSCDocs/datasheets/H20E.PDF
  cure schedule: 3h@80degC, 15min@120degC, I do 1h@90degC
Cured for 1h@100degC.
Rebond everything, because I did inner ring (numbers 1 through 12) while
Zurich uses outmost numbers C1 through C12.

__2007-03-13-Tue_____________________________________________________________
  Note: todays measurements done:
  - together with Slavo Kicin,
  - at ETH Zurich, Solid State Physics Laboratory, HPF B19,  ethz ETHZ
    Schaffmattstrasse 16, 8093 Zurich, Switzerland,
  - in a pumped helium cryostat, oxford instruments
  - using the insert "VTI-Dewar(C15)" from a different cryostat
  - observed for the first time Coulomb oscillation in SET structures.
    after lunch at 13h43, Toxford=1.65K, Rab=8.9kOhm=2.9K
  - we are very pleased
```

Appendix B

Student course

The duties of local Ph.D. students' include teaching responsibilities. One of them is the bi-annual week-long (40h) blockcourse taught to M.Sc. level nanoscience students. This chapter contains extracts from a makeshift teaching manual which was written as a guide to give guidance on how to prepare and run the course. It contains process recipes and gathered data, as an illustration of what can reasonably be achieved and expected from the students. It is not a sample template report.

It is given as an appendix, because it illustrates how the experimentally observed interaction of electron beam with resist can be tied to the theoretical point exposure distribution model.

B.1 Preparation

B.1.1 Goals

Student's should retain some or all of the following topics:

- Introduction into electron beam lithography (EBL).
- Set up and perform the experiments that measure the normalized point exposure distribution, and extract the fundamental parameters for proximity effect correction.
- Design, simulate, write and develop EBL patterns accounting for proximity effect.

- Write a report to communicate their accomplishments, using the structure of a scientific paper, such as Introduction, Methods, Results And Discussion (IMRAD).

B.1.2 Documentation for students

The students should receive and read before the start of the course following articles.

- S. A. Rishton and D. P. Kern:
  Point exposure distribution measurements for proximity correction in electron beam lithography on a sub-100 nm scale.
  J. Vac. Sci. Technol. B, **5** (1987) 135-141.

- T. H. P. Chang:
  Proximity effect in electron-beam lithography.
  J. Vac. Sci. Technol., **12** (1975) 1271-1275.

- C. Dix, P. G. Flavin, P. Hendy and M. E. Jones:
  0.1μ scale lithography using a conventional electron beam system.
  J. Vac. Sci. Technol. B, **3(1)** (1985) 131-135.

Furthermore, to get an overview on electron beam lithography, they should skim the "Chapter 2: Electron beam lithography" of "Volume 1: Microlithography" of the book "SPIE Handbook of Microlithography, Micromachining and Microfabrication", which is available either online at the Cornell NanoScale Science and Technology Facility, or as a local, standalone version at samlab-imt.

The articles and the overview will familiarize the students sufficiently with the topic to reduce the complete surprise factor when they start the course.

B.1.3 Samples for the experiments

B.1.3.1 Silicon chips

The goal is to observe the interaction of electrons with matter. Electron beam lithography is chosen, because the interaction of electrons with matter can be observed by the traces that are left in the electron beam resist. Samples are needed to hold and support the resist that is exposed. The resist is applied using a spin coater, which holds the sample by suction, therefore the major limitation is that the sample must be reasonable flat, in order to make the vacuum suction seal with the rotating chuck. An easy

way to obtain substrates is to take a Silicon test wafer and have it diced into 15mm × 15mm sized chips. No alignment to primary flat necessary. No standard cleaning necessary. A 4" wafer yields about 21 such chips. If there is no rush, dicing jobs are accumulated in order to make it worth while to turn on the equipment one day for a couple of hours, instead of on every day for 15 minutes. Therefore, and as a courtesy, the plan to dice should be announced a couple of days ahead of time. Factor in that the wafer must sit on the 'blue tape' film for some time to enhance adhesion, typically an hour, better an entire morning or overnight.

If needed, mark numbers in the corners of the chips with a diamond tip before reentering the clean room. Clean with acetone, isopropanol, deionized water (DI), dry with nitrogen jet. It is important to do this thoroughly, to reduce the dirt brought into the clean room, and eventually into the electron beam system.

B.1.3.2 Metal coatings

To be able to observe two or three distinct backscattering behaviors, some of the chips will require metal coating. The metals Au and Ti of thicknesses 500Å were selected, cf. p. 192, but it can be any other. The evaporation experience recommends an 50Å Cr adhesion layer for Au, none for Ti.

B.1.3.3 Resist

Before the start of the course, sufficient amounts of electron beam resist must be available, or must be prepared, in the required dilutions. The recipe used in this course can be consulted on p. 195. Diluting and filtering a fresh bottle of resist can take the better part of an hour, wall time, and is not the most exiting thing on earth to be waiting for, especially not with three students waiting as well. Be prepared. A resist system is only complete with sufficient developer (MIBK+IPA) and stopper (IPA). [MIBK: Methyl Isobutyl Ketone, IPA: Isopropyl Alcohol or Isopropanol.]

B.1.4 Software

B.1.4.1 Raith

For each student, a computer with a standalone version of the Raith software installed on it is needed. For the last installation done on windows xp computers, administrator privileges were required, i.e. user name and password for "administrator" are needed, and usually granted by the IT

manager for limited time, typically a day. It is believed that administrator privileges are necessary to install the driver for the hardlock, i.e. the USB-key that is needed to run the raith program, and also because Raith installs itself directly into the `C:` drive, not into the `C:\Program Files` folder. Necessary service packs for Raith must be applied at the same time. The software must be run from the student accounts, not any other user, because "guest student" accounts have supplementary restrictions compared to common user accounts.

B.1.4.2 Electron trajectories simulator

A free Monte Carlo simulator for electron trajectories in solids called casino is available.If needed, it can be installed by the students themselves, such as on their "desktop", as there are no special privileges required.

B.1.4.3 Parameter fitting to harvested data

A key section of the result analysis is the fitting of curves to the data harvested from the SEM micrographs. The data can be gathered in any spreadsheet software, such as microsoft excel, available through campus license. The curve fitting to the gathered data points requires any capable program. In the past the locally available Origin, version 6.1, online at version 7.5 (March 2007) was used. Origin's nonlinear least square fitter has its peculiarities, trials are recommended ahead of time to get and understanding of what the students will have to face.

If so inclined, Matlab may be used for the same task. Suitably exported datafiles, i.e. without any empty fields, so that csvread does not have to perform any data conditioning, are fed into fitting function scripts, obtained and adapted from document "Using Matlab for Curve Fitting in Junior Lab" [MIT Department of Physics, Advanced Experimental Physics I & II, (Dated: February 28, 2007)].

This works well, but only for simple fits, not for combined double-gaussian with exponential contribution. The used algorithm has similar convergence problems as the Origin implementation.

B.2 Experiments

B.2.1 Monte Carlo simulations

This is an optional part of the course and not necessary. It helps to understand the forward and backward scattering through the use of a

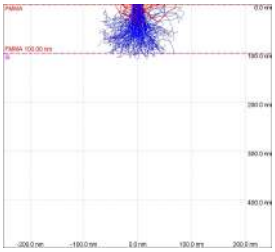

Figure B.1: *2keV*

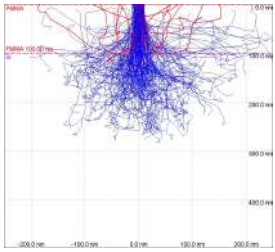

Figure B.2: *4keV*

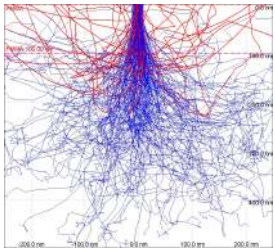

Figure B.3: *6keV*

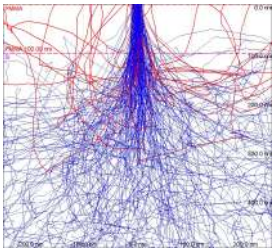

Figure B.4: *8keV*

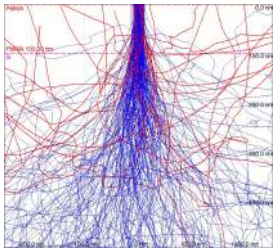

Figure B.5: *10keV*

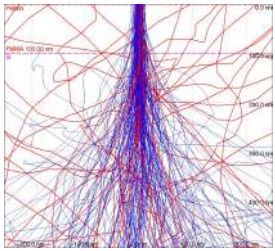

Figure B.6: *15keV*

simulator.

For the modeling of PMMA, 100nm thickness is used, and for its composition the formula $C_5O_2H_8$ of the monomer.

B.2.1.1 Choice of electron energy

It was decided to use 10keV electron energy, mostly because it is the standard setting given by the electron beam vendor. But the simulations show that in bare Silicon, the electrons are driven sufficiently deep into the substrate, without backscattering too much. In the following pictures, there are 100nm of PMMA spun on Silicon. The plots are 500nm deep, 500nm wide, blue trajectories are forward scattering, red trajectories are backward scattering.

As a quantitative observation, it can seen that starting 8keV electron energy, the forward scattering diverges into the typical pear-shaped form beyond the 100nm electron beam resist layer, probably also a reason that the manufacturer has chosen 10kV as the default acceleration voltage.

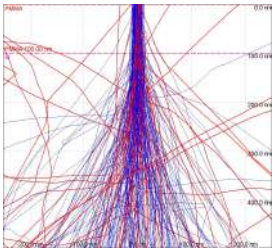

Figure B.7: *20keV*

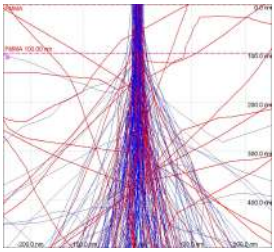

Figure B.8: *25keV*

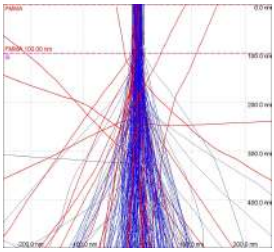

Figure B.9: *30keV*

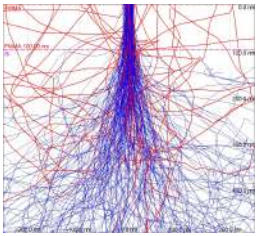

Figure B.10: *Silicon substrate, 100nm PMMA. 10keV*

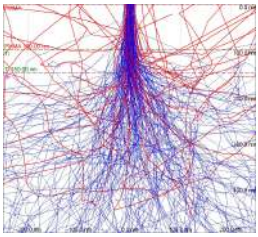

Figure B.11: *Silicon substrate, 50nm Ti, 100nm PMMA. 10keV*

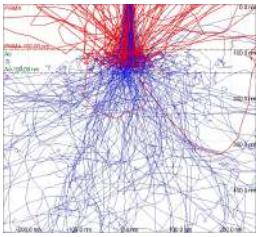

Figure B.12: *Silicon substrate, 50nm Au, 100nm PMMA. 10keV*

B.2.1.2 Choice of substrate

Silicon was chosen as substrate, because, just as in the planet's crust, it is the most abundant element in the clean room. As forward and backward scattering observation is intended, the substrates are coated with nothing, Titanium and Gold, which are expected to have different scattering behaviors based on their atomic number. Film thicknesses of of 500Å Au and Ti were selected. On a ^{14}Si substrate, the metal ^{79}Au of much higher atomic weight will result in more backscattering, i.e. more elastic scattering with trajectory broadening, due to larger nucleus and larger number of electrons to interact with, compared to both bare ^{14}Si, and ^{22}Ti. The forward scattering, i.e. inelastic scattering, is predominant in bare ^{14}Si and ^{22}Ti, leading to deeper penetration and less trajectory broadening.

The simulations show little effect of the Ti, but a lot of backscattering due to the Au. It is expected that this will allow for well observable differences, both in clearing dose, and proximity effect in the experimental section.

B.2.2 Clearance dose determination

B.2.2.1 Resist spread recipe

The standard positive electron beam resist used is Microchem's PMMA 950k molecular weight. For a 100nm thick layer, the 2% solids in Anisole dilution is chosen, see the datasheet.

A coating recipe to obtain a 100nm thick layer is:

- (optional: 30min oxygen plasma to clean the surface, no adhesion promoter such as HMDS necessary)
- spread: 5s@500rpm, acceleration 5 (5s to spin up)
- spin: 45s@1500rpm, acceleration 5 (5s to spin up)
- bake: 10min@180°C on hotplate

B.2.2.2 Resist develop recipe

A developing recipe

- develop: 30s MIBK:IPA 1:3
- stop: 10s IPA
- rinse: 30s deionized water (DI)
- dry: N_2 blow dry

There are many other recipes that will work, such as baking 30min at 170°C, or spinning only 30s, or 45s developing, etc., etc. Above recipe is the same as the one given by Microchem, except that the bake time is increased from 90s to 10min.

I recommend that only above recipe is used, or that it is only changed for a good reason.

B.2.2.3 Experiment resist contrast - bake time influence

- Spin coat 3 pieces of Si chips (1500rpm, 2% → 100nm), bake one of the pieces not at all, one for 10s on the hotplate at 180°C and one for 10min.
- expose squares of 50μm × 50μm size with increasing dose, write labels at about $60\mu C/cm^2$ such that you recognize at what dose the square was exposed

- develop in MIBK:IPA 1:3 for 30s, rinse in IPA for 10s and then in deionized water (DI) for 30s, blow dry in N_2
- inspect the sample under optical microscope: which one of the squares is fully open?
- measure the height of the resist of each structure by means of the alpha-step (profilometer) or the AFM,
- Plot the resist height as function of the exposure dose. Define the contrast and the clearance dose. Compare the results of the three different substrates.

B.2.2.4 Experiment resist contrast - developer influence

- Spin coat 3 pieces of a Si wafer (1500rpm, 2% → 100nm), bake all pieces for 10 min on the hotplate at 180°C
- Expose squares of 50μm = × 50μm size with increasing dose, write labels at about $60\mu C/cm^2$ such that you recognize at what dose the square was exposed.
- develop in MIBK:IPA a) 1:4, b) 1:3, c) 1:1 solution for 30s. Rinse in IPA for 10s and deionized water (DI) for 30s, blow dry in N_2.
- inspect the sample under optical microscope: which one of the squares is fully open?
- measure the height of the resist of each structure by means of the alpha-step (profilometer) or the AFM,
- Plot the resist height as function of the exposure dose. Define the contrast and the clearance dose. Compare the results of the three different substrates.

B.2.3 Experiment point spread function

Measuring the point spread function

- Set-up a position list for dot-exposures at different dose values (use at least 256 points). The spacing must be such that the points will not interfere with each other, i.e. 10μm. Include 4 alignment marks and prepare your GDSII file for the automatic imaging of the exposed feature. Include 5 large ($10\mu m^2$) fields of different dose (clearance

dose, -10%, -5%, +5%, +10%) for controlling the actual value for your settings.

- prepare 4 samples, 2 bare Si one with Cr-Au, one with Cr or Ti metallization. Dehydrate the sample for 30min on the hot plate at 180°C, spin coat 100nm of PMMA 950k and bake it for 10min at 180°C on the hotplate.

- Expose and develop your sample.

- Inspect the pattern on one of the bare Si samples, take pictures for your report!

- test the automatic measuring routine on this sample, check for contamination after the measurement.

- measure the dimensions for the three other samples without inspecting them in the SEM (why no inspection?)

- Plot the spread function and fit a double Gaussian to it, extract alpha, beta and eta, compare and interpret the values between the different substrates.

B.2.4 Experiment proximity effect

- Select exposure parameters based on the values of the previous experiments. Motivate your selection of dose and contrast.

- Design a pattern of your choice where small structures (1μm and less) are close together, include also some larger patterns of 10μm. Take the writing time into consideration

- Use the computer generated proximity correction to define areas that need different dose.

- Correct your pattern manually

- Expose your pattern without proximity correction and with the manual and automatic correction. Compare the results.

Figure B.13: *Optical microscope image, Si substrate, 10s prebake, exposure dose 60$\mu C/cm^2$. Green-gray background is unexposed resist. Big squares on left side are 50μm × 50μm and fully cleared, i.e. the resist is entirely removed. Small squares changing color from dark brown, over yellow to bright brown indicate the evolution from insufficient dose which only exposes partially the resist layer to sufficient dose which entirely removes the resist.*

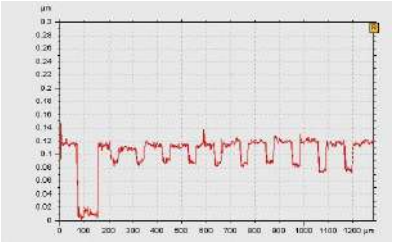

Figure B.14: *Profilometer trace, substrate Si, 10s prebake. The trace runs through the lowest row of Fig. B.13 and shows the initial fully cleared big square, followed by the increasingly deep partially developed small squares.*

B.3 Results

B.3.1 Data gathering

B.3.1.1 Clearance dose

It must be known before starting where the clearance dose roughly will be, otherwise a parameter space to large has to be exposed to find the contrast switching. The datasheet specifies: electron beam: Dose 50 - 500μC/cm^2 depending on radiation source/equipment & developer used. By our experience, for 100nm PMMA thickness, the clearing dose is in the vicinity of 50 to 60μC/cm^2.

Figure B.13 shows on the left side five squares, each of 50μm sidelength, and five rows with each ten smaller squares of 30μm sidelength. The 50μm squares are exposed to clear, and are used as optical navigational aids to do the coarse positioning when using the profilometer. It shows that low doses, way below clearing dose, remove sufficiently of the resist to be optically distinguishable.

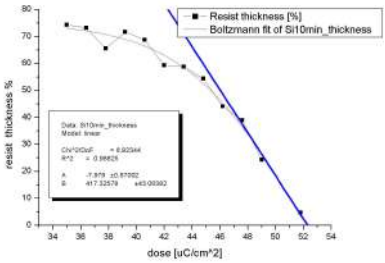

Figure B.15: *Bare Si*

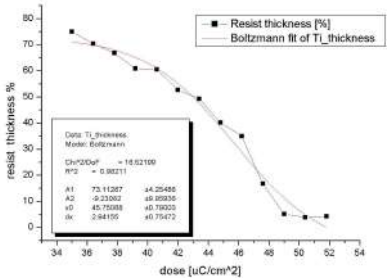

Figure B.16: *Ti on Si*

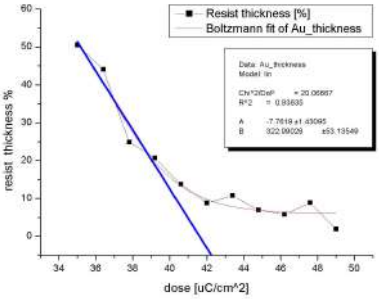

Figure B.17: *Au on Si*

substrate	clearing dose [μC/cm^2]
bare Si	52
Ti on Si	49
Au on Si	42

Figure B.18: *Clearing dose*

Figure B.14 is a profilometer trace, showing the steady increase in depth of the exposed 30nm squares. The values are plotted against the resist thickness.

The resist for the following three references is identical, same postbake. Figure B.15 is bare Silicon, B.16 is Silicon with a 50nm Titanium coating, B.17 is Silicon with 50nm Gold coating. The extracted values for the clearing doses, to be used in later experiments, are reported in table B.18.

Note that in the Au case B.17 the exposure dose was swept in an interval which resulted in the lowest dose already exposing 50% of the total resist thickness. That is why only little of the whole curve could be gathered.

B.3.1.2 Resist sensitivity

The samples used are prebaked a) not a all, b) for 10s, c) for 10min. The values for a) are missing. Figure B.19 shows no conclusive data. To be

redone.

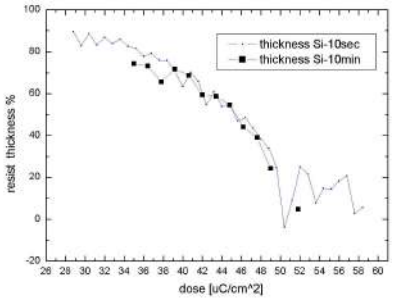

Figure B.19: *Resist sensitivity*

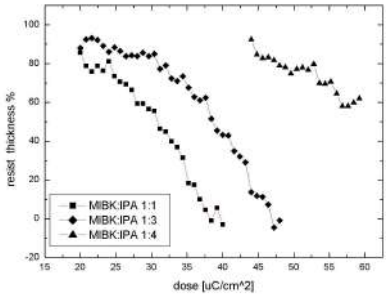

Figure B.20: *Resist contrast*

B.3.1.3 Resist contrast

The samples used are developed in MIBK:IPA dilutions a) 1:1, b) 1:3, and c) 1:4. Figure B.20 shows that for the least dilution, the development is very aggressive with a high sensitivity, but also a high contrast, e.g. a high slope of the curve. For 1:3 the slope is less and the clearing dose as well, for 1:4 it only can be guessed that the slope is even lower, and the clearing dose even higher.

B.3.1.4 Point spread distribution

A raith position list takes images of the exposed "dots", which were patterned with increasing doses. The diameters are measured manually on the screen on each image, and transcribed into a spreadsheet. The double gaussian functions are fitted to the values or this normalized point spread distribution.

B.3.2 Data fitting

Proximity function, Chang formulation, double gaussian:

$$f = \frac{1}{\pi(1+\eta)} \left(\frac{1}{\alpha^2} e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\beta^2} e^{-\frac{r^2}{\beta^2}} \right)$$

Proximity function, Dix formulation, double gaussian and exponential:

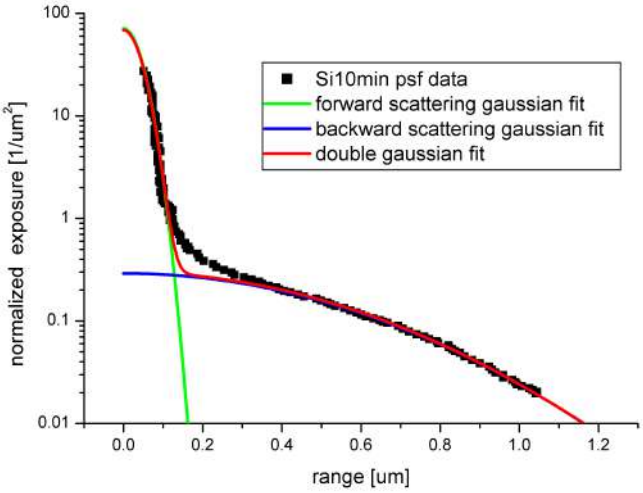

Figure B.21: *Si fit*

$$f = \frac{1}{\pi(1+\eta+\nu)}\left(\frac{1}{\alpha^2}e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\beta^2}e^{-\frac{r^2}{\beta^2}} + \frac{\nu}{2\gamma^2}e^{-\frac{r}{\gamma}}\right)$$

Origin fits to obtain proximity correction factors for the double gauss fit, and the double gauss with exponential fit.

sample	alpha α [μm]	beta β [μm]	eta η [1]	gamma γ [μm]	nu ν [1]
bare Si	0.054	0.63	0.6	-	-
Ti on Si	0.04	0.6	0.5	-	-
Au on Si - fit1	0.09	0.59	0.15	0.128	0.5
Au on Si - fit2	0.075	0.12	4.93	0.175	2.6

The two Au cases were not possible to fit using Origin, without extensively guessing the right values, there seems to be a convergence problem in the default algorithm.

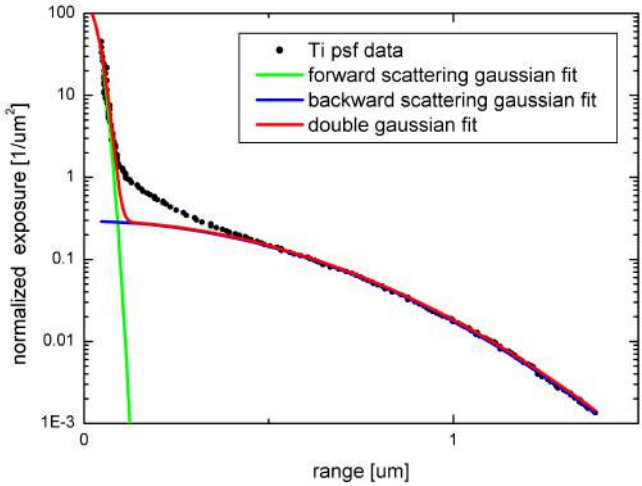

Figure B.22: *Ti fit*

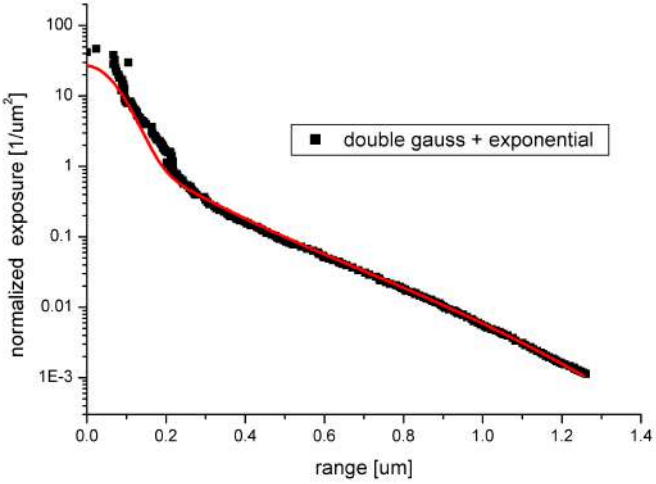

Figure B.23: *Au fit*

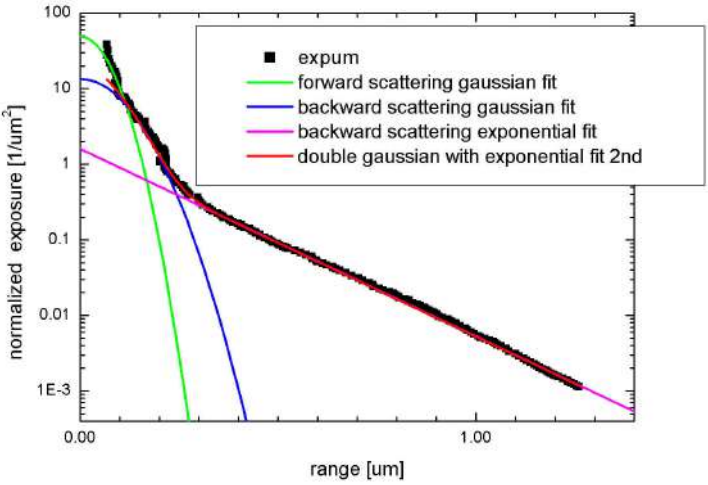

Figure B.24: *Au fit 2nd*

B.3.3 Proximity corrected design

The clearing dose calculated seemed to be to low in the proximity corrected experiments, therefore a second batch was exposed with clearing doses ranging from 50 to 80μC/cm^2 in increments of 10μC/cm^2.

The layout data is shown in fig. B.25. The clearance dose for Si and

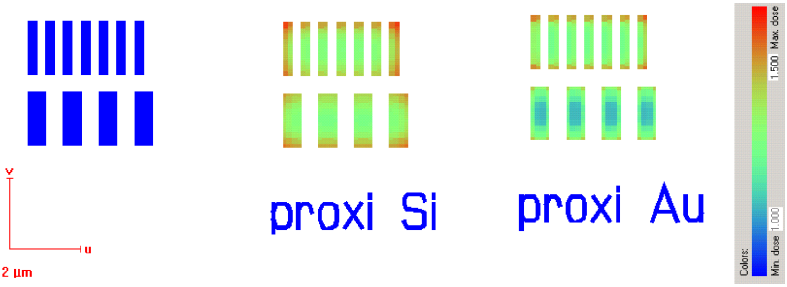

Figure B.25: *Layout data corrected for proximity effect. left) Uncorrected layout data in blue (dark tone, corresponds to bottom of colormap, dose factor 1). center) Layout data with proximity correction for Si. The dose in the center of the structures is green (dose factor 1.2), the corner areas are red (dose factor 1.5). Higher doses compensate for lack of scattering from neighboring exposures. right) Layout data with proximity correction for Au. The dose in the center of the structures is blue-ish (dose factor 1.1), the corner areas are green-yellow (dose factor 1.3). The dose correction is less important, because the Au layer's backscattering contribution is much higher. (Scalebar=2μm, colorbar from blue to red, dose factor 1 to 1.5).*

Au have been extracted earlier and are 52 and 42μC/cm^2, respectively. In fig. B.26, the Si substrate sample with dose 40μC/cm^2 the uncorrected structure is not developed, while the one corrected for Si is. The clearance dose for the Si substrate reveals the uncorrected structure only at seemingly too high dose of 80μC/cm^2 (cf. fig. B.38). In fig. B.28, the Au substrate sample with dose 40μC/cm^2 the uncorrected structure is not developed, but the wide rectangles (0.5μm) in the lower row start to be distinguishable. The clearance dose for the Au substrate reveals the uncorrected structure only at the expected dose of 50μC/cm^2 (cf. fig. B.29). The proximity correction parameters seem to be correctly chosen for Au. It is suspected that the clearance dose determination for Si (cf. fig. B.15) did not have enough data points to yield a correct value, which falsifies the result for the proximity corrected results.

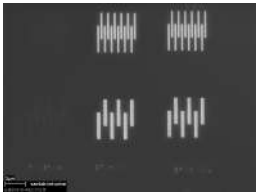

Figure B.26: *Si* $40\mu C/cm^2$

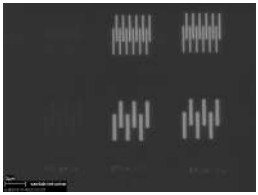

Figure B.27: *Ti* $40\mu C/cm^2$

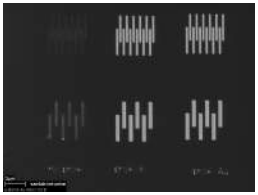

Figure B.28: *Au* $40\mu C/cm^2$

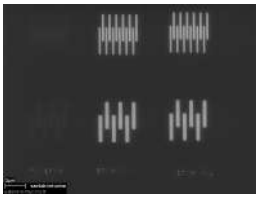

Figure B.29: *Si* $50\mu C/cm^2$

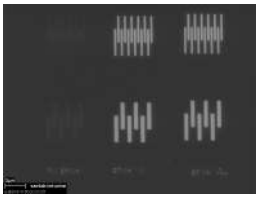

Figure B.30: *Ti* $50\mu C/cm^2$

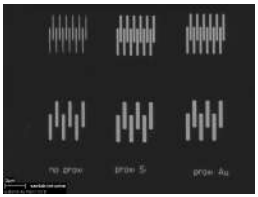

Figure B.31: *Au* $50\mu C/cm^2$

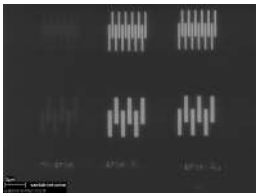

Figure B.32: *Si* $60\mu C/cm^2$

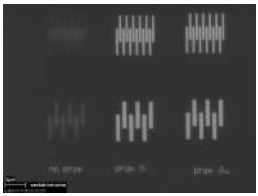

Figure B.33: *Ti* $60\mu C/cm^2$

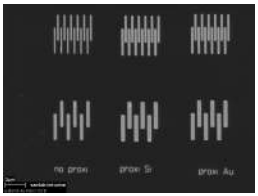

Figure B.34: *Au* $60\mu C/cm^2$

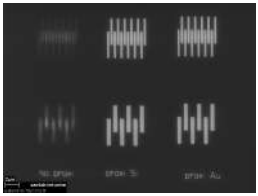

Figure B.35: *Si* $70\mu C/cm^2$

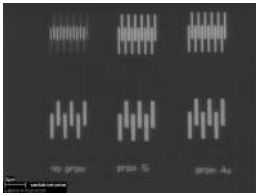

Figure B.36: *Ti* $70\mu C/cm^2$

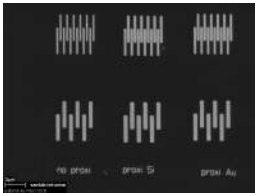

Figure B.37: *Au* $70\mu C/cm^2$

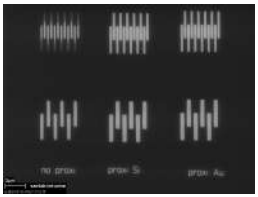

Figure B.38: *Si* $80\mu C/cm^2$

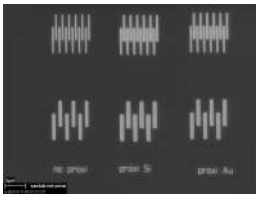

Figure B.39: *Ti* $80\mu C/cm^2$

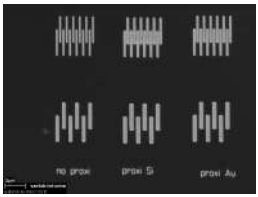

Figure B.40: *Au* $80\mu C/cm^2$

B.4 Conclusion

Clearance doses and scattering parameters were gathered, and used in an exposure to correct for proximity effect.

Acronyms

2DEG	two dimensional electron gas
AFM	atomic force microscope
Al-etch	Aluminum etchant (mixture of $H_3PO_4/HNO_3/CH_3COOH$)
BHF	buffered hydrofluoric acid
BOX	buried oxide layer
calixarene	calixarene hexaacetate p-methylcalix[6]arene
CB	Coulomb blockade
CDM	charged device model
CD	compact disc
CGPM	Conférence Générale des Poids et Mesures
CIPM	Comité International des Poids et Mesures
CMOS	complementary metal-oxide-semiconductor
CMP	chemical mechanical polishing
CSEM	Swiss Center for Electronics and Microtechnology
CVD	chemical vapor desposition
DI	deionized water
DNQ	diazonaphthoquinone
DRIE	deep reactive ion etching

DUV	deep ultraviolet
DVD	digital versatile disc
ε_0	permettivity of vacuum, $\varepsilon_0 = 8.8542 \times 10^{-12} A \cdot s \cdot V^{-1} \cdot m^{-1}$
EBID	electron beam induced desposition
ESD	electrostatic discharge
ETHZ	Swiss Institute of Technology Zurich
FCDM	field induced charge device model
$\mathbf{H_3PO_4}$	phosphoric acid
HBM	human body model
HSQ	hydrogen silsesquioxane
IPA	isopropanol
IR	infrared
k_B	Boltzmann constant, $k_B = 1.3807 \times 10^{-23} J \cdot K^-1$
KOH	potassium hydroxide
LB	Landauer-Büttiker
LAO	local anodic oxidation
LP	long play
LPCVD	low pressure chemical vapor deposition
MAA	methyacrylic acid
MBE	molecular beam epitaxy
MIBK	methyl isobytil ketone
MMA	methyl-methacrylate
MOCVD	metal organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field-effect transistor
PECVD	plasma enhanced chemical vapor deposition

PGMEA propylene glycol monomethyl ether acetate ($C_6H_{12}O_3$)

PMMA poly(methyl-methacrylate)

QPC quantum point contact

RIE reactive ion etching

SEM scanning electron microscope

SET single electron transistor

SI Système International d'Unités

SINIS superconductor-insulator-normal conductor-insulator--superconductor

SISIS superconductor-insulator-superconductor-insulator--superconductor

SOI silicon on insulator

SPM scanning probe microscope

SQUID superconducting quantum interference device

SSET scanning single electron transistor

STM scanning tunneling microscope

TF tuning fork

TLA three letter acronym

UniNE University of Neuchâtel

UV ultraviolet

ZEP poly(methyl-α-chloroacrylate-co-α-methylstyrene)

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Publications

T. Akiyama, K. Suter, N. F. de Rooij, A. Baumgartner, A. E. Gildemeister, T. Ihn, K. Ensslin, U. Staufer: *Scanning probe with tuning fork sensor, microfabricated silicon cantilever and conductive tip for microscopy at cryogenic temperature*, Jpn. J. Appl. Phys. **45** (2006), 1992.

Kaspar Suter, Terunobu Akiyama, Nicolaas F. de Rooij, Andreas Baumgartner, Thomas Ihn, Klaus Ensslin and Urs Staufer: *Tuning Fork AFM with Conductive Cantilever*, AIP Conf. Proc **696(1)** (2003), 227.

Kaspar Suter and Terunobu Akiyama and Nicolaas F. de Rooij and Urs Staufer: *Local Oxidation of Titanium Using Dynamic-Mode Tuning-Fork Probe with Microfabricated Silicon Cantilever*, Jpn. J. Appl. Phys., **45** (2006), 2099–2102.

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Biography

Kaspar Suter received his M.S. in Microengineering from the Swiss Federal Institute of Technology in Lausanne, where he studied from 1987 through 1992.

He was hired in 1992 as a contract engineer working on Microcontroller (HC05, HC11) IC Design for Motorola, Semiconductor Products Sector in Geneva, Switzerland, which he subsequently joined in 1993 working as a CAD engineer.

In 1996 he transferred to the Motorola subsidiary "Pico Design" in Sunnyvale, CA, USA, working as Senior CAD Engineer.

From 1998 to 2001, he worked for Cadence Design Systems, San Jose, CA, USA, on physical verification products Dracula, Vampire, Diva and Assura, occupying roles ranging from Application Engineer in a Sales Core Competency Group, Methodology Engineer in Services, to Product Engineer in R&D.

Since 2002, he is pursuing a Ph.D. degree, working on the fabrication of a scanning single electron transistor, in the Nanotools group of Professor Urs Staufer at the Sensors, Actuators and Microsystems Laboratory (SAMLAB) of Professor Nico De Rooij at the Institute of Microtechnology (IMT) at the University of Neuchâtel, Switzerland.

He lives a quiet and quite enjoyable private life with other amazingly primitive ape-descended life forms, at a non-disclosed location on an utterly insignificant little blue green planet orbiting a small unregarded yellow sun, far out in the uncharted backwaters of the unfashionable end of the western spiral arm of the galaxy[252].

Colophon

Content written with vim 7.0, an improved version of the vi editor distributed with Unix systems. vi was designed to be a full screen editor that worked on a terminal connected over a 300 baud modem to a computer. It was a world that is now extinct. Used because it does one thing well, moving around in the documents doesn't require the hands to leave the home row keys, and the buffer can be passed through any shell command.

Document produced with the MiKTEX 2.6 implementation of the typesetting system TEX. LATEX is an interface to the fully programmable TEX system, a set of higher level macros and constructs which facilitate typesetting, providing a document markup language and document preparation system. LATEX cannot be compared with "what you see is what you get" (WYSIWYG) type word processors, such as the currently marketwise predominant package called Word, because the two don't do the same job.

During the typing of this document no thoughts have been given to what what typically drives users of WYSIWYG editors to tears, when two days before the deadline, an apparently benign property adjustment induces a cascade of obscure formatting errors, problems with styles, mathematical formulae and equation writing, page numbering, figure, equation and table numbering, figure, equation, table referencing throughout the text, bibliography referencing, generation of table of contents, list of figures, list of tables, indexing and index generation, figure floating and caption insertion and placement, etc. . These structural tasks should be done by the tool, not by a sleep deprived frantic author. LATEX allows to worry about content and structure, and to forget about typesetting. My biased opinion is that LATEX is typographically unequalled by any other tool. LATEX is not for everybody, but it could be for you.

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and softwares used were: `pdftex` for direct pdf output, `graphicx` for including of jpg, png and pdf graphics, `amsmath` for typesetting equations, `makeidx` for index generation, `fancyhdr` for the page headers, `acronym` for acronym management and glossary generation. Helpful for draft version with explicit annotations are `layouts` to move around textbody and margins, `showkeys` to intext overlay used references of any type, `eso-pic` for watermark insertion. Bibliographical references managed with JabRef 2.2, an open source application running on a Java VM, using BibTeX as native file format. Many small and simple drawing were coded *inline* with TikZ (TikZ ist kein Zeichenprogramm) a syntax layer to PGF (portable graphics format), which defines a number of TeX commands that draw graphics. Three dimensional wireframe figures done with Fig4TeX a set of TeX macros designed to create a figure at compilation time of the TeX document, and to write text on it. Images, photos and pictures manipulated with the gimp 2.2, the GNU image manipulation program, or CorelDraw X3, or Irfanview.