

**SYNCHRONOUS AND ASYNCHRONOUS
DETECTION OF ULTRA-LOW LIGHT LEVELS
USING
CMOS-COMPATIBLE SEMICONDUCTOR
TECHNOLOGIES**

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presented by
CHRISTIAN LOTTO
born April 12 1979
christian.lotto@a3.epfl.ch

Examiners:

Prof. Dr. PETER SEITZ, examiner
Prof. Dr. EDOARDO CHARBON, co-examiner
Prof. Dr. CHRISTIAN ENZ, co-examiner
Prof. Dr. PIERRE-ANDRÉ FARINE, co-examiner

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Synchronous and Asynchronous Detection of Ultra-Low Light Levels Using CMOS-Compatible Semiconductor Technologies

Christian LOTTO

UNIVERSITE DE NEUCHATEL

FACULTE DES SCIENCES

La Faculté des sciences de l'Université de Neuchâtel,
sur le rapport des membres du jury

P. Seitz (IMT-UniNe, directeur de thèse), P.-A. Farine (IMT-UniNe),
E. Charbon (TU-Delft, EPFL) et C. Enz (CSEM, EPFL)

autorise l'impression de la présente thèse.

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Le doyen :
F. Kessler

Abstract

This work presents significant improvements of noise performance in synchronous CMOS image sensors and in asynchronous energy-sensitive single-photon X-ray imaging systems.

A detailed analysis of synchronous CMOS low-noise image sensors using conventional architectures reveals room for potential noise performance improvements, namely noise in switched-capacitor column-parallel amplifiers as well as imperfections in the low-pass filtering properties provided by such switched-capacitor amplifiers.

A novel low-noise CMOS image sensor topology with pixel-level open-loop voltage amplification alleviates the identified issues to a large extent. An image sensor based on this concept has been designed and fabricated. Characterization shows that the image sensor achieves a readout noise equivalent charge below 0.9 electrons and an overall noise floor as low as 1.4 electrons including photodiode leakage shot noise at an exposure time of 1/60 s. Performance parameters that are potentially compromised due to the use of open-loop amplification, such as linearity and photoresponse non-uniformity, are shown to be absolutely competitive with conventional image sensors thanks to an advantageous feedback configuration for the sense node reset. Implementations of the presented topology are simple and elegant circuits requiring generally less silicon area in the periphery of the pixel field and less power consumption than conventional architectures.

A second novel low-noise CMOS image sensor topology combining conventional pixel-level source-followers with column-level open-loop degenerate common-source amplifiers is proposed. This architecture provides an attractive combination of very low sense node capacitance, flawless low-pass filtering of noise from the pixel-level electronics by the use of column-level open-loop amplification, and advantageous noise performance of open-loop degenerate common-source amplifiers in comparison to OTA based switched-capacitor amplifiers. Theory, circuit simulation, and measurement of implemented test circuits indicate that image sensors based on this advantageous topology can potentially outperform the noise performance not only of conventional image

sensor architectures but even of the presented topology using pixel-level voltage amplification.

Analysis of charge-sensitive amplifiers (CSA), as used in conventional asynchronous single particle and high-energy photon detectors, explains the need for a sensing device with low capacitance in order to achieve good noise performance at reasonable power consumption. For instance, photogates or buried photodiodes in combination with a scintillator layer are sensing devices for X-rays with a very low capacitance.

A novel charge pulse detecting circuit using a source-follower buffer plus a band-pass filter instead of a CSA with a band-pass filter is presented in this thesis. In the case of low sensing device capacitance, comparison of this circuit vs. CSAs shows that the trade-off between noise and power consumption is systematically advantageous in favor of the presented buffered charge pulse detecting circuit. A test structure implementation of a buffered charge pulse detecting circuit in conjunction with a lateral drift field photogate has achieved an equivalent noise charge of 12 electrons. This excellent noise performance will allow X-ray single-photon imaging with very low detection threshold and excellent energy resolution.

This work contributes to further progress in cutting-edge noise performance of asynchronous single-photon X-ray image sensors and of synchronous low-light CMOS image sensors. Thanks to their extremely low thermal noise, the presented novel topologies of synchronous CMOS image sensors will experience an immediate further improvement of noise performance in case of future progress in process technology either leading to reduced dark current of buried photodiodes or to a lower flicker noise power spectral density.

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Chapter 1

Introduction

Over the past decade, electronic imaging devices, and in particular CMOS image sensors, have found an increasing number of applications in a wide variety of disciplines and are omnipresent in our daily lives. Certain applications of image sensors require very high sensitivity, i.e. image sensors with very low light detection limits. Some of the most demanding missions in terms of sensitivity are found in the fields of industrial machine vision, security and surveillance systems, space, scientific, and medical imaging, such as live cell microscopy, biochip reading and detection of single fluorescent molecules.

The capability to detect very low amounts of light is either limited by noise generation in the detector system, i.e. the image sensor, or by noise already included in the optical signal. Since detection of light by using semiconductor devices is not the most obvious concept, a more intuitive analogy is drawn in the context of this introduction.

Synchronous measurement of light is, in many aspects, similar to measuring the rate of rainfall by collecting raindrops in a water bucket during a set time interval and subsequent measurement of the accumulated water level using a ruler. To represent the sensor's noise in this analogy, the water in the bucket is assumed to be boiling. The mechanical fluctuation of the boiling water, in analogy to thermal agitation of electrons in the sensor, results in a finite limited accuracy of the water level measurement. Additionally, in analogy to leakage current of an image sensor, evaporation of the water introduces a measurement inaccuracy which increases with the duration of the measurement interval.

Besides the noise of the measurement system, an additional noise component is already contained within the signal to be detected for two reasons. First of all, rain is not a continuous flow of water, but a series of raindrops of finite size. Secondly, the raindrops hitting the surface of the measurement bucket arrive erratically rather than in a set rhythm. In other words, the sound of the rain impacting in the measurement bucket sounds like noise rather than the

ticking of a watch. Due to this discrete nature of the raindrops and their erratic arrival times, a random variation of the exact number of raindrops hitting the bucket within a set time is observed. Just like the rain in our example, the nature of light is quantized and, in most cases, the arrival of light quanta, called *photons*, is erratic. The random component of the signal of photons observed within a set interval is called *photon shot noise*. Considering these aspects of the nature of light, the ultimate goal in synchronous light measurement is obviously single-photon resolution imaging or, in our analogy, a measurement accuracy of a single raindrop.

If the signal light is not situated in the visible range of the spectrum but in the range of higher energies, such as X-radiation, it can be possible and highly desirable to go even further than detecting single X-ray photons. The next step is the additional determination of the photon *energy*. This method is called energy-sensitive single-photon imaging. Returning a last time to our analogy, X-ray photons correspond to very big raindrops and their energy corresponds to the volume of water contained within the raindrop. In order to determine a drop's volume, the chronometered approach is not suitable, since it would be impossible to determine whether an accumulated level of water over the chronometered period results from a low number of large drops or of a high number of small drops. To tackle the problem, continuous observation of the water level, detection of any significant level change, and immediate measurement of the level change are required. Note that the described method is an *asynchronous* measurement, as it is triggered by the photon detection event itself rather than an externally applied chronometering interval.

Despite the fact that a larger signal per photon is detected in the case of X-rays than in the case of visible-light photons, improvement in the sensor's noise is still highly desirable. The reason for this is that reduction of the measurement system's noise lowers the threshold of minimum photon energy required for successful photon detection and improves the accuracy of the energy measurement. As a consequence of reduced image sensor noise, the performance of many applications of energy-sensitive single-photon X-ray imaging is enhanced. Depending on the application, this can either be due to a more precise distinction between irrelevant and relevant X-ray photons selected according to the criterion of their energy, or due to a more precise determination of the information contained in the photon's energy. As a highly appreciated consequence, lower radiation doses can be used for medical X-ray imaging, or material inspection systems or security scanners may determine the composition of scanned samples more accurately.

Detector circuit design for low-noise synchronous image sensors, in particular CMOS image sensors, as well as for asynchronous energy-sensitive single-photon X-ray imaging has been researched intensely in the past. As a result, commonly used state-of-the-art circuit topologies have been established in both

fields. Intense research activity in the field of enhanced semiconductor process technology for low-noise image sensors, e.g. for reduced flicker noise or lower photodiode leakage, is currently ongoing. However, electronic noise in detector circuits, including thermal noise, remains a significant, in many cases predominant, component of the overall noise of state-of-the-art image sensors.

In the context of this thesis, the electronic noise performance of state-of-the-art synchronous CMOS image sensors, as well as asynchronous single-photon energy-sensitive X-ray image sensors has been reviewed, and circuit design methods have been used in order to achieve further reductions in electronic noise when compared to state-of-the-art detector circuits. As a result, the novel detector topologies and architectures presented in this thesis define the current cutting edge of noise performance while using simple and elegant circuits with competitive or even advantageous power consumption and silicon area expenditure.

The noise performance of the proposed topologies of synchronous CMOS image sensors is limited by flicker noise of one single transistor in the signal processing chain as well as leakage current of the employed buried photodiodes. Future advances in process technology leading to improvement in flicker noise power spectral density or reduction in diode leakage current density will result in an immediate improvement of the overall noise performance of these novel image sensor topologies thanks to their extremely low thermal noise components.

This thesis is organized in two parts. The first part, spanning from chapter 2 to 4, is dedicated to the topic of *synchronous* CMOS image sensors. Chapter 2 gives an overview of the state of the art in low-noise CMOS image sensors and an analytical discussion of electronic noise in CMOS image sensors. Chapter 3 introduces a novel topology of ultra-low-noise CMOS image sensor based on pixel-level open-loop amplification and discusses the results from characterization of an implemented image sensor employing this concept. Chapter 4 describes an alternative novel architecture for ultra-low-noise CMOS image sensors using conventional source-follower based pixel circuits in conjunction with column-level open-loop degenerate common-source amplifiers. The implementation of test structures using this concept and their characterization is discussed in the same chapter.

The second part of this thesis consisting of chapters 5 and 6 covers the topic of *asynchronous* energy-sensitive single-photon imaging. An introduction to the topic as well as a discussion of established detector circuit topologies is provided in chapter 5. Finally, chapter 6 introduces a novel detector circuit topology based on a buffer in conjunction with a shaper circuit. Besides circuit analysis, characterization results from an implemented test structure of the proposed circuit are presented.

Chapter 2

Low-Noise CMOS Image Sensors

2.1 Introduction

Electronic Imaging Devices have experienced a strong increase of their production volume over the past decades. Besides the growing number of used devices, a broadening of the field of applications has been observed. On one hand, reduced manufacturing cost has led to embedding of electronic imaging devices in low-cost high-volume products such as mobile phones. On the other hand, performance improvement of electronic imaging devices has led to their use in cutting-edge applications or has even enabled new applications. Many existing and emerging applications require or benefit from increased light sensitivity. The ultimate limit in terms of sensitivity, defined by the quantized nature of light, is imaging with single-photon resolution. This resolution limit is currently approached by semiconductor sensors to a degree which depends on the type of image sensor and on accepted compromises on other performance parameters. Charge-Coupled Devices (CCD), for instance, can achieve single-photon resolution in case of operation at very low data rates. Single-photon avalanche diodes (SPAD) achieve single-photon resolution, which is inherent to their operating principle. Detection probability lower than 100% and low fill factor, however, impose some limitations on the light sensitivity. CMOS Image Sensors, i.e. image sensors fabricated by Complementary Metal-Oxide-Semiconductor processes, are very interesting devices for high-sensitivity applications, since they combine resolution of nearly one photo-electron and high fill factor at decent quantum efficiencies. Besides the resulting very high sensitivity, CMOS imagers can generally be operated at higher data rates than CDDs without excessive impact on noise performance.

Optimization of sensitivity in CMOS image sensors has established a commonly adopted architecture making use of buried photodiodes, rolling shutter operation, Correlated Double Sampling (CDS) and column-parallel voltage amplification. In most implementations of this architecture, electronic noise of the source-follower transistor of the pixel circuit as well as of column-parallel processing circuit defines the sensitivity limit. Analysis indicates room for improvement concerning thermal noise of the mentioned source-follower transistor and the impact of thermal noise in the column-parallel processing circuit.

The current chapter is organized as follows: Sect. 2.2 provides an overview over the most common and interesting types of low-noise images sensors, Sect. 2.3 discusses noise sources encountered in semiconductor sensor based imaging techniques, Sect. 2.4 introduces the generic architecture of low-noise CMOS image sensors, and Sect. 2.5 develops quantitative noise analysis of such sensors.

2.2 Synchronous Semiconductor Image Sensors

Semiconductor Image Sensors generally rely on the photoelectric effect, i.e. on generation of charge carriers by absorption of photons in a semiconductor material, and the direct or indirect detection of the generated charge carriers. Synchronous Image Sensors are clocked integrated circuits comprising a two-dimensional array of pixel circuits. Each pixel circuit accumulates photon detection information over a clock period, outputs the accumulated result at the end of the clock period, and resets its accumulated information before the start of the next clock period. The output of each pixel is, therefore, a representation of the mean light intensity on the pixel over the past clock period. Consequently a synchronous semiconductor image sensor is able to produce a stream of intensity images available at periodic intervals, i.e. at a known and controlled *frame rate*.

The following three subsections provide a very short introduction to three very interesting and popular families of semiconductor image sensors for synchronous high-sensitivity imaging and their respective properties.

2.2.1 Charge-Coupled Devices

In CCDs every pixel contains a Metal-Oxide-Semiconductor (MOS) Capacitor with an optically transparent top electrode. This electrode's bias voltage is set to deplete the semiconductor under the oxide during an exposure period. Electron-hole pairs generated by photon absorption are separated in the field of the depletion zone. The signal carriers, usually electrons, are confined and

accumulated at the semiconductor-oxide interface¹. During a readout sequence following each exposure period, signal charge packets accumulated in the pixels are transferred from pixel to pixel at the semiconductor-oxide interface of adjacent MOS capacitors of neighboring pixels. The transfer is achieved by application of a clocked pattern of gate voltages which results in a clocked pattern of varying potentials at the semiconductor surface. The clocked gate voltage pattern is chosen in order to systematically shift signal charge along columns of pixels. At the edge of the pixel array, signal charge of the columns enters another arrangement of adjacent MOS structures, a so called-horizontal CCD shift register. The horizontal shift register is clocked at a higher clock frequency than the columns of the CCD pixel field. In fact, during one clock cycle of the pixel array CCD the horizontal CCD register serially transfers one charge packet per column onto a sense node at its end. The sense node of a CCD is one terminal of a reverse biased p-n junction diode which is left electrically insulated (floating) when a charge packet is transferred from the horizontal shift register. At each charge transfer, a sense node voltage change depending on the signal charge amount is thus observed. Between two charge transfer operations, the sense node is connected to a reference potential (reset potential) by a reset switch. The signal charge is, therefore, removed at every clock cycle and the sense node p-n junction always stays reverse biased. A source-follower's gate input is connected to the sense node and drives a buffered representation of the sense node voltage on an output pad of the CCD chip. Usually, the output voltage after resetting of the sense node, i.e. the reset level, and the output voltage after charge transfer onto the sense node, i.e. the signal level, are sampled for each charge packet. Subtraction of the reset level from the signal results in elimination of reset noise. This procedure is called correlated double sampling.

CCDs are fabricated using dedicated fabrication processes with optimized substrate dopings and large gate oxide thickness. Therefore, they withstand high gate voltages required for successful operation and high charge handling ability per pixel even at small pixel area. The use of a dedicated process also implies increased manufacturing cost. Furthermore, pure CCD processes are not very suitable for implementation of analog or digital integrated circuits. Besides the output source-followers and sense node reset transistors, CCD chips thus do not contain any additional integrated electronic functionality.

The virtual absence of analog electronic circuits in the signal chain of CCD image sensors has two effects. On one hand, electronic noise of CCDs can be very low, since reset noise can be canceled easily by application of CDS, and the noise of the only remaining source of electronic noise, i.e. the on-chip source-follower, can be optimized quite easily. On the other hand, the absence

¹In so-called buried channel CCDs the signal electrons are confined to a depth of minimum electron potential energy situated in the bulk of the semiconductor.

of chip-level analog electronics also implies absence of voltage amplification, given the fact that a source-follower circuit has approximately unity voltage gain. The chip-level conversion factor between signal charge and output voltage is, therefore, entirely defined, and usually limited to relatively low values, by the capacitance of the sense node. This means that noise of off-chip electronics used for further processing has an important impact on the input referred equivalent noise charge (ENC). For this reason, achievement of single-photon resolution with CCDs implies high complexity of discrete electronics design.

When it comes to low frame rates and high exposure times, CCDs are still a very interesting choice due to their very low values of leakage currents and consequently low leakage current shot noise.

Extensive coverage of CCDs is found, for instance, in [1] or [2].

2.2.2 Single-Photon Avalanche Diode Arrays

Single-Photon Avalanche Diodes (SPAD) provide a high-amplitude, easy to digitize voltage pulse at every photon detection event. They thus inherently achieve single-photon resolution and benefit from virtual absence of electronic noise, since the signal is converted to digital at the earliest stage of the processing chain.

Usually, SPADs are implemented as p-n or p-i-n photodiodes that are reverse biased beyond their breakdown voltage². For a relatively short time such a diode does not conduct any current, even if biased beyond breakdown voltage. Absorption of a photon in the depleted zone creates an electron-hole pair. These two primary charge carriers will drift in opposite directions in the electric field of the depletion zone. Since the junction is reverse biased at a high voltage, the avalanche effect will take place. This means that the created hole and electron will be accelerated in the electric field of the depletion zone to a sufficient kinetic energy for creating further electron-hole pairs by impact ionization. These carriers will themselves be accelerated and create further secondary carriers. Since the junction is biased beyond breakdown voltage, the generation rate is higher than the collection rate at the anode and cathode terminals of the diode [3]. If the bias voltage would be maintained beyond breakdown voltage, virtually infinite diode current would be the consequence of a single absorbed photon. SPADs are commonly used in conjunction with an active or passive quenching circuit, which temporarily lowers the bias voltage below breakdown voltage in order to stop the avalanche as soon as a certain diode current is exceeded [4].

Additionally a comparator, which may even be part of the quenching circuit, is most commonly used with SPADs in order to provide a digital pulse for each avalanche detection.

²This regime is also referred to as Geiger mode.

SPADs are, in their nature, asynchronous detectors without any memory functionality. In other words, they do not accumulate and store photon-detection information in the detector element, as opposed to CCDs for instance, that accumulate generated charge in the MOS capacitor of each pixel. A synchronous intensity-mode image sensor is obtained by combining a SPAD with a comparator and a periodically reset digital counter [5]. In two-dimensional SPAD arrays, the digital counter can either be shared by a column of pixels or be implemented on pixel level. In the first case [6] the rows of the array need to be scanned, which leads to poor frame-rates and short exposure times, as only one row is sensitive at a time. In the second case, implementation of the counter results in high transistor count per pixel, i.e. reduced fill factor [7], [8].

Thanks to their operating principle, SPADs perform virtually noise-free detection of single photons and, depending on the counter bus width, very high dynamic range. Due to detection probability lower than unity and low fill factor, their light sensitivity and responsivity is, however, significantly inferior to those of CCDs and CMOS image sensors in some cases. Photon detection probability typically ranges around 30% and fill factors span from a fraction of a percent to a few percent depending on pixel pitch, process technology, and the amount of circuitry implemented at pixel level [7], [9]. The pixel pitch of SPAD based image sensors is relatively high, i.e. in the range of several tens of micrometers, while maximum pixel count is significantly lower than in the case of CCDs and CMOS image sensors.

Despite the absence of electronic noise, SPADs are subject to random thermal generation of charge carriers in the semiconductor. The conceptual equivalent of dark current are dark counts in SPADs. Dark counts are avalanches triggered by a thermally generated electron-hole pair. Since the occurrence of dark counts is random, they give rise to a noise component which is equivalent to dark current shot noise.

SPAD arrays can be fabricated in CMOS fabrication processes, in particular those featuring extensions for high-voltage integrated circuits. Due to their fundamental difference in topology and operating principle they are not covered by the term "CMOS Image Sensor" in the scope of this work.

2.2.3 Synchronous Integrating CMOS Image Sensors

CMOS image sensors owe their name to the CMOS process technology used for their manufacturing. They contain a reverse biased or depleted photodiode per pixel, where signal charge is generated by photon absorption. Over the past decade buried photodiodes³ (BPD), as described in more detail in Sect. 2.4.1, have found increasing popularity for a wide variety of applications. The photodiodes of CMOS image sensors are able to accumulate and store generated

³Buried photodiodes are also referred to as pinned photodiodes.

charge carriers, i.e. they offer pixel-level analog memory functionality. Integrated signal charge is, however, not transferred outside the pixel for readout, as in the case of CCDs. Instead, the charge signal is converted into a voltage signal inside the pixel. An active buffer circuit contained in each pixel is able to reproduce this voltage signal with low impedance and to drive a shared column line, which is shared by all pixels in a column of a 2-dimensional pixel array. Image sensors comprising an active buffer per pixel are called active pixel sensors⁴ (APS).

In contrast to CCD technology, CMOS process technology allows for monolithic integration of complex analog and digital circuits in image sensors. Popular integrated functionality in CMOS image sensors are column-parallel signal amplification, column-parallel analog-to-digital conversion, analog and digital signal processing, and sensor control logic. The high density of CMOS circuits even allows for integration of fairly complex circuits in each pixel, a trend which has given rise to the term *smart pixel* [10]. So far, even the pixel-level integration of analog-to-digital converters (ADC) has been reported [11].

If no smart pixel functionality is required, the maximum pixel count of CMOS image sensors compares to that of CCDs and pixel pitch can be very low, e.g. as low as 1.1 μm [12]. For high-sensitivity sensors, which are the focus of this work, pixel pitch is somewhat larger, but still significantly lower than in SPAD arrays, e.g. in the range of 4 - 12 μm .

Fill factor (FF), quantum efficiency (QE), as well as leakage current values of CMOS image sensors are nowadays approaching the performance parameters of CCDs. A recent trend towards backside illuminated CMOS image sensors has resulted in a performance alignment with backside illuminated CCDs at 100% fill factor and very good quantum efficiency [13], [14], [15].

For the comparison of electronic noise in CMOS image sensors and CCDs two effects have to be considered. On one hand, the only source of electronic noise in CCDs is the output source-follower whereas CMOS image sensors contain more analog integrated circuits, which generate possibly higher noise if not optimized carefully. On the other hand, CMOS image sensors can offer analog on-chip signal amplification, which leads to chip-level conversion factors significantly beyond those of CCDs resulting in reduced impact of board-level noise on the ENC of the sensor. In the more extreme case of CMOS sensors with on-chip ADCs, the impact of board-level noise is even virtually eliminated. For this reason and thanks to optimization of electronic noise of on-chip circuits CMOS image sensors reach or even outperform the noise performance of CCDs.

For the reason of low sensitivity to board-level noise as well as the high integration of functionality and the absence of high operating voltage, CMOS image sensors allow for low-complexity, low-power, and low-cost imaging system

design. These arguments are increasingly important even in the performance driven market of high-sensitivity, low-noise imaging.

2.3 Noise Sources in Semiconductor Sensor Based Imaging Techniques

Semiconductor sensor based imaging systems suffer from noise of various natures that affect the system at different stages. Statistical variation, i.e. photon shot noise, is present in the optical signal even before being detected by the imaging system. Photon shot noise is, therefore, the natural benchmark for an imaging system. If photon shot noise is the predominant noise source in an imaging system, the system operates at a physical performance limit and can be considered well-designed. The most important noise sources to be controlled in semiconductor image sensors are the leakage current shot noise of the sensing element, electronic noise of circuits used for chip-level and board-level signal processing, and possibly also quantization noise, if the system has a digitized output.

The following subsections describe the fundamental properties of the noise sources mentioned above. The specific impact of these noise sources on CMOS image sensors will be analyzed in Sect. 2.5.

2.3.1 Photon Shot Noise

Emission of photons by a light source is a statistical process. Photons are thus not emitted with periodic timing but in a random manner, which leads to a statistical variation of the number of emitted photons in a known time window, such as the integration period of an image sensor. The statistical description of the emission process obviously depends on its physical nature. Under realistic conditions, most major types of light sources exhibit photon statistics approximately following a Poisson distribution, as shown in [16]. It is also shown that absorption of photons and generation of signal charge carriers in semiconductor sensing devices is a binomial selection process with a fixed probability defined by the quantum efficiency. Charge carriers generated by Poisson distributed light, therefore, also follow a Poisson distribution. The variance is thus equal to the mean number of photogenerated charge carriers as expressed in (2.1).

$$q_{n,\text{photon}} = q\sqrt{n_{\text{pc}}} \quad . \quad (2.1)$$

⁴Nowadays virtually all CMOS image sensors are active pixel sensors.

In the above expression $q_{n,\text{photon}}$ is the root mean square (RMS) noise charge delivered by the sensing element due to photon shot noise, q is the elementary charge and n_{pc} is the mean number of photogenerated charge carriers.

This result shows that for a mean signal of one single photoelectron, an RMS shot noise of one electron is expected. Since the holy grail in low-noise imaging is shot-noise limited noise performance over the entire reasonable intensity range, i.e. down to a single photo-electron per exposure period, this result also defines the ambitious requirement of sub-electron input referred noise for the image sensor.

2.3.2 Leakage Current Shot Noise

Semiconductor devices are generally subject to charge leakage by thermal generation and recombination processes, also called dark noise. In silicon, the predominant mechanism of charge leakage is indirect generation-recombination via energy states in the semiconductor band [17]. The generation rate, i.e the leakage current of a depleted semiconductor volume, therefore, depends on the density of certain impurities in the semiconductor and can be expressed as a carrier lifetime [18]. Due to its mechanism of thermal generation, leakage current displays an exponential increase with temperature. It is also understandable, that the leakage charge, i.e. the integral of leakage current over a known time window, is subject to statistical variation due to the random occurrence of generation-recombination events. It can be shown, that the number of generated charge carriers in a defined time interval follows a Poisson distribution, very much like photons generated in a light source, which leads to the expression of (2.2) for the leakage variation, i.e. leakage shot noise.

$$q_{n,\text{leak}} = q\sqrt{n_{\text{leak}}} = \sqrt{q i_{\text{leak}} t_{\text{leak}}} \quad (2.2)$$

In this expression, $q_{n,\text{leak}}$ is the RMS noise charge due to leakage shot noise, n_{leak} is the mean number of thermally generated charge carriers over a time period t_{leak} , and i_{leak} is the leakage current. The above representation is very convenient for analysis of the leakage current integrated on a floating node. For analysis in a continuous-time circuit the following representation as a one-sided⁵ current noise power spectral density $S_{n,i,\text{leak}}^2$ is more convenient [19]:

⁵Unless stated otherwise, noise PSDs given in this thesis are considered one sided, i.e. their corresponding RMS noise is the square root of the PSD's integral from zero to infinity frequency

$$S_{n,i,\text{leak}}^2 = 2q i_{\text{leak}} \quad (2.3)$$

Leakage current shot noise theoretically affects every reverse-biased p-n junction of the electronic circuits of an imaging system. The impact of these contributions on the overall noise performance of the imaging system is, however, insignificant for well-designed systems. The only leakage shot noise components which usually have an important impact are the leakage shot noise of the sensing device and of storage nodes for photogenerated charge. For this reason, process technologies for semiconductor image sensors are highly optimized for low sensing device leakage. Given the strong temperature dependence of leakage, externally cooled image sensors are used for low-noise imaging applications with long exposure times and high pixel area, e.g. in astronomy imaging.

2.3.3 Electronic Circuit Noise

In the scope of this work, the term "electronic noise" shall refer to noise generated in electronic circuits used for signal readout and signal processing. As mentioned in the previous section, this noise might include a component of leakage current shot noise, which is negligible in most cases. The predominant components of noise in electronic circuits are thermal noise in transistors and resistors as well as low-frequency noise in MOS transistors.

Thermal Noise

Thermal noise in resistors describes a random voltage between the terminals of an isolated resistor or a random current flowing in a shorted resistor arising from random diffusive motion of charge carriers due to their thermal, i.e. kinetic, energy. Thermal noise is also referred to as Johnson-Nyquist noise and has a white spectrum. Modeling of thermal noise either as a noise voltage source in series with the resistor or as a noise current source in parallel with the resistor, as shown in Fig. 2.1, is convenient for the analysis of noise in complex circuits. The thermal noise voltage and current power spectral densities depend on the resistor value and are given in (2.4) and (2.5) respectively:

$$S_{nv,\text{thermal},r}^2 = 4kTR \quad (2.4)$$

and

$$S_{ni,thermal,r}^2 = \frac{4kT}{R}, \quad (2.5)$$

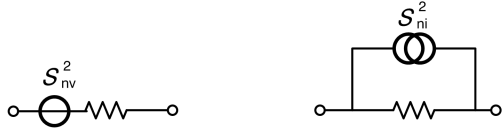


FIGURE 2.1 Modeling of thermal noise in a resistor as a series noise voltage (left) or as a parallel noise current (right)

where T is the absolute temperature, k is the Boltzmann constant, and R is the resistance. The above thermal noise expression, as found by Nyquist, can also be derived by consideration of Poisson statistics of charge carrier movement, similarly to the considerations of leakage current shot noise. To derive thermal noise in a resistor conducting zero average net current, thermal movement is modeled as two diffusion currents of opposite directions⁶. The consideration of Poisson statistics of these diffusion currents leads to the well known result of (2.5) [19].

Thermal noise is also generated in the channels of MOS transistors and, under some conditions, similar calculations apply. The most important difference with respect to consideration of thermal noise in a homogeneous fixed-value resistance is the fact that the inversion charge density varies from the source to the pinch-off point. Analysis of the integrated noise impact of a sum of infinitesimally small series connected resistor elements needs to be performed [20], since the amplitude of the noise source associated with each infinitesimal resistor element as well as the impact of this noise source both depend on the location along the channel. This analysis leads to the expressions of (2.6) and (2.7) for the thermal noise power spectral densities of a drain-source parallel noise current source or a noise voltage source in series with the gate connection of the MOS transistor, as illustrated in Fig. 2.2.

$$S_{ni,thermal,mos}^2 = 4kT\gamma g_m \quad (2.6)$$

⁶Note that diffusion actually corresponds to the process of random thermal movement in presence of a concentration gradient.

and

$$S_{nv,thermal,mos}^2 = \frac{4kT\gamma}{g_m}, \quad (2.7)$$

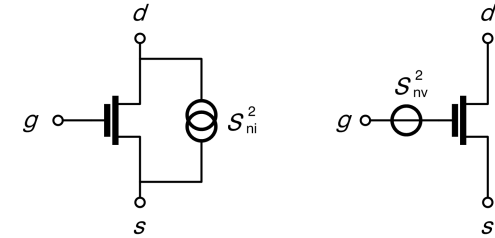


FIGURE 2.2 Modeling of noise in an MOS transistor as a drain-source current (left) or a gate voltage (right)

where g_m is the transconductance of the MOS transistor. The most important difference between the expressions for thermal noise in resistors and MOS transistor channels is the factor of γ . The theoretical analysis mentioned above suggests a value of $\gamma = 2n/3$ in the case of strongly inverted and saturated transistors, of $\gamma = n/2$ for weakly inverted and saturated transistors, and of $\gamma = n$ for transistors in triode region⁷ independently of their inversion state [20]. In these expressions, n is the slope factor of the transistor, which is usually close to unity.

The factor γ is, however, also used for modeling of excess noise and, therefore, is referred to as the *thermal excess noise factor*. While the above analytical results fit measurements with decent accuracy for long channel transistors, higher noise, i.e. higher values of the excess noise factor, is observed for short transistor channel length. For sub-micron transistor channel length the excess noise factor in strong inversion and saturation has been measured to be as high as $\gamma = 1.4$ to $\gamma = 7.9$ for $L = 0.7 \mu\text{m}$ [21]. Physical explanation and consistent modeling of excess noise is still under active research. Increases and decreases in γ have been shown to be due to carrier heating and mobility degradation, respectively [22]. It should be noted that both effects have an increasing impact with reduced channel length.

⁷The triode operation region is also referred to as linear region or conduction region.

Flicker Noise and Random Telegraph Signal Noise

Additionally to the flat spectrum of thermal noise, MOS transistors exhibit low-frequency noise, i.e. a noise component characterized by a noise power spectral density proportional to the inverse frequency. Inspired by its time domain behavior, this noise frequency component is called flicker noise, or, according to its spectral properties, pink noise or $1/f$ noise. The most important mechanism causing flicker noise is believed to be trapping and release of charge carriers at defects at the semiconductor-oxide interface⁸ of the MOS transistor resulting in a fluctuation of the number of mobile electrons in the channel. Flicker noise is most conveniently modeled as a noise source in series with the transistor gate connection. The most common quantitative expression of the flicker noise gate voltage power spectral density, as given in (2.8), is based on its empirical behavior [23].

$$S_{nv,flicker}^2 = \frac{K}{C_{ox}WL} \frac{1}{f}, \quad (2.8)$$

where f is the frequency, K is the flicker noise constant for a given process technology and transistor type, W is the gate width, L is the gate length, and C_{ox} is the gate oxide area density. Note that flicker noise is generally reduced with increasing gate area. This is explained to be due to the increasing averaging effect of trapping and releasing with the increasing number of traps and mobile charge carriers in the channel. Additionally flicker noise decreases with increasing gate oxide capacitance density. This effect can be understood by considering that the equivalent gate voltage required to compensate for a trapped charge carrier at the interface is inversely proportional to the gate oxide capacitance density.

According to the expression of (2.8) and the suggested theory of interface state trapping, flicker noise is independent of the gate-source voltage and transconductance. Depending on process technology and channel carrier type, there are, however, practical cases of flicker noise exhibiting significant voltage dependence [23], [24]. In this case, fluctuations of carrier mobility in the transistor channel or, if present, in the lightly doped drain zone (LDD) are believed to be the cause of flicker noise rather than free carrier number fluctuations.

Furthermore, flicker noise exhibits, in some cases, frequency behavior deviating from the $1/f$ behavior. Frequency dependency ranging from $1/f^{0.7}$ to $1/f^{1.2}$ has been reported. Various reasons, such as non-uniform spatial distribution of traps, could explain such behavior [24].

⁸The interface traps are also referred to as slow states.

The amount of flicker noise as well as the gate-source voltage and frequency dependence are reported to be different for n-type and p-type channel MOS transistors in a given process. The differences are not consistent for all processes. Very generally speaking p-channel transistors often have lower flicker noise and stronger gate-source voltage dependence than their n-channel counterparts. In some processes, this might be due to a p-type threshold adjusting implant used in the channel region of the p-channel transistors. Besides lowering the threshold voltage, this shallow implant also results in moving channel location, i.e. the minimum of hole potential energy, to a buried depth in the bulk, some distance away from the oxide-semiconductor interface. At this interface, where trap density is high due to surface defects, the semiconductor is permanently depleted and the trapping and release probability is consequently low.

A particular case of flicker noise is random telegraph signal (RTS) noise. As suggested by its name, RTS manifests itself by a temporal noise waveform displaying two distinct levels or, in other words, by the presence of two distinct peaks in the histogram of measured amplitude values [25]. This behavior is explained by a trapping and release process involving one single trap state. Therefore, RTS is more likely to be observed with transistors of small gate geometry. Compared to other noise sources, the impact of RTS noise shows a larger statistical spread between the samples of a group of transistors of identical design and operating point. This is understood when considering the huge impact of absence or presence of a single trap-state in a transistor. Furthermore the RTS noise power, i.e. the impact of a trap state, depends on the exact location between the source and the channel pinch-off point of the transistor as well as the characteristic trapping and release time constants. Considering this, it is not surprising, that the frequency dependence of RTS noise may significantly deviate from exact $1/f$ behavior and is possibly subject to transistor-to-transistor variation.

2.4 Low-Noise CMOS Image Sensor Architecture and Operation

Over the past decade, a standard architecture for low-noise CMOS image sensors commonly used in research and industry has emerged [26], [27], [28] [29]. The photoelectric sensing devices contained in the pixels of these sensors are buried photodiodes. The principal reason for this choice is the low leakage current density of buried photodiodes and their fully depleted integration site which allows for complete charge transfer onto an isolated sense node. This latter feature provides a high pixel-level conversion factor simultaneously with high responsivity and enables the use of a specific timing sequence for optimum

noise performance.

The key principle employed in such low-noise operating sequences is correlated double sampling (CDS) with short sampling time difference, which simultaneously cancels reset noise, reduces flicker noise of pixel-level electronics, and keeps the impact of sense node leakage low. CDS with a short sampling time difference naturally implies rolling shutter operation.

Another common feature of low-noise CMOS image sensors is column-parallel voltage amplification and the use of output multiplexing or analog-to-digital conversion after the amplification stage.

The set of architectural choices described above results in a fundamental architecture, as schematically illustrated in Fig. 2.3, common to most low-noise CMOS image sensors that have been recently reported. In such a sensor each pixel contains a buried photodiode with a transfer gate associated sense node diffusion, a select transistor M_{sel} , a source-follower transistor M_{sf} , and a reset transistor M_{res} ⁹. The latter is used to periodically connect the sense node for a short time to a fixed reset voltage V_{res} , i.e. to reset the sense node charge. For the majority of the time, the reset transistor is turned off and the sense node is floating. The source-follower transistor in conjunction with the column bias current source acts as a buffer which reproduces the sense node voltage on the column line col_i while conserving low sense node capacitance. This source-follower buffer is only active during pixel selection, i.e. when the select transistor M_{sel} of a pixel connects the distributed elements of the buffer being the pixel-level source-follower transistor and the column-wise shared bias current source.

Besides the bias current source, each column line is connected to a switched-capacitor voltage amplifier with embedded CDS functionality. The amplified column voltage signals of all columns are multiplexed to one or several analog output buffers driving the signal on one or several pins of the image sensor chip. Alternatively each column circuit slice may additionally contain an ADC converting the output of the column-level amplifier. In this case, the analog multiplexer is obviously replaced by a digital multiplexer and no analog output buffer is required. Commonly used architectures of column-level ADCs are single slope and dual slope ramp converters [26], [30], [31], successive approximation register converters [32], and cyclic converters [33]. More recently, the use of a $\Sigma - \Delta$ converter has been proposed [34].

Each pixel receives select transistor and reset transistor control signals sel_i and res_i as well as the transfer gate control signal tx_i used for triggering charge transfer from the active area of the buried photodiode to the sense node. These control signals are generated by a row decoder and are common to all pixels in the same row. Consequently, all pixels of a row are synchronized in their

⁹For the reason of its transistor number, this pixel topology is also referred to as 4-T Pixel.

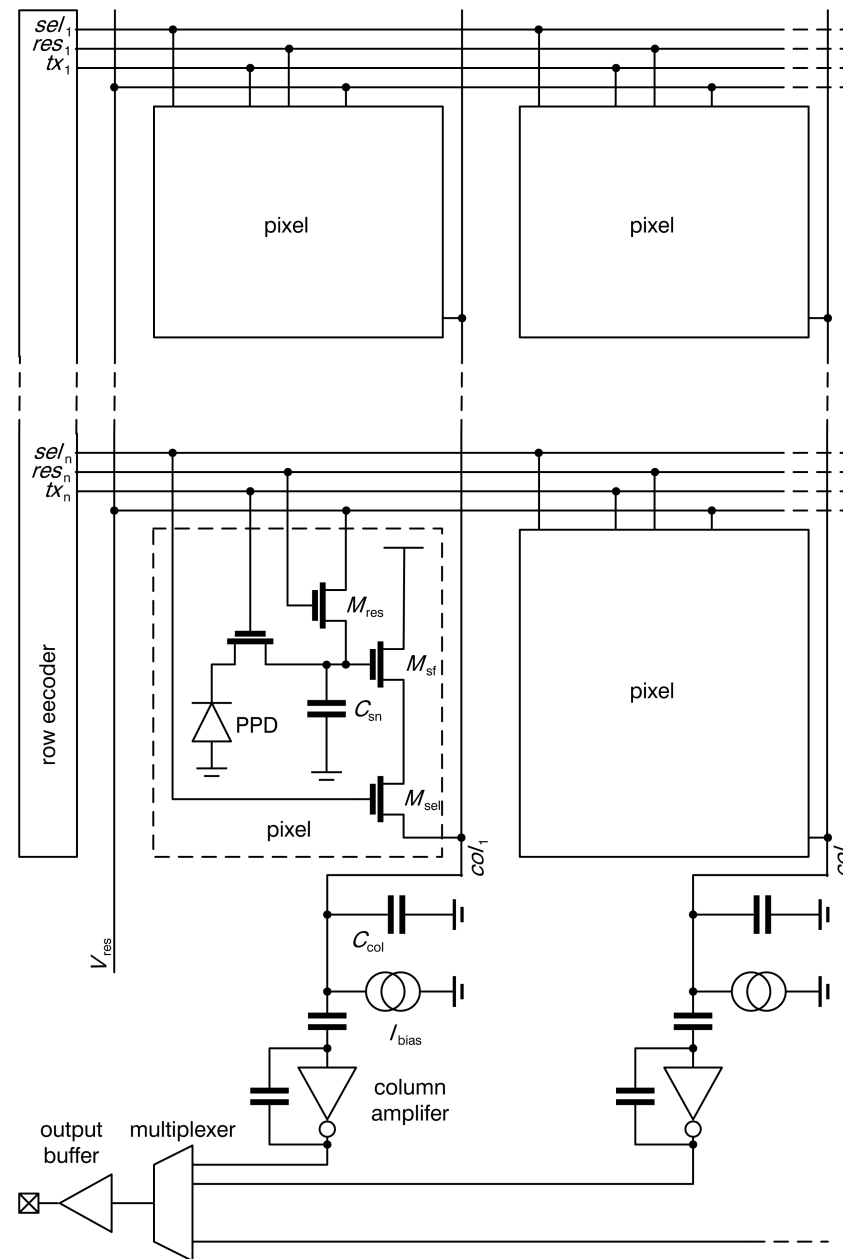


FIGURE 2.3 Schematic diagram of a state-of-the-art low-noise analog CMOS image sensor architecture

operation. Since the column bias current source and the column amplifier are shared amongst all pixels of a column, the select transistors of only one row can be activated at a time.

One possible solution respecting this criterion is the rolling shutter timing, as illustrated in Fig. 2.4. The select, reset, and transfer gate control signals are row-wise staggered. While a row of pixels is selected, their sense nodes are first reset to V_{Res} by a pulse of the reset transistor gate voltage. This procedure results in a random charge fluctuation of the sense node charge, which is frozen once the reset transistor is turned off. The sense node reset voltage and its random component called the reset noise are then reproduced on the column line by the source-follower. This time period is used for auto-zeroing of the column-parallel switched-capacitor amplifiers, i.e. the reset level is sampled and stored in the input capacitance of the column amplifier. In the next step, charge is transferred from the buried photodiode to the sense node by applying a pulse to the transfer gates of the selected row of pixels. The charge transferred to the sense node is the signal charge integrated in the buried photodiode since the charge transfer action of the previous image frame. The transfer of signal charge results in a change in the sense node voltage, which is reproduced on the column signal line by the source-follower. Since the column-level amplifier has been autozeroed during the presence of the reset level on the column line, the output of the amplifier will now settle to the amplified difference of the signal level and the reset level, i.e. to an amplifier output voltage proportional to the transferred signal charge. While this voltage is present on the column amplifier output, the analog multiplexer will sequentially connect all column amplifiers to the output buffer. All pixel signals of a row will, therefore, appear serially on the chip output.

The described row operation sequence is sequentially repeated row by row. The exposure periods of the different rows, as defined by the period between two consecutive charge transfer operations, are thus staggered. The exposure period duration T_{exp} is, however, constant for all rows.

Note that the sampling time difference between reset level sampling and signal level sampling is very short in comparison to the exposure time, typically of the order of magnitude of $T_{\text{Row}}/2$.

The transfer gates of all pixels of the array could theoretically be operated simultaneously in order to achieve global shutter operation, i.e. simultaneous exposure of all pixels in the array. For the reason of shared column circuitry, the readout would still need to be rolling. Therefore, the sampling time difference between sampling the reset level of a pixel, which must be sampled prior to the global charge transfer action, and the sampling of the signal level, which for the last row of the rolling readout sequence is delayed by the sequential readout time of all the previous rows, is relatively high. Such an increase in sampling time difference of correlated reset levels and signal levels would

lead to a significant increase in noise, as will be understood from the following subsections. Furthermore, correlated reset levels and signal levels, i.e. reset and signal levels containing identical frozen reset noise, would not be available on the shared column lines immediately following each other. This fact implies, that the analog subtraction of reset and signal levels in the column amplifier would not work any longer. In other words, reset levels would need to be read out of the chip, converted to digital and stored until the correlated signal becomes available¹⁰. Consequently, the required analog output bandwidth or, in case of an image sensor featuring on-chip analog-to-digital conversion, the required ADC conversion rate would be doubled.

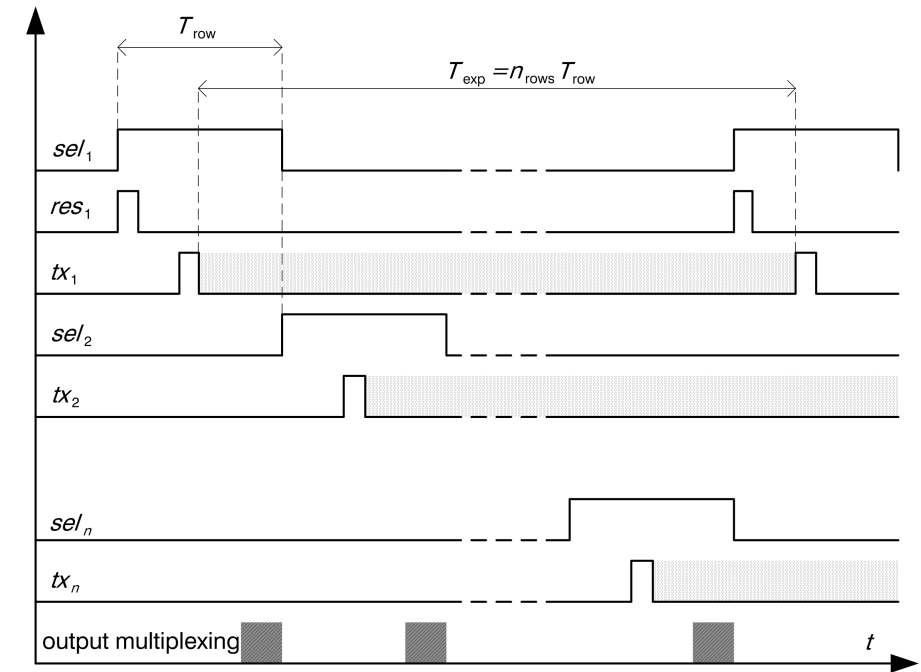


FIGURE 2.4 Timing diagram for rolling shutter operation of an active pixel sensor with buried photodiodes

The following three subsections will investigate different elements of the architecture introduced above with an emphasis on explaining low-noise aspect of this often adopted architecture.

¹⁰This method is referred to as Digital Correlated Double Sampling (DCDS)

2.4.1 Buried Photodiodes

Buried photodiodes (BPD) are sensing devices fabricated in CMOS technologies with an additional specific implants [35]. They have been inspired by buried channel CCDs (BCCD) and conceptually speaking, are the equivalent of the last CCD element of a BCCD row plus the sense node diffusion of a CCD sensor. Instead of the metal-oxide electrode employed in BCCDs, buried photodiodes make use of a shallow high-doping p-type surface implant. As illustrated in the cross-section of Fig. 2.5, the diode part of a BPD is an n-type implant in a p-type substrate with the p-type surface implant on top of it. A MOS-stack, called the *transfer gate*, is adjacent to the diode. On the opposite side of the transfer gate an n+ drain diffusion, called sense node diffusion, is implemented.

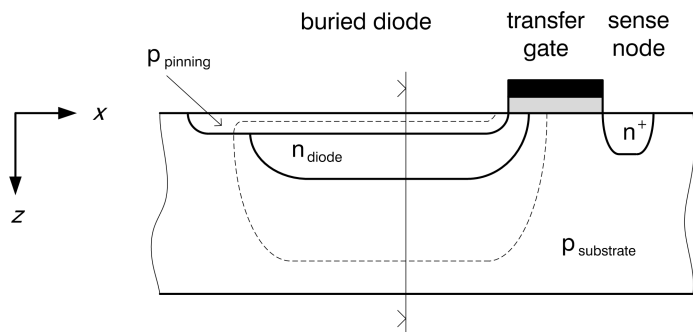


FIGURE 2.5 Cross-section and qualitative implant profile of a buried photodiode. The area inside the dashed line is completely depleted in absence of photo-generated charge

The doping concentrations of the substrate and the p-type surface layer as well as the implant depth and doping concentration of the n-type implant of the diode are chosen in order to achieve abutment of the depletion zones of the $p_{\text{pinning}} - n_{\text{diode}}$ and $p_{\text{substrate}} - n_{\text{diode}}$ junctions. As a result, the diode n-type implant zone is completely depleted as are adjacent portions of the surface implant and the substrate (cf. zone inside the dashed line in Fig. 2.5). The resulting space charge densities, the vertical field component, and the vertical evolution of the electron potential energy are illustrated qualitatively in Fig. 2.6. The vertical field and potential evolution indicates that separation of charge carriers created by photon absorption in the depletion zone will take place by electron drift towards a potential energy minimum $\Phi_{e,\text{min}}$ and hole drift to the substrate or the non-depleted portion of the surface implant.

Investigation of the lateral evolution of the minimum electron potential energy, which is found at a bulk location in the photodiode but at the semiconductor surface under the transfer gate, shows that a buried photodiode has

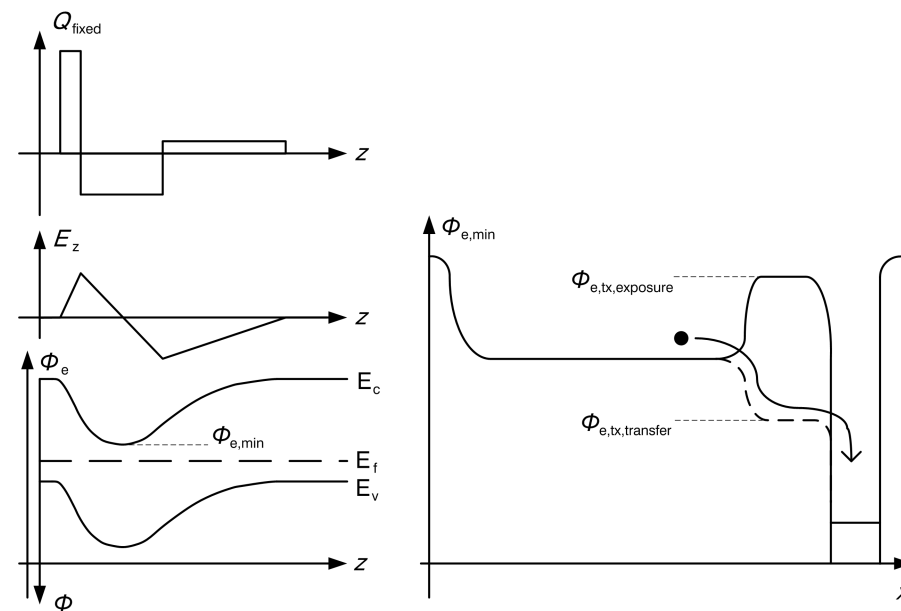


FIGURE 2.6 Left (from top to bottom): Qualitative vertical distribution of fixed space charge density, vertical field component, and band diagram. Right: horizontal distribution of the vertical minimum of free electron energy in exposure state and charge transfer state (dashed line)

two fundamental operation states depending on the gate voltage of the transfer gate. If a low voltage is applied to the transfer gate, the photodiode and the sense node are electrically isolated due to an electron potential energy barrier between them. In this state, called exposure state in the scope of this work, electrons created by photon absorption are integrated and stored in the photodiode. If, however, a high voltage is applied to the transfer gate, the energy barrier is removed and electrons can travel from the photodiode to the sense node. Due to the electron energy being higher in the photodiode than in the sense node, the net charge movement is directional towards the sense node. After sufficient time, all mobile electrons are transferred from the photodiode to the previously reset sense node. The electron transport mechanism in this charge transfer state is self-induced drift and diffusion for electron transport inside the photodiode portion up to the transfer gate, whereas drift in fringing fields is the predominant mechanism under the transfer gate.

It is important to point out that the described charge transfer is complete. This means, that the photodiode is reverted to a completely depleted state during charge transfer. The charge transfer action, therefore, corresponds to

a reset action of the BPD, which is not to be confused with reset of the sense node. Since no mobile charge is left in the BPD after charge transfer, no charge fluctuation at reset can occur. The BPD reset by charge transfer is, therefore, inherently noise-free.

A significant advantage of BPDs in comparison with conventional p-n photodiodes arises from the electrical isolation between the diode and the sense node in addition to the complete charge transfer ability. It is actually possible to design a relatively large photodiode while using a geometrically small sense node. This combination provides very high responsivity, since electrons absorbed in a large photodiode volume are converted to a high signal voltage on a sense node with low capacitance. Besides high responsivity, low sense node capacitance also helps achieving high sensitivity, since the sense node referred electronic noise *voltage* of the readout circuitry is converted back to a low input referred noise *charge*.

2.4.2 Correlated Double Sampling

The rolling shutter operating sequence described above implements correlated double sampling. The basic principle of this method is to cancel reset noise by exploiting its DC nature, i.e. the fact that reset noise remains frozen at a constant, but random, level once the reset operation has finished. As mentioned previously, the reset of the BPD by charge transfer is noise-free. This does, however, not hold true for the sense node. Resetting the sense node by turning on and off the reset transistor does leave a frozen random reset noise charge on the sense node, as will be explained in Sect. 2.5.2. Such a noise component $v_{n,res}$, which is constant over an entire readout cycle, can easily be canceled out by first sampling and storing the noise amplitude $V_{sn,r}$ and subtracting it from a second sample $V_{sn,s}$ containing the identical frozen noise component plus a signal component. The subtraction result ΔV_{sig} is the signal component not affected any longer by reset noise, as can be easily understood from (2.9).

$$\begin{aligned} \Delta V_{sig} &= V_{sn,s} - V_{sn,r} \\ &= (V_{res} + v_{n,res} + Q_{sig}/C_{sn}) - (V_{res} + v_{n,res}) \\ &= Q_{sig}/C_{sn} \quad . \end{aligned} \quad (2.9)$$

Despite the fact that a BPD based sensor still needs CDS for reset noise cancellation of the sense node, the noise-free photodiode reset is one of its most important advantages. Thanks to the noise-free photodiode reset and the possibility of complete charge transfer, a sense node reset level and a correlated

signal level, i.e. a signal level containing *identical* reset noise, can be established and sampled within a low sampling time difference. As opposed to conventional p-n photodiodes, which impose a sampling time difference at least as long as the exposure time, the reset level on the sense node of a BPD can be established and sampled a very short time before charge transfer while signal electrons have already been integrated in the buried photodiode.

The practical advantage of CDS with short sampling delay is the possibility of short-term analog reset level storage in a column-wise shared circuit, such as a sample-and-hold stage or an autozeroed switched-capacitor amplifier, since during the short delay between reset sampling and signal sampling the column-parallel circuit does not need to be used for readout of other rows. Note that this column-parallel analog CDS method is tightly linked to the use of a rolling shutter operating sequence.

Besides this practical advantage, CDS with short sampling delay has a beneficial effect on the impact of two different noise sources in CMOS image sensors.

First of all, the impact of sense node leakage current is improved with reduced CDS sampling time difference. This is due to the fact that the sense node leakage current only affects the charge measurement during the duration between the reset level sampling and the signal level sampling. The shorter the sampling time difference, the lower the integrated number of leaked electrons and hence the lower their shot-noise component. This aspect is of significant importance in BPD pixels, as the sense node leakage current density is usually more than an order of magnitude higher than the highly optimized photodiode leakage.

Secondly, CDS generally attenuates low-frequency noise. Qualitatively speaking, noise components varying more slowly than the sampling time difference are suppressed by the subtraction operation. This consideration illustrates that the attenuation of low-frequency noise, e.g. flicker noise, is improved with reduced CDS sampling time difference.

Independently of the sampling time difference, CDS suppresses any DC components and, most attractively, offsets affecting the signal up to the column-parallel circuit where CDS is performed. Dark fixed pattern noise (FPN), predominantly caused by threshold variation of the source-follower transistors, is therefore canceled by CDS. Note that this benefit is obviously not requiring correlation of the reset noise component of the subtracted samples and is therefore even achieved by non-correlated double data sampling (DDS) methods.

2.4.3 Column-Parallel Voltage Amplification

As illustrated in Fig. 2.3, the state-of-the-art low-noise CMOS image sensor architecture uses column-parallel voltage amplification.

While column-parallel *voltage amplification* might be an approach specific to low noise CMOS image sensors, general column-parallel signal processing or at least buffering is commonly used in any kind of modern CMOS video rate image sensor. The reason for this is basically the high analog bandwidth requirement for circuits used in video frame rate sensors which, due to high pixel number and moderate frame rates, require high pixel rates. Consider a CMOS image sensor without column-parallel circuitry. In such a sensor, the column lines would be fed to the input of an analog multiplexer that connects one column line at a time to the output buffer or alternatively to a chip-level ADC. The multiplexer would sequentially switch all the column lines to the output buffer within one single row time T_{ROW} , or in other words, every column signal line would be connected to the output buffer for a duration of $T_{\text{ROW}}/n_{\text{COL}}$, where n_{COL} is the number of columns multiplexed to one output buffer. Within this short period, the pixel-level source-follower would have to drive the reset level and the signal level on the column capacitance plus the load capacitance of the multiplexer and the buffer. Given typical values of column capacitance and a row time resulting from typical video frame rates and sensor array line numbers, the required transconductance of the source-follower would be very high. In order to reach this transconductance while maintaining a reasonable voltage swing of the sensor, a large pixel-level source-follower transistor would be required. This means that, assuming a reasonably small pixel size, only little space would be left for the photodiode or, in other words, the fill factor of the pixel would be poor.

In the case of a column-parallel processing architecture, the pixel-level source-follower is given one row period of time to drive the column line to the reset level and to the signal level. The requirement of quickly driving the multiplexer and the output buffer has to be fulfilled, in this case, by the column-parallel circuit rather than the pixel-level source-follower. This is less of a problem, since significantly more circuit area for large transistors is available in a column-parallel circuit on the periphery than in a pixel circuit. Additionally, the wiring capacitance between the column-parallel circuits and the multiplexer can be significantly lower than the wiring capacitance of a column line.

A vast majority of low-noise CMOS image sensors feature column-level voltage amplification for two principal reasons. First of all, it is well known from fundamental signal theory that signal amplification reduces the impact of noise sources situated in the signal processing chain after the amplification stage. This effect is illustrated in the expression of the input referred noise charge $q_{\text{n,post amp}}$ due to the overall post-amplification noise voltage

$v_{\text{n,post amp}}$ for a sensor with a column-level voltage amplification of A_{amp} , as given in (2.10).

$$q_{\text{n,post amp}} = C_{\text{sn}} \frac{1}{A_{\text{sf}}} \frac{1}{A_{\text{amp}}} v_{\text{n,post amp}} \quad (2.10)$$

In the above expression, C_{sn} is the capacitance of the sense node and A_{sf} is the near-unity gain of the pixel-level source-follower. Thanks to the division by the voltage gain A_{amp} , the impact of post-amplification noise components, such as chip-level output buffer and board-level signal acquisition electronics or quantization noise of column-parallel ADCs, is often reduced to a negligible level.

A second reason for the use of column-parallel amplification is bandwidth limitation of thermal noise of the pixel-level source-follower [36], [37], [38]. As explained in Sect. 2.5.3, the approach of limiting the noise bandwidth of the source-follower by capacitive loading of the column line requires excessive capacitance. A low-pass filtering column-level circuit, therefore, is the only practical solution for noise reduction. If a unity-gain column-parallel circuit is used, the same problem will concern this circuit, i.e. white noise of the column-parallel circuit will require excessive load capacitance. The load capacitance multiplication effect of voltage amplification applied to the column-level circuit provides practical and implementable column-parallel signal processing circuits with reasonably low self-generated noise. The effectiveness of these circuits for bandwidth reduction of pixel-level source-follower noise is, however, subject to some limitations as will also be discussed in Sect. 2.5.3.

In a very large majority of currently reported CMOS image sensors column-parallel amplification is performed by a switched-capacitor amplifier, as illustrated in Fig. 2.7. The principal reason for this type of circuit's popularity is the built-in CDS functionality. The embedded CDS functionality is explained in the following description. An amplifier reset, or autozeroing, is performed by activating the amplifier reset signal $\Phi_{\text{res,amp}}$ while the pixel reset level is available on the column line, i.e. after the sense node reset but prior to charge transfer. Due to the reset configuration of the switched-capacitor amplifier, as illustrated in the top right diagram of Fig. 2.7, the reset level, including the offset of the pixel-level source-follower and frozen sense node reset noise, is stored on the input capacitor C_1 with respect to the virtual ground potential of the transconductance amplifier. At the transition between amplifier's reset and amplification phases, when $\Phi_{\text{res,amp}}$ goes low, the pixel reset level remains stored as charge information in C_1 . As long as no change of the column voltage occurs, the output V_{amp} of the switched-capacitor amplifier settles to

a reference level $V_{\text{ref,amp}}$, which can be seen conceptually as a zero signal output level. Once charge is transferred from the buried photodiode to the sense node of the pixel by activation of the tx_i signal, the column voltage settles to its signal level. Due to the charge sharing principle, V_{amp} now decreases by the *change* of the column signal voltage amplified by the ratio of input capacitance to feedback capacitance C_1/C_2 . The output of the amplifier is, therefore, proportional to the *difference* of the column reset level and column signal level which is a perfect implementation of CDS.

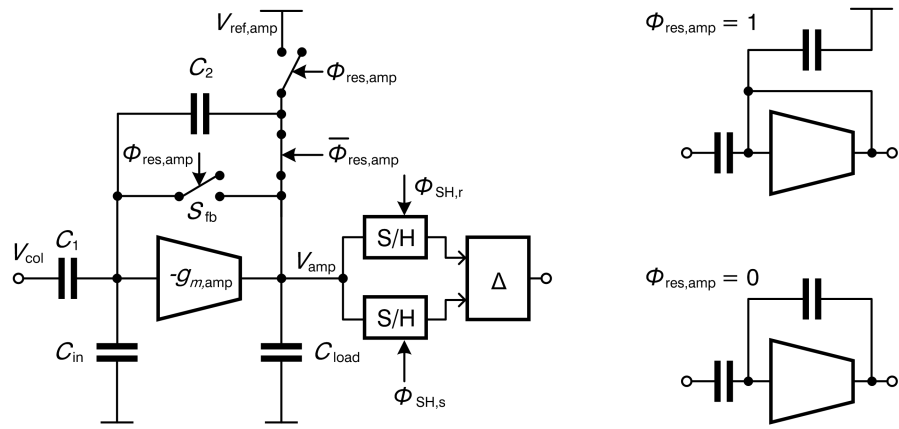


FIGURE 2.7 Left: Switched-capacitor amplifier topology used for column-parallel amplification in state-of-the-art CMOS image sensors. Right: Configuration during reset phase (top) and during amplification phase (bottom)

Theoretically, this value of V_{amp} free of pixel-level offset and sense node reset noise could be used as an image sensor output or for further processing. This procedure is, however, not used in most designs and to understand why, it has to be considered what happens at the transition between the reset phase and the amplification phase of the switched-capacitor amplifier. At the end of the reset phase the feedback switch S_{fb} of the amplifier is opened and the virtual ground node of the amplifier turns into a charge storage node. At this moment the instantaneous amplitude of the transconductance amplifier's temporal noise is frozen on the virtual ground node. Furthermore, a thermal noise component of the opened feedback switch is also frozen on the virtual ground node. The sum of these two random noise components, which are constant, i.e. frozen, during the amplification phase, is referred to as the *freeze noise* of the switched-capacitor amplifier.

Given the constant amplitude of the freeze noise during the amplification phase, methods very similar to the case of sense node reset noise can be applied. It is actually common to apply a further CDS operation to the output V_{amp}

of the switched-capacitor amplifier¹¹. A first sample of the settled amplifier output taken prior to charge transfer contains only the freeze noise. A second sample of the amplifier taken after charge transfer contains identical freeze noise plus the sense node reset noise free and offset corrected pixel signal. Subtraction of these two samples, or in other words a second CDS operation, provides a signal free of amplifier freeze noise.

It is worth pointing out that the cancellation of freeze noise comes at the prize of sampling twice the temporal noise of the switched-capacitor amplifier in amplification mode. Concerning the noise power of the column-level amplifier a choice between either twice the noise power of the amplification mode (dual CDS) or once the noise power of the amplification mode plus the freeze noise power (single CDS) has to be made. It has been shown that for unity gain of the switched-capacitor amplifier single CDS is advantageous, whereas for higher values of C_1/C_2 , as generally used in low-noise sensors, dual CDS is favorable.

Note that the CDS circuit consisting of two sample-and-hold stages as well as a subtractor, as illustrated in Fig. 2.7, should be considered conceptually. Various implementations are possible. For instance, column-level passive or active sample-and-hold stages can be used in conjunction with a chip-level analog multiplexer, board-level analog-to-digital conversion, and digital subtraction. Alternatively, the second CDS functionality can be embedded in a column-parallel ADC.

Figure 2.8 illustrates the timing of switched-capacitor operation for dual CDS as well as for single CDS (cf. the dashed line). Concerning the signal $\Phi_{\text{res,amp}}$, it should be noted that the timing diagram as well as the circuit schematic of Fig. 2.7 have been simplified for improved readability. In reality different non-overlapping signals are used to control the different switches. For instance, it is important to guarantee that the feedback switch is opened before C_2 is switched from V_{ref} to the amplifier output.

2.5 Analysis of Noise in State-of-the-Art CMOS Image Sensors

This section provides quantitative results of noise analysis in CMOS image sensors based on the commonly used architecture described in the previous section. Unless stated otherwise, the results apply to an implementation and operating mode featuring dual CDS.

¹¹This method is referred to as dual CDS, multiple CDS, or cascaded CDS.

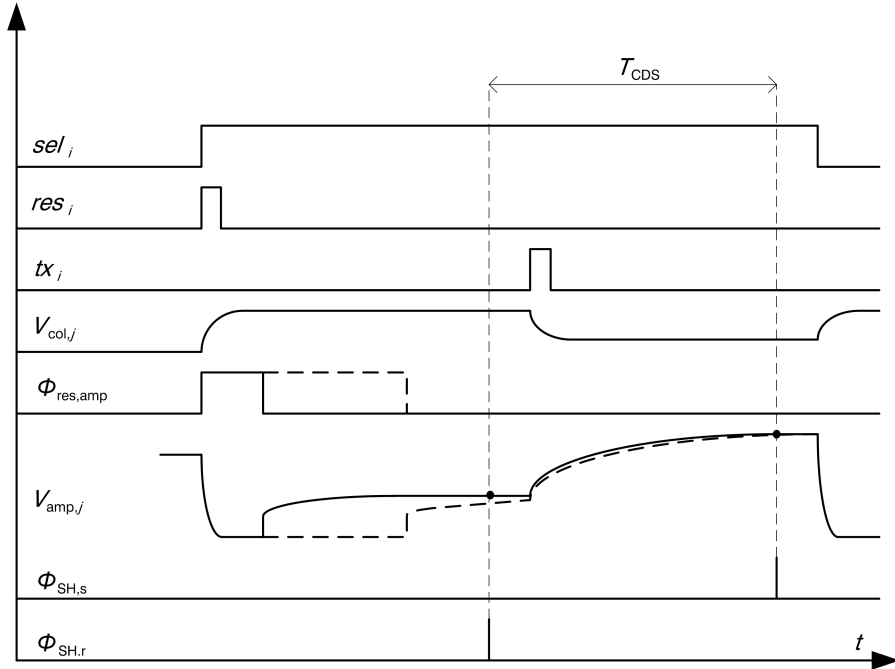


FIGURE 2.8 Row timing of the relevant signals for column-parallel voltage amplification for an architecture featuring dual CDS (solid lines). In the case of single CDS (dashed lines) more settling time of the column signal during amplifier reset is required and reset level sampling of the amplifier output is omitted

2.5.1 Leakage Current Shot Noise

As mentioned in Sect. 2.4.1, two distinct sources of leakage need to be considered when using buried photodiodes. On one hand, the buried photodiode has a relatively large area but a comparatively low leakage current density due to intense technology optimization efforts in past years. On the other hand, the sense node diode, which is equivalent to the source or drain diffusion of a transistor, suffers from higher leakage current density but has generally lower area. A key point for the impact of the two leakage components is their respective integration time. In the case of buried photodiode leakage this integration time is inherently equal to the exposure time. According to 2.2 the leakage shot noise charge of the buried photodiode is given by the following expression:

$$q_{n,\text{leak,bpd}} = \sqrt{q i_{\text{leak,bpd}} T_{\text{exp}}} \quad (2.11)$$

The relevant integration time of the sense node leakage current is, however, equal to the sampling time difference T_{CDS} of the correlated double sampling. This can be understood by considering that the output signal of the CDS operation is a difference of two states of the sense node with a temporal spacing of T_{CDS} . Leakage occurring before or after taking the two samples will not appear in the result after CDS. The shorter the CDS sampling time difference, the lower the impact of sense node leakage, as shown by 2.12. This result actually illustrates one of the major interests of using CDS with short sampling time difference in combination with BPDs.

$$q_{n,\text{leak,sn}} = \sqrt{q i_{\text{leak,sn}} T_{\text{CDS}}} \quad (2.12)$$

For photodiode and sense node area values typically used in low-noise CMOS image sensors and typical ratios of exposure time over CDS sampling time difference, being at least equal to the number of rows, sense node leakage is negligible in comparison to BPD leakage. Even BPD leakage shot noise is as low as one single electron at room temperature for BPD area typically used in scientific image sensors and exposure times of a few milliseconds, i.e. frame rates of tens of Hertz.

2.5.2 Sense Node Reset Noise

Despite the fact that reset noise is canceled by CDS in state-of-the-art image sensors, the amplitude of sense node reset noise is given here for completeness. Sense node reset noise is thermal noise of the reset transistor during sense node reset. Its temporal amplitude is frozen on the sense node when the reset transistor is entirely turned off at the end of the sense node reset phase. The amplitude of reset noise is practically independent of the dimensions of the reset transistor or on its actual on-resistance value. This is due to the fact, that the noise power spectral density (PSD) as well as the noise bandwidth of the series RC element of the on-resistance and the sense node capacitance have mutually canceling dependence on the on-resistance.

The reset noise amplitude does, however, depend on the operating region of the reset transistor during reset, i.e. on the noise excess factor γ . Two different reset operation modes are usually distinguished. In the first case called *hard reset* the reset potential V_{res} is chosen lower than the high level of the reset signal res_i by at least the threshold voltage of the reset transistor. In this case, the reset transistor is in strong inversion triode region during the reset phase. At this operating point of zero drain-source voltage, γ is found to be very close to its theoretical value of 1 for the triode operation region with the

slope factor n assumed equal to unity. The currently accepted expression of the reset noise charge is therefore given by (2.13) [39].

$$q_{n,\text{res,hard}} = \sqrt{kTC_{\text{sn}}} . \quad (2.13)$$

For the second possibility of reset operation mode, called *soft reset*, the reset potential V_{RES} is chosen higher than the high level of the reset signal res_i minus the transistor threshold voltage. Therefore, after possibly being operated in strongly inverted saturated mode at the very beginning of the reset phase, the reset transistor is operated in its weakly inverted saturated region at the end of the reset phase. In this operating region, only fluctuation of the forward current needs to be considered, while the reverse current is negligible. In more arithmetic words, $n\gamma$ is close to $1/2$ which results in a reduction of the reset noise charge by square root of two in comparison to the hard reset case:

$$q_{n,\text{res,soft}} = \sqrt{\frac{1}{2}kTC_{\text{sn}}} . \quad (2.14)$$

Evaluation of (2.13) and (2.14) for typical sense node capacitance values of a few femto-Farads results in tens of electrons of reset noise at room temperature, a result which illustrates the crucial necessity of CDS in low-noise CMOS image sensors.

For image sensors without CDS, *active reset* methods have been shown to reduce the reset noise below the soft-reset value [40]. Implementation of such methods usually involves, instead of a transistor connecting the sense node to a fixed reset voltage, a regulator comparing the column voltage to a low-noise reference potential and actively regulating the sense node voltage. The success of such reset noise attenuation methods, besides other effects, relies on the regulation effect during the, usually gradual, transition between the regulated reset state and the floating state of the sense node.

2.5.3 Source-Follower Noise

Electronic noise from the pixel-level source-follower M_{sf} is a very important noise component for two principal reasons. First of all, since for obvious reasons no electronic signal amplification can be applied beforehand, the first stage in a signal processing chain is always a critical noise contributor. Additionally, given the restricted area in pixel circuits and the need for low sense node

capacitance, little design freedom is available for the gate dimensions of the source-follower transistor. In this section, it will become apparent that noise shaping and filtering by the subsequent signal processing stages is, therefore, crucial for successful control of source-follower noise.

Thermal noise and flicker noise are both non-negligible components of source-follower noise and will be considered separately in the following two sub-sections. Since both noise contributions can be modeled as noise sources in series with the transistor gate, the schematic of Fig. 2.9 can be used for both considerations. The noise analysis needs to consider the effect of the column-parallel voltage amplification as well as of the CDS operation, since this signal processing has an important impact on the actual amplitude of the source-follower noise contribution to the output signal.

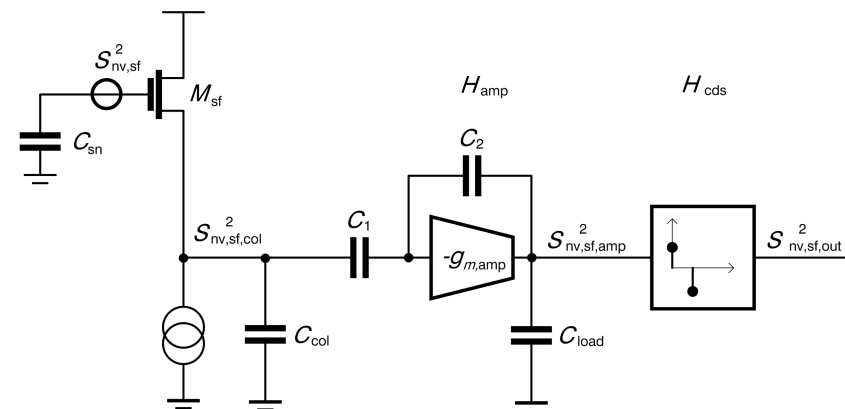


FIGURE 2.9 Equivalent schematic for the analysis of source-follower thermal and flicker noise

Thermal Noise

In order to understand the need for frequency-domain processing of the source-follower output, it is instructive to investigate the source-follower thermal noise on the column signal. As a matter of fact the PSD of thermal noise on the column line generated in the source-follower transistor channel is band-limited, as shown in (2.15). Note that, for the sake of readability of the results, this formula does not cover thermal noise from the column current source used for biasing the source-follower transistor. This component can, however, be included by multiplication by a factor of $1 + g_{m,\text{source}}/g_{m,\text{sf}}$ in the noise power domain, where $g_{m,\text{source}}$ is the transconductance of the saturated n-channel MOS transistor used as a current source implementation. In a low-noise image

sensor this factor is designed to be close to unity by choice of relatively low $g_{m,\text{source}}$.

$$S_{\text{nv,sf,col,th}}^2 = \frac{4kT\gamma}{g_{m,\text{sf}}} A_{\text{sf}}^2 \left| \frac{1}{1 + sC_{\text{col,tot}}/g_{m,\text{sf}}} \right|^2. \quad (2.15)$$

In this expression s is the complex signal frequency, γ and $g_{m,\text{sf}}$ are the noise excess factor and the transconductance of the source-follower transistor respectively, A_{sf} is the voltage gain of the source-follower and the total column capacitance $C_{\text{col,tot}}$ is equal to $C_{\text{col}} + C_1$. The concept of bandwidth control implies that low noise PSD and low bandwidth are required for achievement of low noise. Investigation of (2.15) shows that changing the transistor transconductance has opposite effects on noise PSD and bandwidth. Column capacitance is, therefore, the only degree of freedom for reduction of thermal noise in the column signal. The equivalent noise charge on the sense node corresponding to the thermal noise on the column signal is actually found to be equal to $C_{\text{sn}} \sqrt{kT\gamma/C_{\text{col,tot}}}$. Achieving a source-follower thermal noise charge of 0.5 electrons, which is desirable for a sensor with one electron overall noise, at a sense node capacitance of 5 fF and a noise excess factor of two would require a total column capacitance as high as 46 pF. Column-wise capacitors of this size take a silicon area of the same order of magnitude as the pixel array and the resulting image sensor would be anything but competitive in terms of package size and silicon fabrication cost.

This consideration illustrates that, rather than directly band-limiting the column line noise, it is more attractive to use a wide-bandwidth low-PSD noise spectrum on the column line with bandwidth limitation in the subsequent stage. As a matter of fact, the column-parallel switched-capacitor voltage amplifier does, under certain circumstances, act as an effective low-pass filter. For evaluation of the noise filtering effect of the switched-capacitor amplifier used with dual CDS operation, the amplifier characteristics while taking the two samples for CDS, i.e. in amplification configuration, needs to be considered. The input to output voltage transfer function of the switched-capacitor amplifier in amplification mode is given by the following expression:

$$H_{\text{amp}} = -A_{\text{amp}} \frac{1 - s/2\pi f_{z,\text{amp}}}{1 + s/2\pi f_{p,\text{amp}}} \quad (2.16)$$

where

$$A_{\text{amp}} = \frac{C_1}{C_2}, \quad (2.17)$$

$$f_{z,\text{amp}} = \frac{g_{m,\text{amp}}}{2\pi C_2}, \quad (2.18)$$

and

$$f_{p,\text{amp}} = \frac{g_{m,\text{amp}}}{2\pi (C_1 + (1 + A_{\text{amp}}) C_{\text{load}})}. \quad (2.19)$$

In the above expressions, A_{amp} is the switched-capacitor amplifier voltage gain in amplification mode, C_1 is the input capacitance, C_2 is the feedback capacitance, C_{load} is the load capacitance and $g_{m,\text{amp}}$ is the transconductance of the operational transconductance amplifier (OTA) used for implementation of the switched-capacitor amplifier.

Obviously, the effect of correlated double sampling on any noise source affecting the signal chain prior to the CDS operation needs to be considered. From a signal processing point of view, the CDS operation can be considered as two subsequent operations. First of all, the noise is, at least conceptually speaking, periodically sampled with a sampling period of T_{cds} . Secondly, subtraction of the sampled data values results in a discrete-time high-pass filtering. Two mathematical approaches to determine the RMS noise in the computed difference of samples may be adopted. In a first approach, the two-sided noise power spectrum¹² at the input of the conceptual CDS block is folded into the baseband by convolution with a Dirac pulse train corresponding to the sampling. The folded noise PSD in the baseband is subsequently shaped, i.e. multiplied, by the squared transfer function of the discrete-time high-pass filtering. Finally, the noise power, i.e. the square of the RMS noise voltage in the subtraction result, is determined by the integral of the folded and shaped noise PSD in the frequency range from $-1/(2T_{\text{cds}})$ to $1/(2T_{\text{cds}})$. An equivalent alternative mathematical approach deals with one-sided spectra from zero to infinite frequency, which may be called equivalent non-sampled spectra. The sampling and folding of noise, as well as its frequency shaping by the subtraction of sampled data, is taken into account by periodic extension of the discrete-time high-pass filtering function from the baseband frequency range to

¹²The two-sided noise power spectra are generally obtained by symmetrical extension to negative frequencies and by division by two in order to achieve power conservation

infinite frequency. To apply this second method, the one-sided continuous-time noise power spectrum is multiplied by the square of a transfer function H_{Cds} obtained from periodic extension of the baseband portion of the sampled-data high-pass transfer function representing the time-domain sample subtraction. The correspondingly shaped one-sided PSD is then integrated from zero to infinite frequency in order to obtain the square of the RMS noise affecting the output value of the CDS operation. For the remainder of this thesis, this second approach is used for calculations and presentation of noise spectra.

The baseband transfer function $H_{\text{Cds}}(f)$ is obtained from replacing z by $j\omega T_{\text{Cds}}$ in the z -transform representing the CDS operation. Since the amplitude of this baseband transfer function is periodic with a frequency period of $1/T_{\text{Cds}}$, the periodically extended representation of $|H_{\text{Cds}}|$ is described by the identical mathematical expression, i.e. by the sine-wave function given in (2.20) and reported in [41].

$$\begin{aligned} H_{\text{Cds}}(z) &= 1 - z^{-1} \\ |H_{\text{Cds}}(f)| &= \left| 1 - e^{-j2\pi f T_{\text{Cds}}} \right| \\ &= \left| 2\sin(\pi f T_{\text{Cds}}) \right| \end{aligned} \quad (2.20)$$

From (2.15), (2.16), and (2.20) the equivalent RMS noise charge $q_{\text{n,sf,th}}$ of the source-follower thermal noise can be expressed as follows:

$$q_{\text{n,sf,th}} = C_{\text{sn}} \frac{1}{A_{\text{sf}}} \sqrt{\int_0^\infty |H_{\text{Cds}}(f)|^2 \left| \frac{H_{\text{amp}}(2\pi f)}{A_{\text{amp}}} \right|^2 S_{\text{nv,sf,col,th}}^2(2\pi f) df} \quad (2.21)$$

The source-follower's thermal noise PSD on the column line, the amplifier transfer function, and the CDS transfer function are visualized in Fig. 2.10. It is evident that effective reduction of source-follower thermal noise is achieved, if the amplifier bandwidth, i.e. its pole frequency $f_{\text{p,amp}}$, is lower than the noise bandwidth on the column line. In other words, the switched-capacitor column-parallel amplifier allows low-pass filtering of the wide-bandwidth low-PSD noise source of the pixel-level source-follower. Taking a first order approximation, the noise charge is defined by the product of the amplifier bandwidth and the thermal noise PSD at low frequency of the source-follower, which gives rise to two practical limitations of the source-follower noise charge. First of all, the thermal noise PSD can not be reduced arbitrarily, since the value of source-follower transconductance is limited by criteria of current consumption

and pixel area consumed by the source-follower transistor. Secondly, the amplifier bandwidth has to remain sufficiently high to fulfill its signal processing task in the available timing period. The timing diagram of Fig. 2.8 actually shows that the amplifier output needs to settle a first time between the end of the amplifier reset phase and the reset level sampling as well as a second time between the pixel charge transfer and the signal level sampling. This requirement leads to the criterion of (2.22), which shows direct proportionality between the minimum, hence optimum, amplifier bandwidth $f_{\text{p,amp}}$ and the sensor frame rate f_{fr} . This proportionality is an expression of the trade-off between a sensor's noise performance and its frame rate.

$$\begin{aligned} n_\tau \frac{1}{2\pi f_{\text{p,amp}}} &\leq T_{\text{Cds}} \leq \frac{T_{\text{row}}}{2} \\ &\leq \frac{1}{2 n_{\text{rows}} f_{\text{fr}}} \end{aligned} \quad (2.22)$$

In (2.22) T_{row} is the readout time of a row, n_{rows} is the number of rows in the pixel array and n_τ , the number of amplifier time constants needed for settling of the amplifier output to the required precision is typically as high as 8 to 10.

Figure 2.10 also illustrates the limitations of using a switched-capacitor amplifier for noise bandwidth limitation. Due to feedthrough of the input signal across the feedback capacitance C_2 , the amplifier transfer function displays a zero. Beyond $f_{\text{z,amp}}$, noise is attenuated by a constant attenuation factor rather than being attenuated proportionally to the inverse frequency. The described effect will, therefore, affect the noise spectrum between $f_{\text{z,amp}}$ and the bandwidth of the column line. Compared to an ideal first-order low-pass filter of identical bandwidth the source-follower noise suppression by use of a switched-capacitor amplifier is, therefore, slightly disadvantageous.

The investigation of the CDS transfer function, which further shapes the output of the switched-capacitor amplifier, leads to the conclusion that CDS does not have a fundamental effect on the impact of source-follower thermal noise. The sine wave frequency shaping has little effect on the integrated noise power, if the sampling time difference T_{Cds} is several times longer than the amplifier's time constant. In this case, the noise power spectral density has a considerable amplitude over several periods of H_{Cds} , which, therefore can be approximated by its mean value, as given in (2.23), without introducing a major error.

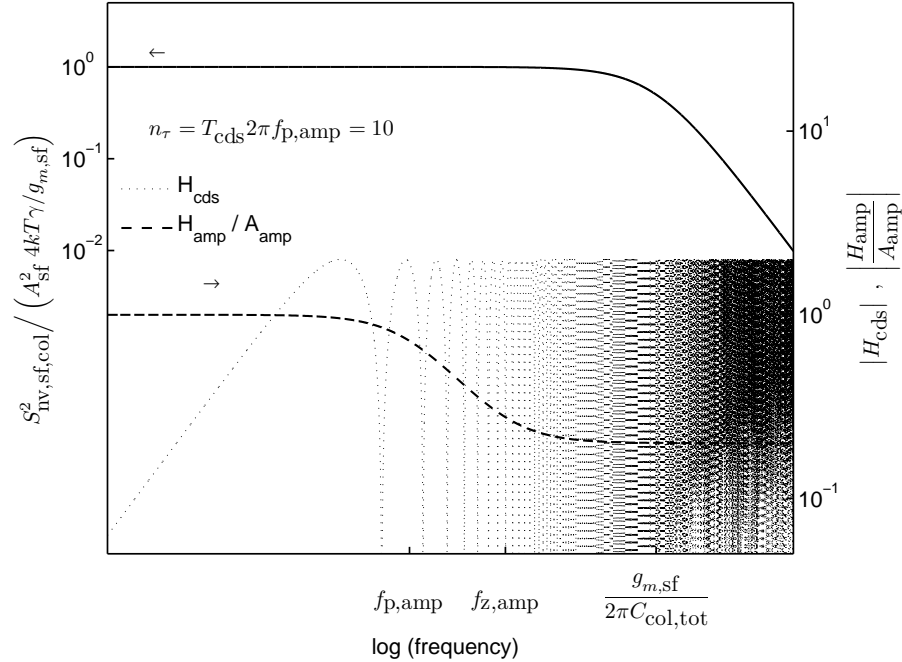


FIGURE 2.10 Normalized noise PSD of the source-follower thermal noise on the column line and normalized transfer functions of the column-parallel amplifier and of the CDS operation

$$\overline{|H|^2} = \frac{1}{\pi} \int_0^\pi 4 \sin^2(x) dx = 2 \quad (2.23)$$

The approximation of H_{CDS} by its mean flat spectrum is equivalent to assuming that the thermal noise components in the two samples used for CDS are completely uncorrelated. Accordingly, CDS does not have an impact on the thermal component of the source-follower noise apart from multiplying its amplitude by a factor of $\sqrt{2}$, as two uncorrelated samples of noise are subtracted.

Flicker Noise

The analysis of the impact of source-follower flicker noise on the overall noise performance is, obviously, similar to the analysis of thermal noise. The result will, however, show that, besides low-pass filtering, also CDS has a fundamental effect on the impact of flicker noise.

In analogy to (2.15) and (2.21) the flicker noise PSD on the column signal and the equivalent noise charge corresponding to the output flicker noise are given in (2.24) and (2.25) respectively. The flicker noise contribution of the current source used for biasing of the source-follower transistor is neglected, since this component can be reduced to a insignificant amount by increasing the gate area of the column biasing current source transistor.

$$S_{\text{nv,sf,col},1/f}^2 = \frac{K}{C_{\text{ox}}WL} \frac{1}{f} A_{\text{sf}}^2 \left| \frac{1}{1 + sC_{\text{col,tot}}/g_{m,\text{sf}}} \right|^2. \quad (2.24)$$

$$q_{\text{n,sf},1/f} = C_{\text{sn}} \frac{1}{A_{\text{sf}}} \sqrt{\int_0^\infty |H_{\text{cds}}(f)|^2 \left| \frac{H_{\text{amp}}(2\pi f)}{A_{\text{amp}}} \right|^2 S_{\text{nv,sf,col},1/f}^2(2\pi f) df} \quad (2.25)$$

Comparison of the flicker noise PSDs on the column signal and on the output of the CDS function, as given in Fig. 2.11, shows, that a *band-pass* filtering effect arises from the combination of low-pass filtering by the column-parallel amplifier and the high-pass filtering effect of CDS. This high-pass filtering, which has been neglected for thermal noise analysis due to its relatively low transition frequency, plays an important role in the case of flicker noise, which has very high amplitude at very low frequency. A linear low-frequency approximation of the sine wave shaped CDS transfer function allows to conceptually consider the CDS transfer function as a first order high-pass filter with a high-frequency amplitude of 2 and an equivalent transition frequency of $f_{\text{eq}} = 1/(\pi T_{\text{CDS}})$. These considerations lead to the understanding that optimum filtering of flicker noise is achieved with the lowest possible CDS sampling time difference and the lowest possible column-parallel amplifier bandwidth. As a matter of fact, the minimum ratio of amplifier bandwidth over CDS transition frequency is given by the settling requirement of the column amplifier within the CDS sampling time difference, as expressed in (2.22). This settling

requirement leads to a minimum ratio of $f_{p,amp}/f_{eq}$ equal to $n_\tau/2$. This optimum filtering of source-follower flicker noise can practically be reached by use of the short sampling time difference CDS operation enabled by rolling shutter timing, and the isolated integration sites and complete charge transfer capability of buried photodiodes. It is worth pointing out that, in contrast to the case of thermal noise, bandwidth and frame rate reduction can not improve flicker noise, once the mentioned optimum ratio between the amplifier bandwidth and CDS transition frequency is reached. Proportionally reducing both of these two frequencies will result in a proportional reduction of the noise bandwidth, which will, however, be compensated by a proportional increase of the flicker noise PSD in the band of interest. This frame-rate independent flicker noise performance resulting from optimum filtering is, therefore, called *flicker noise limit*.

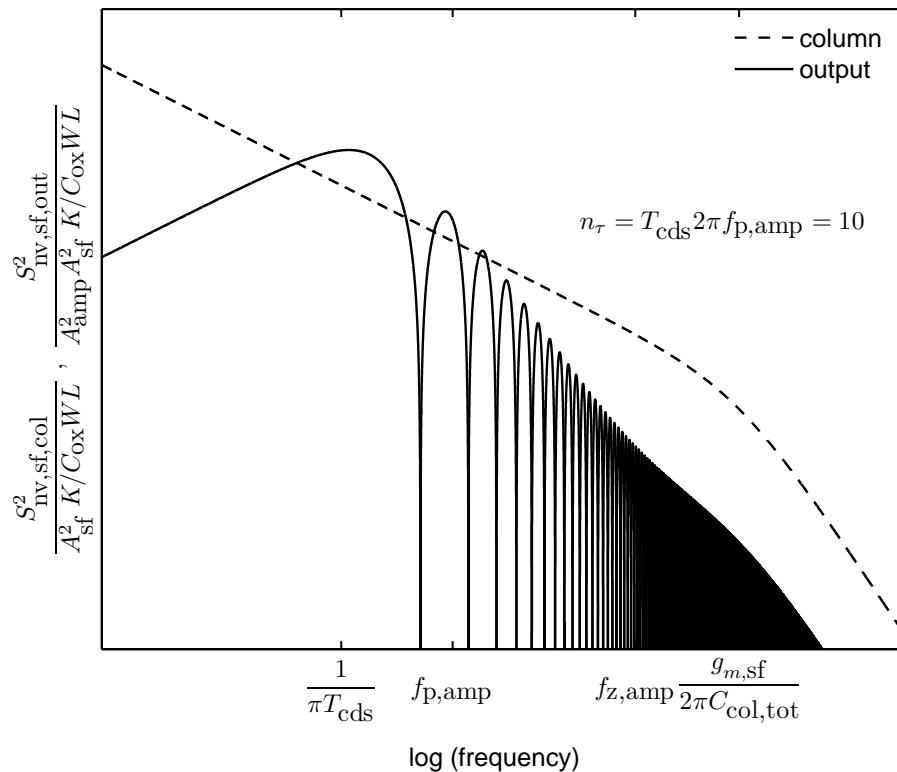


FIGURE 2.11 Normalized noise PSD of the source-follower flicker noise on the column line and on the output of the CDS operation

Expressed in other words, the short sampling time difference of two samples of a low-frequency noise affected signal and good smoothing of high-frequency components results in a high degree of correlation between the noise amplitudes contained in both samples and, consequently, in good noise suppression by subtraction of the samples.

The mentioned flicker noise limit still depends on the flicker noise constant K , which is a function of the source-follower transistor type and process technology. Some recent work has explored the reduction of K by use of buried channel source-follower transistors, which are not subject to channel charge trapping and release at the silicon-oxide interface [42], [43].

2.5.4 Column-Parallel Amplifier Noise

The column-parallel voltage amplifier's benefit of filtering source-follower noise and of drastically attenuating the impact of subsequent circuits of the readout chain has been analyzed in the previous sections. While reducing the impact of other noise sources, this amplifier also generates itself an additional noise component. For the analysis of the amplifier noise, the switched-capacitor amplifier in amplification mode needs to be considered. Note that the amplifier reset phase does not need to be analyzed, if freeze noise is canceled by dual CDS operation. Only thermal noise will be investigated, since available area in column-parallel circuits as well as parasitic capacitance requirements of the involved transistors generally allow design of sufficiently large transistor gate dimensions for flicker noise to become negligible.

The source of thermal noise in a column-parallel amplifier in amplification mode is the OTA used in the switched-capacitor amplifier. OTAs most commonly used in column-parallel amplifiers of low-noise CMOS image sensors are single-ended cascode or regulated cascode amplifiers. If these topologies are well designed for optimum noise-to-power and noise-to-area ratio, the input transistor is the predominant thermal noise contributor. Under these conditions, the amplifier output noise PSD is given by (2.26).

$$S_{n,amp}^2 = \frac{4kT\gamma}{g_{m,amp}} (A_{amp} + 1)^2 \left| \frac{1}{1 + s/2\pi f_{p,amp}} \right|^2, \quad (2.26)$$

where γ is the noise excess factor of the input transistor which is usually operated in moderate inversion saturated region and $g_{m,amp}$ is the transconductance of the input transistor, and hence of the transconductance amplifier. From this first order band-limited spectrum and inserting the value of the amplifier bandwidth from (2.19) the sense node referred equivalent noise charge

of the amplifier thermal noise, as given in (2.19), is found under approximation of the CDS transfer function by its flat-spectrum average value of 2.

$$q_{n,\text{amp}} = \sqrt{2}C_{\text{sn}} \frac{1}{A_{\text{sf}}} \frac{A_{\text{amp}} + 1}{A_{\text{amp}}} \sqrt{\frac{kT\gamma}{C_1 + (A_{\text{amp}} + 1)C_{\text{load}}}}. \quad (2.27)$$

As $(A_{\text{amp}} + 1)/A_{\text{amp}}$ is not a very strong function of the amplifier gain and the source-follower gain is always close to unity, the noise performance mainly depends on the factor $C_1 + (A_{\text{amp}} + 1)C_{\text{load}}$. For $A_{\text{amp}} = 1$ a huge amplifier load capacitance C_{load} would be required for achieving single-electron resolution, according to a similar calculation as the one performed for unfiltered source-follower column noise in Sect. 2.5.3. Moderate to high voltage amplification, typically ranging from 4 to 32, therefore helps to achieve low column-parallel amplifier noise at reasonable expense of capacitance per column. This effect is actually due to the bandwidth reduction effect of voltage amplification.

2.5.5 Conclusions of the Noise Analysis

The noise analysis presented in this section has quantitatively explained that CDS using short sampling time difference is a crucially important operating method for reducing sense node leakage shot noise and source-follower flicker noise in low-noise CMOS image sensors. The components required for implementation of this type of sensor operation, i.e. buried photodiodes and rolling shutter timing, are, therefore, key enabling elements of low-noise CMOS image sensors.

Expressions (2.21), (2.25), and (2.27) of the equivalent noise charge due to source-follower noise as well as amplifier noise all show proportionality to the sense node capacitance, i.e. to the inverse sense node conversion factor. Low sense node capacitance, which is a further advantage of buried photodiodes, is thus a key parameter for low-noise CMOS image sensors. The trend towards low sense node capacitance [44], [45], in combination with moderate to high column-parallel amplification, which is a further prerequisite for good noise performance, leads to a significant decrease of effective full well capacity in low-noise sensors. Various efforts aiming at recovery of this loss of full well capacity by use of dynamic range recovery methods such as adaptive amplification [46], [47], dual-gain parallel readout path [31], or dynamic range enhancement methods such as lateral overflow integration capacitors (LOFIC) [44], [48], [49], [50], blending of multiple exposure time signals [51], [52], [53], or logarithmic photocurrent-to-voltage conversion [54] have been reported.

Analysis of thermal noise in the commonly used state-of-the-art architecture of low noise CMOS image sensors has identified room for improvement in the following two aspects:

Filtering of source-follower thermal noise: The low-pass filtering of the source-follower's thermal noise by column-parallel amplifier is not perfect. Due to a zero in the transfer function of commonly used switched-capacitor amplifiers thermal noise in a certain frequency range out of the useful signal band is not ideally attenuated.

Thermal noise of the column-parallel amplifier: Due to unity gain of the pixel-level source-follower, noise of the column-parallel amplifier has a considerable weighting in the expression of the overall noise performance. Given finite power and silicon area budgets as well as, to some extent, thermal noise excess factors considerably exceeding the theoretical values, amplifier noise will always be a significant component of the overall noise performance. Reducing thermal noise generated in the column-parallel circuit or reducing its impact on the overall noise performance, therefore, is of major interest.

Chapter 3

A Novel Ultra-Low-Noise CMOS Image Sensor Based on Pixel-Level Open-Loop Voltage Amplification

3.1 Introduction

In chapter 2, the essential advantages in terms of low-noise performance of buried photodiodes, correlated double sampling, and rolling shutter operation have been explained. Analysis of the architecture commonly used in state-of-the-art low-noise CMOS image sensors has led to identification of two aspects for possible thermal noise reduction. First of all, low-pass filtering of the pixel-level source-follower's thermal noise by the column-parallel amplifier is, in some cases, not optimized due to a signal and noise feed forward effect found in the switched-capacitor amplifier. Secondly, thermal noise of the column-parallel amplifier has a significant impact on the equivalent noise charge due to the near-unity voltage gain of the pixel-level source-follower. At reasonable expense of power and silicon area, column-parallel amplifiers thus contribute with a non-negligible component to the overall noise budget.

The novel approach of pixel-level open-loop voltage amplification, as presented in this chapter, addresses the two mentioned problems [55], [56]. First order low-pass filtering, free of zeros, of the pixel-level thermal noise is achieved by the suggested open-loop amplifier. Furthermore, thanks to pixel-level voltage amplification, column-parallel voltage amplifiers are not necessarily required and noise of column-level, chip-level, and board-level electronics has

a drastically reduced, in most cases negligible, impact. In conjunction with the use of buried photodiodes, correlated double sampling, and rolling shutter operation, implementations of the suggested architecture achieve noise performance very close to the flicker noise limit, even at standard video frame rates, e.g. up to 60 frames per second.

A test image sensor of 256 x 256 pixels has successfully been designed, fabricated, and characterized in order to prove the performance of this novel approach. This sensor achieves a readout noise equivalent charge as low as 0.9 electrons and an overall dark noise floor including BPD leakage shot noise of 1.4 electrons at room temperature and an exposure time of 1/60 s. Photo-response non-uniformity and linearity, which are potentially critical parameters of the proposed open-loop amplifiers, are absolutely competitive with state-of-the-art image sensors.

The current chapter is organized as follows: Section 3.2 explains the architecture and analyzes the performance of a sensor using pixel-level open-loop voltage amplification, whereas section 3.3 covers aspects of designing and characterizing such an image sensor.

3.2 Topology and Analysis

The topology of the suggested CMOS image sensor relies on achieving moderate voltage amplification of roughly one order of magnitude at the pixel level, i.e. between the pixel sense node voltage and the column line. For this purpose, a distributed common-source voltage amplifier, consisting of a common-source connected amplifier transistor in each pixel and a column-wise shared load resistor, is used.

This amplifier configuration has been chosen for multiple reasons. First of all, the reduction of the pixel-level amplifier elements to a single transistor achieves reasonably high fill factor. Secondly, an open-loop common-source amplifier satisfies the obvious criterion of infinite DC input impedance required for amplification of charge signals on a floating node.

Concerning the load device, a resistor has been chosen for a number of reasons. First of all, a resistor is quite convenient for achieving the target voltage gain of about 10 in comparison to a diode connected saturated MOS transistor, which would require a huge gate length to width ratio and a potentially excessive gate-source voltage in order to achieve high enough load impedance. The alternative option of a current source connected saturated MOS transistor simply has much too high a drain-source impedance to be used for moderate voltage amplification. Finally, a strongly inverted MOS transistor operated in triode region as a load device would be problematic as well, since the load impedance would be approximately constant only within a limited voltage swing and would be subject to a drastic increase as the transis-

tor crosses over from the triode to the saturated region. Furthermore, a resistor is an attractive choice of load device concerning the noise performance of the amplifier. The ratio of the common-source transistors thermal noise current PSD over the load resistors's noise PSD is found to be equal to the product of the noise excess factor γ of the common-source transistor times the voltage amplification A_{pix} of the pixel-level amplifier. Assuming values of 10 for A_{pix} and greater or equal to 2/3 for γ , the thermal noise of the load device is negligible in comparison to the common-source transistor thermal noise. Similar consideration apply to successful implementations of a load transistor operated in triode region or a diode-connected saturated load transistor. Using a saturated current-source connected transistor as a load device could, however, be disadvantageous in terms of noise, since the transconductance of such a device would necessarily be significantly higher than its drain-source conductance. For a given load resistance, significantly higher thermal noise PSD, defined by the transconductance of the load transistor, would be the consequence.

The use of an open-loop amplifier leaves, however, an important issue to be solved. As opposed to feedback amplifiers, which usually *add* their input referred amplifier offset to the output signal, open-loop amplifiers *amplify* their input referred offset. Note that source-followers, as used in state-of-the art CMOS image sensor architectures, are unity-gain amplifiers and amplification of the offset is conceptually equivalent to adding offset to the output. Offset amplification by the moderate-gain voltage amplifier could have a detrimental impact on the operating point of the amplifier, if the sense node was reset to a constant reset voltage, as in the case of source-follower based active pixel sensors. Such shifts of the amplifier's operating point would possibly result in excessive loss of signal swing and in variations of small signal amplification, i.e. in photo-response non-uniformity.

The problem of amplifier offset is addressed by use of a self-biased reset operation instead of resetting the amplifier input, i.e. the sense node, to a fixed DC voltage.

All the above considerations have led to the suggested pixel and sensor architecture, as illustrated in Fig. 3.1. Besides a buried photodiode with a transfer gate and an associated sense node diffusion, each pixel contains a common-source connected p-channel amplifier input transistor M_{CS} , a p-channel select transistor M_{sel} , and a reset transistor M_{RES} connected between the sense node and the column line which allows self-biased sense node reset by use of a unity-gain feedback configuration. A load resistor R_1 is connected to every column line and acts as a shared load device to all the pixel-level voltage amplifiers of the column. Note that, in contrast to the conventional state-of-the-art architecture, an image sensor with pixel-level voltage amplification will usually not need column-parallel amplifiers but can instead use active or passive sample-and-hold stages for sampling the reset level as well as the signal level of the

column line.

The operation sequence, as shown in Fig. 3.2, is very similar to the the operation of a conventional low-noise CMOS image sensor and features CDS with short sampling time difference thanks to the use of a rolling shutter timing scheme. The principal differences are the replacement of the timing signals of the switched-capacitor amplifier by timing signals for the column-level sample-and-hold circuits as well as the polarity inversion of the select and reset signal due to the use of p-channel transistors.

Consideration of the sensor architecture and of the timing reveals two fundamentally different configurations of the pixel-level amplifier, as illustrated in the simplified circuit diagrams of Fig. 3.3.

In the *sense node reset configuration*, when the sel_{n_i} and res_{n_i} signals of a row i are both low, the inverting pixel-level amplifier is operated in a unity gain feedback configuration, since the activated reset transistor provides a feedback path from the output to the input of the amplifier, i.e from the column line to the sense node. This reset method results in a sense node reset voltage which tracks offsets of the common-source connected transistor's threshold voltage and, therefore, attenuates the impact of this offset on the photo-response, as will be analyzed in Sect. 3.2.1. In the second configuration, called the *amplifying configuration*, the circuit is arranged as an open-loop amplifier producing a voltage level on the column line, which is roughly equal to the sense node and column line reset voltage as long as the sense node charge remains unchanged and amplifying the sense node voltage difference after signal charge transfer. An important detail of the pixel circuit and its operation is the use of the select transistor M_{sel} as a cascode device. For this purpose, the activation level the select transistor is not the ground potential, but an intermediate voltage level chosen in order to operate the select transistor in saturation region. As a consequence, the drain voltage of the common-source transistor is fixed to an approximately constant voltage. This cascoding effect avoids multiplication of the gate-drain overlap capacitance by the Miller effect. If in addition the parasitic wiring capacitance between the sense node and the column line can be minimized, no major increase of the effective sense node capacitance due to the Miller effect with inverting voltage amplification is observed, as discussed in Sect. 3.2.4.

Note that the cascode operation of the select transistor does not significantly modify the open-loop voltage gain, i.e the product of the common-source transistor's transconductance and the DC impedance of the column line. This holds true as, at the intended voltage gain, the load resistance is significantly lower than the drain-source resistance of the common-source transistor, even without cascoding.

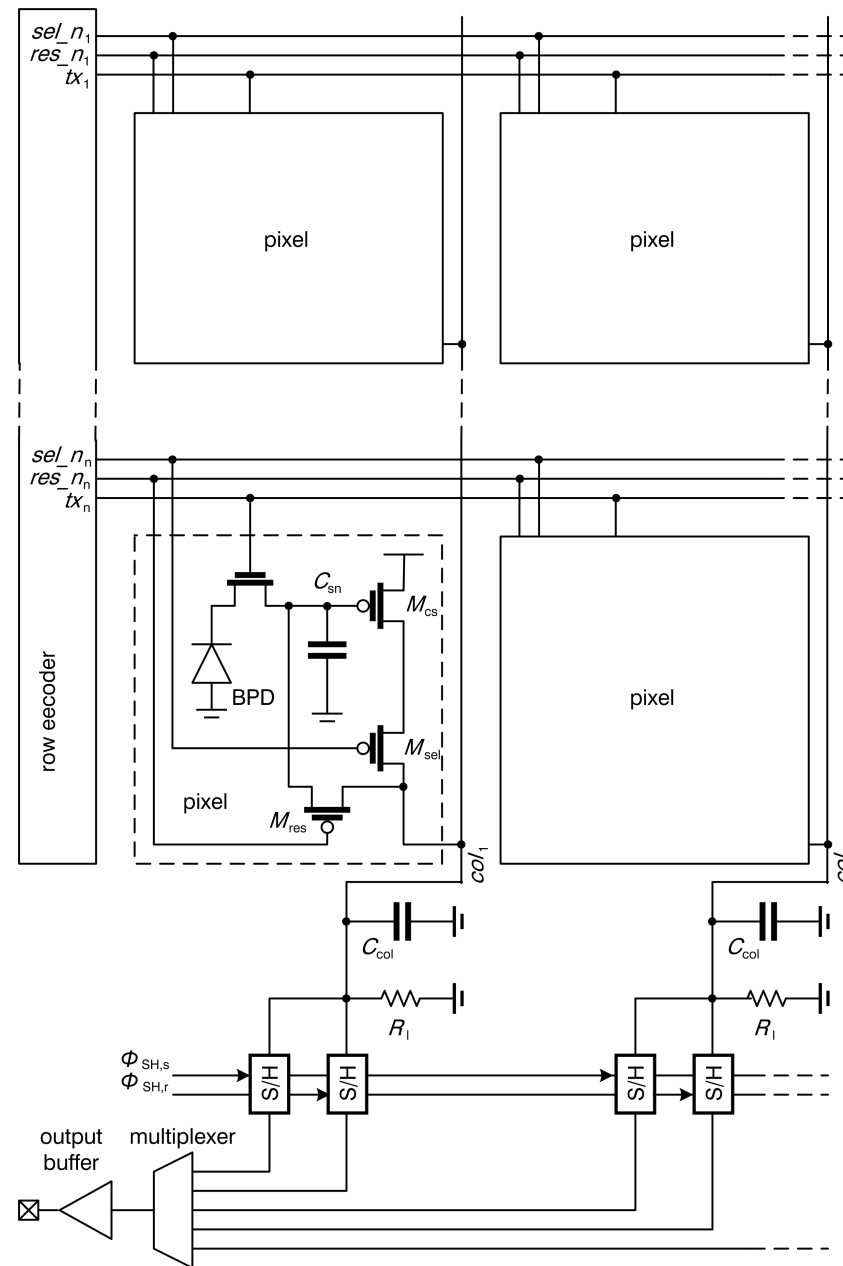


FIGURE 3.1 Architecture of an analog low-noise CMOS image sensor with pixel-level open-loop common-source amplifiers

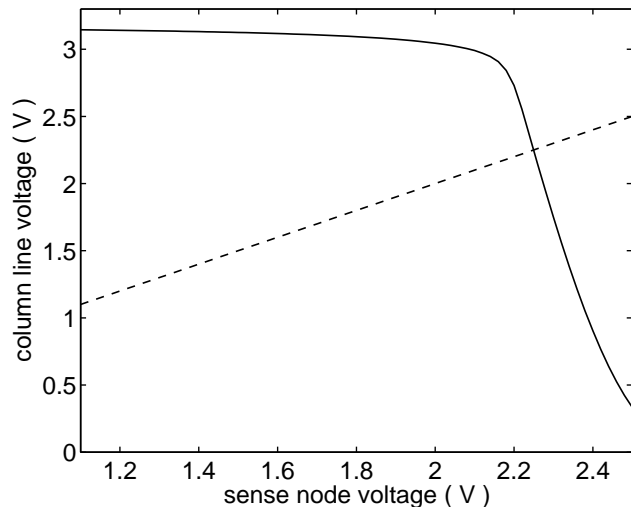


FIGURE 3.4 Sense-node-to-column-line DC voltage transfer function of the pixel-level amplifier and definition of the feedback condition of sense node voltage being equal to column line voltage (dashed line)

a rather high threshold voltage. In the presented implementation of the pixel-level amplification concept, as discussed in Sect. 3.3, a p-channel device of the 3.3 V supply option of the used 0.18 μm technology is employed. In combination with a slight reset voltage shift due to the mentioned charge-injection effect, this choice provides about 1 V of linear swing, which actually makes full use of the input swing of column-level and chip-level readout circuits typically implemented in the standard 1.8 V power supply domain.

$$V_{\text{sn,res}} = V_{\text{dd}} - V_{\text{th}} - \frac{1}{\beta R_1} \left(1 + \sqrt{1 + 2\beta R_1 (V_{\text{dd}} - V_{\text{th}})} \right) , \quad (3.1)$$

where

$$\beta = \mu C_{\text{ox}} \frac{W}{L} . \quad (3.2)$$

In (3.2), W , L , μ , and C_{ox} are the gate width, the effective gate length, the hole mobility, and the gate oxide capacitance density of the common-source transistor. In the presented calculations, the slope factor n is approximated to a value of one and the effect of channel length modulation is neglected in order to obtain simple and closed-form analytical expressions. The small signal voltage amplification A_{pix} , as given in (3.3), corresponds to the product of the load resistance and the transconductance at the reset operating point. Note that considerations concerning the area and input capacitance of the pixel-level common-source transistor may impose some restrictions on the achievable values of β . The choice of the column-level load resistance R_1 , however, provides a real degree of freedom for defining the pixel-level voltage gain.

$$A_{\text{pix}} = g_{m,\text{cs}} R_1 = 1 + \sqrt{1 + 2\beta R_1 (V_{\text{dd}} - V_{\text{th}})} . \quad (3.3)$$

Investigation of the voltage gain expression reveals the benefit of the implemented reset method based on feedback operation. The impact of threshold voltage variation on the amplifier gain, i.e. on the photo-response non-uniformity (PRNU), is significantly reduced, as shown by the analytical expression of the gain sensitivity on the threshold voltage given in (3.4).

$$\frac{d A_{\text{pix}}}{d V_{\text{th}}} = \frac{-\beta}{g_{m,\text{cs}}} . \quad (3.4)$$

In the case of resetting the sense node to a fixed potential, the sensitivity of the amplifier gain on the threshold voltage would be as high as $-\beta R_1$. Comparison of this result to (3.4) illustrates a reduction of the PRNU due to threshold voltage mismatch by a factor of A_{pix} thanks to the effect of feedback in the reset configuration.

Similar calculations concerning the impact of a variation in β prove that the gain spread due to geometry and mobility fluctuations is equivalent to the case of fixed-voltage reset.

3.2.2 AC Characteristics of the Pixel-Level Amplifier

The AC signal transfer function of the open-loop common-source amplifier is a simple first-order low-pass function, as given in (3.5).

$$H_{\text{pix}} = \frac{g_{m,\text{cs}}R_1}{1 + sR_1C_{\text{col,tot}}} = \frac{A_{\text{pix}}}{1 + sA_{\text{pix}}\frac{C_{\text{col,tot}}}{g_{m,\text{cs}}}} \quad (3.5)$$

The second expression illustrates the effect of reduced bandwidth at a given transconductance and load capacitance due to voltage amplification. Since the transconductance is limited by finite space available for the pixel-level common-source amplifier, high-speed imaging requiring the readout of several million rows per second is not practically possible with implementations using state-of-the-art process technologies. The required bandwidth for conventional video frame rate imaging is, nonetheless, comfortably achieved. Furthermore, the bandwidth reduction due to voltage amplification is advantageous for low-pass filtering of the thermal noise generated by the common-source transistor, as discussed in Sect. 3.2.3.

3.2.3 Noise Analysis

Many noise components in the suggested image sensor using pixel-level amplification are identical or very similar to those in conventional low-noise image sensors and will not be covered for a second time in this chapter. Leakage current shot noise of both the BPD as well as the sense node diffusion, for instance, follow the simple laws introduced in Sect. 2.5.1. Note that the sense node leakage current of the discussed implementation is higher than in the case of the conventional image sensor architecture due to the additional component of the p-type drain diffusion of the reset resistor.

Reset noise might differ from the amplitude given by the formula of (2.13) due to an active reset effect depending on the transition speed of turning off the reset transistor at the end of the reset phase. No further analysis of the reset noise is presented here, since in the presented sensor, reset noise is canceled out by CDS.

The most interesting and important differences between noise in conventional image sensors and an image sensor featuring pixel-level amplification are found in the analysis of electronic circuit noise. First of all, pixel-level amplification reduces the impact of noise in column-level and chip-level circuits to a very high degree. Therefore, noise of a well designed column-level, chip-level, and board-level signal chain is usually negligible and is thus not analyzed here

in more detail. Besides understanding the advantageous suppression of electronic noise in the post-pixel readout chain, it is important to analyze the noise generated by the pixel-level circuit, i.e. the pixel-level amplifier. The following two sub-sections will separately analyze thermal and flicker noise of the pixel-level amplifier and provide a comparison to the noise of pixel-level circuits of conventional low-noise image sensors, i.e. of their pixel-level source-followers. The equivalent schematic of Fig. 3.5 is considered for analysis of thermal noise and flicker noise.

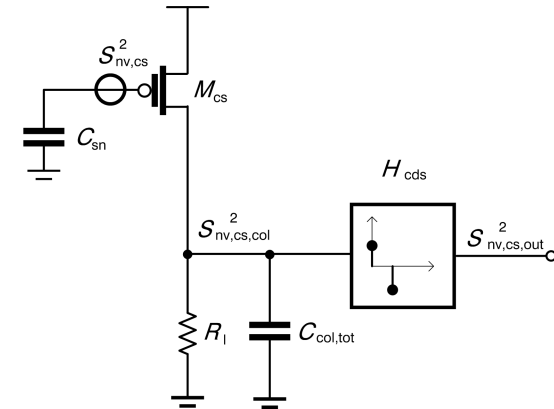


FIGURE 3.5 Equivalent schematic for the analysis of amplifier thermal and flicker noise

Thermal Noise of the Pixel-Level Amplifier

The thermal noise of the pixel-level amplifier is predominantly generated in the channel of the common-source transistor. The thermal noise power of the load resistor, which can be shown to be lower than the common-source transistor thermal noise by a factor of γA_{pix} , can thus be neglected in a first approximation. The thermal noise power spectrum of the amplifier observed on the column line, as expressed in (3.6) and illustrated in Fig. 3.6, corresponds to the gate voltage power spectral density shaped by the amplifier's transfer function.

$$S_{\text{nv,cs,col,th}}^2 = 4kT\gamma \frac{g_{m,\text{cs}}R_1^2}{\left|1 + sR_1C_{\text{col,tot}}\right|^2} \quad (3.6)$$

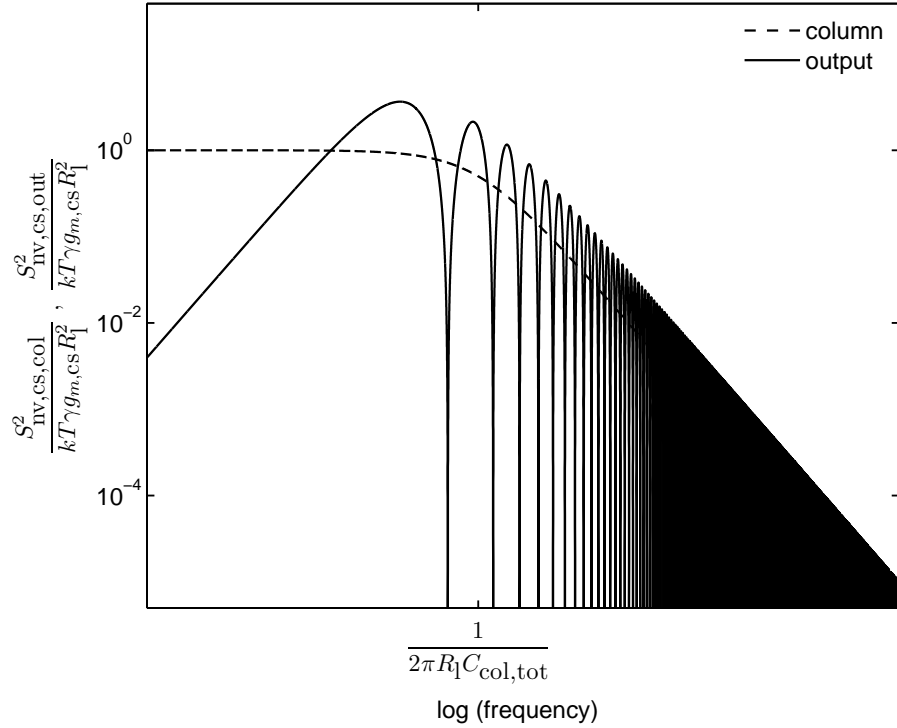


FIGURE 3.6 Normalized PSD of the pixel-level amplifier's thermal noise on the column line and at the output of the CDS operation

The equivalent noise charge of the amplifier thermal noise is found by referring the output noise after CDS back to the sense node, as shown in (3.7), where H_{cds} is the sine wave shaped frequency response of the CDS operation, as given in (2.20).

$$q_{\text{n,cs,th}} = C_{\text{sn}} \frac{1}{A_{\text{pix}}} \sqrt{\int_0^{\infty} |H_{\text{cds}}(f)|^2 S_{\text{nv,cs,col,th}}^2 (2\pi f) df} \quad (3.7)$$

Due to the absence of a column-level switched-capacitor amplifier, the frequency shaping of the pixel-level amplifier noise is solely defined by the first-order low-pass filtering of the pixel-level amplifier and the frequency response of the CDS operation. If H_{cds} is approximated by its average frequency re-

sponse amplitude of $\sqrt{2}$, the equivalent noise charge takes the simple expression of (3.8).

$$q_{\text{n,cs,th}} \approx C_{\text{sn}} \sqrt{\frac{2kT\gamma}{A_{\text{pix}} C_{\text{col,tot}}}} \quad (3.8)$$

Note that the approximation of H_{cds} is valid for any well-designed implementation, since the column line bandwidth has to be chosen to ensure settling of the column signal with sufficient accuracy within the CDS sampling time difference. In analogy to the considerations concerning the column-level amplifier of conventional sensors, as given in (2.22), the following criterion applies to the pixel-level amplifier's bandwidth:

$$\begin{aligned} n_{\tau} R_1 C_{\text{col,tot}} &\leq T_{\text{cds}} \leq \frac{T_{\text{row}}}{2} \\ &\leq \frac{1}{2 n_{\text{rows}} f_{\text{fr}}} \end{aligned} \quad (3.9)$$

Two conclusions can be drawn from expression (3.8) of the pixel-level amplifier's thermal noise. Actually, the expression corresponds to the equivalent charge of the RMS noise voltage on the column line multiplied by a factor of $\sqrt{2}$. In other words, CDS does not significantly shape the thermal noise of the pixel-level amplifier and there is no low-pass filtering element such as a column-parallel voltage amplifier.

The more important conclusion from this analysis is that the thermal noise on the column line can have very low bandwidth and hence very low RMS amplitude at reasonably low total column line capacitance thanks to the bandwidth reduction or load capacitance multiplication effect due to voltage amplification. Comparison of (3.8) to the thermal column line noise equivalent charge of $C_{\text{sn}} \cdot \sqrt{2kT\gamma/C_{\text{col,tot}}}$ of an image sensor without pixel-level amplification illustrates that the effect of the amplification on the thermal noise corresponds to a multiplication of the column capacitance by the voltage gain. In analogy to the calculation example presented in Sect. 2.5.3, evaluation of (3.8) shows that a pixel-level amplifier's thermal noise charge of 0.5 electrons at a sense node capacitance of 5 fF can be achieved with a total column capacitance of 4.6 pF, assuming a pixel-level voltage gain of 10. This capacitance value can be implemented for each column without use of excessive silicon area. For rather large pixel arrays, comprising for instance 1000 rows, the parasitic

capacitance of the column line in combination with the input capacitance of the sample-and-hold circuit may even be sufficient to provide the required total column capacitance.

Flicker Noise of the Pixel-Level Amplifier

Based on the schematic of Fig. 3.5, the flicker noise spectrum on the column line generated by the common-source transistor is given by (3.10) and illustrated in Fig. 3.7.

$$S_{\text{nv,cs,col},1/f}^2 = \frac{K}{C_{\text{ox}}WL} \frac{1}{f} \left| \frac{A_{\text{pix}}}{1 + sR_1C_{\text{col,tot}}} \right|^2, \quad (3.10)$$

where W , L , K , and C_{ox} are the gate width, the gate length, the flicker noise constant, and the gate oxide capacitance density of the common-source transistor. Apart from being amplified by the pixel-level gain and being band-limited at a reduced low-pass filtering frequency, this spectrum is very similar to the spectrum of source-follower flicker noise in a conventional CMOS image sensor. In an image sensor using pixel-level amplification this noise spectrum is directly filtered by the CDS transfer function without any further bandwidth limitation by a column-level amplifier, which leads to the expression of (3.11) for the equivalent noise charge of the pixel-level amplifier flicker noise.

$$q_{\text{n,cs},1/f} = C_{\text{sn}} \frac{1}{A_{\text{pix}}} \sqrt{\int_0^\infty |H_{\text{cds}}(f)|^2 S_{\text{nv,cs,col},1/f}^2 (2\pi f) df} \quad (3.11)$$

Note that despite the absence of a column-level amplifier, the flicker noise of a sensor with pixel-level amplification can conveniently be reduced to the flicker noise limit defined in Sect. 2.5.3 thanks to the low-pass filtering effect of the pixel-level amplifier. To reach the flicker noise limit, the CDS sampling time difference, the total column capacitance and the load resistor of the amplifier need to fulfill the criterion of $T_{\text{cds}} = n_\tau R_1 C_{\text{col,tot}}$.

Summary of the Noise Analysis

Analysis of the predominant noise components in an image sensor with pixel-level open-loop amplification and comparison to the corresponding noise components in conventional low-noise image sensors has shown important differ-

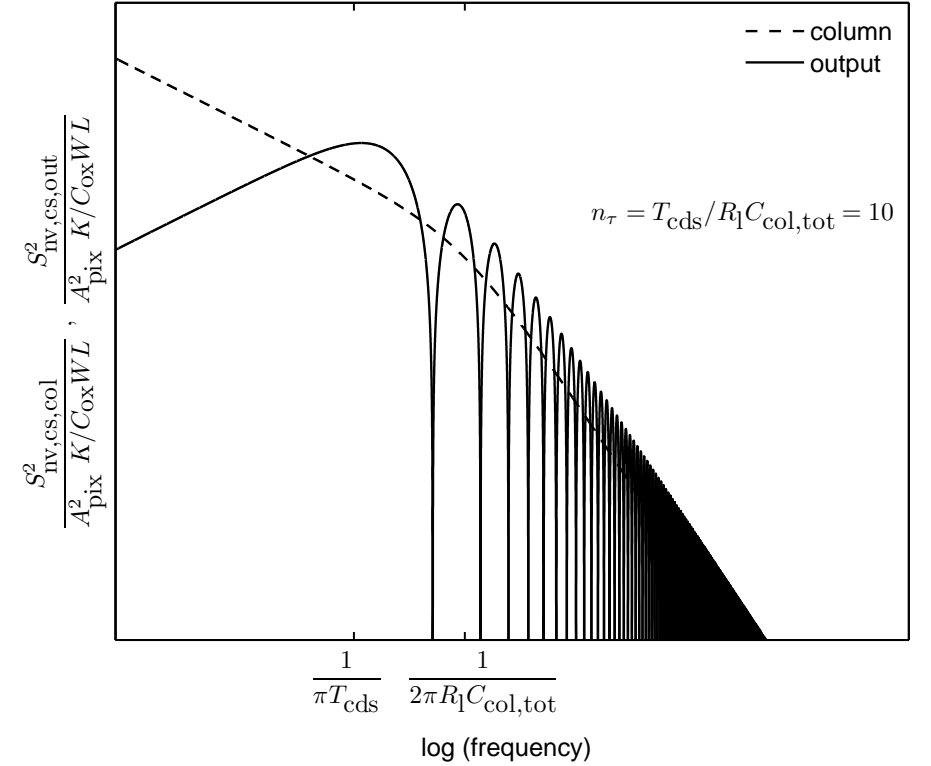


FIGURE 3.7 Normalized noise PSD of the pixel-level amplifier's flicker noise on the column line and on the output of the CDS operation

ences concerning electronic circuit noise, which generally is a significant noise component.

As opposed to conventional low-noise imagers, an image sensor using open-loop pixel-level amplification achieves effective bandwidth limitation, and hence low thermal noise of the pixel-level electronics, already on the column signal at reasonably low expenditure of column line capacitance. Therefore, such a sensor, does not need to rely on a column-level low-pass filter, such as a column-level voltage amplifier. Consequently, imperfections in the low-pass filtering behavior due to noise feed forward observed in switched-capacitor circuits are not an issue in an image sensor with pixel-level open-loop voltage amplification thanks to the perfect first-order low-pass frequency response free of zeroes.

In comparison to conventional low-noise image sensors, voltage amplifica-

tion is provided at an earlier stage. This results in nearly complete suppression of noise from downstream circuits in the signal processing chain. Particularly the noise due to column-level circuits is suppressed.

The virtually complete suppression of column-level circuit noise and the improved filtering of high-frequency thermal noise components of the pixel-level electronics results in a clear thermal noise performance advantage of the presented image sensor with column-level amplification over conventional low-noise image sensors.

3.2.4 Sense Node Capacitance

It has been outlined in Sect. 2.5.5 that sense node capacitance is a key parameter in a low-noise CMOS image sensor, as it influences the conversion factor from generated signal charge to signal voltage. Given the limited voltage swing, which can be processed by pixel-level, column-level, and chip-level circuits, the sense node conversion factor, and hence the sense node capacitance, defines the full well capacitance, i.e. the maximum amount of signal charge which can be processed. However, this consideration conflicts with the requirement of low sense node capacitance for the achievement of low electronic circuit noise equivalent charge, particularly for noise components affecting the signal chain prior to the application of voltage amplification. In the case of an image sensor with pixel-level voltage amplification, this consideration concerns the pixel-level voltage amplifier, as indicated by (3.8) and (3.11).

For analysis of the sense node capacitance of the implemented sensor with pixel-level voltage amplification, an equivalent schematic containing all relevant parasitic capacitances is given in Fig. 3.8. The resulting sense node capacitance is given in expression (3.12).

$$C_{sn} = C_{jun,n} + C_{ovlp,tx} + C_{jun,p} + C_{ovlp,res} + C_{wire,vcst} + C_{wire,sncol} (1 + A_{pix}) + C_{gs} + C_{gd}, \quad (3.12)$$

where $C_{jun,n}$ is the junction capacitance of the n-type sense node diffusion of the BPD, $C_{ovlp,tx}$ is the overlap capacitance of the same diffusion and the polysilicon transfer gate, $C_{jun,p}$ is the drain junction capacitance of the p-channel reset transistor, $C_{ovlp,res}$ is the gate-drain overlap capacitance of the reset transistor, $C_{wire,sncol}$ is the parasitic wiring capacitance between the sense node and the column line, $C_{wire,vcst}$ is the lumped remainder (not shown in Fig. 3.8) of the sense node parasitic wiring capacitance, C_{gs} is the gate-source capacitance of the common-source transistor, and C_{gd} is the gate-

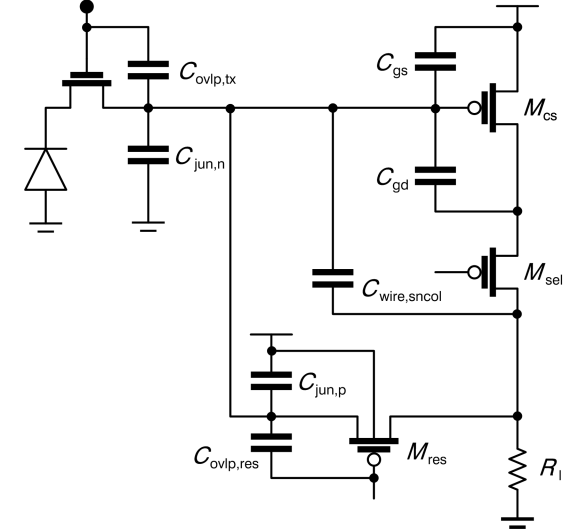


FIGURE 3.8 Parasitic capacitance components in a pixel with pixel-level voltage amplifier

drain overlap capacitance of the common-source transistor.

Detailed investigation of (3.12) reveals that particular attention has to be paid to the impact of capacitance multiplication by the Miller effect. This effect can be avoided for the non-negligible C_{gd} by imposing a constant drain voltage to the common-source amplifier thanks to cascode operation of the select transistor. The remaining Miller capacitance from the sense node to the column line $C_{wire,sncol}$ is a parasitic wiring capacitance. As opposed to C_{gd} , this capacitance can, however, be virtually eliminated by careful layout of the connecting metal tracks.

Besides capacitance multiplication by the Miller effect, which is avoided by the above mentioned measures, there are two differences between the sense node capacitance of a conventional pixel and the proposed pixel with pixel-level voltage amplification. First of all, the component of $C_{jun,p}$ might not exist in a conventional pixel, if the drain junction of the n-channel reset transistor and the n-type sense node diffusion of the BPD are merged in the physical design.

Furthermore, the impact of the gate-source capacitance of the source-follower transistor in a conventional pixel circuit is less pronounced than the impact of gate-source capacitance of the common-source transistor of a pixel-level amplifier. This is due to the fact that instead of fully contributing to the sense node capacitance, the gate-source capacitance of a source-follower transistor is weighted by a factor of $(1 - A_{sf})$, where the source-follower gain A_{sf} is positive

and close to unity. Therefore, the source-follower's gate-source capacitance contribution to the sense node capacitance is actually attenuated due to Miller effect involving a non-inverting near-unity-gain amplifier.

A compromise concerning the gate area of source-followers in conventional pixels or common-source transistors in pixel-level amplifying pixels needs to be found. While increased gate area reduces the flicker noise PSD, it also reduces the sense node conversion factor by increasing sense node capacitance. Optimization of the gate area is particularly important for image sensors featuring pixel-level amplifiers, since the contribution of the gate-source capacitance to the total sense node capacitance is not attenuated by Miller effect with non-inverting unity-gain amplification.

3.3 Sensor Implementation

A prototype sensor has been implemented in order to demonstrate the excellent noise performance achievable through pixel-level voltage amplification, as outlined in previous sections. Table 3.1 summarizes the most important specification points of the prototype which has been fabricated in an open-access $0.18\ \mu\text{m}$ process technology by UMC with optional image sensor process steps for fabrication of buried photodiodes.

TABLE 3.1 Selected parameters of the implemented prototype image sensor with pixel-level amplification

Parameter	Value
die size	$5 \times 5\ \text{mm}^2$
spatial resolution	256×256 pixels
pixel dimensions	$11 \times 11\ \mu\text{m}^2$
T_{row}	$16.7\ \mu\text{s}$

Die size was chosen equal to one seat size on a multi-project-wafer run in order to limit prototype fabrication cost. The resulting spatial resolution of 256×256 pixels is sufficient for prototype demonstration in many applications. Nevertheless, the entire design has been prepared for effortless upscaling to 1000 rows per column. This means that pixel arrays of up to 5.5 MPixels can be realized without any fundamental design modification in a 4:3 aspect ratio, if the column lines are split in the middle of the pixel array and readout circuits are situated at the top as well as at the bottom of the pixel array. The chosen row timing allows operation of the upscaled image sensor at a maximum speed of 60 frames/sec, if a relatively high number of analog multiplexers, buffers, and output pads are used, or if column-level ADCs with the ability of

conversion during column readout are incorporated. Figures 3.9 and 3.10 show a photograph of the packaged chip and a micrograph of a detail in the pixel array respectively.

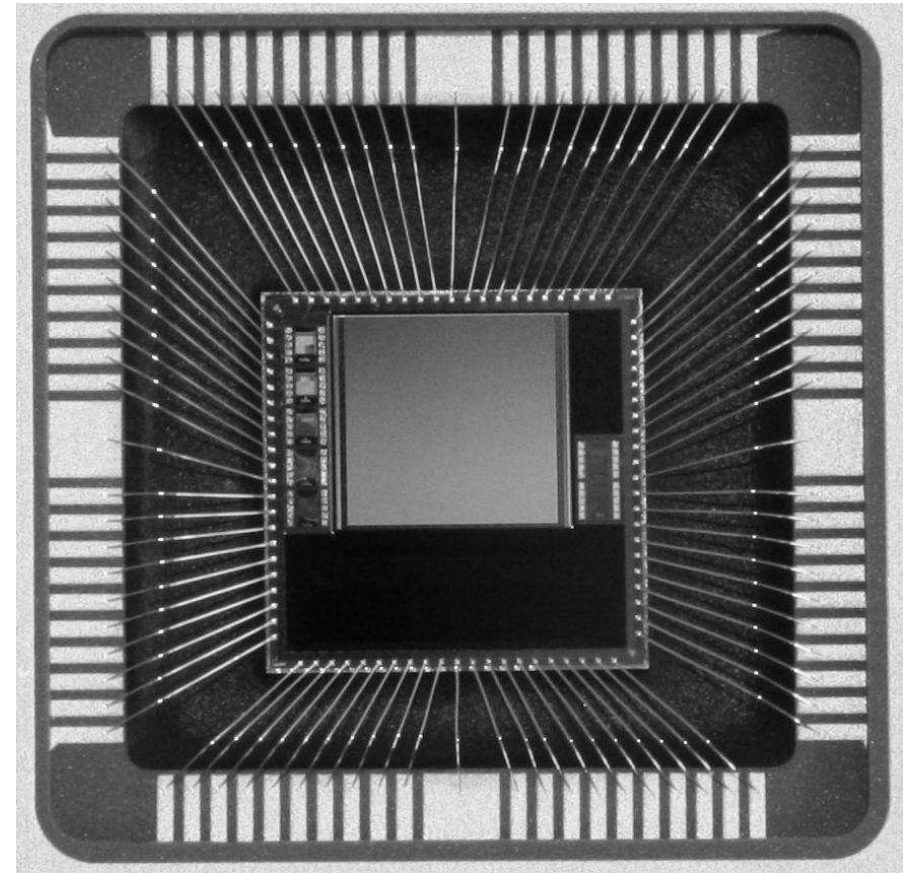


FIGURE 3.9 Macro photograph of the packaged prototype sensor

3.3.1 Aspects of the Sensor Design

The implementation of a prototype image sensor involves designing of many circuit blocks. Since most of them are based on well-known standard topologies, they are not covered in detail here. Instead emphasis is made on the design of the pixel including a pixel-level open-loop voltage amplifier.

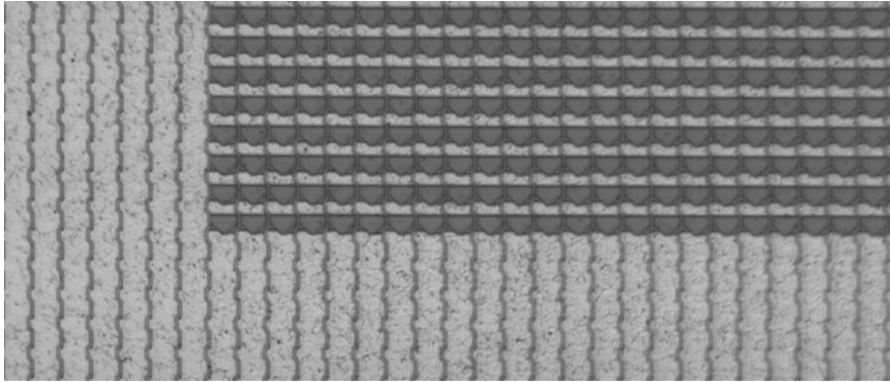


FIGURE 3.10 Micrograph showing a detail of the pixel array. The bottom and left sections show black (light shielded) pixels

Design Procedure for the Pixel-Level Amplifier

Despite the simplicity of the implemented pixel-level common-source open-loop amplifier, the dimensioning of such a circuit offers a few degrees of freedom. Conversely, a certain number of specified parameters usually need to be satisfied. In order to systematically fulfill specification criteria and optimize the performance of the circuit, the following design procedure can be used for instance. Obviously, several iterations might be needed in order to converge to a practical and feasible design.

Choice of pixel-level gain. The pixel-level gain is usually chosen based on the specification of the linear full-well capacity, the maximum voltage swing of column-level and chip-level processing circuits and an assumption of the total sense node capacitance. Since the pixel-level gain should be as high as possible for the best suppression of column-level circuit noise, but just low enough to avoid readout and processing of the full-well signal without saturation, the pixel-level voltage gain is chosen equal to the product of the voltage swing of the processing circuits times the sense node capacitance divided by the full-well charge. With A_{pix} being defined, inversion of (3.3) provides a unique value of the product of βR_1 for given power supply and transistor threshold voltages.

Choice of column capacitance. For a desired thermal noise equivalent charge, the required column capacitance $C_{\text{col,tot}}$ is found by inversion of (3.8).

Choice of R_1 and W/L . The frame rate and row number specifications in combination with the exact architecture dependent timing define T_{row} and T_{cds} . Insertion of the number of required time constants n_τ for accurate settling into (3.9) provides the value of the column time constant $R_1 C_{\text{col,tot}}$. This consequently defines the value of the load resistor R_1 , as $C_{\text{col,tot}}$ has been determined previously. This load resistor value also defines the value of β , i.e. of the W/L ratio of the common-source transistor, since the product of βR_1 has already been defined by the choice of pixel-level gain A_{pix} .

Optimization of the gate area. At this stage of the design procedure, the gate area of the common-source transistor is the last degree of freedom. A compromise between sense node capacitance and flicker noise PSD leads to the existence of an optimum common-source transistor gate area for minimum equivalent noise charge, as given by (3.13).

The optimum gate area is found by minimizing the sum of squares of the equivalent thermal noise and flicker noise charges, as given by (3.8) and (3.11), where the gate area dependent expression (3.12) of the sense node capacitance is inserted. In the general case, this optimization involves factorization of a 6th order polynomial equation. A simple closed analytical expression of the optimum gate area is found, however, if the gate width dependent gate-drain overlap capacitance of the common-source transistor is neglected:

$$a_{\text{cs,opt}} \approx \frac{V_{1/a}^2}{4V_{\text{cst}}^2} \left(-1 + \sqrt{1 + \frac{8V_{\text{cst}}^2 C_{\text{cst}}}{V_{1/a}^2 C_a}} \right), \quad (3.13)$$

where

$$C_{\text{cst}} = C_{\text{jun,n}} + C_{\text{ovlp,tx}} + C_{\text{jun,p}} + C_{\text{ovlp,res}} + C_{\text{wire,vcst}} + C_{\text{wire,sncol}} (1 + A_{\text{pix}}), \quad (3.14)$$

$$C_a = \frac{2}{3} C_{\text{ox}}, \quad (3.15)$$

$$V_{\text{cst}}^2 = \frac{2kT\gamma}{A_{\text{pix}} C_{\text{col,tot}}}, \quad (3.16)$$

and

$$\begin{aligned}
 V_{1/a}^2 &= \frac{K}{C_{\text{OX}}} \int_0^\infty |H_{\text{cds}}(f)|^2 \left| \frac{1}{1 + 2\pi f R_1 C_{\text{col,tot}}} \right|^2 \frac{1}{f} df \\
 &\approx \frac{K}{C_{\text{OX}}} \int_{1/\pi T_{\text{cds}}}^{n_\tau/2\pi T_{\text{cds}}} 2 \frac{1}{f} df \\
 &= \frac{2K}{C_{\text{OX}}} \ln\left(\frac{n_\tau}{2}\right) .
 \end{aligned} \tag{3.17}$$

Numerical parameter values of the design procedure, as described above are given in Table 3.2. The parameters of the gate area optimization are listed separately in Table 3.3, where $C_{\text{OX}} = 5 \text{ fF}/\mu\text{m}^2$ and $K = 1.2 \cdot 10^{-24} \text{ V}^2\text{F}$ have been assumed. Additionally, the total flicker and thermal noise for the design values listed in Tables 3.2 and 3.3 according to the model of the gate area optimization, i.e. neglecting the common-source transistors's gate-drain capacitance, is shown in Fig. 3.11 as a function of gate area.

TABLE 3.2 Design parameters of the pixel-level open-loop amplifier

Specified Parameter	Value	Calculated Parameter	Value
A_{pix}	10	βR_1	14.8 V^{-1}
$C_{\text{col,tot}}$	3.3 pF		
T_{cds}	$8 \mu\text{s}$	R_1	303 k Ω
n_τ	8	β	48.9 $\mu\text{F}/\text{Vs}$
μC_{OX}	$16.4 \mu\text{F}/\text{Vs}$	W/L	2.98

Simulation Results

Design of an entire image sensor involves a number of simulations for verification of connectivity and functionality of the chip as well as for verification of design parameters that have been obtained by hand calculations. For instance, the simulated pixel-level amplifier transfer curve, as shown in Fig. 3.4, has been used in order to verify the calculated reset voltage and small signal gain values.

Simulations can, assuming validity of the involved simulation models, be used for empirical optimization. A combination of AC simulations for deter-

TABLE 3.3 Parameters of the common-source transistor's gate area optimization

Parameter	Value
C_{cst}	3.8 fF
C_a	$3.33 \text{ fF}/\mu\text{m}^2$
V_{cst}^2	$167 (\mu\text{V})^2$
$V_{1/a}^2$	$665 (\mu\text{V})^2(\mu\text{m})^2$
$a_{\text{cs,opt}}$	0.81 μm^2
W	1.55 μm
L	0.52 μm

mination of the sense node capacitance based on circuit extraction of parasitic capacitances in the pixel and small signal noise simulations have been used in order to optimize the equivalent noise charge. The result of the analytical gate area optimization, as presented above, has been used as a starting point for a series of such simulations. The optimum gate area of $0.48 \mu\text{m}^2$ found by simulation is slightly smaller but not fundamentally different from the analytical solution, which confirms the validity of the presented analytical optimization method. The difference may be explained, besides many other approximations taken in the analytical approach, by the following two reasons: First of all, neglecting the gate-drain overlap capacitance of the common-source transistor, which is proportional to the square root of the gate area, leads to slightly too high gate area from the analytical optimization. Secondly the noise PSD of the flicker noise in the simulation must be slightly lower than the assumed value for analytical calculation, since the optimum equivalent noise charge from simulation is smaller (1.2 electrons) even at smaller gate area than the analytical solution (1.3 electrons).

For the implementation of the image sensor, the optimum gate area from simulation has been chosen, which in comparison to the gate area from analytical optimization provides an improved pixel fill factor resulting from the smaller common-source transistor geometry. The final design parameters thus exactly correspond to the values given in Tables 3.2 and 3.3 except for the gate dimensions which are $W = 1.2 \mu\text{m}$ and $L = 0.4 \mu\text{m}$ from simulation based optimization. The simulated column line noise PSD for the implemented design is shown in Fig. 3.12 and a breakdown of the results of the extracted AC simulation and noise simulation is given in Table 3.4. For the simulated pixel conversion factor of $300 \mu\text{V}/e^-$, noise of well-designed readout and signal processing circuitry will be perfectly negligible and the pixel-level amplifier noise can be considered approximately as the overall noise. Furthermore, the previ-

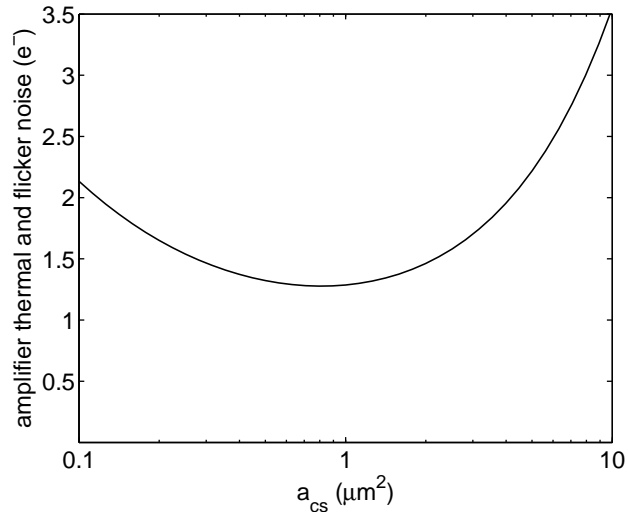


FIGURE 3.11 Calculated thermal noise and flicker noise equivalent charge as a function of the common-source transistor gate area

ously assumed approximation of negligible thermal noise from the load resistor is confirmed by the simulation result. These considerations confirm that pixel-level amplification can virtually suppress electronic noise of all involved circuits except for one single transistor, i.e. the common-source transistor of the pixel-level amplifier. Comparison of the thermal noise and flicker noise components of the common-source transistor shows that the capacitance multiplication effect due to voltage amplification reduces thermal noise to a level clearly below flicker noise. This flicker noise level actually constitutes the flicker noise limit, since the CDS sampling time difference in this sensor corresponds to the absolute minimum required for signal settling thanks to rolling shutter operation and the use of buried photodiodes. In more quantitative words, the simulation results show that the overall electronic circuit noise of the presented CMOS image sensor with pixel-level amplifiers exceeds the flicker noise limit by less than 10%.

Pixel Layout

The implemented pixel has a horizontal and vertical pixel pitch of $11 \mu\text{m}$ as listed in Table 3.1. The pixel layout is, however, not drawn in a square shape, but using a staggered shape, as shown in Fig. 3.13, in order to achieve a more convenient aspect ratio of the pixel-level electronics. The fill factor of the pixel, i.e. the ratio of sensitive area to overall area, is 50%. Particular attention has

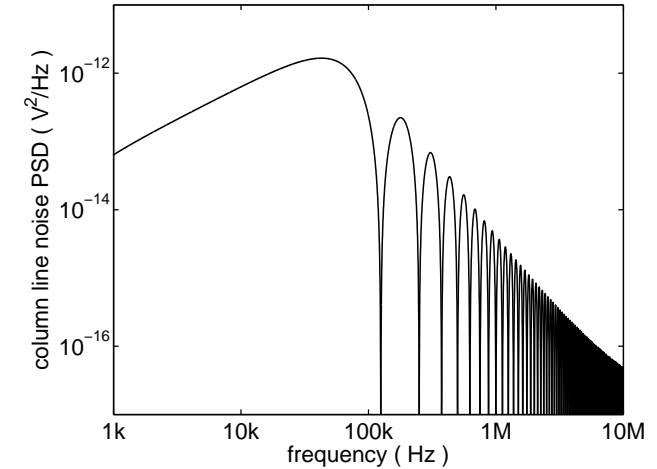


FIGURE 3.12 Simulated noise power spectral density of the pixel-level amplifier

been paid to minimizing the parasitic wiring capacitance $C_{\text{wire,sncol}}$ between the sense node and the column line, which would have a multiplied impact on the effective sense node capacitance due to Miller effect. Since the sense node wiring is implemented using the first metal layer of the process and the column line necessarily needs to be connected to the select transistor and the reset transistor by use of the first metal layer, significant sidewall coupling capacitance between these metal elements could arise. In order to avoid this effect, a shielding structure connected to the DC power supply voltage, as illustrated in Fig. 3.13, has been inserted between the metal elements of the sense node and the column line. Layout parasitic extractions have shown this measure to reduce $C_{\text{wire,sncol}}$ below a detection threshold of 0.01 fF at an acceptable increase of the remainder of the sense node capacitance due to the additional metal element used for shielding.

Sensor Layout

The layout of the prototype image sensor, as shown in Fig. 3.14, demonstrates the fact that little silicon area is required for excellent thermal noise performance thanks to the use of pixel-level voltage amplification.

The parasitic capacitance of a larger pixel array could be sufficient to achieve the required low-pass filtering effect. In the case of the prototype sensor with as few as 256 pixels per column, an additional capacitance of 2.25 pF per column in parallel with the load resistor has been physically placed between the pixel array and the load resistors. The load resistors have been implemented as polysilicon resistors with a p-type doping and a relatively low sheet

TABLE 3.4 Simulated noise of the implemented pixel-level open-loop amplifier

Parameter	Value	
C_{sn}	5.3 fF	
A_{pix}	10	
pixel conversion factor	302 $\mu\text{V}/e^-$	
Noise Component	Column Voltage	Equivalent Charge
M_{CS} flicker	337 μV	1.1 e^-
M_{CS} thermal	120 μV	0.4 e^-
R_1 thermal	44 μV	0.15 e^-
total	366 μV	1.2 e^-

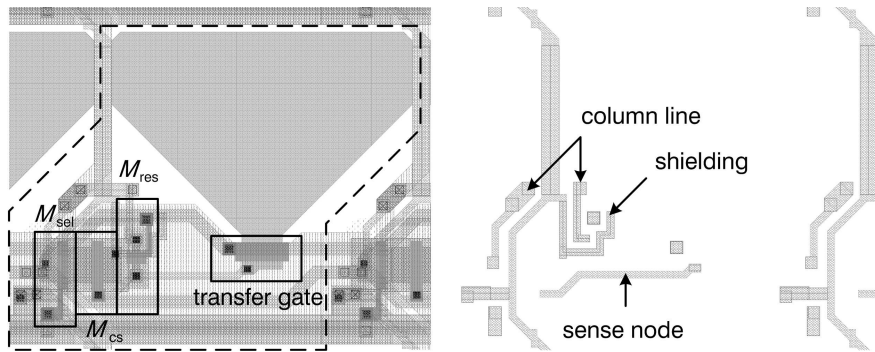


FIGURE 3.13 Pixel layout of a pixel with a pixel-level amplifier (left) and first metal layer of the layout (right)

resistance of about 300 Ω /square. Note that the additional column load capacitance and the load resistors are less than 200 μm long, which corresponds to less than 20 rows of pixels in the array. For larger image sensors not requiring any additional column line load capacitance and using high-ohmic polysilicon resistors of several $\text{k}\Omega$ /square to several tens of $\text{k}\Omega$ /square, as available in most CMOS process technologies, the required area for the column periphery can potentially be reduced even further.

Note that for historic reasons the sample-and-hold circuits as well as the routing between the sample-and-hold circuits and the analog multiplexers are not area optimized. For the design of an area-efficient upscaled image sensor, these peripheral circuits, which are not critical for the noise performance, would need to be modified or, if an image sensor with column-parallel ADCs is implemented, they would be replaced anyway.

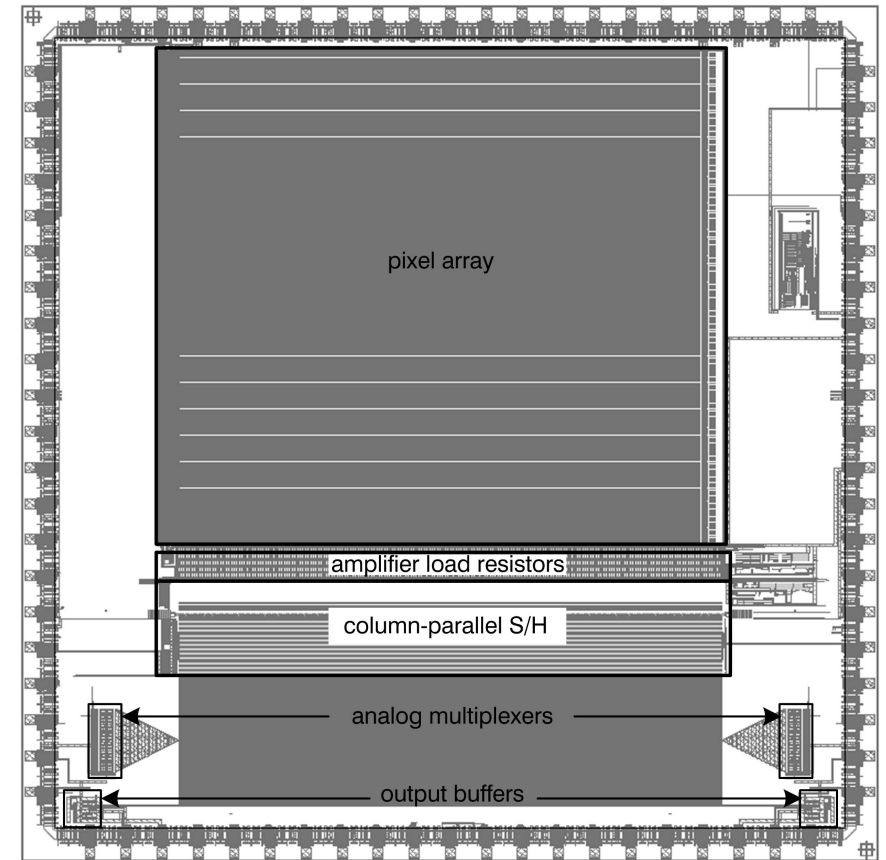


FIGURE 3.14 Layout of the prototype image sensors with 256 x 256 pixels with pixel-level voltage amplifiers

3.3.2 Characterization Results

The implemented image sensor with pixel-level voltage amplifiers has been characterized using an electronics board containing a Field Programmable Gate Array (FPGA) for flexible control of the sensor timing, board-level ADCs and a Universal Serial Bus (USB) interface for data transfer to a computer. For many measurements red light-emitting diodes (LED) in an integration sphere (Ulbricht sphere) have been used in order to create homogeneous illumination of the pixel array. An optical power meter coupled to the integration sphere was used in order to monitor irradiance values. However, reproducible positioning of the sensor with respect to the opening of the integration sphere

and calibration of the actual irradiance on the sensor with the optical power meter proved difficult. Therefore, irradiance values displayed in the presented results should not be considered as absolute values. Note that the precision of the most important numerical parameters, such as readout noise, dark noise, full well capacity, dynamic range, linearity, and PRNU, do not rely on these measured irradiance values. For the generation of low irradiance, optical attenuation filters have been used. Unless otherwise stated, a default exposure time of 16 ms has been used with all measurements being performed at room temperature.

The following subsections provide a non-exhaustive set of measurement results with an emphasis on precise evaluation of the noise performance as well as on linearity and photoresponse non uniformity which are potentially problematic parameters of an image sensor based on open-loop voltage amplification.

Photoresponse and PRNU

The measured photoresponse, as shown in Fig. 3.15, qualitatively reflects the DC characteristics of the pixel-level voltage amplifier, as shown in Fig. 3.4. The linear part of the photoresponse extends up to $0.2 \mu\text{W}/\text{cm}^2$, whereas an irradiance swing of $1.4 \mu\text{W}/\text{cm}^2$ is achieved, if the compressed part of the photoresponse is used as well.

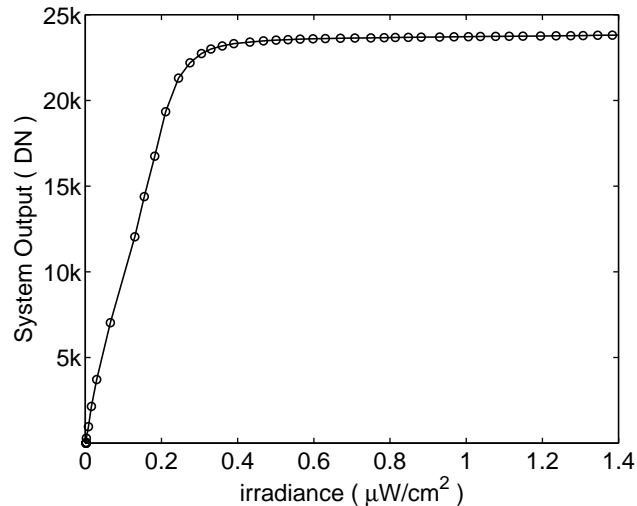


FIGURE 3.15 Mean photoresponse of the image sensor with pixel-level voltage amplification at an exposure time of 16 ms

The non-linearity in the linear range is shown in Fig. 3.16 and the peak linearity error, as defined by the EMVA Standard 1288 [57], in the range from zero to $0.2 \mu\text{W}/\text{cm}^2$ is 1.7%. This non-linearity is acceptable for a very wide range of applications and is fully competitive with the non-linearity of conventional CMOS image sensors.

A periodic component of non-linearity with a period of approximately $0.03 \mu\text{W}/\text{cm}^2$ is observed. This component is believed to be a measurement artifact possibly due to subrange switching of the optical power meter used for the irradiance measurement. The amplitude of this component does, however, not have a significant impact on the measured peak linearity error.

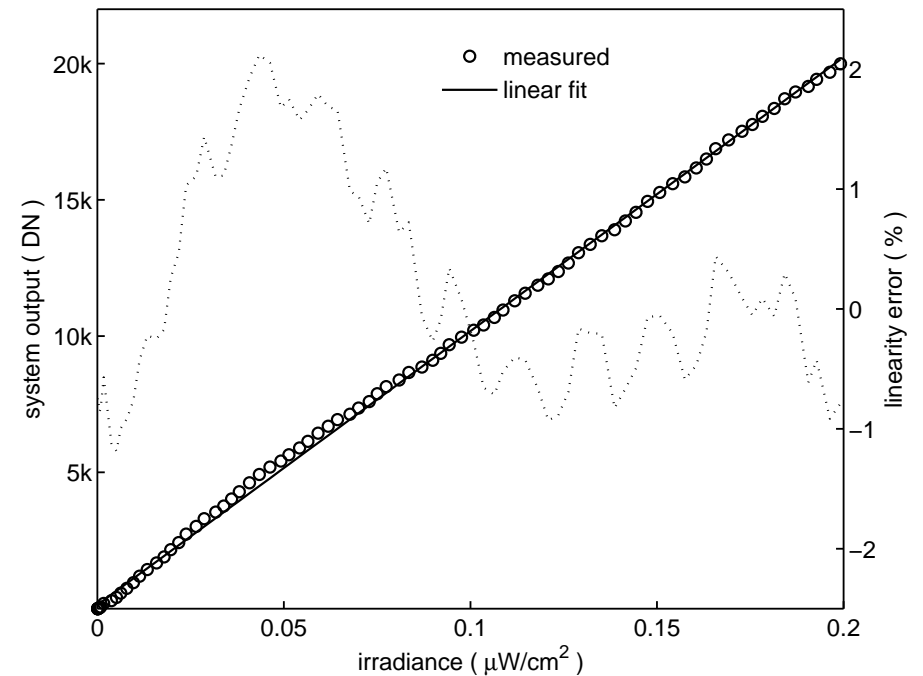


FIGURE 3.16 Linear part of the photoresponse, linear fit, and linearity error

A further critical parameter of a CMOS image sensor employing open-loop amplification is pixel-to-pixel spread of the photoresponse. As illustrated in Fig. 3.17, the spread has different impact on the linear part and on the compressed part of the response. As a matter of fact, the kink between the linear and compressed parts corresponds to the transition of the common-source transistor's operation region from saturated to triode. The swing between the reset

point, i.e. the zero signal in Fig. 3.17, and the kink is approximately equal to the threshold voltage of the common-source transistor. This illustrates that the combination of the reset configuration in unity gain feedback and CDS does not eliminate the impact of threshold mismatch on the kink spread. Figure 3.17 shows that uncompressing the compressed part of the response using a fixed inverse compression function will not provide any satisfying results, since the spread of the response has the same order of magnitude as the amplitude of the entire compressed part. Separate readout of the reset levels of all pixels, i.e. of the common-source transistor's threshold voltage, and uncompressing the response of every pixel with a threshold-voltage-dependent function would, therefore, be required to make use of the compressed part of the photoresponse.

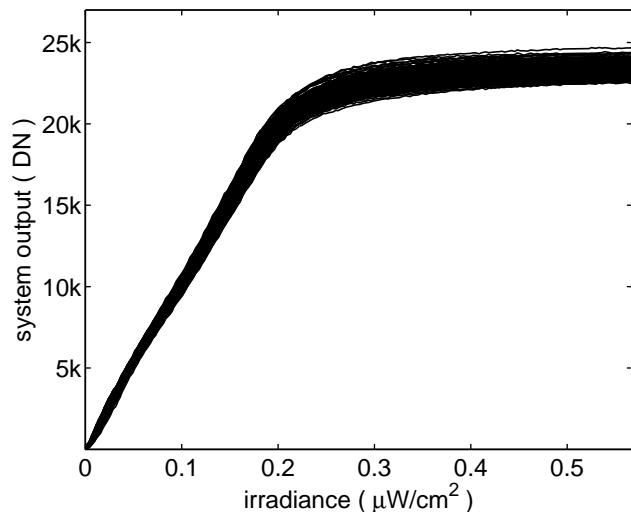


FIGURE 3.17 Photoresponse curves of 256 different pixels

Investigation of the linear part of the photoresponse shows, however, that the impact of threshold mismatch on the amplifier's open-loop-gain is successfully suppressed by use of the reset configuration using unity-gain feedback, as described in Sect. 3.2.1. Analysis of the linear responsivity histogram, as shown in Fig. 3.18, provides a photoresponse non-uniformity (PRNU) of 2.5%, a value which is absolutely competitive with conventional CMOS image sensors. Besides decent suppression of the threshold voltage mismatch, this result also illustrates that mobility and geometry variations do not have an excessive impact on the gain spread of the pixel-level amplifier.

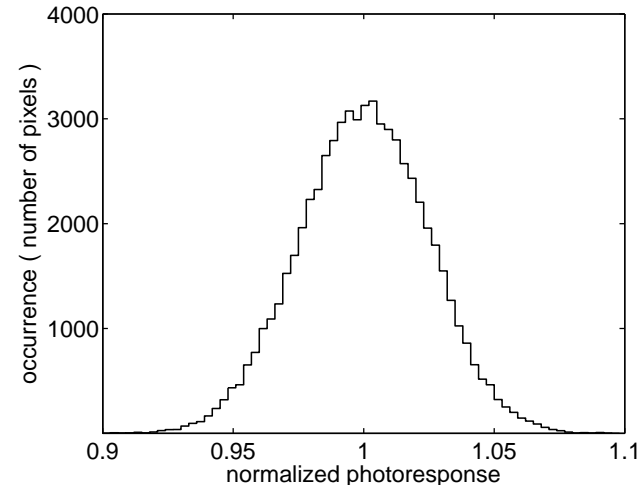


FIGURE 3.18 Histogram of the linear responsivity of 65536 pixels

Conversion Factor

The system conversion factor CF_S , i.e. the digital output of the board-level ADC per signal charge on the sense node of a pixel, is a crucial value for the evaluation of the equivalent noise charge of an image sensor. CF_S can, for instance, be expressed as a product of the pixel conversion factor times the signal processing gain from column-parallel circuits to the output of the board-level ADC. Whereas the signal processing gain is usually well known from simulations and calculations, the pixel conversion factor, i.e. the ratio of column line voltage over sense node signal charge is usually less predictable. The main reason for this is that the sense node capacitance is in a very low region, where calculation models for junction capacitances and layout extraction algorithms for parasitic wiring capacitance may suffer from limited precision. Although not straightforward, measurement of CF_S is, therefore, more desirable than relying on a theoretical value.

A good way to extract CF_S from measurements is the interpretation of the system's photon transfer curve, as suggested in [58]. This method relies on the properties of photon shot noise and involves plotting of the noise of the system versus the mean output of the system in the logarithmic domain for a series of different image sensor illumination values. In the region of high irradiance, where photon shot noise is the predominant noise component, the following y -axis and x -axis values of the photon transfer curve are derived from (2.1):

$$x = \log(CF_s n_{pe}) \quad , \quad (3.18)$$

$$y = \log(CF_s \sqrt{n_{pe}}) \quad , \quad (3.19)$$

and

$$y = \frac{\log(CF_s)}{2} + \frac{1}{2}x \quad . \quad (3.20)$$

In the above expressions the system conversion factor CF_s is expressed in digital number (DN) per electron and n_{pe} is the number of generated photoelectrons. Investigation of (3.20) reveals that the photon shot noise dominated part of the photon transfer curve is identified by its slope of 1/2 in the logarithmic domain and, more importantly, that the offset of the photon transfer curve, which is equal to $0.5 \log(CF_s)$, is purely depending on the system conversion factor. The system conversion factor is, therefore, obtained from extrapolating the value at $x = 0$ of the photon shot noise dominated part of the photon transfer curve.

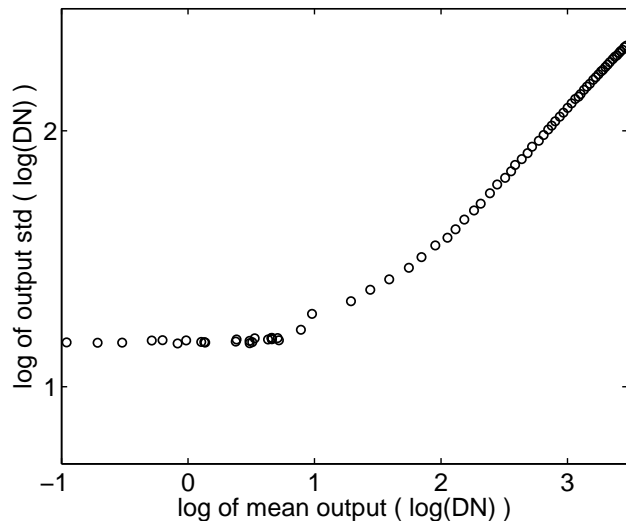


FIGURE 3.19 Photon transfer curve

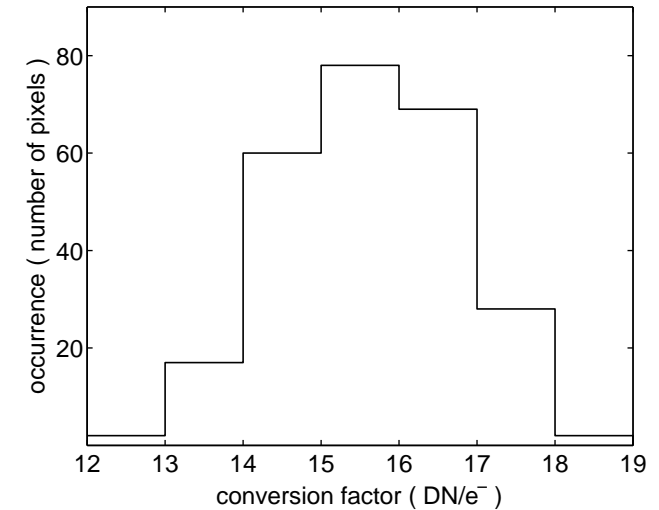


FIGURE 3.20 Histogram of calculated conversion factor values for 256 pixels

Several hundred measurements have been acquired with 256 pixels for each step of a series of irradiance values. From the mean values and standard deviation values of the measurements for each irradiance step, a photon transfer curve for each pixel is obtained. Figure 3.19 shows the average of the photon transfer curves of all pixels and Fig. 3.20 gives the histogram of the system conversion factors for all pixels. Note that the spread of calculated conversion factors is wider than the measured PRNU. This illustrates that the number of measurements was not sufficient to reduce the interpolation accuracy below the actual spread of the conversion factor. The average system conversion factor of 15.6 DN/e⁻ is, however very reproducible over different pixel subsets of the array and over repeated measurements. The distribution of the slopes of the photon shot noise dominated part of the photon transfer curve, as shown in Fig. 3.21, is centered around the value of 0.52, which is reasonably close to the ideal value of 0.5. Calculation of the pixel conversion factor from the obtained system conversion factor and the theoretical signal chain amplification results in a value close to the designed value of 300 $\mu\text{V}/e^-$.

Dark Noise and Dynamic Range

The noise equivalent charge for the entire system is easily obtained from measurement of the output noise thanks to the knowledge of CF_s . Note that this determination of the noise equivalent charge fully relies on measured data. Thanks to the high pixel conversion factor as well as the use of high resolution board-level ADCs, the noise of board-level electronics is negligible and the

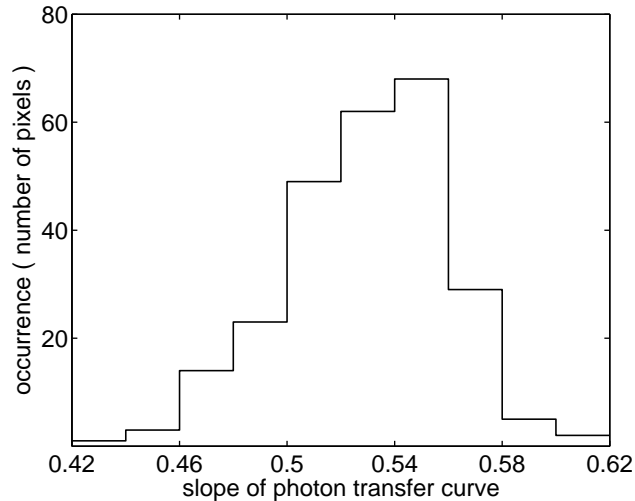


FIGURE 3.21 Histogram of the fitted photon transfer curve slope for 256 pixels

measured system noise can be considered equal to the image sensor noise. The *readout noise* has been measured by use of the standard operating sequence but using a very short exposure time of $50 \mu\text{s}$ in order to suppress the effect of photodiode leakage.

Analysis of the readout noise reveals a component of temporal row noise which is due to power supply voltage noise. The underlying mechanism is that a random temporal variation of the power supply voltage, used as a source voltage of the pixel-level common-source amplifier, between the sampling times of the column line reset level and the signal level results in a random error in the output signal after CDS. This random error is, however, approximately *identical* for the *simultaneously* sampled signals of an entire pixel row. The implemented sensor, therefore, includes 16 black columns, i.e. 16 pixels on each row that are shielded from light. The average over these black pixels' outputs gives a good approximation of the temporal row noise and the subtraction of the average black pixel level from the active pixel output results in effective cancellation of temporal row noise. This noise correction is a very quick and simple calculation in terms of computing power, since the black pixel data is available simultaneously with the values of a row's active pixel and the correction computation is a simple averaging of 16 values per row plus a single subtraction per pixel. For these reasons, very short computation time is used and virtually no memory is required, since the row noise correction is a real-time row-wise operation. Figure 3.22 gives the histogram of the RMS readout

noise equivalent charge for 256 pixels with row noise corrections based on the 16 available black columns and Table 3.5 gives the median noise of all pixels without row noise correction, with row noise correction based on the black columns, as well as the temporal standard deviation of temporal row noise measured by the average of the black pixels of one single row. Additionally, the degree of row noise cancellation by using 16 black columns is compared to the full noise cancellation by subtracting the mean value of the entire row including the active pixels. This cancellation procedure obviously has no practical use, since it works only in the dark. This ideal value is, however, not much lower than the readout noise charge of 0.86 electrons achieved with practical correction based of a few black columns.

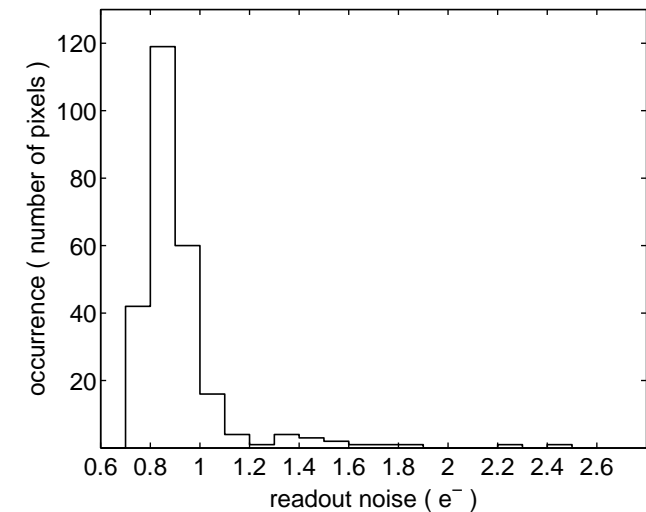


FIGURE 3.22 Histogram of the total RMS readout noise equivalent charge for 256 pixels at an exposure time of $50 \mu\text{s}$

TABLE 3.5 Median readout noise equivalent charge

Measured Noise	Equivalent Noise Charge
RMS temporal row noise	$0.60 e^-$
without row noise correction	$1.02 e^-$
with full row noise correction	$0.81 e^-$
with black column based correction	$0.86 e^-$

Combining the noise measurements with the full well capacity, as calculated from the photoresponse and the conversion factor, the linear dynamic range and the full dynamic range are summarized in Table 3.6.

TABLE 3.6 Calculation of full well capacity and dynamic range

Parameter	Linear Part	Full Photoresponse
maximum irradiation	$0.2 \mu\text{W}/\text{cm}^2$	$1.4 \mu\text{W}/\text{cm}^2$
linear system responsivity	$3.19 \times 10^5 \text{ DN cm}^2/\mu\text{W}$	$3.19 \times 10^5 \text{ DN cm}^2/\mu\text{W}$
lin. sys. conversion factor	$15.6 \text{ DN}/e^-$	$15.6 \text{ DN}/e^-$
readout noise	$0.86 e^-$	$0.86 e^-$
Full well capacity	$4091 e^-$	$28637 e^-$
Dynamic Range	73.5 dB	90.4 dB

Note that the linear system responsivity used in the dynamic range calculations is not consistent with the data displayed in Figs. 3.15 and 3.16. The reason for this is a minor shortcoming in the validation board which required switching of the board level gain in order to measure the compressed part of the photoresponse. The calculated full well capacity value and dynamic range values are, however, achieved by the image sensor in a single readout operation without mode switching. In other words, the presented dynamic range values are an expression of the actually achieved intra-scene dynamic range.

As a complementary information to the readout noise, the dark noise was determined at a target exposure time of 16 ms. With black column based correction of the temporal row noise due to power supply noise, the median dark noise, as found from the distribution in Fig. 3.23, is 1.4 electrons. The difference of this result and the measured read noise noise at virtually zero exposure time is due to leakage shot noise. A dark current shot noise component of about 1.2 electrons is calculated which corresponds to an integrated mean dark current signal of about 1.5 electrons in 15 ms.

Pictures

Despite their very qualitative nature, test pictures can provide a global information about the combined effect of fixed pattern noise, photoresponse non-uniformity, pixel defects and temporal noise. The test image provided in Fig. 3.24 is a raw image without correction of temporal row noise taken with lighting conditions adjusted to use a substantial share of the linear full well capacity in the brighter pixels.

The picture of Fig. 3.25 shows the same scene in low-light conditions with temporal row noise correction based on the sensor's black columns and column fixed pattern noise correction based on 5 black rows of the pixel array. Both

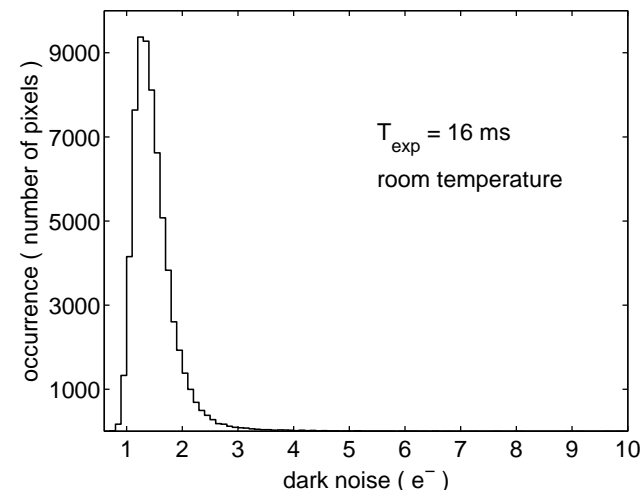


FIGURE 3.23 Histogram of the total RMS dark noise equivalent charge for all 65536 pixels at an exposure time of 16 ms. Median value: $1.4 e^-$

corrective computations are based on data available with every frame and, therefore, do not require acquisition of any calibration data. The average signal in this picture is 6 photoelectrons which, according to (2.1), results in a photon shot noise of 2.4 electrons. Comparison of this result to the sensor's dark noise floor of 1.4 electrons illustrates that the signal-to-noise ratio in most regions of the picture is still photon shot noise limited even at these very low signal conditions.

Conclusions from the Characterization Results

Characterization of the noise performance has revealed a readout noise performance even slightly better than the simulated performance. The difference is believed to be due to an overestimation of the flicker noise PSD by the simulation model. The readout noise floor of 0.9 electrons as well as the dark noise floor of 1.4 electrons actually define the presently achievable cutting edge noise performance of CMOS image sensors.

Given its very low noise thermal noise component, the presented CMOS image sensor architecture with pixel-level voltage amplifiers will take a direct benefit from future improvements in BPD leakage current by process technology improvements or from reduction of the flicker noise constant due to technology improvements or use of buried channel transistors.

Characterization has also shown that potentially critical parameters of an image sensor with pixel-level amplification such as susceptibility to power sup-



FIGURE 3.24 Raw image of the sensor with good lighting conditions



FIGURE 3.25 Row temporal noise corrected and column fixed pattern noise corrected image with a maximum of 24 and an average of 6 photoelectrons per pixel

ply noise, linearity, and photoresponse non-uniformity can be well controlled and are absolutely competitive with conventional low-noise CMOS image sensors.

Chapter 4

A Novel Ultra-Low-Noise CMOS Image Sensor Concept Based on Column-Level Open-Loop Amplification

4.1 Introduction

State-of-the-art low-noise CMOS image sensors suffer from noise generated by their column-level amplifiers as well as imperfections in the low-pass filtering function applied to the thermal noise of the pixel-level source-follower. An image sensor with pixel-level open-loop voltage amplifiers, as presented in chapter 3, solves both of these issues and achieves an extremely low sense node referred noise voltage. It has been shown in section 3.2.4 that the sense node capacitance of an image sensor with pixel-level amplifiers is slightly higher than in the case of conventional CMOS image sensors. The resulting reduction of the sense node conversion factor is, however, more than compensated by the reduction of sense node referred noise voltage. The image sensor with pixel-level voltage amplification, therefore, defines the current cutting edge in terms of of readout noise equivalent charge in combination with excellent dynamic range thanks to its large full-well capacity resulting from relatively high sense node capacitance. The concept of using a unity-gain pixel-level buffer, i.e.

a conventional source-follower, and a moderate-gain open-loop column-level amplifier, as presented in this chapter, combines the advantages of low sense node capacitance and effective low-pass filtering of the pixel-level circuit's thermal noise. Concerning the self-generated noise of the column-level open-loop amplifier, a compromise between noise performance and load capacitance, i.e. silicon area, has to be found. If the column-level open-loop amplifier has a degenerate common-source topology, this trade-off is found to be advantageous in comparison to the switched-capacitor amplifiers in conventional image sensors.

Calculations and simulation results show that the presented concept based on column-level open-loop amplification can potentially achieve even lower equivalent noise charge than an image sensor with pixel-level amplification at the price of increased silicon area of the column-parallel circuits as well as reduced full well capacity due to reduced sense node capacitance.

Measurement results of fabricated test circuits have reached 1.0 electron of readout noise equivalent charge without suppression of power supply noise. Row noise suppression based on black columns can potentially reduce the readout noise to a value below 0.8 electrons in future implementations of a full pixel array.

4.2 Topology and Analysis

Conventional APS pixels with pixel-level source-followers can achieve lower sense node capacitance than pixels with a pixel-level voltage amplifier. As outlined in section 3.2.4, the main reason for this is the reduced weighting of the gate-source capacitance of a source-follower transistor in comparison to the gate-source capacitance of a common-source amplifier input transistor. The image sensor topology presented in this chapter takes advantage of the low sense node capacitance of pixels employing source-followers, but uses them in conjunction with degenerate common-source column-level open-loop amplifiers. This amplifier topology provides first order low-pass filtering of the source-follower noise without occurrence of any zeroes in the relevant frequency range, i.e. without noise feed forward effect. Furthermore, the noise performance of degenerate common-source amplifiers is advantageous over the noise performance of conventional OTA based column-level amplifiers with noise excess factors of the input transistors greater than one. The noise of the open-loop amplifier of the presented topology is, therefore, lower than the noise of a conventional column amplifier with equal required capacitance area in the column-parallel circuit.

The potential problems of excessive operating point variations of the open-loop amplifier are avoided with a solution similar to that one used in the pixel-level amplifier described in the previous chapter. A voltage feedback configuration of the column-level open-loop amplifier for sense node reset is

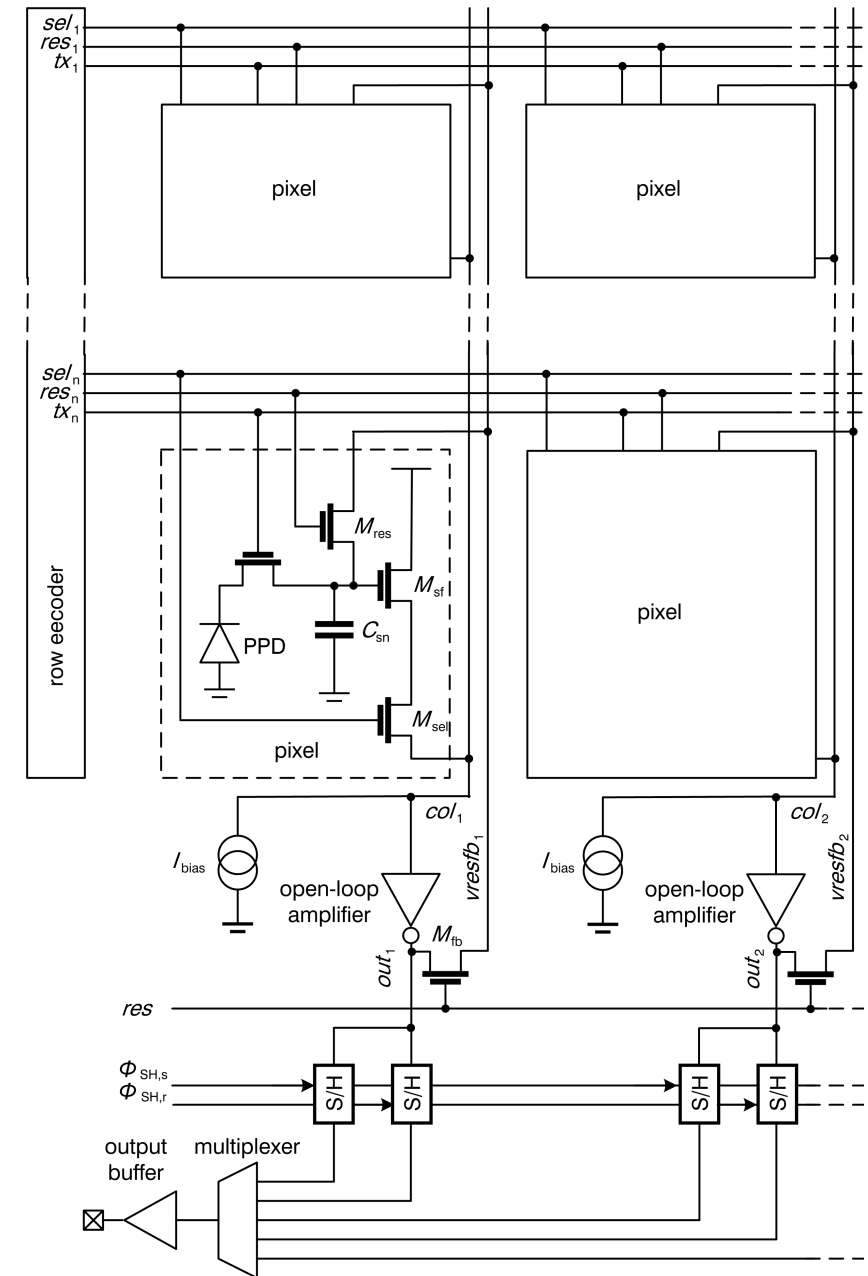


FIGURE 4.1 Architecture of an analog low-noise CMOS image sensor with column-level open-loop amplifiers

used instead of a reset to a given constant voltage, as employed in conventional image sensors. This means that a reset voltage feedback line from the amplifier's output to the drain of the pixel-level reset transistor is needed. As illustrated in the architecture schematic of Fig. 4.1 this reset signal v_{resfb_i} is a column-wise shared line. Since this reset line replaces the globally shared reset node used in a conventional image sensor, the number of wires per pixel is not increased. The only, very acceptable, restriction is that the feedback reset signal needs to be routed along the vertical direction of the pixel array, whereas the global reset wiring in conventional sensors may be vertical or horizontal. Besides this detail, the pixel array of the presented architecture is actually identical to pixel arrays of conventional image sensors.

The column-parallel circuitry consists of a bias current source, an open-loop amplifier, two sample-and-hold circuits for sampling of the reset level and the signal level from the output of the open-loop amplifier, and a feedback switch M_{fb} which can connect the output of the open-loop amplifier to the reset voltage feedback line.

The presented sensor concept with column-level open-loop amplification can be used with a rolling shutter operating sequence and short sampling time difference CDS operation, as illustrated in the timing diagram of Fig. 4.2. Note that the res signal is used to connect the column feedback line to the output of the open-loop amplifier whenever the reset transistor in any of the pixels of the column is active.

This operation results in two different possible configurations of the open-loop column-level amplifier and a selected pixel of the array, as illustrated in Fig. 4.3. In the first configuration, called the sense node reset configuration, a closed negative feedback loop exists between the sense node of the selected pixel, the source-follower, the column signal line, the inverting open-loop amplifier and the column feedback line. The reset voltage of the sense node established in this configuration is defined by the operating point of the amplifier with its input voltage equal to its output voltage minus the gate-source voltage shift of the pixel-level source-follower. In other words, the sense node reset voltage is defined by the intersection of the column line-to-output DC transfer function of the open-loop amplifier and the sense node-to-column transfer function of the source-follower, as sketched in Fig. 4.4. This graphical illustration shows that a shift of the amplifier characteristics due to threshold voltage variation of the input transistor, i.e. a horizontal shift of the amplifier transfer function along the column voltage axis, is tracked by a shift of the sense node reset voltage. This tracking results in a shift of the amplifier output voltage in the reset state by as little as the threshold variation of the amplifier's input transistor. Note that the amplifier's output shift would have been as high as the input transistor's threshold variation *amplified by the open-loop gain* if the sense node had been reset to a fixed voltage. This comparison illus-

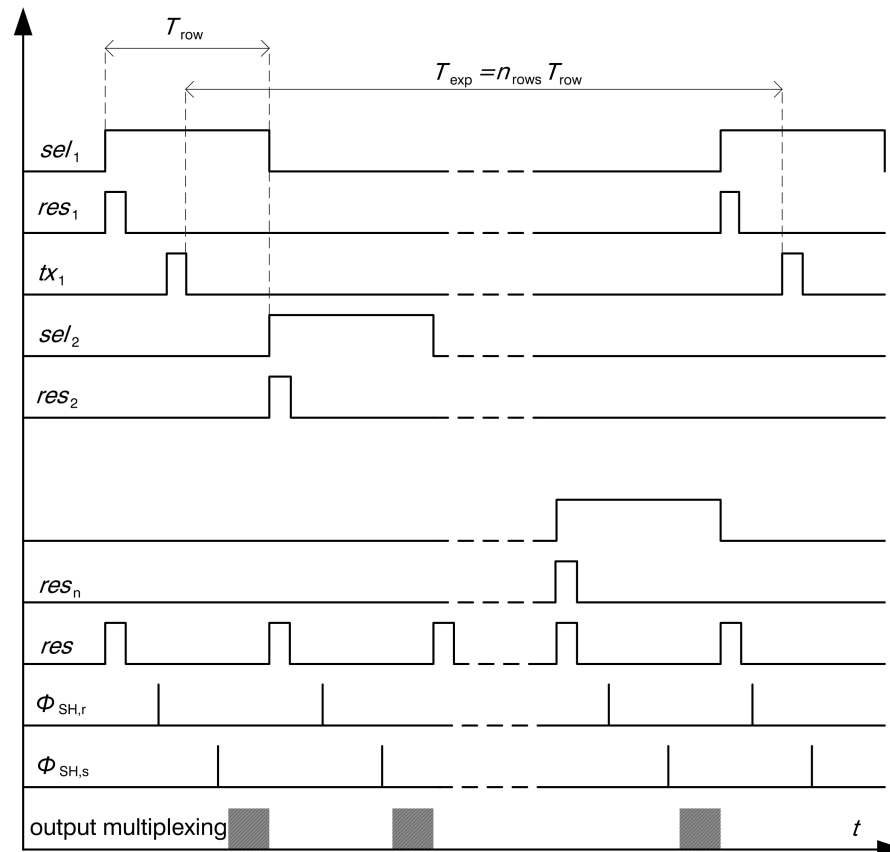


FIGURE 4.2 Timing diagram for rolling shutter operation of the CMOS image sensor with column-level open-loop amplifiers

trates that due to the tracking of the amplifier's input offset by the sense node reset voltage, the described feedback reset configuration attenuates the impact of amplifier offset by a factor of the open-loop gain. A similar consideration illustrates that the offset of the pixel-level source-follower is also attenuated by the same factor in comparison to using constant sense node voltage reset.

Besides the principal reason of advantageous noise performance, as analyzed in Sect. 4.2.2, the degenerate common-source amplifier with resistive load, as shown in Fig. 4.3, is an ideal candidate for use as an open-loop column-level amplifier for the reason of its moderate gain, decent open-loop linearity, and low gain sensitivity to process variations and to column-to-column mismatches.

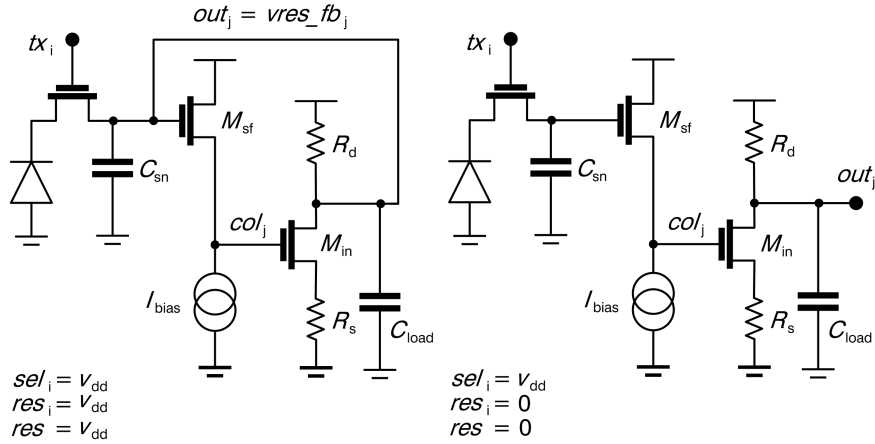


FIGURE 4.3 Pixel-level source-follower and column-level amplifier in sense node reset configuration (left) and in amplifying configuration (right)

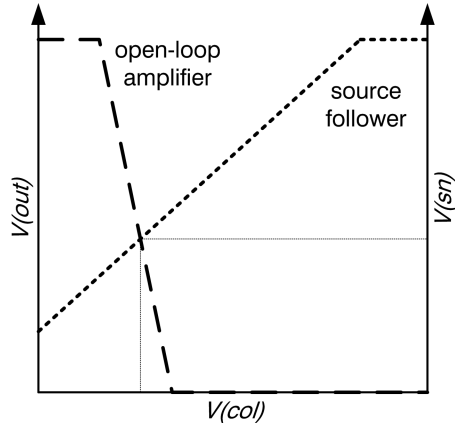


FIGURE 4.4 Conceptual sketch of the amplifier output voltage as a function of the column line voltage and of the column line voltage as a function of the sense node voltage

These characteristics are best understood considering the low-frequency small-signal gain A_{oamp} of the open-loop amplifier, as expressed in (4.1), including the effect of channel length modulation of the input transistor M_{in} .

$$A_{oamp} = \frac{g_{m,in} R_{ds} R_d}{R_d + R_{ds} + g_{m,in} R_{ds} R_s}, \quad (4.1)$$

where R_s , R_d , $g_{m,in}$, and R_{ds} are the source resistor value, the drain resistor value, the transconductance of the input transistor and the drain-source resistance due to channel length modulation of the input transistor respectively. In the above expression the product of $g_{m,in} R_{ds}$ has been assumed much greater than unity. If R_{ds} is also greater than R_d , the effect of channel length modulation on the small-signal gain becomes negligible as expressed in (4.2).

$$A_{oamp} \approx \frac{g_{m,in} R_d}{1 + g_{m,in} R_s}, \quad (4.2)$$

In the ideal case, $g_{m,in} R_s$ is much higher than unity and the gain of the degenerate common-source amplifier is equal to the ratio R_d/R_s of the drain resistor over the source resistor. This means that the small signal open-loop gain is independent of the amplifier input and output voltage, i.e. perfectly linear. The independence of the transistor transconductance and drain-source resistance also means that the open-loop gain is not subject to process variations and mismatch of these parameters. The only source of variation in open-loop gain is mismatch of the resistor ratio R_d/R_s which can be very small if the source and drain resistors are implemented using the same physical resistor type and if layout matching techniques are applied.

In reality, the influence of the input transistor's finite transconductance is never completely suppressed. In fact, the product of the input transistors transconductance times the source resistor increases with the current flowing in the amplifier, i.e. with the source voltage applied across the source resistor, hence this source voltage should be as large as possible. It should be considered though that the voltage across the drain resistor is defined by the source voltage multiplied by the resistor ratio R_d/R_s , as both resistors conduct the same current. This voltage across the drain resistor should by no means be high enough to cause the input transistor to operate in the triode region, since this would destroy most aspects of the circuit's proper operation. Given the restriction of the voltage across the drain resistor and the desire to achieve

moderate voltage gain by a resistor ratio of about one order of magnitude, the source voltage is restricted to a value one order of magnitude below the voltage across the drain resistor. Typical values of the source voltage, therefore, cannot exceed 100 to 200 mV for a power supply voltage of 3.3V. In this range of voltages across the source resistor and for reasonable dimensions of the input transistor the influence of finite transconductance can not be fully neglected in the expression (4.2) of the open-loop gain, but decent linearity and insensitivity to process parameter spread can still be reached.

4.2.1 AC Characteristics and Stability during Reset

Open-Loop AC Transfer Function of the Amplifier

The small signal AC response of the open-loop amplifier is a crucial aspect of its characteristics, since it defines the quality of low-pass filtering applied to the source-follower noise. The AC response is an ideal first-order low-pass filter, if the parasitic capacitances of the input transistor are neglected. Taking into consideration of non-zero gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} of the input transistor results in the AC response of (4.3).

$$H_{\text{Oamp}} = \frac{g_{m,\text{in}} R_d}{1 + g_{m,\text{in}} R_s} \frac{1 - sC_{gd} \left(R_s + \frac{1}{g_{m,\text{in}}} \right) - s^2 \frac{R_s C_{gs} C_{gd}}{g_{m,\text{in}}}}{\left(1 + sR_d (C_{gd} + C_{\text{load}}) \right) \left(1 + s \frac{R_s C_{gs}}{1 + g_{m,\text{in}} R_s} \right)} \quad (4.3)$$

Note that the left and right half plane real zeros as well as the non-dominant pole due to the parasitic capacitances of the input transistor are absolutely negligible in practice. As a matter of fact, their frequency spacing from the dominant pole, defined by the load capacitance and the drain resistor of the degenerate common-source amplifier, is as high as two to three orders of magnitude. This statement assumes a design with an open-loop gain of about ten, decent $g_{m,\text{in}}$ for process-spread independence of the gain, and C_{load} dimensioned for optimized noise performance, as discussed in section 4.2.2.

Stability in Reset State

The AC characteristics of the open-loop amplifier also play a crucial role concerning the stability of the system in reset configuration, when a feedback loop between the source-follower, the column line, the open-loop amplifier, and the reset voltage feedback line is established. The equivalent circuit of the feedback system is shown in Fig. 4.5 and the open-loop transfer function $H_{\text{Res,open}}$ of the feedback system is given in (4.4).

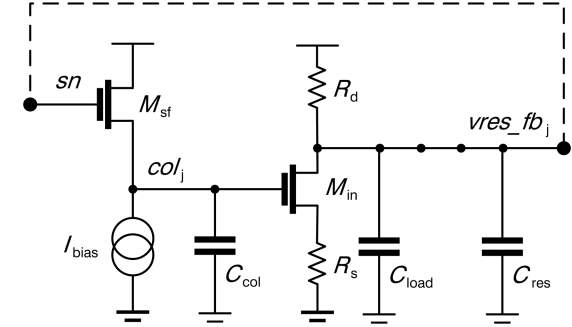


FIGURE 4.5 Equivalent circuit for analysis of the stability in feedback configuration

$$H_{\text{Res,open}} = \frac{A_{\text{Oamp}}}{\left(1 + sC_{\text{col}}/g_{m,\text{sf}} \right) \left(1 + sR_d (C_{\text{load}} + C_{\text{res}}) \right)} \quad (4.4)$$

where C_{col} is the capacitance on the column line, C_{res} is the capacitance on the reset voltage feedback line including the sense node capacitance, and $g_{m,\text{sf}}$ is the source-follower's transconductance. The gate-source capacitance, gate-drain capacitance and drain-source resistance of the degenerate common-source amplifier's input transistor are neglected in the above calculation. The dominant pole of the feedback loop is the dominant pole of the degenerate common-source amplifier, whereas a non-dominant pole is given by the source-follower loaded by the column capacitance. In order to avoid instability of the feedback loop, the non-dominant pole should be spaced from the dominant pole by a ratio of at least the open-loop amplifier's voltage gain. Mathematically speaking, this statement corresponds to (4.5), if the amplifier's gain is approximated by the drain-resistor-to-source-resistor ratio R_d/R_s .

$$g_{m,\text{sf}} R_s \geq \frac{C_{\text{col}}}{C_{\text{load}} + C_{\text{res}}} \quad (4.5)$$

This criterion is usually satisfied without any additional measures, if the circuit is optimized for low noise and high linearity, but should definitely be verified during the design process, since the phase margin can be rather small for certain designs.

4.2.2 Noise Analysis

Given the use of BPDs, rolling shutter operation, and CDS with short sampling time delay, many noise components of the presented image sensor concept with column-level open-loop amplifiers are described by the considerations already discussed for the case of conventional image sensors. For this reason, the reader is referred to section 2.5 for calculation of BPD leakage current shot noise, sense node leakage current shot noise, as well as an explanation concerning the cancellation of reset noise. The following three subsections will cover the quantitative analysis of thermal as well as flicker noise of the pixel-level source-follower and, most importantly, the thermal noise of the open-loop degenerate common-source amplifier.

Thermal Noise of the Pixel-Level Source-Follower

The thermal noise spectral density on the column line created by the source-follower is equal to the expression (2.15) of a conventional image sensor, for the obvious reason of equivalent pixel circuit topology. As a principal difference in comparison to conventional image sensors, the bandwidth of the source-follower's noise is limited by the open-loop column-level amplifier in the present case, whereas a switched-capacitor amplifier accomplishes this task in conventional image sensors. The expression of the thermal noise equivalent charge is, therefore, equal to (2.21), where H_{amp} and A_{amp} have to be replaced by the transfer function and gain of the open-loop amplifier H_{Oamp} and A_{Oamp} , as given in (4.3) and (4.1), respectively. As outlined in section 4.2.1 the parasitic pole and the two parasitic zeroes have characteristic transition frequencies two to three decades above the dominant pole. The transfer function of the open-loop amplifier can, therefore, be considered as an ideal first-order low-pass filtering function with a pole at $-1/R_d C_{\text{load}}$. This results in the simple analytical result of (4.6), where the CDS transfer function H_{CDS} has been approximated by $\sqrt{2}$ and the band-limit of the column line has been neglected, since it is significantly higher than the low-pass filtering frequency of the open-loop amplifier.

$$q_{\text{n,sf}} = C_{\text{sn}} \sqrt{\frac{2kT\gamma}{g_{m,\text{sf}} R_d C_{\text{load}}}} \quad (4.6)$$

In the above expression γ is the thermal noise excess factor of the source-follower transistor. Very low thermal noise equivalent charge of the source-follower can be achieved for Megapixel resolution standard video frame rate image sensors, with reasonable values of $g_{m,\text{sf}}$, i.e. reasonable gate width and

drain current of the source-follower transistor, if the open-loop amplifier bandwidth is chosen optimally. This optimum choice corresponds to the minimum possible bandwidth yet allowing accurate settling of the amplifier output signal within the CDS sampling time difference. This optimum choice is analogous to (2.22) and can be expressed as (4.7), where n_τ is the number of amplifier time constants required for accurate settling of the output signal.

$$R_d C_{\text{load}} = \frac{T_{\text{cds}}}{n_\tau} \quad (4.7)$$

Flicker Noise of the Pixel-Level Source-Follower

The effect of the source-follower's flicker noise can be derived from the calculation for conventional image sensors by a similar consideration as in the thermal noise case. The noise power spectral density on the column line is identical to the case of a conventional image sensor, as given in (2.24). Since the only difference is the low-pass transfer function, the expression (2.25) of the flicker noise equivalent charge remains valid, if H_{amp} and A_{amp} are replaced by H_{Oamp} and A_{Oamp} respectively. The quantitative difference of flicker noise equivalent charge between a conventional image sensor and the presented approach using open-loop column-level amplifiers is, however, not as pronounced as the difference in thermal noise, since the difference between the low-pass filtering functions H_{amp} of a switched-capacitor amplifier and H_{Oamp} of an open-loop amplifier is found at high frequency, where the flicker noise PSD is low anyway. Conventional as well as open-loop column-level amplifier based image sensors can both achieve flicker noise performance very close to the flicker noise limit. In the case of the presented image sensor with open-loop column-level degenerate common-source amplifier, the flicker noise limit is reached if condition (4.7) is satisfied.

Noise of the Column-Level Open-Loop Amplifier

Given unity voltage gain of the pixel-level source-follower, the electronic noise of the column-level open-loop amplifier might have an important impact on the overall noise performance of the image sensor and, therefore, requires careful analysis. As a first component, the noise equivalent charge due to thermal noise of the source resistor R_s is given by (4.8).

$$q_{\text{n,rs}} = \sqrt{2} C_{\text{sn}} \frac{1}{A_{\text{sf}}} \sqrt{\frac{R_s}{R_d} \frac{kT}{C_{\text{load}}}} \approx q_{\text{n,oamp}} \quad (4.8)$$

The thermal noise equivalent charge of the degenerate common-source amplifier's input transistor corresponds to expression (4.9), where γ is the noise excess factor of the input transistor M_{in} usually operated in moderate or weak inversion saturation region.

$$q_{\text{n,mos}} = \sqrt{2} C_{\text{sn}} \frac{1}{A_{\text{sf}}} \sqrt{\frac{kT\gamma}{g_{m,\text{in}} R_{\text{d}} C_{\text{load}}}} . \quad (4.9)$$

The thermal noise of the drain resistor R_{d} is described by the equivalent charge of (4.10).

$$q_{\text{n,rd}} = \sqrt{2} C_{\text{sn}} \frac{1}{A_{\text{sf}}} \sqrt{\left(\frac{1 + g_{m,\text{in}} R_{\text{S}}}{g_{m,\text{in}} R_{\text{d}}}\right)^2 \frac{kT}{C_{\text{load}}}} . \quad (4.10)$$

Comparison of (4.8), (4.9), and (4.10) clearly shows that the source resistor's thermal noise is the predominant noise component of a degenerate common-source amplifier. Since $g_{m,\text{in}}$ is significantly larger than R_{S} and the square of the voltage gain is much larger than the approximate voltage gain of $R_{\text{d}}/R_{\text{S}}$, the noise power due to the drain resistor and the input transistor are both about one order of magnitude lower than the source resistor's noise power. Neglecting their contribution is approximately equivalent to neglecting noise of the bias current source used in the OTA of a conventional switched-capacitor column-level amplifier. The overall noise equivalent charge due to the degenerate common-source column-level amplifier is, therefore, approximated by expression (4.8) for the source resistor's noise. Note that flicker noise of the input transistor is easily reduced to a negligible level by using a sufficiently large gate area. The multiplication factor of $\sqrt{2}$ in the noise expression accounts for the application of CDS.

The approximate expression (4.8) of the open-loop column-level amplifier noise indicates that the product of load capacitance and open-loop gain is the decisive factor for good noise performance. It is, therefore, obvious that excessively large load capacitance would be required if an open-loop amplifier of unity-gain was to be used. Moderate voltage amplification of the column-level open-loop amplifier is, therefore, required not only for suppression of electronic noise from subsequent signal processing stages but also for achievement of low self-generated thermal noise at reasonable capacitance expenditure per column. Similar considerations are found in the case of conventional switched-capacitor column-level amplifiers, as discussed in section 2.5.4.

Comparison of the trade-offs between noise, capacitance expenditure, and amplification of a conventional column-parallel switched-capacitor amplifier vs. a degenerate common-source open-loop amplifier shows an advantage in favour of the degenerate common-source amplifier. This is explained by three principal differences between (2.27) and (4.8):

First of all, the noise excess factor γ of the input transistor of the OTA employed in switched-capacitor amplifiers is absent in the noise expression of the degenerate common-source amplifier which uses a resistor as an input-voltage-to-current transconductance which, hence, plays the role of predominant noise source. Simulation results of a low-noise switched-capacitor column-level amplifier, which has been designed in the wider context of this thesis [54], have revealed noise excess factor values ranging from 1.3 to 2.0 for the input transistor operated in the moderate inversion saturation region in the used process technology. These values being greater than unity result in a corresponding noise advantage for a degenerate common-source open-loop amplifier.

Secondly, there is a slight difference concerning the impact of voltage amplification on the noise performance. In the noise expression of a switched-capacitor amplifier, the amplifier's load capacitance is multiplied by a factor of $A_{\text{amp}}^2/(A_{\text{amp}} + 1)$, whereas the load capacitance multiplication factor in an open-loop degenerate open-loop amplifier is equal to $R_{\text{d}}/R_{\text{S}}$, i.e. approximately A_{Oamp} . For equal values of voltage amplification, the trade-off between capacitance and thermal noise is, therefore, advantageous for an open-loop degenerate open-loop amplifier. For a voltage amplification of e.g. 10, a switched-capacitor amplifier would need about 10% more load capacitance than the open-loop counterpart for this reason alone. If the influence of finite transconductance in the degenerate common-source amplifier was taken into account, the difference would be less pronounced.

Last but not least, an open-loop amplifier does not require any input capacitors and feedback capacitors. In the case of moderate voltage amplification, the feedback capacitance C_2 of a switched-capacitor amplifier is relatively small and hence does not consume much area. The input capacitance C_1 , however, is usually as high as a considerable fraction of the load capacitance but does not benefit from multiplication by the voltage gain.

A calculation taking into account all the above mentioned effects shows that, depending on the value of the noise excess factor, 1.8 to 2.8 times higher capacitance per column is required in the case of a switched-capacitor amplifier in comparison to a degenerate common-source amplifier, assuming a voltage gain of 10 and a dimension of C_1 equal to $0.25 \cdot C_{\text{load}}$.

4.2.3 Sense Node Capacitance

The comparison of equivalent noise charge between the open-loop column-level amplification concept and conventional image sensors implicitly relies on the assumption of equal sense node capacitance C_{sn} . Given the virtually identical pixel topology of the two concepts, identical sense node capacitance is actually a valid assumption which in turn validates the advantage of the concept of open-loop column-level amplification in terms of equivalent noise charge thanks to lower column-level amplifier noise and possibly superior low-pass filtering of source-follower noise. It is, however, more interesting to compare the sense node capacitance of a source-follower based pixel, as given in (4.11), to the sense node capacitance of a pixel with a pixel-level common-source amplifier, as expressed by (3.12).

$$C_{\text{sn}} = C_{\text{jun,n}} + C_{\text{ovlp,tx}} + C_{\text{ovlp,res}} + C_{\text{wire,vcst}} + C_{\text{gd}} + (C_{\text{wire,sncol}} + C_{\text{gs}})(1 - A_{\text{sf}}), \quad (4.11)$$

where $C_{\text{jun,n}}$ is the junction capacitance of the n-type sense node diffusion of the BPD plus the n-type drain diffusion of the reset transistor, if the two diffusions are not physically merged. $C_{\text{ovlp,tx}}$ is the overlap capacitance of the sense node diffusion and the polysilicon transfer gate, $C_{\text{ovlp,res}}$ is the gate-drain overlap capacitance of the reset transistor, $C_{\text{wire,sncol}}$ is the parasitic wiring capacitance between the sense node and the column line, $C_{\text{wire,vcst}}$ is the lumped remainder of the sense node parasitic wiring capacitance, C_{gs} is the gate-source capacitance of the source-follower transistor, and C_{gd} is the gate-drain overlap capacitance of the source-follower transistor.

The sense node capacitance at equal transistor gate dimensions of the compared common-source input transistor and source-follower transistor is lower in the case of the source-follower mainly thanks to multiplication of the gate-source capacitance by the factor of $1 - A_{\text{sf}}$ due to non-inverting near-unity gain between the sense node and the column line. The resulting advantage in conversion factor explains, that a sensor with pixel-level source-follower and column-level open-loop voltage amplification can compete with or even outperform a sensor with pixel-level common-source amplifier despite its large weighting of the column-level amplifier's electronic noise.

Considering the expressions of noise equivalent charge due to source-follower flicker noise, source-follower thermal noise, the column-level open-loop amplifier's noise and the expression of the sense node capacitance, a trade-off concerning the source-follower's gate area exists. On one hand, increasing gate area reduces the source-followers' flicker noise equivalent *voltage*, and high

gate width decreases the source-follower's thermal noise *voltage*. On the other hand, increasing gate dimensions increases the sense node capacitance, i.e. decreases the conversion factor between the equivalent noise *voltage* and the equivalent noise *charge*.

In contrast to the case of an image sensor with pixel-level amplification, where the W/L ratio of the common-source transistor is constrained by frame rate, noise, and voltage gain criteria, the source-follower transistor's aspect ratio can be chosen more freely in the present case. Considering the desire for low gate-source capacitance and high source-follower transconductance for low thermal noise, the ideal gate length of the source-follower transistor corresponds to the minimum gate length allowed by the process technology. An optimum gate width is theoretically found from the sum of squares of the noise equivalent charges according to (2.25), (4.6), and (4.8), as well as the expression (4.11) of C_{sn} , where the gate-drain capacitance and the gate-source capacitance are replaced by their respective gate width dependent expressions. This optimization involves, however, factorization of a 4th order polynomial equation, i.e. no closed analytical solution can be found and numerical solving of the polynomial equation has to be used or optimization by circuit simulation has to be undertaken.

4.3 Circuit Implementation

Test structures of the presented image sensor concept with pixel-level source-follower and column-level open-loop amplifier have been designed and fabricated as additional test columns of the image sensor chip described in section 3.3. Several design variations have been implemented for comparison. Besides the version based on n-channel pixel-level source-follower and amplifier input transistors, a version using p-channel source-follower and amplifier input transistors, as shown in Fig. 4.6, has been implemented.

Furthermore, a version of the open-loop degenerate common-source amplifier with enhanced linearity has been designed. As illustrated by (4.1), in the simplest single-branch implementation of the degenerate common-source amplifier with resistor load, non-linearity arises from the fact that the gain depends on the drain-source resistance of the input transistor, which is a function of the transistor's current and hence the amplifier's input voltage. In the presented high-linearity version of the degenerate common-source amplifier, as shown in Fig. 4.7, the influence of the input transistor's drain-source resistance is reduced by reduction of the drain voltage swing. For this reason, the drain current of the input transistor is mirrored before being injected into the equivalent drain resistor R_{d} . The voltage swing of the diode-connected p-channel input transistor of the current mirror could, theoretically, be designed to be very low by use of high width-to-length ratio of the current mirror transistors.

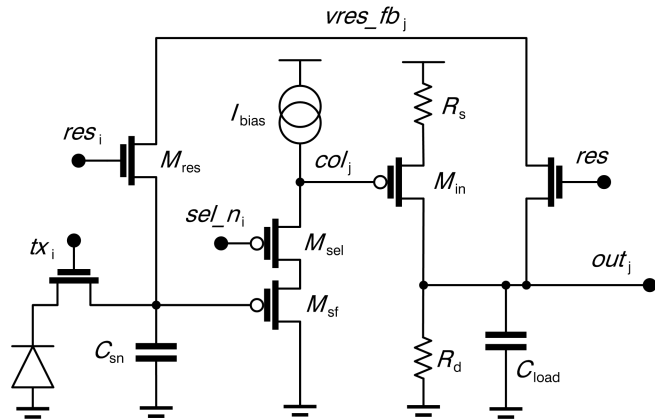


FIGURE 4.6 Pixel circuit with a p-channel source-follower and column-level degenerate common-source amplifier with a p-channel input transistor (single-branch implementation)

To minimize thermal noise from the current mirror transistors, it is, however, preferable to use narrow and long transistors which result in a voltage swing of the current mirror input node higher than the input voltage and source voltage swings. In contrast to the case of a directly connected drain resistor, as illustrated in Fig. 4.6, this approach still leaves enough voltage headroom for reduction of the drain voltage swing by use of a cascode transistor $M_{c,in}$. Ideally, the gate voltage of this transistor $vcasc1$ would be tracking the input voltage in order to minimize the drain-source voltage variation of the input transistor M_{in} . Significant reduction of the impact of the input transistor's finite drain source resistance is, however, already achieved when using a constant gate voltage bias for the cascode transistor.

Further non-linearity of the simplest single-branch version of degenerate common-source amplifier with resistor load, as illustrated in Figs. 4.3 and 4.6, arises from the impact of finite input transconductance $g_{m,in}$ in comparison to the source resistor R_s , as illustrated in the approximation of (4.2). For a source resistor value which has been defined by the requirements on the amplifier's load capacitance, bandwidth, and gain, the product of $g_{m,in}R_s$ increases approximately proportionally to the square root of the drain current of the input transistor, i.e. of the voltage drop over the source resistor.

The version of the column amplifier with enhanced linearity, as illustrated in 4.7, makes use of a bias current source I_{ref} in order to increase the input transistor's drain current to a value which, in the case of the simple implementations as shown in , as illustrated in Figs. 4.3 and 4.6, would cause the voltage across the drain resistor of the simplest implementation to exceed the

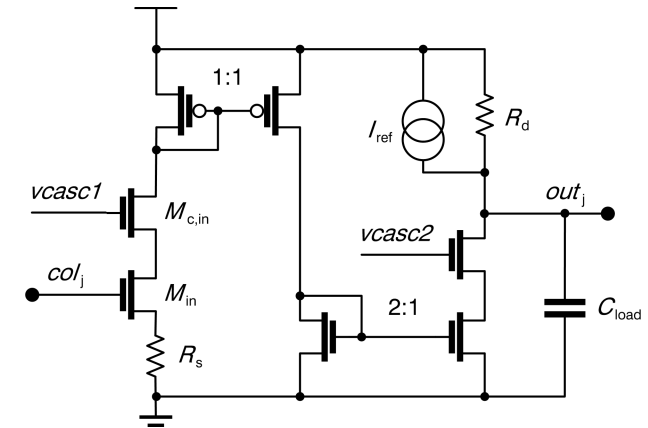


FIGURE 4.7 Column-level open-loop degenerate common-source amplifier with enhanced linearity

supply voltage. The reference current is generated by a replica of the input transistor and the source resistor in order to achieve optimum compensation of temperature and process variations.

The combination of the described use of current mirrors and the reference current source allows achieving open-loop amplification with excellent linearity. Two effects concerning the noise performance have to be considered when using this amplifier topology with enhanced linearity. On one hand, additional noise from the current mirrors and the reference current source needs to be considered. Therefore, relatively low transconductance of the current mirror transistors, preferably below $1/R_s$, has to be used.

On the other hand, the use of a current mirror ratio smaller than one, e.g. of 0.5, reduces the gain for a given ratio of R_d/R_s . In other words, for a given gain, e.g. of 10, the ratio of R_d/R_s is increased by the inverse of the mirror ratio, e.g. by a factor of 2. The expression of the source resistor's noise equivalent charge (4.8), however, remains unchanged, since the input referred noise PSD is still defined by R_s and the noise bandwidth is still governed by the product of R_dC_{load} . This means, that for a given product of gain and load capacitance, the equivalent noise charge of the source resistor is improved by the square root of the inverse mirror ratio. The same noise reduction by the mirror ratio obviously applies to all transistors of the current mirror except for the last transistor which conducts the downscaled current. The described property of the amplifier version with enhanced linearity allows a reduction of the amplifier's noise at a fixed bandwidth at the unavoidable cost of power consumption, but without the expenditure of increased load capacitor area or

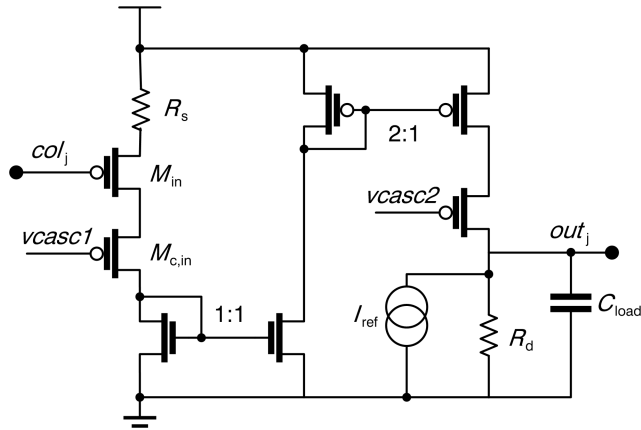


FIGURE 4.8 Degenerate common-source amplifier with enhanced linearity using a p-channel input transistor

an excessively high gain value which would lead to an unacceptable loss of input signal swing.

Besides the described highly linear degenerate common-source amplifier using an n-channel input transistor, a complementary highly linear version based on a p-channel input transistor for application in conjunction with p-channel pixel-level source-follower transistor has been implemented, as shown in Fig. 4.8.

4.3.1 Simulation Results

Combination of n-channel and p-channel pixel-level source-follower transistors with their respective simple single-branch and enhanced linearity versions of open-loop column-level amplifiers has led to the implementation of four different test column structures. Due to the absence of a closed analytical expression for the optimum source-follower gate width, this design parameter has been optimized for minimum equivalent noise charge by several iterations of noise simulations and of AC simulations for determination of the sense node capacitance. A gate length of $0.4 \mu\text{m}$ instead of the minimum allowed gate-length of $0.34 \mu\text{m}$ is used to avoid poor transistor matching at minimum dimensions. At this arbitrarily chosen length, optimum values of $2.0 \mu\text{m}$ and $1.8 \mu\text{m}$ have been found for the transistor width of p-channel and n-channel source-follower transistors respectively. This optimization has been based on the designs of the simple single-branch degenerate common-source amplifiers, as shown in Figs. 4.3 and 4.6. The same pixel-level source-follower dimensions have been used in combination with the open-loop amplifiers with enhanced linearity, de-

spite the fact that the optimum gate width is, in this case, slightly narrower due to the higher input-referred noise voltage of the amplifiers with enhanced linearity. A summary of design parameters and simulation results of the implemented optimized designs is given in Table 4.1.

TABLE 4.1 Design parameters and simulation results for n-channel and p-channel pixel-level source-follower transistors and their corresponding column-level open-loop amplifiers

	n-channel input transistor (Fig. 4.3)	p-channel input transistor (Fig. 4.6)	n-channel, enhanced linearity (Fig. 4.7)	p-channel, enhanced linearity (Fig. 4.8)
C_{load}	4 pF	8 pF	8 pF	8 pF
amplifier current	$6.5 \mu\text{A}$	$9.5 \mu\text{A}$	$60 \mu\text{A}$	$68 \mu\text{A}$
sense node non-linearity	0.7	0.02	0.2	0.02
source-follower non-lin.	0.4	0.4	0.5	0.3
amplifier non-linearity	0.8	1.2	0.3	0.2
C_{sn}	3.3 fF	3.8 fF	3.2 fF	3.8 fF
A_{oamp}	9.4	8.3	9.4	8.3
readout noise	$0.93 e^-$	$0.58 e^-$	$0.95 e^-$	$0.85 e^-$

The sense node capacitance of the pixel with a p-channel source-follower is slightly higher than the sense node of the n-channel counterpart despite the fact of having slightly smaller gate area. The origin of the discrepancy is a higher sense node parasitic wiring capacitance resulting from increased distance between the sense node diffusion and the source-follower gate contact due to different spacing rules for the p-channel transistors.

The amplifier's current consumption is computed at the reset operating point of the sensor and will vary as a function of the optical signal after charge transfer from the BPD onto the sense node. Note that the amplifiers with enhanced linearity consume significantly more current than the simple versions due to their additional branches. The current consumption is particularly increased by the use of a mirror ratio smaller than one.

Despite increased power consumption, the amplifiers with enhanced linearity increase the overall readout noise due to thermal noise from the current mirrors as well as the additional current source.

In return for the increased amplifier noise, a clear linearity enhancement with respect to the simple single-branch counterpart is achieved, as can be seen by comparison of the peak linearity error over an amplifier output voltage swing

of approximately 1 V, as given in Table 4.1. Whereas the non-linearity of single-branch degenerate common-source amplifiers is higher than the non-linearity of pixel-level source-followers and the non-linearity of the charge-to-voltage conversion on the sense node capacitance, their more complex counterparts are more linear than the pixel-level source-followers. It is, however, important to put the simulated linearity of the electronic circuits in the context of the image sensor application. As a matter of fact, the non-linearity of a BPD's photoresponse can easily reach a value of more than 1%, i.e. an order of magnitude higher than the non-linearity of the investigated electronic circuits. From this point of view, the simple single-branch degenerate common-source amplifier with resistive load is the more interesting solution thanks to more than sufficient linearity and excellent noise performance.

It is also interesting to compare the simulated noise values to the noise performance of a sensor with pixel-level voltage amplification, as discussed in chapter 3. The simulated noise equivalent charge of the presented image sensor concept with pixel-level source-follower and column-level open-loop amplifier outperforms the simulated and even the measured noise performance of image sensors with pixel-level amplification. As a matter of fact, the comparison shows, that thanks to the very low input referred noise voltage of the degenerate common-source amplifier, the disadvantage of lacking pixel-level amplification can be more than compensated by the smaller sense node capacitance in comparison to a circuit with pixel-level amplification.

4.3.2 Measurement Results

Characterization of the implemented test circuit has revealed an important parameter discrepancy between the simulation model and the characteristics of the pixel-level n-channel MOS transistors. In fact, the threshold voltage of n-channel transistors in the pixel field, where many implants, such as the substrate background doping, are processed separately from the remaining chip area, has been shown to be about 500 mV below the target value. Since the column-level open-loop amplifiers are situated in the circuit periphery, their properties are not affected. The reduced threshold voltage of pixel-level n-channel transistors does not have an influence on the proper operation of reset transistors and select transistors. The reduced threshold voltage of the n-channel pixel-level source-follower transistors in conjunction with the implemented reset configuration relying on feedback operation results, however, in a sense node reset voltage about 500 mV below the simulated value. In the case of the single-branch degenerate common-source amplifier with n-channel input transistor, the resulting sense node electron potential energy at reset is higher than the minimum electron potential energy in the buried photodiode. Operation and characterization of this implementation version is, therefore, impossible. For this reason, this section presents only the results of the test

circuits using p-channel pixel-level source-follower transistors, as well as those using n-channel source-followers with the column-level open-loop amplifier design with enhanced linearity which can be successfully operated all the same thanks to their generally higher sense node reset voltage.

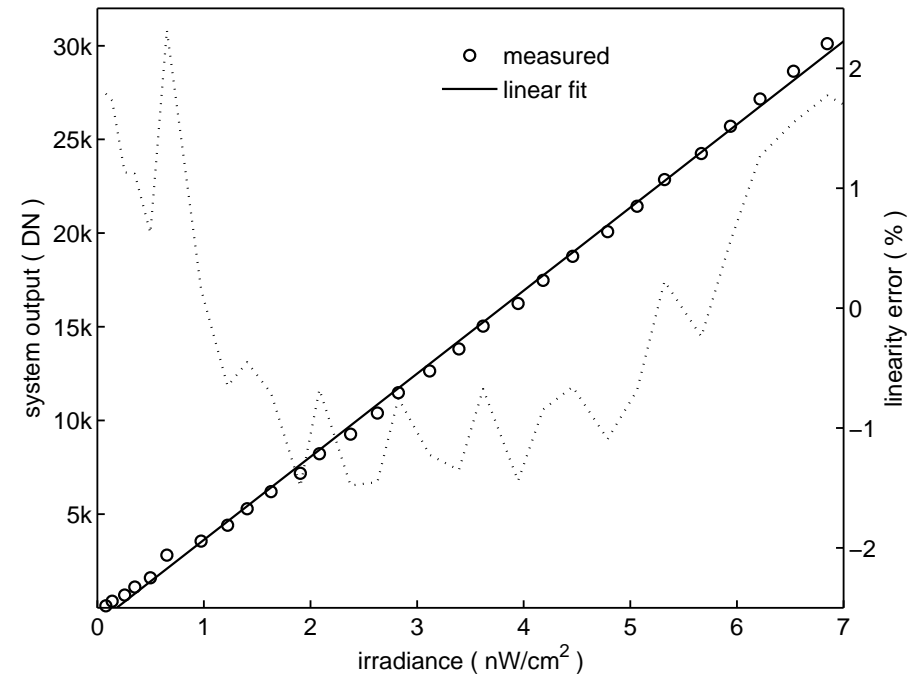


FIGURE 4.9 Measured photoresponse and linearity error for an n-channel pixel-level source-follower with a column-level degenerate common-source amplifier with an n-channel input transistor and design for enhanced linearity

Figures 4.9, 4.10, and 4.11 show the photoresponse and non-linearity of the designs using n-channel source-followers with the amplifier for enhanced linearity, p-channel source-followers with the single-branch amplifier, and p-channels with the amplifier design for enhanced linearity respectively.

Note that the irradiance axis values of the mentioned figures can not be easily compared to each other or to the measurement results of Sect. 3.3.2. This is due to the location of the test pixel column at the border of the pixel field of the test chip described in section 3.3.1, where relatively large zones of unused silicon are left open between some of the test columns. Photoelectrons generated in the slightly doped substrate of these open spaces between columns have a substantial probability of traveling to the BPDs of adjacent test columns

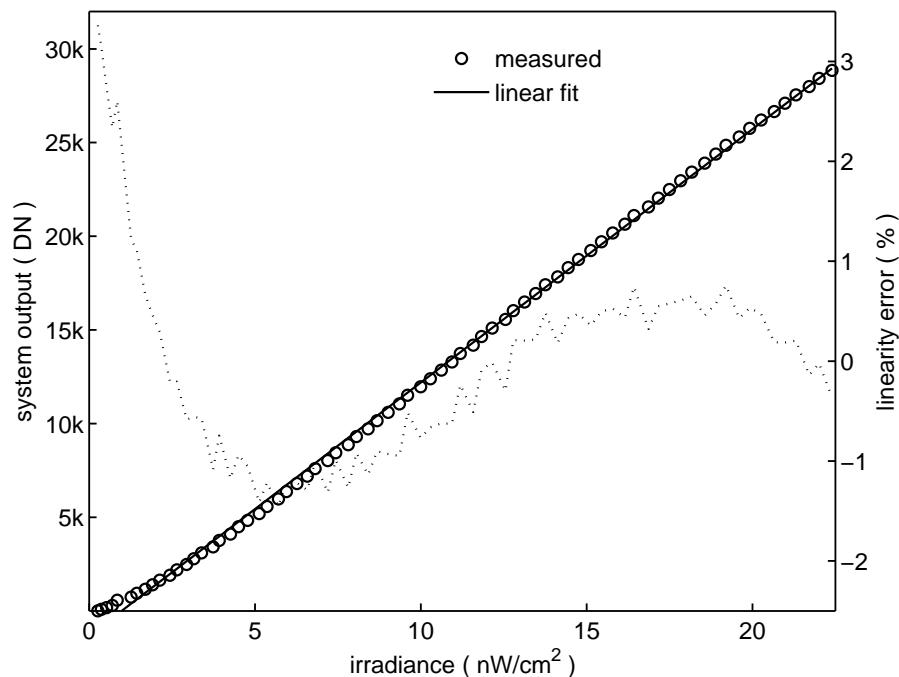


FIGURE 4.10 Measured photoresponse and linearity error for a p-channel pixel-level source-follower and a column-level degenerate common-source amplifier with a p-channel input transistor and single-branch topology

by diffusion transport. This effect results in higher responsivity or, in other words, higher effective diode area of test pixels neighboring zones of unused silicon.

Note that the peak linearity over the full voltage range of the chip-level readout chain of about 1 V has similar peak linearity errors for all three designs. The fact that the non-linearity for the p-channel source-follower designs is nearly identical independently of the topology of column-level open-loop amplifier illustrates that the non-linearity of the image sensor is predominantly defined by the linearity of the BPD rather than the linearity of the open-loop column-level amplifier. This conclusion is underlined by the fact that the measured non-linearity is significantly higher than the simulated non-linearity of the electronic circuits, as given in Table 4.1.

A particularly high photodiode non-linearity is observed at low irradiance, which can be explained by the presence of a potential pocket in the BPD, i.e. by a vertical minimum electron potential energy in the BPD which is horizontally

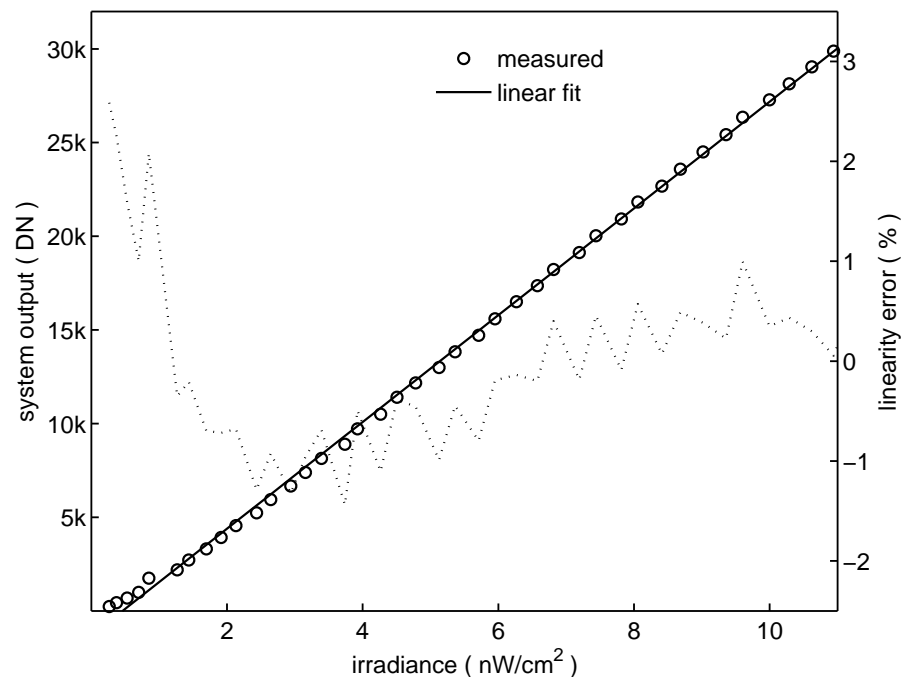


FIGURE 4.11 Measured photoresponse and linearity error for a p-channel pixel-level source-follower with a column-level degenerate common-source amplifier with a p-channel input transistor and design for enhanced linearity

increasing from the far end of the photodiode towards the transfer gate. Such a potential pocket causes a certain amount of photogenerated electrons to remain constantly in the BPD despite periodic charge transfer action. At zero absolute temperature, this small number of electrons remaining in the BPD would not have an influence on the responsivity, since the rate of electrons transferred to the sense node would be equal to the photogeneration rate in the BPD. At non-zero temperature, however, electrons constantly stored in the buried photodiode have a certain probability of vertically diffusing from the buried minimum potential energy location either up to the surface p-type implant or down to the non-depleted part of the substrate. These mobile electrons which diffuse out of the depleted region are removed by recombination with mobile majority holes in the surface implant or the substrate. The rate of electrons transferred onto the sense node is, therefore, equal to the rate of electron photogeneration *minus* the rate of electrons disappearing by vertical diffusion and recombination. Qualitatively speaking, this effect is noticeable if

the number of constantly stored electrons is high with respect to the number of photoelectrons accumulated and transferred during each exposure period. For this reason, the effect is visible at low irradiance and depends on the photodiode characteristics. In particular, it has been shown, that the presence of potential pockets depends on the geometrical layout of the photodiode shape and the transfer gate [59], [60]. It is, therefore, not surprising to observe a difference between the non-linearity of the pixel designs with n-channel source-followers and p-channel source-followers, since different photodiode geometries have been implemented for the two versions of source-follower types as a result of the different geometry of the pixel-level transistors.

Column-level voltage amplification without compression implies that the non-clipped output swing of the column-level amplifier covers only a fraction of the sense-node swing or the column-line swing. As opposed to the pixel-level amplification architecture, the open-loop column-level amplification architecture does, however, provide a non-amplified signal representation on the column line. The column line voltage can, therefore, be read out in addition to the amplifier output. Pixel-wise signal fusion using the amplifier's output signal in case of low intensity and the column line signal in case of intensities beyond the signal clipping point of the amplifier can be employed in order to restore a high-swing low-noise image. Such a scheme using two parallel readouts has been implemented in the test column of the n-channel pixel-level source-follower with highly linear column-level open-loop amplifier. A column-level source-follower has been used in order to buffer the column line-signal for non-amplified readout. Figure 4.12 shows the photoresponse of the non-amplified and amplified outputs.

Due to the feedback operation during reset phase, the reset voltage of the sense node might be lower than in the case of conventional image sensors, depending on the operating point of the column-level open-loop amplifier and the gate-source voltage shift of the pixel-level source-follower. If only the open-loop amplifier is used for signal readout, this is not a major concern, since the output signal swing is limited by the amplifier output swing rather than the sense node swing. However, if a dual readout scheme, as described above, is used the sense node swing should be maximized in order to maximize the swing of the non-amplified signal. First of all, tuning of the pixel-level source-follower's voltage shift and tuning of the amplifier's operating point can increase the reset voltage, i.e. the upper limit of the sense node voltage range. Secondly, an optimum voltage for activation of the BPD's transfer gate is required in order to make successful use of the lower end of the sense node voltage range. The transfer gate's activation voltage should be chosen as low as possible in order to allow low sense node voltage without forming a charge channel in the semiconductor underneath the transfer gate, but still high enough to allow full charge transfer, i.e. removal of the potential barrier between the BPD and the

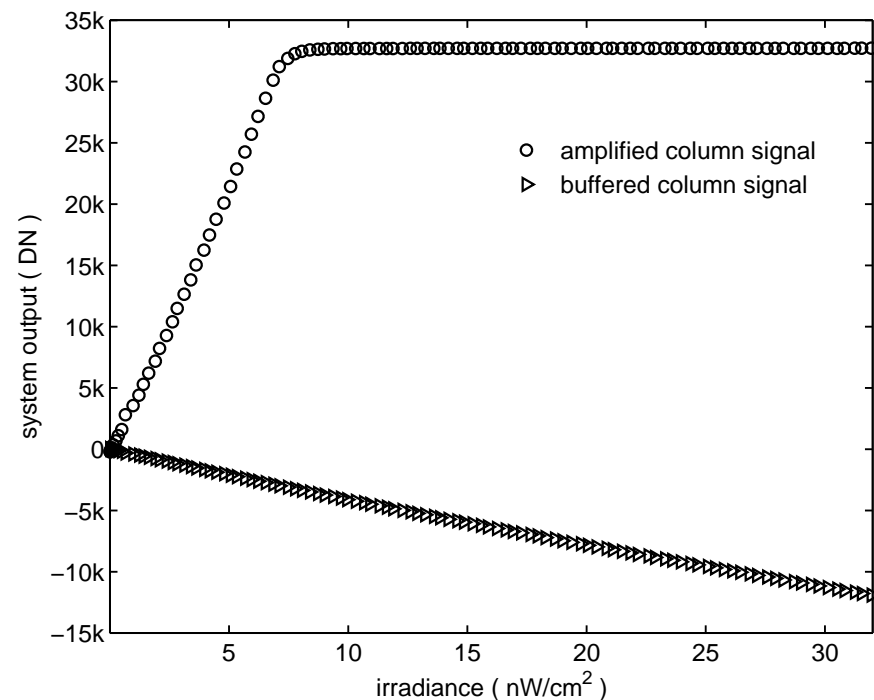


FIGURE 4.12 Measured photoresponse of the amplifier output and the buffered column signal (n-channel pixel-level source-follower, highly linear column-level amplifier)

sense node.

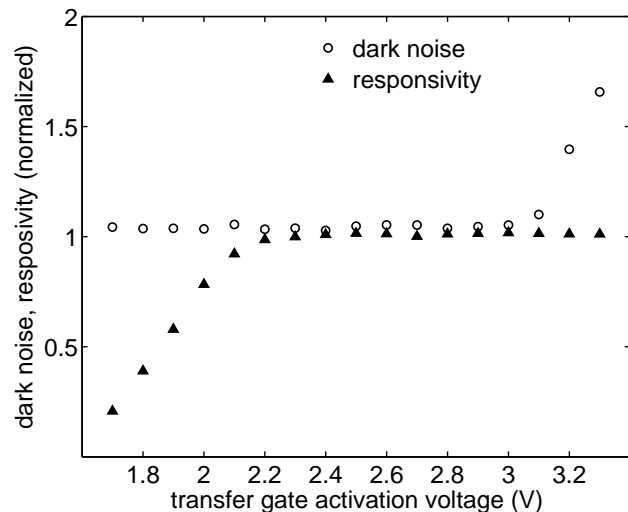


FIGURE 4.13 Responsivity (buffered column signal) and dark noise (output of open-loop column-level amplifier) as a function of the transfer gate activation voltage

In order to determine the optimum transfer gate voltage in the activated state the responsivity and dark noise have been measured as a function of the transfer gate voltage. As shown in Fig. 4.13, a gradual reduction of the responsivity is observed below a transfer gate voltage of 2.2 V. This responsivity loss is explained by incomplete charge transfer due to a remaining potential barrier underneath the transfer gate at insufficient voltage. First of all, the amount residual charge, which increases with decreasing transfer gate voltage, results in proportional signal charge loss due to vertical diffusion of photoelectrons towards the substrate and the p-type surface layer of the BPD. Secondly and more importantly, residual charge in the buried photodiode reduces the overall thickness of the depletion zone and, consequently, leads to reduced quantum efficiency, i.e. reduced responsivity. Concerning the dark noise, a significant increase is observed at transfer gate voltages above 3.0 V. This effect is explained by electrons flowing from the sense node to the semiconductor surface underneath the transfer gate during the phase of high transfer gate voltage. This channel charge is partially injected into the buried photodiode at the end of the transfer phase and is added to the signal charge of the subsequent exposure. The random component of the injected channel charge results in the observed increase of dark noise. If a transfer gate voltage of 2.2 V is used, the described effect of charge injection does not take place unless the sense node signal voltage swing exceeds 800 mV. According to this consideration

the combined measurements of dark noise and responsivity as a function of transfer gate voltage provide an indirect measurement of the sense node voltage swing which is found to be 800 mV in the case of a n-channel pixel-level source-follower transistor in combination with the highly linear open-loop column-level amplifier design.

Besides the peak linearity error, Table 4.2 lists the readout noise performance of the three implementations that have been characterized. These results have been obtained through measurement methods already used for characterizing the image sensor with pixel-level open-loop amplification: The system output noise is measured in the dark at a very short exposure time for suppression of photodiode leakage shot noise. The noise equivalent charge is subsequently calculated based on the system conversion factor CF_S obtained from measurement of the photon transfer characteristics. The readout noise histograms of the three characterized implementation versions are shown in Figs. 4.14, 4.15, and 4.16. The noise of the majority of the pixels of the implementation using an n-channel pixel-level source-follower transistor is in the same range as the noise of pixels with p-channel source followers, i.e. between 0.5 and 1.5 electrons. The fraction of pixels with higher noise, i.e. the right-side tail of the histogram in Fig. 4.14 is, however, higher in the case of n-channel source followers than in the case of p-channel source followers. Measured time-domain waveforms of selected pixels confirm, that the predominant noise source in pixels with high noise is random telegraph signal (RTS). As a consequence, it can be concluded that the fraction of pixels suffering from RTS is higher in the case of n-channel source-followers than in the case of p-channel source-followers with the employed process technology.

TABLE 4.2 Measured readout noise equivalent charge and peak linearity error for different source-follower transistor types and column-level open-loop amplifier versions

implementation version	peak linearity error	readout noise charge
n-channel, enhanced linearity	1.65 %	1.45 e ⁻
p-channel, single branch	2.20 %	0.98 e ⁻
p-channel, enhanced linearity	2.15 %	1.19 e ⁻

The equivalent readout noise values include power supply noise. Row noise correction is not possible, since only single test columns of each version are implemented and no dark columns of identical designs are available. In the case of the two implementations with a p-channel input transistors of the degenerate common-source amplifiers, this component is assumed to be significant. The electronic noise performance which can be achieved with row-noise cor-

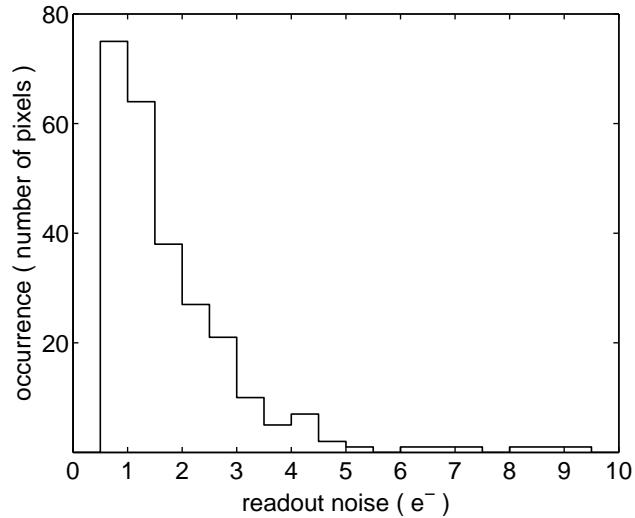


FIGURE 4.14 readout noise histogram of 256 pixels with an n-channel pixel-level source-follower and an open-loop column-level amplifier with enhanced linearity

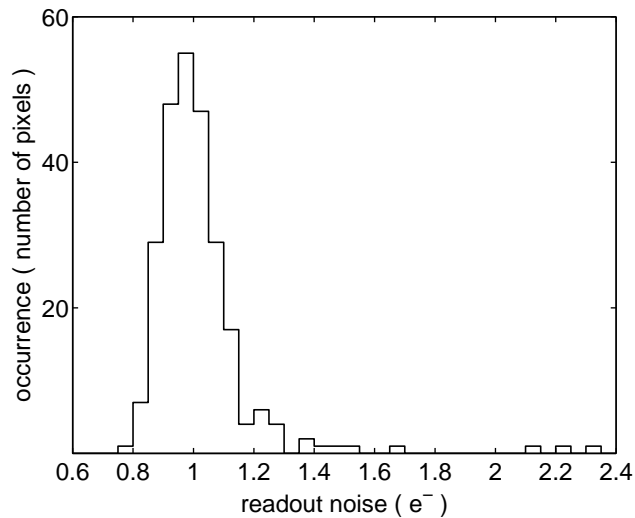


FIGURE 4.15 readout noise histogram of 256 pixels with a p-channel pixel-level source-follower and an open-loop column-level single-branch amplifier

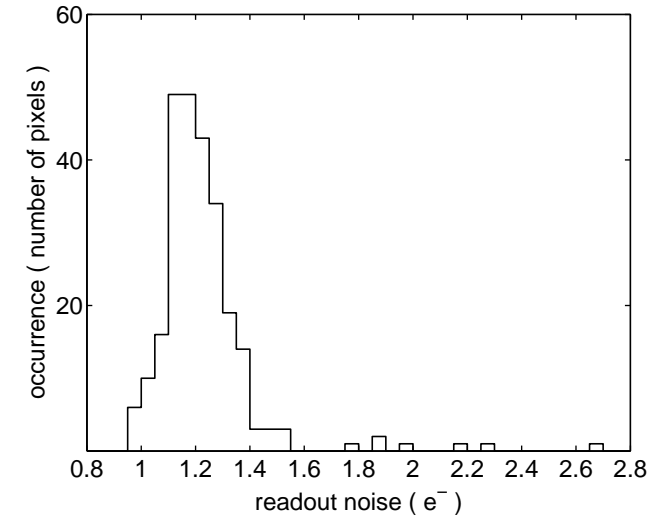


FIGURE 4.16 readout noise histogram of 256 pixels with a p-channel pixel-level source-follower and an open-loop column-level amplifier with enhanced linearity

rection can, unfortunately, only be estimated. For an estimation, the following information should be considered:

Measurements with artificially increased power supply noise have shown higher overall noise increase in the case of the sensor with p-channel input transistor column-level open-loop amplification than in the reference case of the image sensor with pixel-level amplification. From this very qualitative measurement, the power supply noise component in the test columns with column-level open-loop amplifiers using p-channel input transistors is estimated to be equal or greater than the value of 0.6 electrons, as measured for the image sensor with pixel-level amplification.

The logical assumption from a circuit analysis point of view is that the power supply noise has identical amplitude for the single-branch version as well as for the version with enhanced linearity of the column-level open-loop amplifier with p-channel input device. A row noise component of 0.8 electrons is calculated, assuming that the *ratio* of the electronic noise components of the mentioned two amplifier versions corresponds to the simulated ratio of $0.58 \text{ e}^- / 0.85 \text{ e}^-$, as given in Table 4.1, and considering that the measured readout noise, as given in Table 4.2, is the square root of the sum of squares of electronic readout noise and the row noise component.

4.3.3 Interpretation of Simulation and Measurements

From the above considerations an equivalent readout noise charge as low as 0.6 electrons to 0.8 electrons is estimated for a future array implementation of an image sensor with a p-channel pixel-level source-follower and an open-loop column-level single-branch degenerate common-source amplifier with row noise correction based on black columns.

Simulation of circuit linearity and knowledge of the linearity of BPDs illustrate that degenerate common-source open-loop amplifiers provide more than sufficient linearity for processing of image sensor signals even in their simplest single-branch implementation. This result has been confirmed by measurements. The simple single-branch implementation is, therefore, preferred over more complex versions with enhanced linearity but suffering from increased noise.

Chapter 5

Energy-Sensitive Single-Photon X-ray and Particle Detectors

5.1 Introduction

Energy-sensitive single-photon or particle imaging systems are able to detect and count single high-energy photons or particles. In addition to detection such systems can also determine the energy of the detected photons or particles. Such imaging systems usually employ semiconductor detectors which sense electrical charge pulses created by the absorption of the photons or particles in an absorbing material. The particles or photons arrive erratically and the imaging system therefore needs to perform asynchronous detection of the resultant discrete charge pulses. The detection of these charge pulses gives only part of the required information, however, as the energy of each particle must also be measured. This energy measurement is performed by determining the amplitude of each of the charge pulses, hence the effective energy resolution depends on the accuracy of the charge measurement.

This chapter is organized as follows: The remainder of Sect. 5.1 gives key application examples and introduces the basic topology of energy-sensitive single-photon and particle imaging systems, Sect. 5.2 gives a brief overview of particle sensing devices, Sect. 5.3 describes various architectures of asynchronous charge pulse detecting circuits with an emphasis on noise analysis, and Sect. 5.4 covers the subjects of voltage pulse processing circuits and information readout schemes. Finally, Sect. 5.5 summarizes the conclusions drawn from the analysis of the charge pulse detector circuits presented in this chapter.

With respect to its interaction with matter, electromagnetic radiation can be considered as quantized into individual particles, the so called photons, with rest mass zero. For the sake of readability, the term particle will therefore include the relevant case of X-ray photons, unless distinction is made explicitly.

5.1.1 Applications

Existing and emerging applications of energy-sensitive single-photon and particle imaging can be found in a variety of fields including security, material science and inspection, medical imaging, or particle physics research. A non-exhaustive selection of examples is given here.

Absorption X-ray imaging uses radiation sources with a relatively broad spectrum. X-ray photons transmitted through a sample are detected. In conventional detectors, optoelectronic charge generated by a high number of detected photons is integrated during an exposure time in order to produce a transmission intensity image. The integration process implicitly performs a weighting of the detected photons by their energy. Since the probability of absorption in the sample generally decreases with increasing photon energy, weighting by energy results in a loss of contrast. Photon-counting detectors avoid weighting by photon energy and can, therefore, inherently achieve better contrast than charge-integrating detectors. Energy-sensitive detectors furthermore allow restriction of the counting to a selected energy window. Spectral ranges having poor absorption can, therefore, be discarded for further contrast enhancement. Generally speaking, energy-sensitive detectors allow selection of a narrow spectral range even if a wide-spectrum source is used. They may, therefore, allow use of X-ray tubes for applications which have previously been reserved for use with synchrotron sources.

The method of *X-ray absorption spectroscopy* determines the X-ray absorption properties of a sample as a function of the photon energy. For this purpose a radiation source of a tunable narrow spectrum is used. Photon counting in a narrow energy window achieves good precision of this spectroscopy method by suppressing detection in non-relevant energy ranges.

In *X-ray fluorescence* experiments a sample is irradiated by primary X-ray photons of high energy. Subsequent electron excitation and relaxation results in emission of secondary X-ray photons of lower energy. The energy of secondary photons is a characteristic of a material's atomic and crystalline structure. Suppression of primary photon detection and energy discrimination of secondary photons are requirements that make energy-sensitive single-photon imagers ideal candidates for this application.

5.1.2 Basic Topology

Energy-sensitive X-ray and particle imagers are segmented detectors consisting of one- or two-dimensional arrays of detector channels or pixels. Due to the potentially high number of pixels the electrical power available per pixel is usually restricted. A single pixel circuit, as shown in Fig. 5.1, generally contains the following three building blocks:

Sensing device: a transduction device which absorbs particles in the target range of energies and produces an amount of charge that corresponds to the energy of the absorbed particle

Electronic charge pulse detecting circuit: an asynchronous electronic circuit able to detect a charge pulse generated by the sensing device and to produce a voltage pulse of an amplitude proportional to the detected amount of charge at any time a charge pulse is created

Voltage pulse processing circuit: an electronic circuit able to process information of incoming voltage pulses. Depending on the application, required functionalities include peak amplitude detection, energy-windowed pulse counting or multi-threshold binning, pulse width detection, as well as storage and readout of detected information.

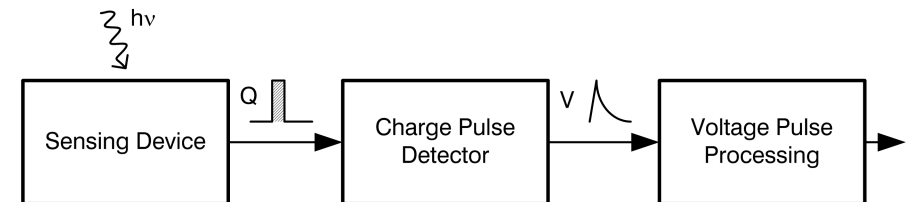


FIGURE 5.1 Functional block diagram of a detector pixel for energy-sensitive particle imaging

5.2 Particle Sensing Devices

Sensing devices for energy-sensitive particle imaging need to meet a specific set of requirements. First of all, they need to be able to absorb particles of their application to a sufficient degree. In addition, the process of absorption and charge collection needs to take place in a period significantly shorter than the maximum particle hit rate of a detector pixel in order to avoid charge pile-up¹

¹The term 'pile-up' denotes accumulation of signal information of consecutive particle detections

from consecutive particle absorptions. Furthermore, as will be explained in Sect. 5.3, meeting the stringent specifications of power consumption and noise in charge pulse detecting circuits requires a maximally low capacitance of the sensing device.

Sensing devices that fulfill the outlined requirements can be classified according to their principle of operation, i.e. direct conversion vs. scintillator-based, and by the type of their manufacturing and assembly, i.e. monolithic integration vs. hybrid manufacturing.

5.2.1 Direct Conversion Sensing Devices

Direct conversion sensing devices are based on mobile charge carrier generation by absorption of high-energy photons or multiple scattering of massive particles in semiconductor materials. Application of a bias voltage across a p-i-n conversion layer depletes the semiconductor and allows for virtually recombination-free separation of mobile electrons and holes generated by the ionizing events. The degree of absorption for a particle of a given energy and the resulting number of created electron-hole pairs generally depends on the thickness and material of the conversion layer. Silicon is a convenient conversion material, as it enables economic fabrication of sensing, detecting and processing circuits in the same material. However, the thickness of a silicon conversion layer for high particle energy can be quite high. Semiconductors with higher atomic number, such as cadmium telluride or germanium, can provide more efficient absorption properties. Thicknesses of conversion layers range from tens to several hundreds of micrometers and bias voltages for depletion may be as high as several kilovolts.

Monolithic Detectors

In the case of monolithic detectors a direct conversion layer is fabricated on the same substrate as the detector electronics. The conversion layer may be part of the substrate used for fabricating the electronics, which is either monocrystalline or epitaxially grown. This approach is limited in practice to silicon and germanium direct conversion layers. The alternative method of growing or depositing direct conversion layers on the detecting circuit substrate gives access to a wider choice of semiconductor materials.

Hybrid Detectors

Hybrid detectors consist of a direct conversion layer and an integrated detector circuit that are manufactured on two different substrates. The substrates are assembled using bump bonding or flip-chip technology with one bonding connection per pixel [61] [62]. Manufacturing technology for the detector

electronics may be chosen without any restrictions concerning the substrate characteristics. Besides a bond pad on the topmost metal layer, the entire area of a pixel may be covered by the electronic circuit.

5.2.2 Scintillators Coupled to Sensing Devices for Visible Light

Scintillator materials are luminescent in response to ionizing radiation such as massive particles or photons of sufficient energy. A scintillator flash, i.e. a pulse of photons of, in most cases, visible wavelength is produced as a result of an ionizing particle hitting the scintillator. The exact mechanism of this process depends on the type of scintillator material as well as the type of ionizing particle. The emission of visible-wavelength photons can be nearly immediate in the case of a fluorescence effect. In the case of phosphorescence or delayed fluorescence the scintillator flash consists of one or several superimposed decays of longer decay times. Depending on the application suitable solid-state scintillator materials include inorganic and organic crystals, glasses, polymers, and powders.

A particle sensing device is created by optically coupling a scintillator layer to a suitable semiconductor sensing device for visible-wavelength photons emitted by the scintillator. Besides being sensitive to the corresponding wavelength, selection criteria for such a sensing device include short response time and low capacitance at a dimension matching the application. Sensing device dimensions for X-ray and particle imaging applications are typically larger than for conventional visible light imagers, e.g. several tens to a few hundred micrometers for medical X-ray imaging to date. The following sub-sections give a short overview of the most common visible-light sensing device types that may be used in conjunction with scintillators.

p-n Photodiodes

p-n photodiodes consist of a junction between a p-type and n-type semiconductor to which a reverse bias voltage is applied. Mobile holes and electrons generated by absorption of a visible-wavelength photon are separated by the resulting electrical field in the depletion zone. The charge collection time of p-n diodes is generally negligible with compared to the width of the visible light peak provided by typical scintillators. Despite their good response time, p-n diodes suffer from relatively high sensing device capacitance since the latter is proportional to the sensing device area.

Photogates

Photogates are Metal²-Oxide-Semiconductor (MOS) devices in which the application of a bias voltage between the semiconductor and the metal electrode creates a depleted zone in the semiconductor where absorption-generated mobile holes and electrons are vertically separated. A p-n junction, biased at a lower electron potential energy than the semiconductor-oxide interface, is adjacent to the MOS structure. Charge carriers that have drifted vertically to the semiconductor-oxide interface diffuse laterally to this p-n junction called the sense node. The sensing device capacitance of a photogate corresponds to the sense node capacitance and is practically independent of the photogate MOS capacitance. Photogates thus have a sensing device capacitance which is area-independent and generally low. The response time of the conventional photogate is limited by the process of lateral diffusion transport and may be excessive for many applications.

Lateral drift field photogates are photogates with a voltage difference applied between two edges of the top electrode. The resulting electrical lateral field at the semiconductor-oxide interface causes drift transport of mobile charge towards the sense node [63]. This method allows overcoming the response time limitations observed with conventional photogates.

Buried Photodiodes

Buried photodiodes are, in many ways, similar to photogates. The fundamental difference being the creation of a depletion zone by the use of a vertical stack of p-type and n-type implants in a p-type substrate instead of a MOS structure. The vertical position of minimum electron potential energy, where generated electrons drift to, is buried at a certain distance below the semiconductor surface. A MOS-type transfer gate is available for triggered charge transfer from the buried photodiode to a p-n junction-type sense node. For asynchronous detection of charge pulses, the transfer gate is continuously active. Diffusion transport is responsible for lateral movement of charge carriers onto the sense node. The use of buried photodiodes is, therefore, restricted to applications where long sensing device response times and relatively small pixel areas are acceptable. Besides low sensing device capacitance, an important advantage of buried photodiodes is their availability in modern CMOS manufacturing processes that allow fabrication of high-performance charge pulse detecting circuits.

²Note that the top electrode of MOS devices is made from polycrystalline silicon in most manufacturing processes.

5.3 Asynchronous Charge Pulse Detecting Circuits

Every pixel of an energy-sensitive particle imager contains an analog circuit able to convert electronic charge pulses into voltage pulses. Destruction of optoelectronic charge after detection, commonly referred to as charge reset, is a further task performed by the detecting circuit. Asynchronous detecting circuits may have continuous, i.e. asynchronous, or clocked, i.e. synchronous, charge reset functionality. Clocked reset operation generally introduces a dead time, where signal charge pulses are destroyed without being detected. From the following analysis it can be understood that clocked reset is a particular case of continuous reset operation. Therefore, the analysis of this chapter only considers the case of continuous reset.

The requirements for charge-pulse detecting circuits suitable for energy-resolved particle detecting pixel circuits are summarized qualitatively in the following list:

- low electronic noise
- low power consumption
- low semiconductor area
- high charge-to-voltage conversion factor
- high linearity of charge-to-voltage conversion

Sections 5.3.1 and 5.3.2 discuss two different topologies of charge-pulse detecting circuits used for energy-sensitive particle imaging.

5.3.1 Charge Sensitive Amplifier

The charge sensitive amplifier (CSA) is employed in many particle detectors, in particular for two-dimensional arrays with small pixel circuits [64]. Its invention dates back to the days of discrete circuits.

As illustrated in Fig. 5.2, a CSA consists of an operational transconductance amplifier (OTA), a feedback capacitor, a feedback resistor R_f in parallel with the feedback capacitor for continuous reset, and a load capacitance C_l on the output of the OTA. The sensing device is connected to the virtual ground node of the circuit. The overall capacitance C_{in} of the virtual ground node is approximately equal to the sum of sensing device capacitance and OTA input capacitance.

Due to feedback operation, a pulse of optoelectronic charge is quickly transferred onto the feedback capacitor and creates a step of the output voltage, as

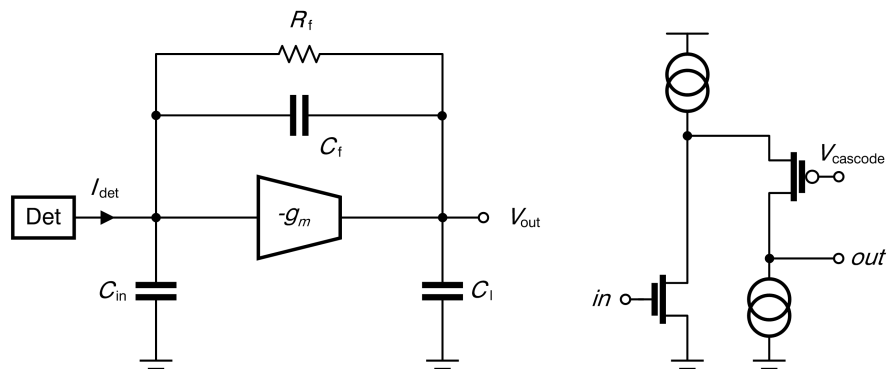


FIGURE 5.2 Left: Circuit topology of a charge sensitive amplifier (CSA). Right: Single-branch folded cascode transconductance amplifier

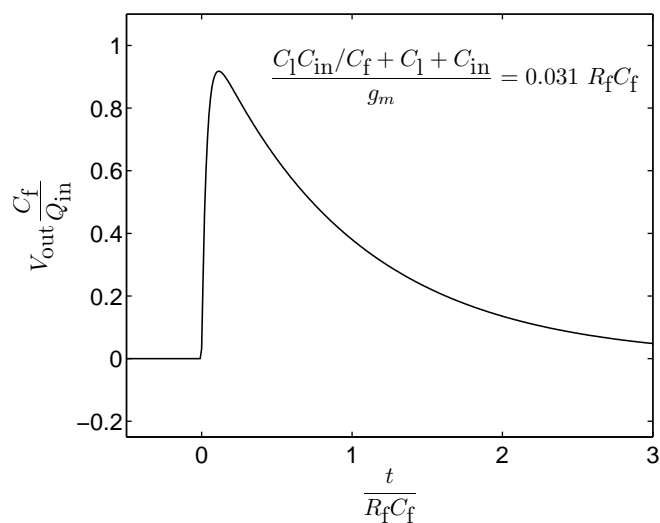


FIGURE 5.3 Normalized CSA response to a Dirac input current pulse

illustrated in Fig. 5.3. The voltage difference across the feedback capacitor is slowly discharged by the feedback resistor. An asymptotic decay, therefore, follows an output voltage peak and brings the detector back to its equilibrium operating point.

The transimpedance function Z_{sig} , which relates the CSA output voltage V_{out} to sensing device current I_{det} , is given by (5.1) and illustrated in Fig. 5.4.

$$Z_{sig} = \frac{R_f (1 - sC_f/g_m)}{1 + s \left(R_f C_f + \frac{C_l + C_{in}}{g_m} \right) + s^2 (C_l C_{in} + C_l C_f + C_{in} C_f) \frac{R_f}{g_m}} \quad (5.1)$$

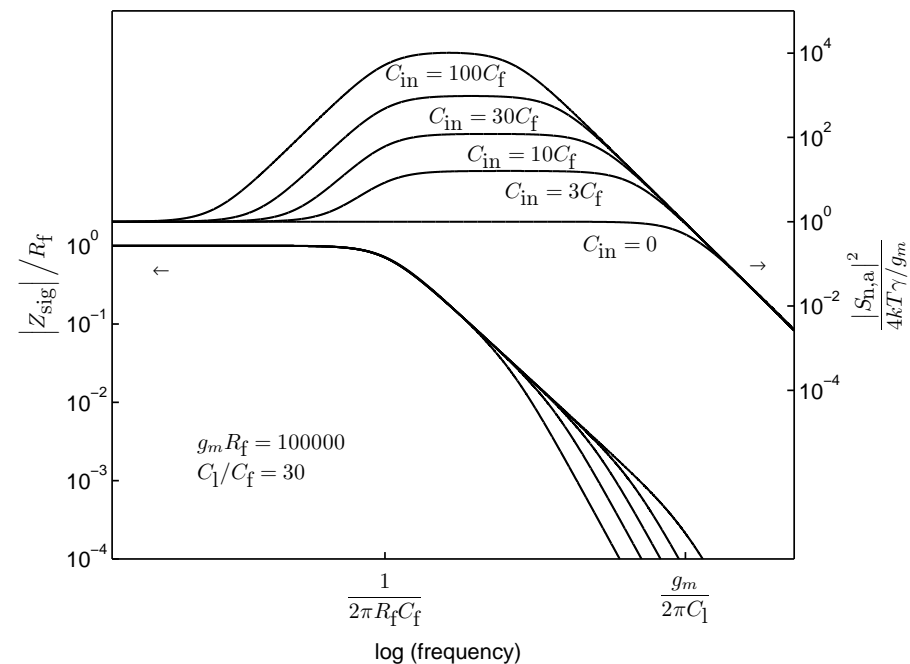


FIGURE 5.4 Normalized signal transimpedance function and amplifier noise power spectral density of a CSA for several values of input capacitance

For sufficiently high transconductance of the OTA, the transimpedance function possesses real dominant and non-dominant poles at $1/R_f C_f$ and $g_m / (C_l + C_{in})$ respectively. The effect of the high-frequency zero at g_m / C_f is usually negligible. The useful frequency span of a CSA is found between the dominant and non-dominant pole frequencies, where the transimpedance function takes an

approximate value of $1/sC_f$. Signal charge pulses shorter than the CSA decay time of R_fC_f are thus converted into output voltage pulses with a conversion factor of approximately the inverse feedback capacitance. The use of small feedback capacitance, therefore, achieves high output voltage for low input charge independently of the input capacitance. The rise time of the output voltage pulse is governed by the non-dominant pole.

Low feedback capacitance and large load and input capacitances require high OTA transconductance in order to keep the non dominant pole frequency sufficiently high for the conversion factor to be governed by the feedback capacitance. Accordingly, high OTA power consumption is the consequence of high sensing device capacitance.

Furthermore, the combination of high input capacitance and low feedback capacitance results in low values of the CSA's voltage feedback factor. Therefore, loss of conversion factor due to finite amplifier gain is observed if the OTA's open-loop voltage gain is not sufficiently high. This open-loop gain is defined by the product of the OTA transconductance and the OTA's output resistance in parallel with the feedback resistor. In case the feedback resistor is lower than the OTA's output resistance, undesired lowering of the open-loop gain can be avoided by inserting a source-follower type buffer between the OTA output and the feedback resistor [65]. However, very high voltage gain, i.e. high OTA output impedance, is still required in cases of sensing device capacitances several orders of magnitude larger than the feedback capacitance. For this reason, regulated cascode amplifiers have been suggested for such applications [66]. For more moderate ratios of input capacitance over feedback capacitance, single-branch folded cascode OTAs, as shown in Fig. 5.2, are good candidates thanks to their low power supply voltage requirement, decent output signal swing, and low parasitic capacitance in parallel with the feedback capacitor [67] [68] [69].

The noise of the detector circuit is a fundamental limit of the energy resolution and, therefore, needs careful consideration in the design of particle detectors. In the following analysis the noise generated in the amplifier³ and in the feedback resistor is investigated. Both noise sources are analyzed separately. Furthermore, Poisson noise of the sensing device leakage current is considered⁴.

Feedback Resistor Noise of CSAs

The principal noise source in the feedback resistor is thermal noise. The power spectral density (PSD) $S_{n,f}^2$ of the voltage noise on the CSA output node contributed by the feedback resistor is given in (5.2):

$$S_{n,f}^2 = \frac{4kT\gamma R_f \left| 1 + s \frac{C_{in}}{g_m} \right|^2}{\left| 1 + s \left(R_f C_f + \frac{C_1 + C_{in}}{g_m} \right) + s^2 (C_1 C_{in} + C_1 C_f + C_{in} C_f) \frac{R_f}{g_m} \right|^2} \cdot \quad (5.2)$$

The thermal noise excess factor γ needs to be considered, if the feedback resistor is actually implemented by use of a MOS transistor. Note that the poles of the feedback resistor noise PSD are equal to the poles of the signal transimpedance function. The frequency of the zero is always higher than the dominant pole frequency in the case of a CSA properly designed for reproducible and high conversion factor. The equivalent noise charge (ENC), as given in (5.3), can, therefore, be approximated by the integral of a first order noise voltage PSD at a bandwidth defined by the dominant pole, divided by the ideal conversion factor.

$$q_{n,f} \approx \sqrt{kT\gamma C_f} \cdot \quad (5.3)$$

Tuning of the feedback resistor has no influence on the ENC, since opposite effects are affecting the spectral density and the bandwidth. For a chosen value of feedback capacitance the feedback resistor noise is constant and defines a limit for the CSA noise performance.

Amplifier Noise of CSAs

The MOS-transistors of the OTA exhibit thermal noise and flicker noise. The analysis presented here is restricted to thermal noise, which is a valid assumption for a wide range of applications and manufacturing processes. The analysis of flicker noise can be extended from the analysis for thermal noise and is described in [70]. The major component of electronic noise in well-designed OTAs is contributed by the input transistors. The output noise PSD, as given by (5.4) and illustrated in Fig. 5.4, is found from a simplified analysis, neglecting the noise of the remaining transistors.

$$S_{n,a}^2 = \frac{(4kT\gamma/g_m) \left| 1 + sR_f (C_{in} + C_f) \right|^2}{\left| 1 + s \left(R_f C_f + \frac{C_1 + C_{in}}{g_m} \right) + s^2 (C_1 C_{in} + C_1 C_f + C_{in} C_f) \frac{R_f}{g_m} \right|^2} \cdot \quad (5.4)$$

³Amplifier noise is also referred to as series noise in literature.

⁴Feedback resistor noise and sensing device leakage current shot noise are also referred to as parallel noise in literature

Besides two poles equal to those of the signal transimpedance function, a zero at $1/R_f(C_f + C_{in})$ causes peaking of the amplifier noise PSD in the useful frequency span. The effect increases with decreasing voltage feedback factor, i.e. with increasing C_{in}/C_f . At a given OTA transconductance, the noise bandwidth is reduced with increasing total input capacitance. Despite this partial compensation, the amplifier ENC increases with C_{in} , as illustrated for an example design in Fig. 5.5.

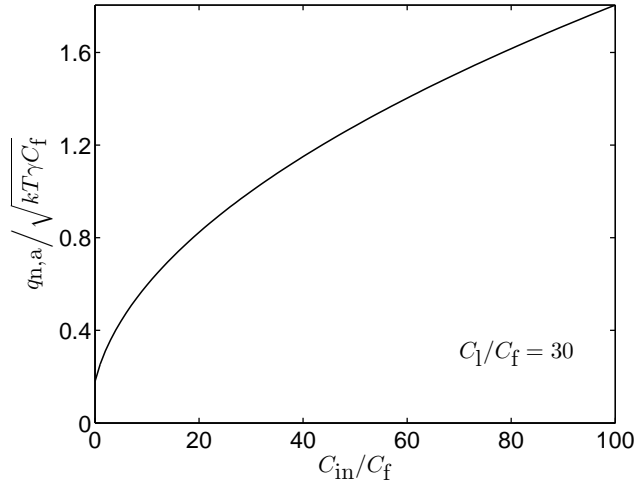


FIGURE 5.5 Normalized ENC of the amplifier noise component versus total input capacitance

A simple approximation of the amplifier ENC is given by (5.5) and suggests a square-root dependence on C_{in} :

$$q_{n,a} \approx \sqrt{kT\gamma \frac{C_f C_{in}}{C_1}} . \quad (5.5)$$

This result illustrates that, as opposed to feedback resistor noise, no fundamental limit exists for amplifier noise. By choosing a high load capacitor amplifier noise can always be reduced to a level below feedback resistor noise. High load capacitance and high input capacitance requires, however, very high transconductance for keeping the non-dominant pole at a sufficiently high value. Considering the implications on circuit area and power consumption, it is obvious that CSA-based highly segmented particle imagers with good energy resolution require low sensing device capacitance.

Sensing Device Leakage Current Poisson Noise in CSAs

Besides signal charge pulses, sensing devices generally deliver leakage current to the detector circuit. In particular, some direct conversion sensing devices suffer from relatively high leakage.

The leakage current's Poisson noise⁵ power spectral density, of $2qI_{leak}$, is multiplied by the square of the signal transimpedance function, $|Z_{sig}|^2$, in order to obtain the output noise PSD. Besides a difference in high frequency zeros, the Poisson noise displays the same spectral shape as the feedback resistor noise, i.e. the noise power is confined to the low-frequency region below the dominant pole frequency of the CSA. The input referred noise charge due to sensing device leakage Poisson noise is described by the simple approximation of (5.6):

$$q_{n,Poisson} \approx \sqrt{\frac{1}{2} R_f C_f q I_{leak}} . \quad (5.6)$$

The impact of sensing device leakage Poisson noise is negligible, if its current PSD $2qI_{leak}$ is significantly below the feedback resistor current PSD of $4kT\gamma/R_f$.

Sensing Device DC Current Compensation

DC input current flowing to the detector circuit consists of leakage current of the sensing device and signal current due to constant background light, if not avoided in the operating setup. In a conventional CSA, of the type illustrated in Fig. 5.2, the described DC current components flow across the feedback resistor and create a DC shift in the CSA output voltage⁶. This can lead to poor performance of the subsequent voltage pulse processing circuit or, in extreme cases, saturation of the CSA output voltage.

A CSA with DC current compensation, as illustrated in Fig. 5.6, has been shown to be an effective solution to the problem [71] [64].

The functionality of the feedback resistor is implemented by the differential pair, since the small signal drain current of the left-side MOS transistor, injected into the left-hand plate of the feedback capacitor, is proportional to the small-signal output voltage.

A low-frequency high-gain feedback path is provided by the right-side drain-current output of the differential pair, a current source, a compensation capacitor C_{comp} , and a common-source transistor M_{CS} . Thanks to its high

⁵Poisson noise is also referred to as shot noise

⁶in literature the DC shift of the output signal is also referred to as baseline shift

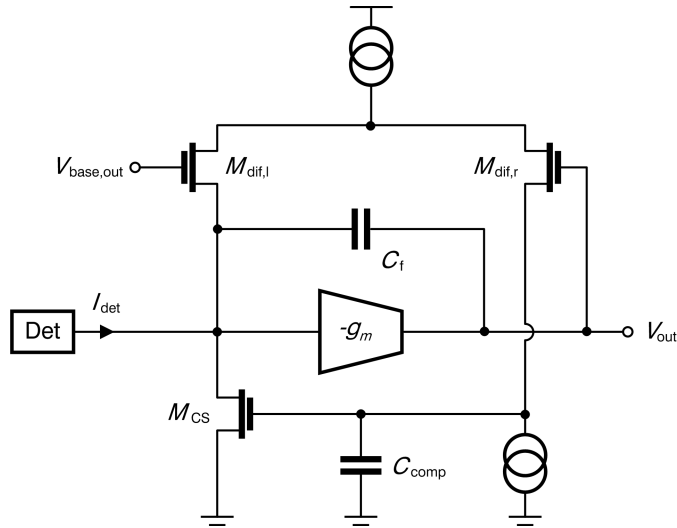


FIGURE 5.6 CSA with sensing device DC current compensation

transconductance, the resulting two-stage transconductance amplifier can deliver significant DC current to the sensing device at very low variations of its input voltage, i.e. the CSA output voltage. The compensation capacitor is chosen such that the bandwidth of the high-gain feedback amplifier is orders of magnitude below the dominant pole frequency of the CSA. Therefore, the feedback amplifier does not influence the detection and processing of the charge pulses. There is, however, additional noise associated with the feedback amplifier. Thermal noise of the common-source transistor M_{CS} is the predominant component of this noise, and it is of the same order of magnitude as the noise of the equivalent feedback resistor. Note that the maximum compensated positive and negative DC currents are not equal. The circuit, as shown in Fig. 5.6 is particularly suited for compensating positive current. For negative DC current, the complementary circuit made from p-type transistors is advantageous.

5.3.2 Charge Sensitive Amplifier with Shaper

The noise performance of CSAs is limited by thermal noise of the feedback resistor. The feedback resistor's noise power is confined to the spectral range below the dominant pole at $1/R_f C_f$, as stated by (5.2). The useful frequency span of the circuit and the relevant content of the signal is found above the dominant pole of the CSA. Charge sensitive amplifiers with shapers make use

of this spectral separation in order to reduce feedback resistor noise by filtering without compromising the signal [68] [72] [73] [74] [75].

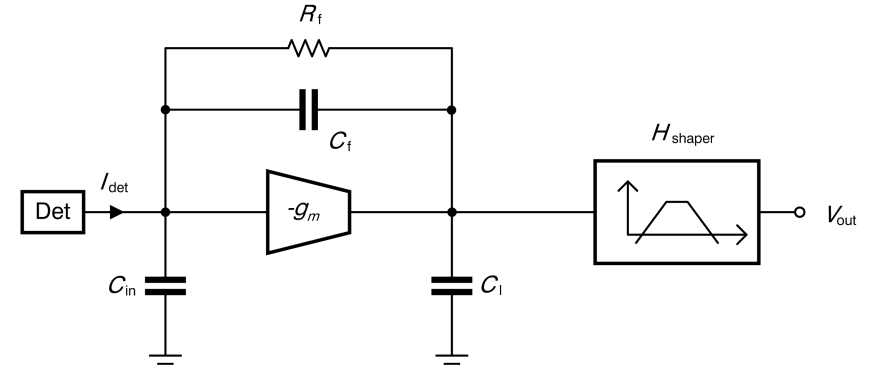


FIGURE 5.7 Topology of a CSA-shaper circuit

Although the basic topology of a CSA used in conjunction with a shaper circuit, as illustrated in Fig. 5.7, is identical to the topology of a non-shaped CSA the design criteria for minimized noise are somewhat different.

The shaper circuit generally is a band-pass filter with a high-pass filtering frequency of f_{hp} and a low-pass filtering frequency of f_{lp} . Shapers are most usually $CR - RC^n$ filters, i.e. a combination of a first order high-pass function and an n^{th} order⁷ low-pass function. The generic shaper transfer function is thus given by (5.7) and illustrated in Fig. 5.8 for the example of a 1st order shaper with unity gain:

$$H_{\text{shaper}} = A_{\text{shaper}} \frac{s / (2\pi f_{hp})}{(1 + s / (2\pi f_{hp})) (1 + s / (2\pi f_{lp}))^n} . \quad (5.7)$$

The resulting signal transimpedance function of a CSA-shaper circuit is given by (5.8).

$$Z_{\text{sig}} = \frac{H_{\text{shaper}} (R_f (1 - s C_f / g_m))}{1 + s \left(R_f C_f + \frac{C_1 + C_{\text{in}}}{g_m} \right) + s^2 (C_1 C_{\text{in}} + C_1 C_f + C_{\text{in}} C_f) \frac{R_f}{g_m}} . \quad (5.8)$$

⁷n is also referred to as the shaper order

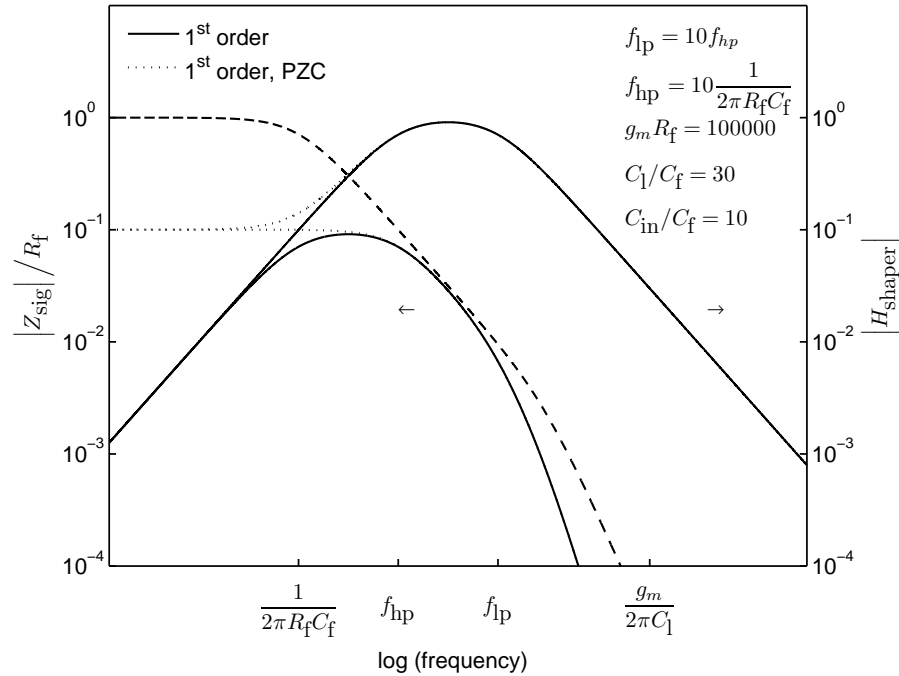


FIGURE 5.8 Normalized shaper transfer function and shaped signal transimpedance function in case of 1st order shaping with pole-zero cancellation (PZC) (dotted lines) and without PZC (solid lines). Signal transimpedance function without shaping (dashed line) for reference

The useful frequency span, where the signal transimpedance function is approximately equal to $1/sC_f$, is now defined by the pass-band of the shaper circuit. The transimpedance function corresponds to the output signal spectrum of the CSA-shaper circuit, stimulated by a Dirac unity current pulse from the sensing device. The shaped pulse at the output of a CSA-shaper circuit will, therefore, display a decay time governed by f_{hp} that will generally be shorter than the decay time of the CSA. Thanks to the use of the shaper, pulses occurring within a short time interval will thus be discriminated more easily by the voltage pulse processing circuit. The rise time of the output pulse is governed by f_{lp} .

The loss in amplitude of the voltage pulse on the shaper output compared to the CSA output⁸ is called the ballistic deficit of the detector. It is a function of the deviation of the transimpedance function in its useful range from the ideal capacitance impedance $1/sC_f$. A significant ballistic deficit can be caused by too narrow a bandwidth of the shaper filter, low spectral spacing between the dominant pole frequency and f_{hp} , or low spectral spacing between f_{lp} and the non-dominant pole frequency of the CSA.

Since the output signal spectrum has a peak at non-zero frequency, the corresponding time-domain response displays some harmonic content, i.e. a signal undershoot, as illustrated in Fig. 5.9. If the signal undershoot would disturb correct operation of the voltage pulse processing circuit, the method of pole-zero cancellation (PZC) can be employed [76] [77] [78] [74] [65]. The basic concept of the method is to compensate the dominant pole of the CSA by a matched zero in the shaper transfer function, as given by (5.9). The resulting signal transimpedance function, and hence the output signal spectrum, therefore has a band-limited flat spectrum, as illustrated in Fig. 5.8. The corresponding time-domain response is a well-damped undershoot-free output signal.

$$H_{\text{shaper,PZC}} = \frac{A_{\text{shaper}} 2\pi R_f C_f f_{hp} (1 + s R_f C_f)}{\left(1 + s / (2\pi f_{hp})\right) \left(1 + s / (2\pi f_{lp})\right)^n} \cdot \quad (5.9)$$

On one hand, a shaper circuit reduces feedback resistor noise and, under some conditions, amplifier noise of a CSA, as discussed in the following sections. On the other hand, a shaper circuit also generates additional noise that should be taken into account when evaluating the overall performance of the charge pulse detecting circuit. The amplitude of shaper circuit noise depends on many

⁸a ballistic deficit may even be observed on the CSA output, if the spacing between the non-dominant and dominant poles is poor or if the response time of the sensing device is longer than the reset time constant

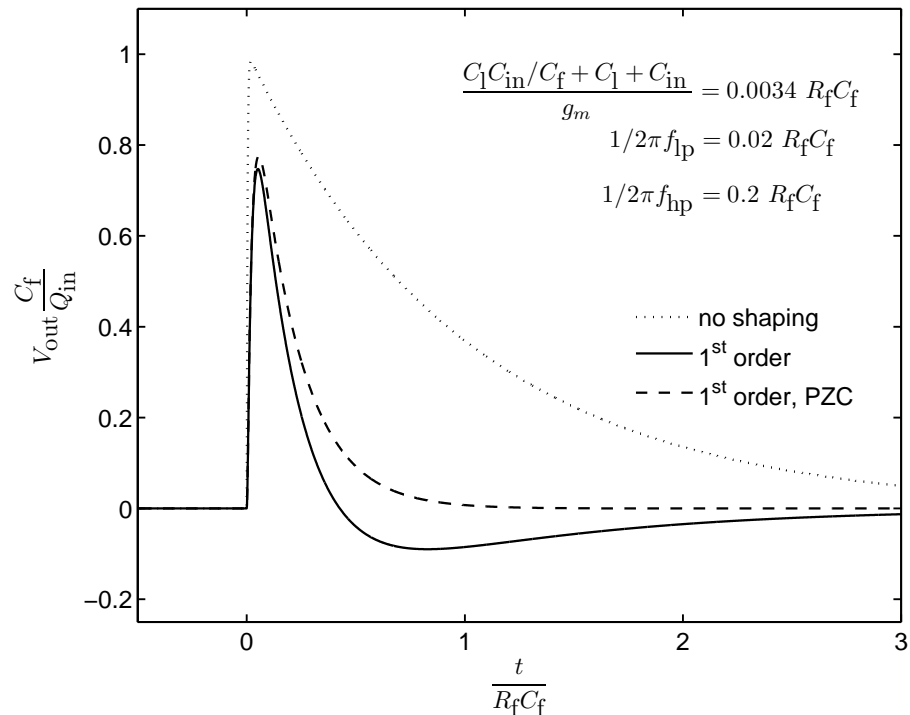


FIGURE 5.9 Normalized CSA-shaper output response to a Dirac input current pulse with PZC (dashed line) and without PZC (solid line). CSA response (dotted line) for reference

properties and parameters of the shaper. Noise analysis for various shaper architectures can be found in literature, e.g. in [74]. The analysis presented here will be limited to the noise components of the CSA.

Feedback Resistor Noise of CSA-Shaper Circuits

A shaper circuit can reduce the input referred noise charge of the feedback resistor below the $\sqrt{kTC_f}$ limit found for CSAs without shapers. The feedback resistor noise power spectral density, as illustrated in Fig. 5.10, corresponds to the product of the noise power spectrum at the CSA output (5.2) and the square of the amplitude of the shaper transfer function (5.7).

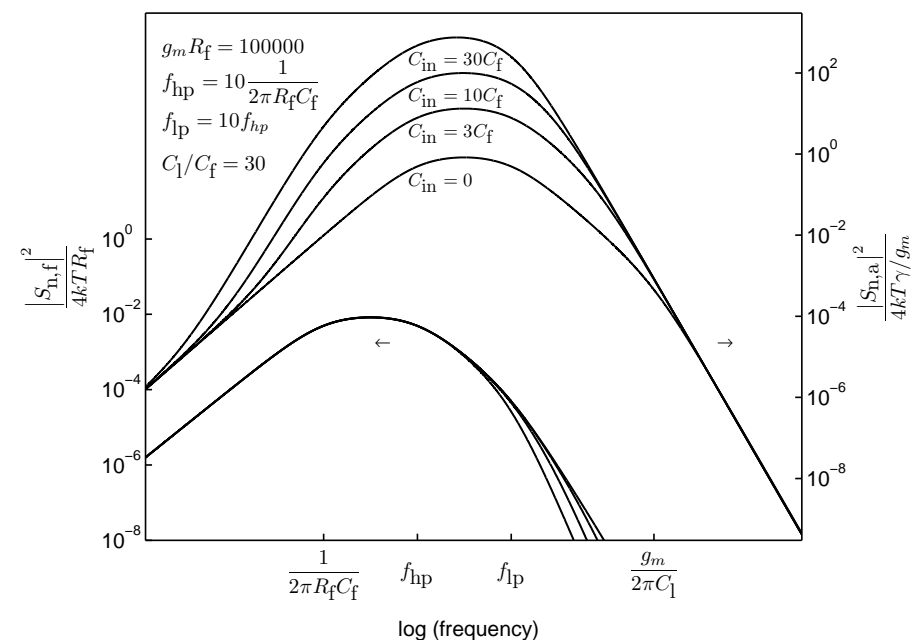


FIGURE 5.10 normalized output noise power spectral densities of the feedback resistor noise and the amplifier noise of a CSA with a first order shaper

For a shaper high-pass frequency significantly higher than the frequency of the CSA dominant pole, shaping has two major effects on the feedback resistor noise spectrum. First of all, the relevant bandwidth of the feedback resistor noise is increased from the dominant pole frequency to the high-pass filtering frequency. Secondly the relevant noise power spectral density is attenuated by the square ratio of high-pass filter frequency over the dominant pole frequency.

The input referred noise charge is, therefore, reduced approximately by the square root of the mentioned frequency ratio, as expressed by (5.10):

$$q_{n,f,\text{shaped}} \approx \sqrt{kT\gamma C_f \frac{1/(2\pi R_f C_f)}{f_{\text{hp}}}} = \sqrt{\frac{kT\gamma}{2\pi R_f f_{\text{hp}}}}. \quad (5.10)$$

It becomes apparent that a high frequency spacing between the CSA dominant pole and the high-pass filter frequency is a key factor for low-noise CSA-shaper detectors. It has to be considered that the maximum possible value of the high-pass filter frequency is constrained by the finite width of charge pulses delivered by sensing devices, as well as by power consumption, which increases with required circuit bandwidth. Therefore, the reduction of feedback resistor noise requires reduction of the dominant pole frequency, i.e. increase of $R_f C_f$. Although an increase of the feedback capacitor lowers the output noise voltage, no reduction of the input referred noise charge is observed, due to the corresponding decrease of conversion factor. For these reasons, noise optimization of CSAs used in combination with shaper circuits involves the design of very high feedback resistance, in particular if a high conversion factor is achieved by use of low feedback capacitance.

As outlined in Sect. 5.3.1, the spectrum at the CSA output created by sensing device leakage Poisson noise is very similar to the feedback resistor noise spectrum. The analysis of feedback resistor noise in CSA-shaper circuits can, therefore, easily be extended to sensing device leakage Poisson noise and yields an input referred noise charge of $\sqrt{qI_{\text{leak}}/4\pi f_{\text{hp}}}$.

A pole-zero-canceling shaper offers less noise attenuation in the frequency range below the zero frequency than a shaper without PZC. The PZC-shaped noise spectrum is, therefore, flat in the frequency range below the zero, instead of having a first-order roll-off. The noise increase due to PZC, which is already included in the approximation of (5.10), is relatively low in the case of well-designed systems with a high ratio of high-pass frequency over dominant pole frequency.

Amplifier Noise of CSA-Shaper Circuits

Besides the significant reduction of feedback resistor noise, the use of a shaper circuit has an impact on amplifier noise as well [79]. The amplifier noise PSD at the shaper output is given by the product of the squared amplitude of the shaper transfer function (5.7) times the amplifier noise power spectrum at the CSA output (5.4). The resulting amplifier noise spectrum, as illustrated in Fig. 5.10, shows that shaping does not change the relevant noise power spectral

density. Unlike in the case of CSAs without shaper, the noise bandwidth is now limited to a frequency generally below the non-dominant pole frequency of the CSA. In the case of a first order shaper, the amplifier noise component of the ENC can be expressed by the simple approximation of (5.11):

$$q_{n,a,\text{shaped}} \approx (C_f + C_{\text{in}}) \sqrt{kT\gamma \frac{2\pi f_{1p}}{g_m}}. \quad (5.11)$$

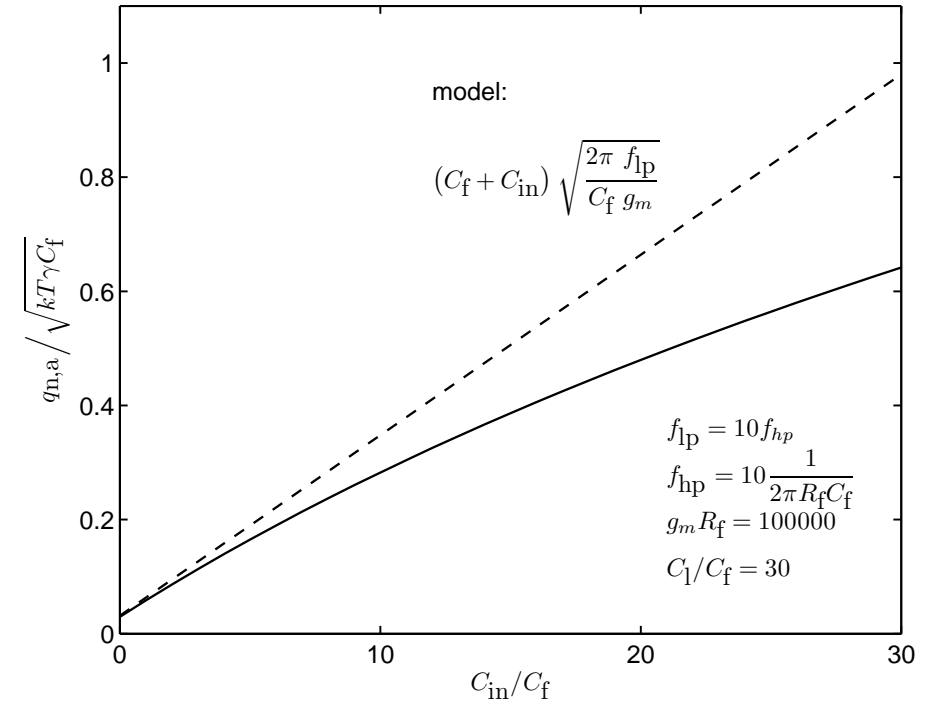


FIGURE 5.11 Normalized ENC of the amplifier noise component versus input capacitance of the CSA with 1st order shaping (solid line) and simplified model of the amplifier noise ENC (dashed line)

A comparison between the ENC calculated by considering the full spectrum and approximation of the full spectrum (5.11) is given in Fig. 5.11 for a constant OTA transconductance. The amplifier ENC deviates from the simple approximation, as the non-dominant pole moves closer to the low-pass filtering frequency for increasing input capacitance.

For CSA-shaper detectors the ENC is reduced for increasing transconductance, since the noise PSD is reduced while the noise bandwidth is kept constant by the shaper. However, increased power consumption and wider input MOS-transistors are required in OTAs with increased transconductance. This results in a higher total input capacitance C_{in} that, in turn, leads to increased amplifier ENC. Increasing the current density of the OTA input transistor is often not a good option, since the thermal noise excess factor γ is increased when going from moderate to strong inversion operation region. An optimum trade-off between increased g_m and increased C_{in} is found as a function of the remainder of the total input capacitance, i.e. the sensing device capacitance [80] [81].

Despite the outlined limitation, the possibility of trading power for amplifier noise without increasing C_1 is a valuable property of CSA-shaper circuits. Nevertheless, the need for low input capacitance for low-noise, low-power performance, as already found in the case of the CSA, equally applies to the CSA-shaper detector circuit.

Feedback Resistor Implementations

The use of very high feedback resistance achieves excellent noise performance in CSA-shaper detectors. In most cases the required value of resistance can not be practically implemented by the use of linear resistor elements available in CMOS process technologies, such as polysilicon resistors. MOS transistors are, therefore, used for the implementation of feedback resistors in most cases.

The non-linearity of the resulting resistance causes distortion of the output pulse. If the distortion affects the peak amplitude, a non-linearity of the detected particle energy is observed.

Feedback resistance decreasing with signal pulse amplitude generally results in an increase of the ballistic deficit, since the dominant pole is temporarily shifted closer to the high-pass filter frequency of the shaper.

If the feedback resistance increases with pulse amplitude, the ballistic deficit is reduced for high pulses. In this case, very low energy non-linearity can be achieved, if the nominal ballistic deficit at low energy is designed to be very low. Conversely, pile-up of signal charge at high detection rates is more likely to occur for such a feedback resistor.

Two examples of feedback resistor implementations using MOS transistors, as illustrated in Fig. 5.12, are introduced and briefly discussed in the following paragraphs.

Feedback Transistor in Triode Region A MOS transistor connected in parallel with the feedback capacitance, operated in triode region, is used in many applications [69] [67]. when using constant gate bias, threshold voltage variation of the feedback transistor M_{fb} as well as offset of the OTA lead to

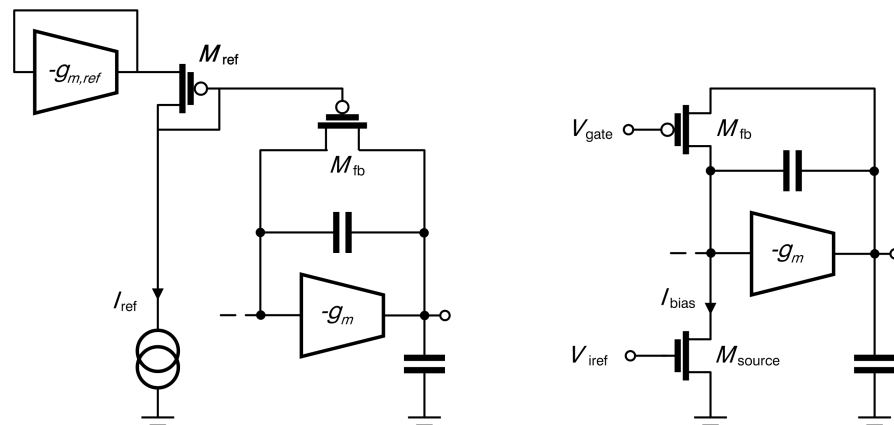


FIGURE 5.12 Implementations of feedback resistors. Left: Feedback transistor in triode region. Right: Common-source transistor in weak inversion region

significant resistance variations that can be reduced by a tracking gate biasing circuit, as suggested in [65] and shown in Fig. 5.12. Nevertheless, the nominal gate bias excess voltage needs to be chosen with a certain margin in order to avoid high variation of the transistor's on-resistance due to the remaining mismatch between the biasing circuit and the feedback transistor plus the OTA. Practically achievable values of feedback resistance are, therefore, limited despite using a transistor with a long and narrow geometry.

A feedback transistor in triode region shows non-linear behavior. Consequently increasing pulse height lowers the on-resistance in the case of electron detection and might, therefore, increase the ballistic deficit. If the charge carriers delivered by the sensing device are holes and the feedback transistor is a p-channel device, the on-resistance increases for high signal pulses. In this case the n-well of this transistor can be connected to the CSA output in order to improve linearity. The diode formed between the n-well and the transistor drain connected to the CSA virtual ground node will be increasingly forward biased for high negative output voltage pulses and will compensate for the increase of the MOS transistors on-resistance [77].

Common Gate Stage in Weak Inversion Region A common gate transistor operated in the weak inversion region, such as illustrated in Fig. 5.12, can achieve very high effective feedback resistance [66]. If the gate bias voltage V_{gate} is chosen sufficiently high compared to the input voltage of the OTA, the feedback resistance, i.e. the transconductance of the common-gate transistor, is controlled by the bias current source independently of OTA input offset.

In the described configuration the quiescent output level is different from

the virtual ground potential and is set by the bias current I_{bias} as well as the gate voltage of the common-gate feedback transistor M_{fb} .

The transconductance of the common gate transistor increases with the output pulse amplitude. Quick return to the baseline and high maximum detection rate are, therefore, achieved at the price of possible distorted energy detection.

Since the additional noise of the bias transistor M_{source} has the same order of magnitude as the common-gate transistor noise, this component should be considered as well for the analysis of the feedback resistor noise.

5.4 Voltage Pulse Processing Circuits

Voltage pulse processing circuits are used in order to extract relevant information from the output signal of the charge pulse detecting circuit. Depending on the application, extracted information comprises pulse arrival time, pulse detection rate or spectroscopic energy information. Voltage pulse processing circuits are generally part of each pixel in a segmented detector with further processing hardware possibly being shared among several pixels.

Readout circuits selectively transfer information from pixel circuits to shared processing hardware. Given the erratic nature of the particle arrival and the potentially huge amount of information collected by a segmented energy-sensitive detector, pixel-level data storage and data readout are a challenging aspect of systems design.

Voltage processing circuits are generally quite specific for the application of the detector. Classification is possible according to the applied method of energy discrimination, as discussed in Sect. 5.4.1. Different approaches to data readout are discussed in Sect. 5.4.2

5.4.1 Energy Discrimination Methods

Voltage pulse processing circuits for energy-sensitive particle imaging can be classified into two general groups. Counting circuits with energy criteria, such as single or multiple threshold discriminating counters, retrieve detection rate information. Spectroscopic detectors, such as amplitude detectors or time-over-threshold detectors, generally provide more precise particle energy information, whereas detection rate information is often discarded.

Multiple Threshold Discrimination

Multiple threshold discriminators are used to count particle arrivals in one or several energy bins. Several comparators with different thresholds and one or more digital counters are used to implement such a processing circuit [64]. The

output of the pixel circuit is, therefore, digital with the binning precision being a function of the charge pulse detector circuit's noise performance.

Amplitude Detection

Amplitude detection methods aim at precise particle energy measurement for spectroscopic applications. Analog amplitude detecting or peak detecting circuits are used to detect and hold the peak value of the voltage pulses from the charge pulse detecting circuit. Asynchronous peak detecting [67] or over-sampled synchronous peak detecting circuits [75] can be used for this purpose. The energy resolution of the amplitude detection directly depends on the noise of the charge pulse detecting circuit.

Time-Over-Threshold Detection

Time-over-threshold detection is an alternative spectroscopic method based on the fact that the absolute pulse width above a constant threshold is proportional to the pulse height, i.e. the input charge for a linear charge pulse detecting circuit. A clock counter can be used in order to generate a digital output that represents the time-over-threshold [82]. This method requires linear charge pulse processing circuits, as non-linear feedback or reset resistors could heavily distort the time-over-threshold.

5.4.2 Information Readout

Pulse counting applications usually involve counting pulses over a defined exposure interval. Furthermore, digital storage of the count numbers in the pixel circuits are possible. Synchronous readout is, therefore, an adequate solution of low complexity for counting applications. The asynchronous nature of pulse arrival and the difficulty of storing energy information for many detected particles in a pixel makes readout of spectroscopic information more challenging. Synchronous readout usually involves discarding a considerable number of detected particles. Self-triggered readout is an interesting, but more complex readout method for spectroscopic voltage pulse processing circuits.

Synchronous Readout

Synchronous readout involves information storage in each detector pixel as well as sequential readout and reset of information using synchronous timing. Each readout circuit is shared and sequentially used by many detector circuits. For spectroscopic energy discrimination, which generates either digital multi-bit or analog information for each detected particle, the amount of information stored in a pixel is usually restricted to one detection. If a synchronous readout

scheme is to be used, the information corresponding to the first or last particle arrival in the observation period is usually read out. Information of remaining detections between two consecutive readout operations is, therefore, discarded.

Self-Triggered Readout

In segmented detectors with self-triggered readout, readout circuits are shared row wise or column wise by several detector circuits, as in the case of synchronous readout. The voltage pulse processing circuits are able to deliver a readout trigger signal upon detection of a particle. The trigger signal is used to select the relevant detector circuit and read its information as soon as the corresponding readout circuit is available. Self triggered readout is not sequential which makes the storage and further processing of the read information more complex. As opposed to synchronous readout, self-triggered readout avoids reading of pixels where no detection has taken place and naturally allocates the readout bandwidth to pixels with non-zero detection rates.

5.5 Conclusions

The energy resolution of particle detectors is, in many cases, limited by the noise performance of the employed charge pulse detecting circuits. The noise performance of state-of-the-art asynchronous charge pulse detecting circuits, as analyzed in this chapter, comprises two predominant components.

First of all, thermal noise of the feedback resistor defines an unavoidable noise limit in CSAs without shapers. This limitation is overcome by the use of shaping in CSA-shaper circuits. Even though an upper limit of the shaper's high-pass filtering frequency is defined by the sensing device's output charge pulse width, the feedback resistor's noise can theoretically be arbitrarily reduced by increasing its resistance value. The challenge of robustly biasing a MOS-transistor implementation of the feedback resistance in presence of amplifier offset defines, however, a practical limit to the achievable feedback resistance noise.

The second important noise component is noise of the amplifier employed in CSAs. Analysis shows that low input node capacitance and feedback capacitance are required in order to achieve low amplifier noise at low power consumption. Mathematically speaking, the amplifier noise component in CSA shapers is approximately proportional to the sum of feedback capacitance plus the total input node capacitance. Sensing devices with low input capacitance, such as BPDs or photogates, can be used in order to reduce the total input capacitance. In this situation, the feedback capacitance as well as the amplifier's contribution to the total input capacitance become significant parameters in the definition of the amplifier's noise contribution.

From the mentioned observations, it can be concluded that for further noise reduction in asynchronous charge pulse detecting circuits two problems need to be tackled. First of all, alternative circuit topologies enabling biasing of even higher recharge resistors in a robust manner, if possible independently of amplifier offset, are required. Secondly, there is a need for circuit topologies with reduced impact or even absence of feedback capacitance and featuring reduced amplifier input capacitance.

Chapter 6

A Novel Buffered X-ray single-photon Detector Circuit

6.1 Introduction

In chapter 5, the interest of small sensing device capacitance for the achievement of low electronic noise at low expense of power consumption has been explained. It has also been outlined that shaper circuits are efficient means to reduce noise contributed by feedback resistors which are used for continuous charge reset in charge sensitive amplifiers. A limitation of this method is, however, the practical difficulty of implementing very high and reproducible values of feedback resistance. CSAs and CSA-shaper circuits have proven high performance over many years, in particular for applications with high sensing device capacitance.

In this chapter, an alternative charge pulse detecting circuit architecture, based on a source-follower buffer, is presented and analyzed [55], [83]. This buffered charge pulse detecting circuit shares many concepts and advantages of CSA-shaper circuits. Its trade-off between noise and power consumption is, however, advantageous in the case of low sensing device capacitance. The proposed detecting circuit is, therefore, an ideal candidate for high-energy-resolution, highly segmented single-photon X-ray and particle imagers, where low power consumption per pixel and low noise are key performance factors.

A practical circuit design targeted at X-ray imaging with scintillators and low capacitance sensing devices, such as buried photodiode or lateral drift field photogates, has been implemented.

The current chapter is organized as follows: Circuit topology and theoretical analysis are discussed in Section 6.2, whereas aspects of designing a practical circuit, simulation results, and measurement results are presented in section 6.3.

6.2 Topology and Circuit Analysis

Noise performance of CSA-shaper circuit is practically limited by two contributions, as discussed in Sect. 5.3.2. First of all, reduction of feedback resistor noise relies on achievement of high feedback resistor values. Stable biasing for very high value resistors implemented by use of MOS transistors has been shown to be challenging. Secondly, at a given power budget and minimum gate length amplifier noise is limited to an optimum value by a trade-off between total input capacitance and OTA transconductance.

In comparison to CSA-shaper circuits, the proposed charge pulse detecting circuit, as shown in Fig. 6.1, pushes the noise limits to higher performance. This noise advantage is principally due to the a significantly reduced proportionality between the equivalent noise charge and the input referred noise voltage thanks to the absence of a feedback capacitor and the very low input capacitance of the source-follower circuit as will be shown in sections 6.2.2 and 6.2.3. For this circuit topology, the sensing device is connected to the input of a source-follower type near-unity-gain buffer. The output of the buffer is filtered by a shaper circuit, very much like in the case of CSA-shaper detectors. Since the source-follower is a buffer circuit without any feedback network, signal charge pulses are converted to voltage steps on the input capacitance C_{in} . A reset resistor R_r continuously removes charge from the input capacitance during a slow decay following a voltage step. Our example uses a first order shaper without PZC. The shaper implementation is a cascade of a passive CR high-pass filter and a source-follower with capacitance load serving as a low-pass filter.

6.2.1 Signal Transfer Function

The signal transimpedance of a buffer-shaper type charge pulse detecting circuit, as given in (6.1), is found under the assumption of exact unity gain of the two source-followers.

$$Z_{sig} \approx \frac{R_r}{1 + sR_r C_{in}} \frac{s/2\pi f_{hp}}{(1 + s/2\pi f_{hp})(1 + s/2\pi f_{lp})(1 + s/2\pi f_{par})}, \quad (6.1)$$

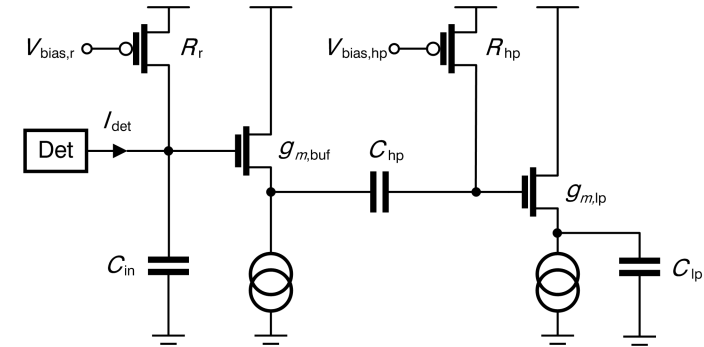


FIGURE 6.1 Implementation example of a buffer-shaper circuit with first order shaping

where

$$f_{hp} = \frac{1}{2\pi R_{hp} C_{hp}}, \quad (6.2)$$

$$f_{lp} = \frac{g_{m,lp}}{2\pi C_{lp}}, \quad (6.3)$$

and

$$f_{par} = \frac{g_{m,sf}}{2\pi (C_{p1} + C_{p2})}, \quad (6.4)$$

In the expression of the parasitic pole frequency f_{par} , C_{p1} and C_{p2} are the parasitic capacitances at the input node of the band-pass filter and the intermediate node of the band-pass filter respectively. These parasitic capacitances are assumed to be significantly lower than the high-pass filtering capacitance C_{hp} . The gain loss due to capacitive voltage division between C_{hp} and C_{p2} is therefore neglected in the presented analysis.

In the useful frequency range, the signal transimpedance takes an asymptotic value of $1/sC_{in}$, which illustrates that the conversion factor is governed by the input capacitance.

Except for the absence of a high frequency zero, the signal transimpedance function of the buffer-shaper circuit bears analogy with the transimpedance function of CSA-shaper detectors, as given in (5.7) and illustrated in Fig. 5.8.

In this analogy, reset resistor R_R corresponds to feedback resistor R_{fb} , parasitic pole $2\pi f_{par}$ corresponds to the non-dominant pole of the CSA, whereas total input capacitance C_{in} corresponds to the charge-to-voltage converting feedback capacitor C_f .

Evaluation of Total Input Capacitance

The total input capacitance C_{in} takes an important role in buffer-shaper circuits, since it defines the conversion factor of the detecting circuit. Furthermore, the noise contribution of the buffer circuit strongly depends on C_{in} , as will be understood from the analysis presented in Sect. 6.2.2. The evaluation of the total input capacitance, therefore, deserves a little attention.

Only relatively low values of total input capacitance are practically useful for this circuit topology. Sensing devices with area-independent, low sensing device capacitance, such as lateral drift field photogates or buried photodiodes, are thus suited best for use with buffer-shaper detectors. For low sensing device capacitance C_{sen} , parasitic interconnect capacitance $C_{par,in}$ as well as buffer input capacitance $C_{in,sf}$ are significant components of C_{in} , as given by (6.5).

$$C_{in} = C_{sen} + C_{par,in} + C_{in,sf} . \quad (6.5)$$

The input capacitance of the source-follower buffer is expressed by (6.6) as a function of the gate-drain capacitance $C_{gd,sf}$ and the gate-source capacitance $C_{gs,sf}$ of the source-follower transistor.

$$C_{in,sf} = C_{gd,sf} + C_{gs,sf} (1 - A_{sf}) . \quad (6.6)$$

The source-follower voltage gain A_{sf} is expressed in (6.7) as a function of the source-follower transistor's transconductance $g_{m,sf}$, its bulk transconductance g_{mb} due to body effect, its drain-source resistance $r_{ds,sf}$, and the output resistance of the biasing current source $r_{o,bias}$.

$$A_{sf} = \frac{\frac{1}{g_{mb}} \parallel r_{ds,sf} \parallel r_{o,bias}}{\frac{1}{g_{mb}} \parallel r_{ds,sf} \parallel r_{o,bias} + \frac{1}{g_m}} . \quad (6.7)$$

6.2.2 Buffer Noise

Electronic noise of the source-follower buffer is a significant contribution to the noise of a buffer-shaper detector. This contribution consists of noise components of the source-follower transistor as well as the biasing current source. By designing the W/L ratio of the n-type MOS current source transistor lower than W/L of the source-follower transistor, the noise component of the source-follower transistor becomes predominant. For the sake of simplicity of the derived expressions, the noise component of the biasing current source is neglected in the following analysis.

The source-follower transistor suffers from thermal noise as well as flicker noise. Thermal noise is expected to be the predominant component. Flicker noise is therefore not considered in the presented analysis. The assumption of negligible flicker noise will, however, be verified by simulation in Sect. 6.3.4.

The output PSD of the source-follower transistor thermal noise is given by (6.8) under the assumption of a high-pass filtering capacitance significantly higher than the parasitic capacitances C_{p1} and C_{p2} .

$$S_{n,sf}^2 \approx \frac{4kT\gamma}{g_{m,sf}} \left| \frac{s/2\pi f_{hp}}{(1 + s/2\pi f_{hp})(1 + s/2\pi f_{lp})(1 + s/2\pi f_{par})} \right|^2 . \quad (6.8)$$

If the shaper's width of the passing band is significantly higher than its lower band limit f_{hp} and the parasitic pole frequency f_{par} is well beyond the upper band limit f_{lp} , a first-order low-pass spectrum can be considered as a slightly overestimating approximation of the buffer noise PSD. This approximation results in the simple expression of (6.9) for the buffer ENC. Figure 6.2 displays the buffer noise PSD and its first order approximation.

$$q_{n,sf} \approx C_{in} \sqrt{kT\gamma \frac{2\pi f_{lp}}{g_{m,sf}}} . \quad (6.9)$$

A noise advantage of buffer-shaper circuits over CSA-shaper circuits is found when comparing OTA noise, as given in (5.11), to buffer noise, as given in (6.9):

First of all, a buffer-shaper's ENC is systematically lower than a CSA-shaper's ENC at equal values of sensing device capacitance C_{sen} and equal dimensions and current consumption of the input device, i.e. equal OTA transcon-

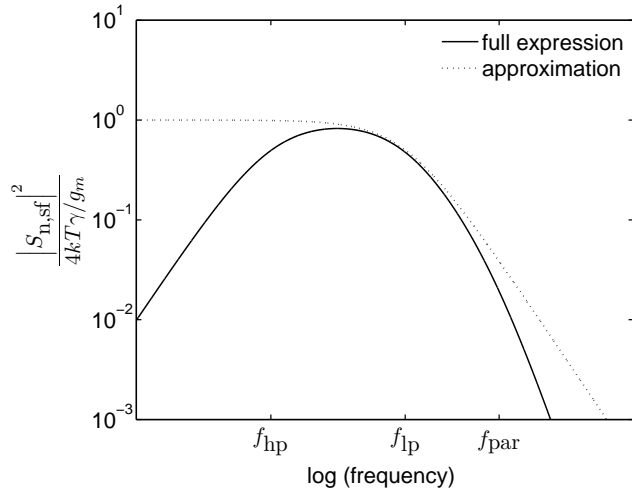


FIGURE 6.2 Source-follower noise PSD for a buffer-shaper circuit (solid line) and first order approximation (dotted line)

ductance g_m and buffer transconductance $g_{m,sf}$. This is due to the difference in relevant capacitance for conversion of the input MOS transistor's equivalent gate noise voltage to equivalent noise charge. In other words, C_{in} is obviously always lower than $C_{in} + C_f$. The advantage in terms of noise of a buffer-shaper over a CSA-shaper circuit becomes significant for low C_{in} , e.g. once C_{in} becomes comparable to C_f .

Furthermore, the source-follower input capacitance $C_{in,sf}$, as given by (6.6), is systematically lower than the input capacitance $C_{in,OTA}$ of a common-source transistor, as used in an OTA of a CSA-shaper circuit, at equal dimensions. This difference is due to the fact that an input transistor's gate node capacitance in a folded cascode OTA is equal to the sum of $C_{gs} + C_{gd}$, whereas the gate-source capacitance of a source-follower contributes to the gate node capacitance only to a small extent. Mathematically speaking $1 - A_{sf}$ is always smaller than unity, for positive values of A_{sf} smaller than or equal to one. For a given transistor bias current and transistor dimensions, i.e. at equal transconductance, the described difference between $C_{in,sf}$ and $C_{in,OTA}$ results in a further noise advantage of a buffer-shaper over a CSA-shaper. The noise advantage becomes important as soon as the input capacitance of the charge-pulse detecting circuit, i.e. the source-follower input capacitance or the CSA input capacitance, contributes a significant share of of the total input capacitance. This is generally the case, if C_{sen} is low.

A final argument worth mentioning is the fact, that the amplifiers used in CSAs are often single-branch folded cascode OTAs, such as illustrated in

Fig. 5.2. In this case the total supply current is split between the common-source input MOS transistor and the cascoded current source load branch, i.e. the bias current of the common-source transistor is only a fraction of the supply current. The transconductance $g_{m,OTA}$ of a folded cascode OTA is, therefore, lower than the transconductance of a source-follower at equal supply current budget and equivalent dimensions of the compared source-follower transistor and the OTA input transistor. As a result of this difference of transconductance a further noise advantage of buffer-shaper circuits over CSA-shapers is observed.

6.2.3 Reset Resistor Noise

The noise of the reset resistor in a buffer-shaper circuit is significantly attenuated by the shaper circuit, very similarly to feedback resistor noise in CSA-shaper circuits. The reset resistor's thermal noise PSD at the shaper output is given by (6.10) under the assumption of unity voltage gain of the buffer as well as of the shaper circuit for frequencies in the passing band.

$$S_{n,r}^2 \approx \frac{4kT\gamma R_r \left| s/2\pi f_{hp} \right|^2}{\left| (1 + sR_r C_{in}) (1 + s/2\pi f_{hp}) (1 + s/2\pi f_{lp}) (1 + s/2\pi f_{par}) \right|^2} \quad (6.10)$$

A simple first order approximation of the reset resistor noise PSD provides good estimates of the ENC if $1/R_r C_{in}$ is much lower than f_{hp} and f_{lp} . Under these conditions the ENC component due to the recharge device is given by the simple expression of (6.11). Note that the simplifying assumption of unity gain of the buffer and the shaper circuit does not influence the result found for the ENC. The reset resistor noise PSD as well as its simple approximation used for determination of the ENC are plotted in Fig. 6.3.

$$q_{n,r} \approx \sqrt{\frac{kT\gamma}{2\pi R_r f_{hp}}} \quad (6.11)$$

Comparison of (5.10) and (6.11) shows that reset resistor noise of buffer-shaper circuits is equivalent to feedback resistor noise of CSA-shaper circuits.

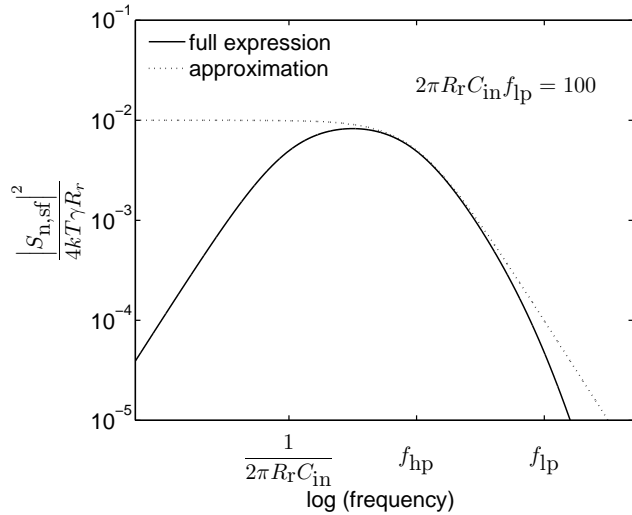


FIGURE 6.3 Reset resistor noise PSD for a buffer-shaper circuit (solid line) and first order approximation thereof (dotted line)

The noise contributions are identical for equal values of reset resistor and feedback resistor. In practical designs, implementation of high reset resistance values in buffer-shaper circuits is often more convenient than the achievement of high feedback resistance in CSA-shapers, as will be explained in Sect. 6.3.2. Practically, reduction of reset resistor noise is, therefore, more easily achieved with buffer-shaper charge pulse detectors.

6.2.4 Shaper Circuit Noise

Noise generated in the shaper circuit can have an important impact on the overall noise performance of the detector circuit and needs to be analyzed as carefully as noise of the source-follower buffer and the reset resistor. In the case of the suggested cascade of a passive CR high-pass filter and a loaded source-follower low-pass filter, noise is contributed by the high-pass filtering resistor and the loaded source-follower.

High-Pass Filter Resistor Noise

The thermal output noise PSD of the high-pass filter is given by (6.12).

$$S_{n,hp}^2 \approx \frac{4kT\gamma R_{hp} |1 + sC_{hp}/g_{m,sf}|^2}{\left| \left(1 + s/2\pi f_{hp}\right) \left(1 + s/2\pi f_{lp}\right) \left(1 + s/2\pi f_{par}\right) \right|^2} . \quad (6.12)$$

In order to achieve low power spectral density of the high-pass filter resistor noise at high frequency, $2\pi f_{lp}$ should be designed lower than $g_{m,sf}/C_{hp}$. This illustrates the importance of the low-pass filtering component of the shaper not only for the reduction of buffer noise, but also for limiting noise of the shaper circuit itself. If the mentioned criterion is respected, the ENC component contributed by the high-pass filter resistor corresponds to the simple approximation of (6.13).

$$q_{n,hp} \approx C_{in} \sqrt{\frac{kT\gamma}{C_{hp}}} . \quad (6.13)$$

Low-Pass Filter Noise

For the noise analysis of the source-follower that implements the low-pass filter of the shaper circuit, flicker noise is neglected. This assumption will be verified in Sect. 6.3.4 by simulation. The thermal noise of the biasing current source transistor of the source-follower is furthermore assumed to be significantly smaller than the thermal noise of the source-follower transistor due to adequate choice of W/L ratios of the involved transistors. In this case, the simple expression of (6.14) gives the ENC component of the low-pass filter.

$$q_{n,lp} \approx C_{in} \sqrt{\frac{kT\gamma}{C_{lp}}} . \quad (6.14)$$

6.2.5 Noise Optimization Procedure

In the previous sections the most important components of electronic noise in buffer-shaper detector circuits have been analyzed. The sum of these noise

power components corresponds to the total electronic noise power of the circuit. The ENC of electronic noise in buffer-shaper circuits is therefore given by (6.15).

$$q_{n,\text{buffer-shaper}} = \sqrt{q_{n,r}^2 + q_{n,\text{sf}}^2 + q_{n,\text{hp}}^2 + q_{n,\text{lp}}^2} . \quad (6.15)$$

From inserting the expressions of the discussed noise components, as given by (6.9), (6.11), (6.13), and (6.14), into (6.15) it becomes apparent that the total electronic noise performance depends on many parameters. Some of these parameters are defined by the application of the detector, whereas others can be chosen by the designer who has to find a trade-off between different noise components for minimum total electronic noise.

A first parameter implicitly defined by the chosen sensing device is the high-pass filtering frequency. As a matter of fact, the high-pass filtering frequency of the shaper is systematically chosen as high as possible in order to reduce the reset resistor noise and to increase the maximum photon count rate of the detector. The practical maximum of f_{hp} has, however, to be low enough to avoid attenuation of signal pulses. This means that the maximum useful high-pass filtering frequency is defined by the charge pulse width, i.e. the response time of the sensing device. Depending on the type of sensing device, the response time is usually defined by the collection time of absorption-generated signal charge or by the decay time of the scintillator flash.

The definition of the shaper's high-pass filtering frequency by the response time of the sensing device implicitly also influences the optimum choice of low-pass filtering frequency. On one hand (6.9) suggests to choose low f_{lp} for minimization of buffer noise. On the other hand investigation of the signal transfer function 6.1 shows that f_{lp} needs to be greater or equal than f_{hp} in order to avoid undesired signal attenuation. The low-pass filtering frequency f_{lp} is, therefore, chosen as a function of f_{hp} and the requirement of low ballistic deficit.

The value of the high-pass filtering capacitance C_{hp} should be chosen as high as possible for minimum thermal noise of the filter, as expressed by (6.13). The available area is often the practical criterion which defines the maximum value of C_{hp} . Besides poor noise performance, small high-pass filtering capacitance might require high values of R_{hp} for achieving a chosen value of f_{hp} . Furthermore, low C_{hp} would increase the impact of parasitic capacitance of the buffer output node and of the high-pass filter output node on the shaper gain.

Similar considerations apply to the choice of low-pass filtering capacitance. According to (6.14) noise optimization would suggest a value of C_{lp} as high

as possible, whereas available area and required power, i.e. required $g_{m,\text{lp}}$, to achieve the desired low-pass filtering frequency will impose a practical maximum.

For a fixed value of the high-pass filtering frequency the reset resistor noise does not share any parameters with the remaining noise components in (6.15). Therefore, it does not need to be considered for optimization of the trade-off between electronic noise components.

The remaining noise components $q_{n,\text{sf}}$, $q_{n,\text{hp}}$, and $q_{n,\text{lp}}$ mainly depend on the total input capacitance C_{in} and the source-follower's transconductance $g_{m,\text{sf}}$ once the parameters f_{hp} , f_{lp} , C_{hp} , and C_{lp} are set according to the criteria outlined above. For minimum electronic noise of a buffer-shaper detector, C_{in} should be low and $g_{m,\text{sf}}$ should be high. The transconductance $g_{m,\text{sf}}$ is high for high bias current as well as short and *wide* gate geometry of the source-follower transistor. Therefore, it is a trivial choice to use minimum transistor length. The maximum source-follower bias current is usually imposed by the available power budget. The total input capacitance C_{in} , as given by (6.5) and (6.6), depends on the source-follower transistor dimensions as well. In particular $C_{\text{gd,sf}}$ as well as $C_{\text{gs,sf}}$ and hence C_{in} are low for *narrow* source-follower transistor gate geometry. This illustrates, that the transistor gate width needs to be optimized for an ideal compromise between high $g_{m,\text{sf}}$ and low C_{in} .

The analytical optimization of source-follower gate width is greatly simplified, if the source-follower gain A_{sf} is assumed independent of the gate width. Equation (6.7) shows that this assumption holds approximately true for n-channel source-follower transistors in a single-well process. In this case $1/g_{mb}$ is significantly lower than $r_{\text{ds,sf}}$ and $r_{\text{o,bias}}$ and consequently A_{sf} purely depends on $1/g_{mb,\text{sf}}$ and $1/g_{m,\text{sf}}$ which are proportional to each other by $g_{mb,\text{sf}} = \eta g_{m,\text{sf}}$, as explained in [84].

Under this simplifying assumption, a closed analytical expression for the optimum transistor width $W_{\text{sf,opt}}$ can be found, as derived in appendix A.2 and given by (6.16):

$$W_{\text{sf,opt}} \approx \left(-\frac{n_{\text{w}}}{4V_{\text{cst}}^2} + \frac{n_{\text{w}}^{1/3} C_{\text{cst}}^{1/3}}{2^{2/3} V_{\text{cst}}^{2/3} C_{\text{w}}^{1/3}} + \frac{n_{\text{w}}^{5/3} C_{\text{w}}^{1/3}}{2^{10/3} V_{\text{cst}}^{10/3} C_{\text{cst}}^{1/3}} \right)^2 , \quad (6.16)$$

where

$$n_w = \frac{kT\gamma_{sf}2\pi f_{lp}\sqrt{L_{\min}}}{\sqrt{2\mu C_{ox}I_{sf}}} , \quad (6.17)$$

$$V_{cst} = \sqrt{kT \left(\frac{\gamma_{hp}}{C_{hp}} + \frac{\gamma_{lp}}{C_{lp}} \right)} , \quad (6.18)$$

$$C_{cst} = C_{sen} + C_{par,in} , \quad (6.19)$$

and

$$C_w = c_{gdw} + (1 - A_{sf}) \left(c_{gsw} + \frac{2}{3}C_{ox}L_{\min} \right) . \quad (6.20)$$

In the above expressions, L_{\min} , μ , C_{ox} , I_{sf} , c_{gdw} , and c_{gsw} are the gate length, the carrier mobility in the channel, the gate oxide unit area capacitance, the bias current, the gate-drain overlap capacitance per unit length and the gate-source overlap capacitance per unit length of the source-follower transistor respectively.

From the above explanations it has become apparent that the summed noise contributions of the buffer and the shaper circuit can be optimized independently of the reset resistor noise. The reset resistor noise is, in a first approximation, a pure function of the high-pass filtering frequency and the reset resistance value. Accordingly, the recharge resistor noise may range from negligible to predominant values in comparison to the buffer and shaper circuit noise components. Generally speaking, a narrow pulse width to be detected, i.e. a large high-pass filtering frequency, and successful implementation of high reset resistance will result in low reset resistor noise.

This consideration can be extended to the extreme case of infinite reset resistance. In practice, this case is reached by operating the buffer-shaper circuit in a mode of asynchronous detection with synchronous, i.e. clocked, reset. In such an operating mode, the reset resistor is transformed into a reset switch that is selectively enabled for short reset periods during which the input capacitance is connected to the reset potential in order to remove accumulated signal charge. During the exposure periods between two reset periods the voltage on the input capacitance decreases by a small step upon each charge

pulse arrival. The shaper does, however, remove the near-DC voltage decrease of the resulting staircase voltage waveform and the filtered pulses appear at the shaper's output very similarly to the case of finite recharge resistance. In contrast to the case of finite recharge resistance, the noise of the reset switch is a frozen DC component rather than having a spectrum of a certain bandwidth. The DC reset noise is, therefore, completely suppressed by the continuous-time high-pass filtering provided by the shaper circuit.

The consequence of a clocked reset is a dead time during and possibly shortly after each reset period. During this dead time, the shaper output is compromised by a relatively large pulse of inverse polarity corresponding to the removal of a possibly large accumulated charge amount from the input capacitance. The duration of the dead time can be reduced by establishing a short-circuit across the high-pass filtering resistor of the shaper circuit during the period of clocked reset. This operation detail will virtually eliminate the reset pulse of inverse polarity from the shaper circuit's output and reduce the dead time to the duration of the reset period.

6.3 Design Implementation

In order to prove the excellent noise performance of detectors with buffer-shaper circuits, a test structure has been fabricated and characterized. The test structure design is targeted at energy-sensitive X-ray photon counting using a scintillator layer and a sensing device for visible light. A lateral drift field photogate is used for the reason of its low and area-independent sense node capacitance as well as its good response time even for large area. A pixel dimension of $30 \mu\text{m} \times 22 \mu\text{m}$ has been chosen, but pixel edges up to one order of magnitude higher can be implemented. The buffer-shaper circuit is designed to process pulses of up to $1 \mu\text{s}$ width. Consequently, a scintillator decay time up to $1 \mu\text{s}$ is acceptable, which enables usage of quite a wide range of materials.

The test structure consists of a sensing device and a buffer-shaper charge pulse detecting circuit. Since the evaluation of the test structure relies on characterization of the charge pulse detecting circuit's output, no voltage pulse processing circuit has been implemented. Instead, a low-noise driver circuit drives the output signal on a pad of the chip.

A $0.18 \mu\text{m}$ process technology from UMC has been employed for the reason of simultaneous manufacturing of test structures making use of the buried photodiode process option. This process technology is, however, not ideal for the implementation of lateral drift field photogates.

6.3.1 Implementation of the Photogate Sensing Device

Drift field photogates rely on application of a potential difference across the top electrode. In continuous polysilicon electrodes a DC bias current is therefore unavoidable. The resulting power consumption for a two dimensional array of a high pixel number is, for most applications, not acceptable, even for low doping, i.e. high resistivity, of the polysilicon. An elegant solution not consuming any power is found in replacing the continuous electrode by a number of isolated adjacent polysilicon strips with linearly increasing bias voltages. In order to avoid spikes of electron potential energy in the semiconductor underneath the gaps between these stripes, either overlapping polysilicon electrodes or narrow electrode gaps in conjunction with sufficient potential difference between adjacent gaps are required. Since neither sufficiently low electrode spacing nor overlapping electrodes are available using the chosen process technology, a continuous polysilicon drift field photogate is used for the implementation of the test structure despite the disadvantage outlined above. The lowest possible polysilicon doping is chosen for highest gate resistance. For the same reason, as well as for good optical transparency, the self-aligned silicide process step is inhibited for the photogate region.

The p-n junction of the sense node is drawn significantly narrower than the width of the photogate for reduced sensing device capacitance seen by the buffer-shaper circuit. A tapered gate shape, as shown in Fig. 6.6, provides external drift transport of photo-electric charge along the entire travel distance, as opposed to rectangular shapes, where charge carriers that have arrived at the edge of high bias voltage are not subject to an electrical field driving them towards the sense node. In this case, having to rely on electron transport by self-induced drift and diffusion would result in significantly increased charge collection time.

The photogate implemented in the test structure is a surface channel device, i.e. the vertical minimum of electron potential energy is found at the semiconductor-oxide interface. This type of sensing device is known to suffer from reduced charge transfer speed and additional noise due to trapping and releasing of signal charge in trap states of the interface defects. Buried channel photogate device have been shown to overcome these problems, since mobile photo-electrons are vertically confined to a potential energy minimum in the semiconductor bulk at some distance below the oxide-semiconductor interface [85]. The shift of the electron potential energy minimum away from the interface is achieved by an additional shallow n-type implant close to the oxide-semiconductor interface, which is not available in the chosen process technology.

6.3.2 Implementation of the Reset Resistor

The chosen maximum signal pulse width of 1 μ s corresponds to the lowest possible time constant of the passive C-R filter, i.e. it defines the high-pass filtering frequency f_{HP} . For the resulting, rather low, value of high-pass filtering frequency a very high reset resistance is required in order to achieve low reset resistor noise according to (6.11).

The p-channel transistor implementation of the reset resistor, as shown in Fig. 6.1, is able to achieve very high small signal resistance if the transistor is operated in its weak inversion region. The drain current I_D of a transistor in weak inversion operation is given by (6.21) [86].

$$I_D = \frac{W}{L} I_{D0} e^{V_G/nU_T} \left(e^{-V_S/U_T} - e^{-V_D/U_T} \right) \quad (6.21)$$

In the above expression V_G , V_S , V_D , I_{D0} , and n are the bulk-gate voltage, bulk-source voltage, bulk-drain voltage, characteristic current, and slope factor of the p-channel transistor respectively while U_T is equal to kT/q . The small signal reset resistance is given by the derivative of the drain current, as given by (6.22):

$$R_R = \left| \frac{1}{\frac{d(I_D(V_S=0))}{dV_D} \Big|_{V_D=0}} \right| = \frac{1}{U_T} \frac{W}{L} I_{D0} e^{V_G/nU_T} \quad (6.22)$$

This expression of the reset resistance holds approximately true for signal amplitudes up to U_T . Beyond that voltage the reset resistance increases strongly with signal amplitude. The maximum slew current of the reset resistor is $W/L I_{D0} e^{V_G/nU_T}$, as can be found from (6.21).

The strong dependence of the reset resistance on the gate-bulk voltage, i.e. gate-source voltage, and on the temperature explain the need for precise and temperature dependent biasing. Precise gate-source voltage biasing is generally easily possible in the configuration of the buffer-shaper circuit, since the source voltage is a fixed supply or reference potential independent of any other transistor parameters of the circuit.

For the test structure implementation the gate-source bias voltage defining the reset resistance is set off-chip. This solution offers very high resistance tuning range but poor temperature stability. This drawback is, however, acceptable for the evaluation of a test structure.

For application in highly segmented detectors with a large number of pixels the following two strategies for biasing of the reset resistance could be applied in the future:

Digital trimming: As illustrated by the example shown in Fig. 6.4, each detector pixel or each cluster of pixels contains a trimming register and a digital to analog converter (DAC).

During a calibration period, a stimulation hardware for the charge pulse detecting circuit, such as a test capacitor driven by a voltage pulse, stimulates the charge pulse detecting circuit. The high-pass filtering frequency of the shaper is tuned to a very high or infinity value. The output of the voltage pulse detecting circuit is then used for direct or indirect measurement of the time constant $R_r C_{in}$.

Alternatively the saturation current of the reset transistor could be measured directly by application of a low potential to the input node of the buffer. However, this would prove difficult and slow in practice, as very small currents need to be measured.

The most important advantages of a digital trimming approach are the absence of pixel-external reference currents or voltages as well as the wide tuning range. Disadvantages include the high amount of hardware needed per pixel, the rather complex time constant measurement for calibration, and the need for recalibration in case of temperature changes.

Analog tracking bias: A tracking bias circuit provides a gate-source bias voltage which automatically compensates for variations of temperature and transistor parameters of the reset resistor. For the example shown in Fig. 6.4, a diode connected transistor biased with a reference current provides the gate-source bias voltage. The bulk-drain voltage of the diode connected reference transistor will be positive and significantly higher than U_T . In this case it appears from 6.21 and 6.22 that R_r is equal to I_{ref}/U_T . The dependence on parameters subject to process fluctuations and intra-chip variations, such as I_{D0} , is eliminated by local matching of the reference transistor and the reset transistor.

Furthermore, a first-order temperature dependence compensation of the reset resistance is achieved, if the reference current I_{ref} is proportional to absolute temperature (PTAT). Generation of PTAT currents is possible in semiconductor circuits at reasonable effort [84].

In order to avoid distribution of one bias current per pixel of the image sensor, a current mirror with a voltage storage capacitor can be used in order to store the bias current in every pixel circuit. The reference current is sampled and stored periodically in order to avoid drifts caused

by leakage of charge from the storage capacitor and to track temperature changes.

The advantage of a tracking bias solution is the absence of any need for pixel-wise calibration as well as the modest circuit complexity required per pixel. The main disadvantage of analog tracking biasing is the susceptibility to leakage and charge-injection from sampling switches due to weak inversion operation of the biasing circuit and handling of small currents.

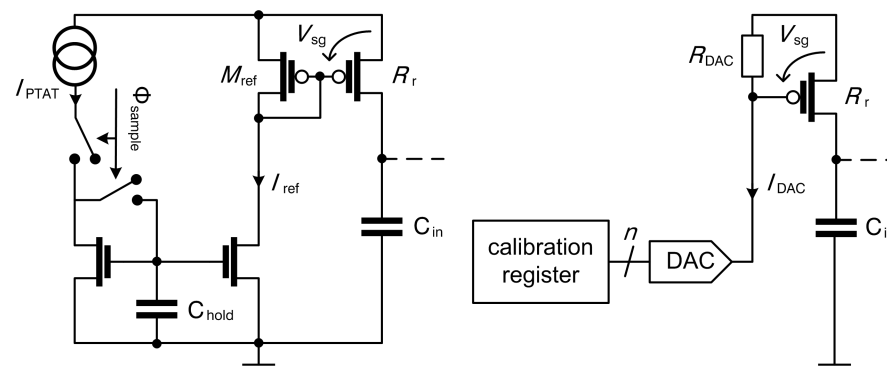


FIGURE 6.4 Options for future pixel-wise biasing of the reset resistance: Analog tracking bias (left) and digital trimming (right)

6.3.3 Implementation of the Buffer and Shaper Circuits

The buffer-shaper circuit has been implemented according to the basic schematic, as shown in Fig. 6.1. N-type MOS transistors are used for implementation of the current sources of the buffer and the low-pass filter. The design uses the 3.3 V supply option of the process for increased swing. As mentioned previously, the maximum signal pulse width has been set to 1 μ s. This choice defines the frequency characteristics of the buffer-shaper circuit, as summarized in Table 6.1, according to the previously explained design criteria.

The circuit has been designed following the noise optimization procedure described in Sect. 6.2.5. A total supply current budget of 2 μ A is allocated to the buffer-shaper circuit. Based on several iterations of the optimization procedure this budget has been split into equal bias currents of 1 μ A for the buffer and the active low-pass filter. At the selected low-pass filtering frequency this allows driving a low-pass filtering capacitance C_{lp} of 1 pF. This capacitor has not been integrated in the compact layout of the test structure, but is composed by a parasitic wiring capacitance and the input capacitance of the pad

TABLE 6.1 Frequency domain parameters of the buffer-shaper circuit

Frequency	Value
$1/2\pi R_{\Gamma} C_{\text{in}}$	37 KHz
f_{hp}	160 KHz
f_{lp}	1.6 MHz

driver. In a pixel design for final application, this load capacitance will mainly consist of the input capacitance of the voltage pulse processing circuit. The high-pass filtering capacitance will be implemented as a polysilicon-polysilicon capacitor. Its value is set to 200fF by consideration of an area criterion.

With these chosen design parameters and the process parameters, as given in Table 6.2, the noise minimization according to (6.16)-(6.20) is performed. In order to achieve limited impact of pixel-to-pixel transistor mismatch, the gate length of the buffer's source-follower transistor is chosen to be 1 μm instead of the minimum gate length of 0.34 μm for transistors in the 3.3V supply option of the process technology. The values of C_{par} and C_{sen} include junction capacitances of the photogate sense node as well as the drain diffusion of the reset transistor, overlap capacitance from the polysilicon to the sense node of the photogate as well as gate-drain overlap capacitance of the reset transistor, and a parasitic capacitance of the sense node wiring. The optimum gate width of 0.24 μm is about equal to the minimum transistor width of the process. It is, however, desirable to design a slightly wider gate in order to avoid excessive pixel-to-pixel mismatch. The analytical calculation of the buffer-shaper circuit noise without reset resistor noise, as shown in Fig. 6.5, illustrates that the noise minimum is relatively flat within a certain range of gate width. A slightly increased gate width of 0.5 μm is, therefore, chosen without a significant disadvantage in terms of noise.

For the chosen source-follower transistor dimensions the calculated value of the total input capacitance C_{in} is 4.3 fF. Based on this value, the noise contributions of the circuit components are calculated according to (6.9), (6.13), (6.14), and (6.11) under the assumption of a reset resistance of 1 G Ω . These noise contributions, as summarized in Table 6.3, result in an overall ENC of 13.5 electrons, which is about a factor of two below the value of kTC_{in} thanks to the use of shaping and the excellent noise performance of buffer-shaper circuits employed with low sensing device capacitance.

Note that due to the relatively low high-pass filtering frequency, which is required to detect pulses of a microsecond, the reset resistor noise is the predominant noise contribution despite the high reset resistance value. If the MOS transistor used for implementation of the reset resistance is operated as a synchronous reset switch, the reset resistor noise is eliminated and an overall

TABLE 6.2 Parameters for noise optimization of the buffer-shaper circuit

Parameter	Value	Resulting Parameter	Value
γ_{sf}	2/3	n_{w}	$2.6\text{e-}12 \text{ V}^2\sqrt{\text{m}}$
γ_{hp}	1	V_{cst}	153 μV
γ_{lp}	2/3	C_{cst}	3.9 fF
L_{min}	1 μm	c_{w}	0.7 fF/ μm
μ	116 cm^2/Vs	$W_{\text{buf,opt}}$	0.24 μm
C_{ox}	5 fF/ μm^2		
I_{buf}	1 μA		
C_{hp}	200 fF		
C_{lp}	1 pF		
C_{sen}	1.0 fF		
$C_{\text{par,in}}$	2.9 fF		
c_{gdw}	0.14 fF/ μm		
c_{gsw}	0.14 fF/ μm		
A_{sf}	0.81		

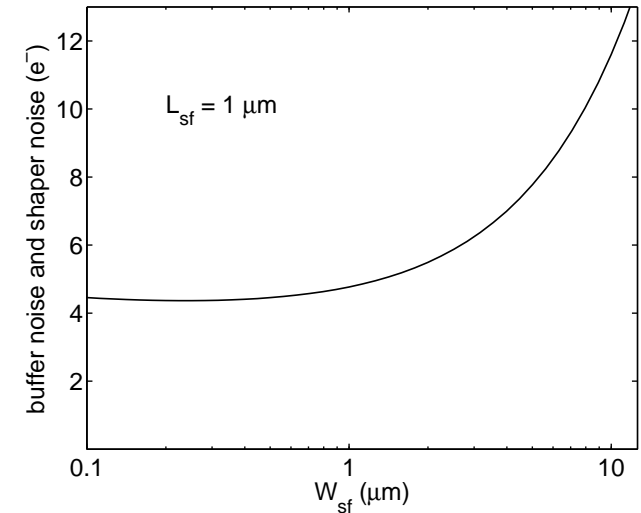


FIGURE 6.5 Calculated thermal noise of the shaper circuit and the buffer circuit (not including reset resistor noise) as a function of the source-follower transistor width

noise performance of 4.6 electrons is calculated. In this case, the optimization of the buffer's source-follower transistor width is, obviously, even more crucial than in the case of asynchronous reset.

TABLE 6.3 Calculated thermal noise components of the buffer-shaper circuit

Circuit Component	ENC contribution
buffer	1.6 e ⁻
high-pass filter resistor	3.9 e ⁻
active low-pass filter	1.4 e ⁻
reset resistor	12.7 e ⁻
total electronic noise	13.5 e⁻

The buffer-shaper circuit has been implemented in a compact layout covering an area of 30 μm x 22 μm . The test structure, as shown in Fig. 6.6, contains a drift-field photogate of 20 μm edge length.

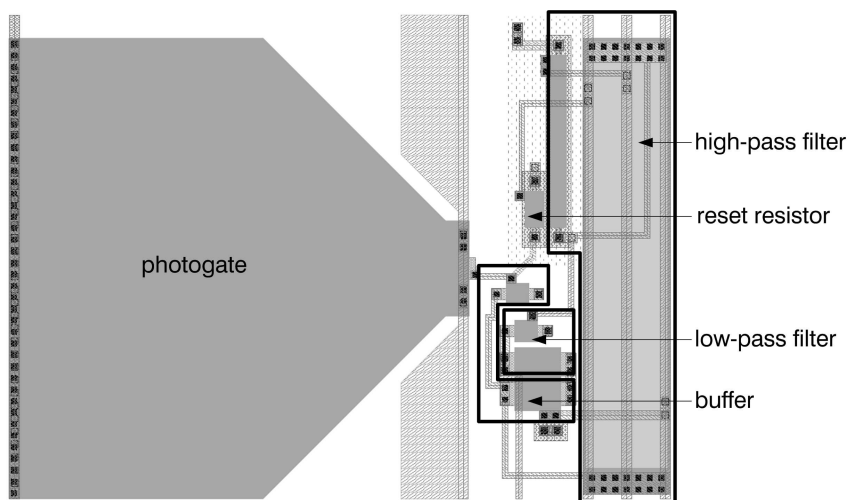


FIGURE 6.6 Layout of the test structure including a lateral drift field photogate and a buffer-shaper circuit

6.3.4 Simulation Results

Circuit simulations of the implemented buffer-shaper circuits have been performed in order to validate the design procedure and for performance verification prior to fabrication. The simulation results presented in the following sub-sections are restricted to typical conditions at room temperature for the sake of readability. The simulations are performed with a schematic based on extraction of parasitic capacitances from the layout. This is particularly important, since the parasitic capacitances of the input node, the buffer output node and the intermediate node of the shaper have a significant impact on performance parameters such as the conversion factor, the parasitic pole frequency, and the gain loss due to capacitive division between the high-pass filtering capacitance and the intermediate node capacitance.

AC Simulation

Linearized small signal alternative current (AC) simulations have been used in order to verify the frequency domain parameters of the design. Comparison of Table 6.1 and Fig. 6.7 shows good agreement of design targets and simulation. AC simulation based on parasitic extraction results additionally allows determination of the conversion factor for which a value of 29.5 $\mu\text{V}/\text{e}^-$ is found.

Transient Simulation

Theoretically speaking, most parameters provided by a transient simulation can as well be obtained from AC simulations. A transient simulation has all the same been performed for the reason of the intuitive simultaneous visualization of time constants, delays, overshoots, and DC operating points. Figure 6.8 shows the time-domain response to a square pulse of 0.5 μs width containing 100 photo-electrons. The conversion factor for this case is found to be 25 $\mu\text{V}/\text{e}^-$. This value is slightly below the value found from AC simulation due to the proximity of the pulse width and the high-pass filtering time constant. It is worth pointing out the overshoot in the shaped waveform which is explained by the absence of pole-zero cancellation.

Noise Simulation

Analytical calculation of circuit noise is an excellent method for understanding design trade-offs and for finding a hand-calculated starting point for optimization. Linearized small signal noise simulation is, however, expected to deliver more precise results, for several reasons. First of all, complex spectral shapes of noise are considered instead of approximations, such as the ones illustrated in Figs. 6.2 and 6.3. Additionally, depending on the quality of the available noise

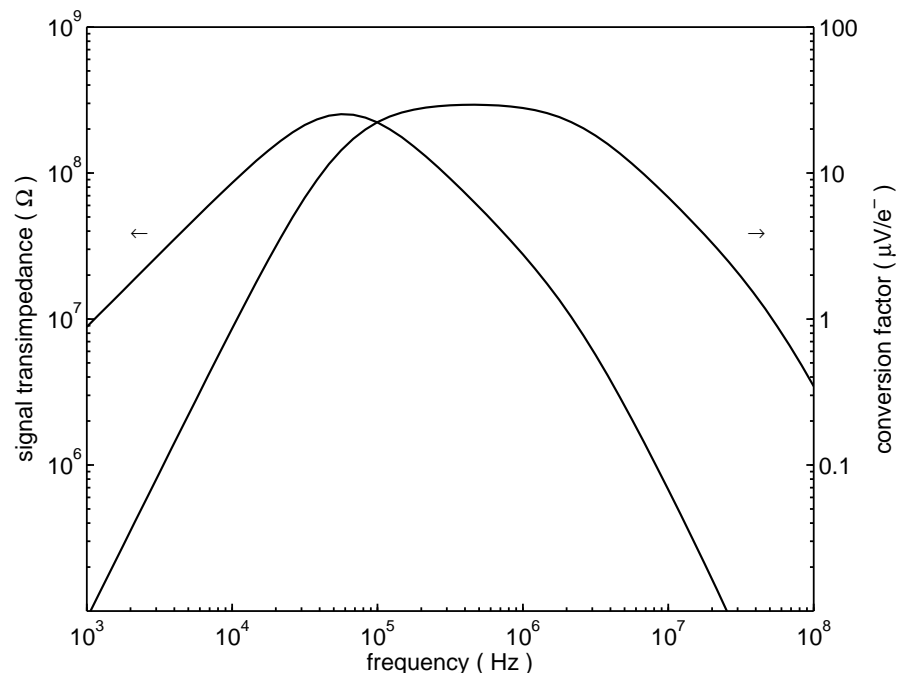


FIGURE 6.7 Results of an AC simulation based on parasitic extraction. Signal Transfer function (left scale) and conversion factor (right scale)

models, a more precise value of the thermal noise excess factor γ is obtained as a function of the transistor dimensions and operating conditions. Last but not least, flicker noise of transistors, which had been neglected in the analysis so far, is also considered in noise simulations. The noise power spectral density of the circuit is shown in Fig. 6.9.

The predominant component in the low-frequency portion of the noise PSD is flicker noise of the active low-pass filter which, as opposed to flicker noise of the buffer, is not filtered by the high-pass filter. The peak of the noise PSD below the high-pass filtering frequency of 160 kHz is contributed by the shaped reset resistor noise. A detailed breakdown of the relevant ENC components is given in Table 6.4.

Comparison of the simulated results to the simplified analytical results, as summarized in Table 6.3, shows good agreement of the thermal noise components of the source-follower transistor of the buffer, the source-follower of the low-pass filter, and the high-pass filter resistor. This is due to a partial compensation of overestimated spectral shapes and underestimated thermal noise excess factors in the analytical calculations.

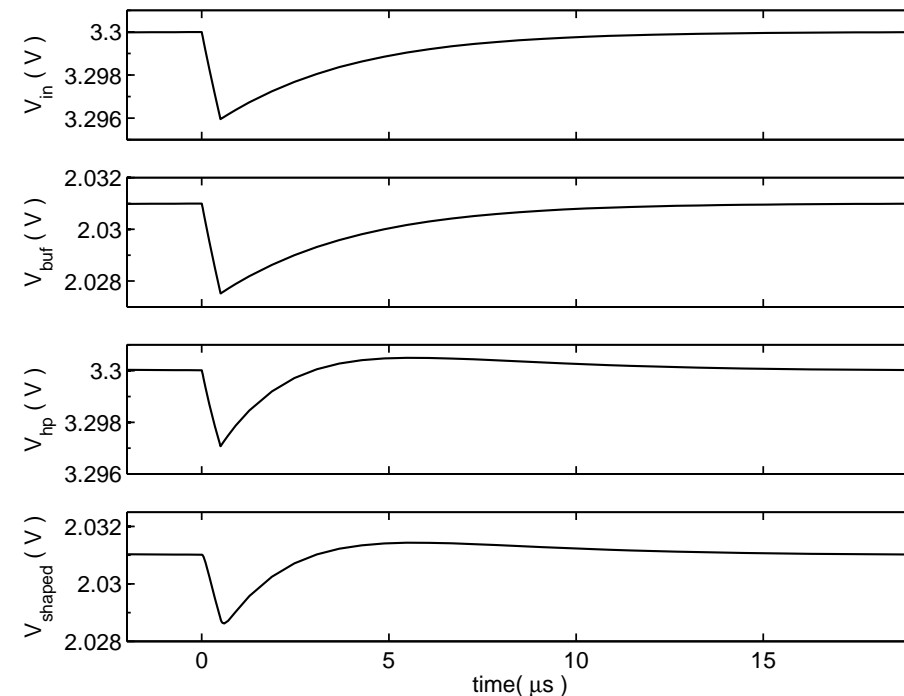


FIGURE 6.8 Time-domain response to a pulse of 100 electrons and a width of $0.5 \mu\text{s}$. Input Voltage, output of the buffer, intermediate node of the shaper, and buffer-shaper output voltage (from top to bottom)

Consideration of the bias current source transistors of the buffer and the active low-pass filter reveals some remaining room for noise optimization. These noise components could be further reduced at the cost of reduced swing by reducing the W/L of the concerned transistors. Given the relatively low noise at the present dimensions, the improvement of the overall noise performance would, however, be very small.

Comparison of thermal noise and flicker noise components indicates that the assumption of thermal noise dominating over flicker noise is at the limit of validity for the presented design of rather low bandwidth. Implementations with higher high-pass and low-pass filtering frequencies, that are optimized for faster sensing device response time and higher count rate, will satisfy the assumption of predominant thermal noise.

The most important noise contribution, i.e. thermal noise of the reset resistance is slightly higher in simulation than analytically calculated. This indicates that the thermal noise excess factor used in the simulator model is

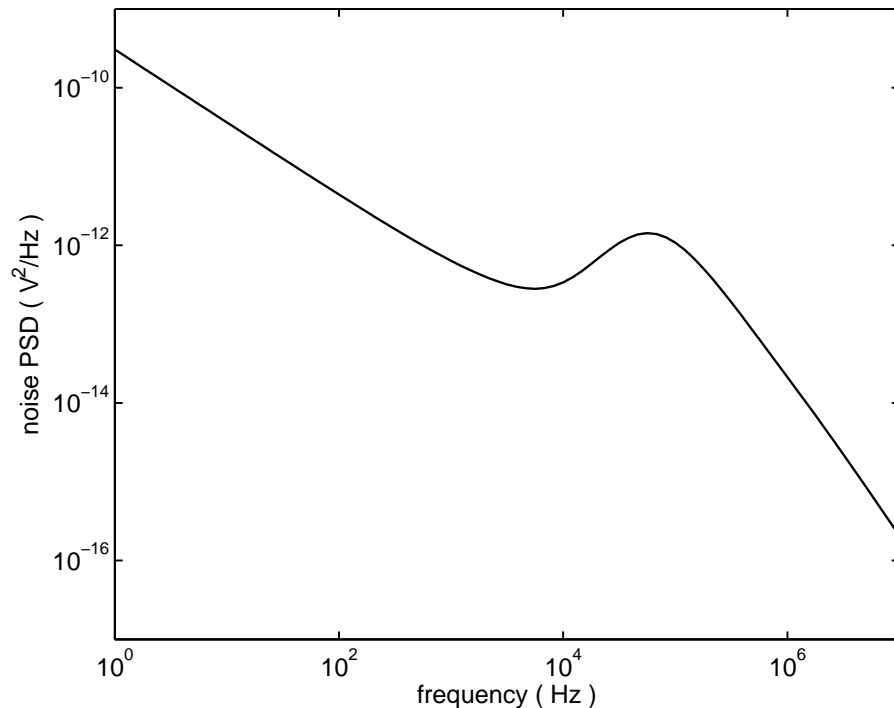


FIGURE 6.9 Simulated noise power spectral density of the implemented buffer-shaper circuit

greater than the assumed value of 1 for the implemented reset transistor in weak inversion operation at zero drain-source voltage.

From the comparison of calculated and simulated noise components it can be concluded that the analytical model and optimization results are in reasonable agreement with simulation results. They can therefore provide a good analytical starting point for simulator-based fine tuning. For high-count-rate designs with short sensing device response time even better agreement of analysis and simulation is expected.

Reset Resistor DC Simulation

The reset resistor is a key element for low overall noise of the buffer-shaper circuit. A reset resistance value of $1 \text{ G}\Omega$, as assumed in Sect. 6.3.3, is required in order to achieve the calculated and simulated noise performance. A pseudo-DC transient simulation is used in order to obtain the small signal reset resistance

TABLE 6.4 Simulated noise components of the buffer-shaper circuit

Circuit Component	ENC contribution
buffer (source-follower, thermal)	1.7 e^-
buffer (source-follower, flicker)	1.8 e^-
buffer (biasing, thermal)	1.7 e^-
high-pass filter resistor	4.0 e^-
active low-pass filter (source-follower, thermal)	1.5 e^-
active low-pass filter (source-follower, flicker)	2.8 e^-
active low-pass filter (biasing, thermal)	1.5 e^-
reset resistor	16.7 e^-
total electronic noise	17.9 e^-

as a function of the source-gate bias voltage. The reset resistance is shown for three different temperatures in Fig. 6.10.

Below a source-gate bias voltage of about 500 mV, the exponential voltage dependence of weak inversion operation is observed. Beyond 600 mV the bias voltage dependence as well as the temperature dependence decrease, as the transistor enters the region of strong inversion.

Based on these simulation results a nominal gate bias voltage of 435 mV is chosen in order to obtain a small signal resistance of $1 \text{ G}\Omega$. This operating point is clearly in the weakly inverted region, where a strong temperature dependence is observed. For instance the small signal resistance variation between operating temperatures of 0°C and 50°C can be as high as one order of magnitude, which would give rise to unacceptable variations in noise, maximum count rate, or ballistic deficit. A sophisticated biasing method, such as analog tracking bias or digital trimming with recalibration in case of temperature changes is therefore required for implementation of reliable multi-pixel X-ray photon detectors.

At the chosen gate bias voltage, the saturation current of the transistor, i.e. the maximum recharge slew current, is 18 pA. This slew limit is found for a drain-source voltage higher than 20 mV, i.e. for charge pulses above 500 electrons.

6.3.5 Measurement Results

The test structure has been characterized without a scintillator layer applied to the chip. Instead, pulses of green light created by a light-emitting diode (LED) have been used for stimulation. Examination of the output waveform, as illustrated in Fig. 6.11, shows correct operation of the circuit.

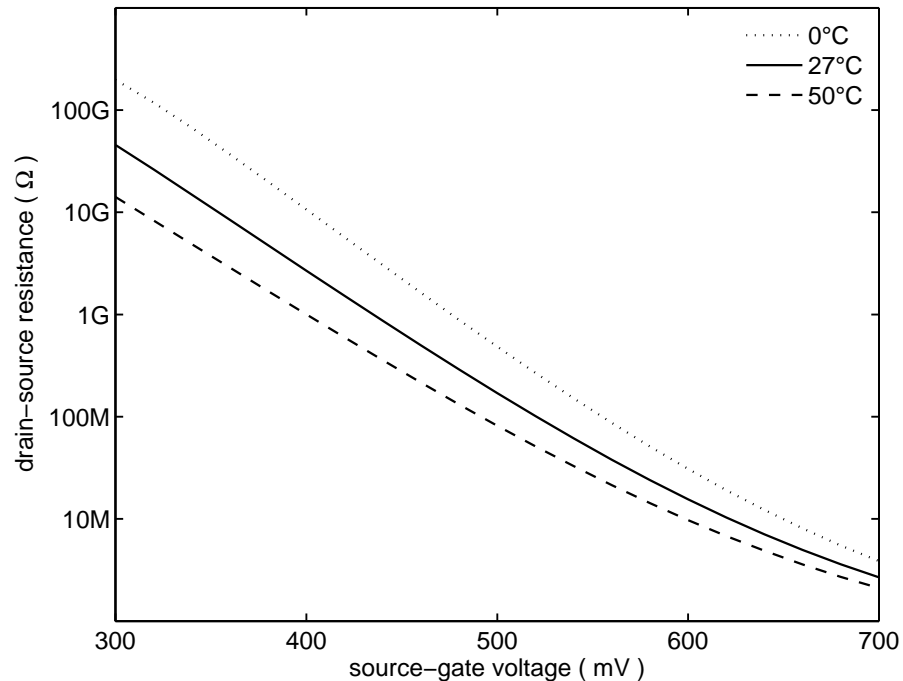


FIGURE 6.10 Simulated reset resistance as a function of the source-gate voltage of the reset transistor

For the chosen example waveform, the width of the optical pulses was $0.5 \mu\text{s}$. Since the falling edge duration of the signal is limited by this pulse width, the waveform neither provides any quantitative information concerning the charge collection time of the photogate nor concerning the low-pass filtering frequency of the shaper. The time constant of the waveform's rising edge does, however, allow determining of the shaper's high-pass filtering frequency. The tunable high-pass filtering resistance of the test structure allowed setting the rising edge time constant to a value of $1 \mu\text{s}$ which corresponds to the nominal design value of 160 kHz of the high-pass filtering frequency.

Note that the biasing of the reset resistance has been manually tuned for this measurement as a function of the temperature and statistical variation of the sample. It is, however, hard to determine an absolute value of the reset resistance. From the absence of signal overshoot it can be concluded that the resistance value is likely to be higher than the designed and simulated value of $1 \text{ G}\Omega$. The reset resistance of the chosen setting is able to reset the sense node at repetition rates up to more than 5000 pulses/sec with approximately

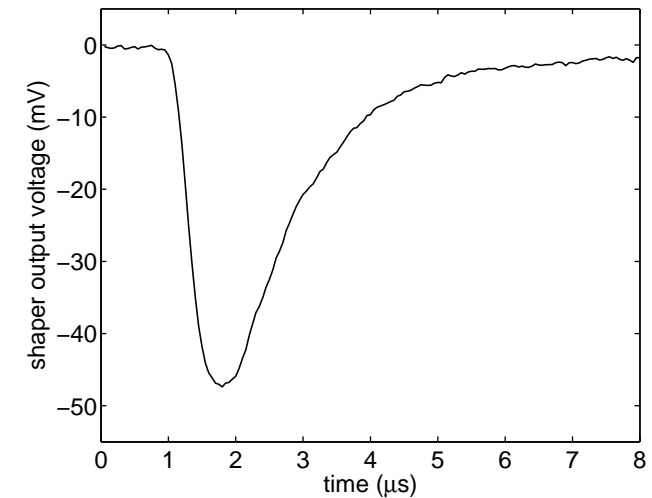


FIGURE 6.11 Measured response of the buffer-shaper circuit to an optical pulse of about 1600 electrons and $0.5 \mu\text{s}$ width at a high-pass filtering frequency of 160 kHz

$1600 \text{ electrons/pulse}$. A selection of measurement conditions and results, such as the measured resistance of the photogate's polysilicon electrode, are given in Table 6.5.

Tuning of the high-pass filtering frequency furthermore allows tuning of the reset resistor noise suppression by the shaper according to (6.11). Maximum detectable pulse width can, therefore, be traded for improved noise performance. Figure 6.12 illustrates the relation between high-pass filtering frequency and measured noise performance. The measured RMS noise voltage has been converted to an input referred charge by use of the conversion factor found from simulation of the extracted netlist.

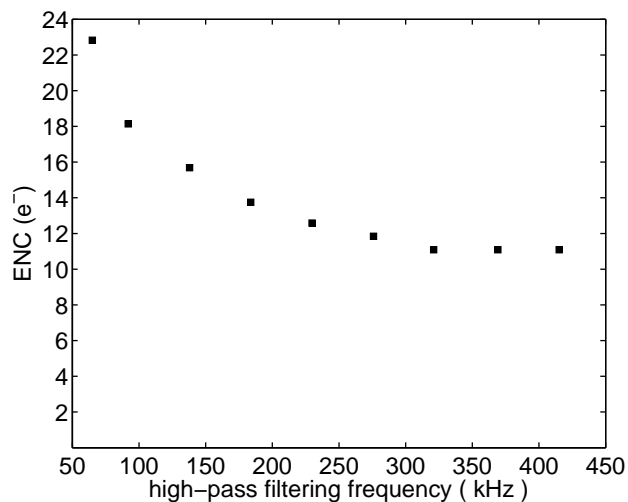
The input referred noise charge of about 14 electrons found at the nominal high-pass filtering frequency of 160 kHz is in good agreement with the results of the simulation and analysis presented previously. The slightly reduced noise with respect to simulation can be explained by the reset resistance being above the nominal value. If the maximum pulse width is restricted to $0.5 \mu\text{s}$, i.e. half the nominal value, an input referred noise charge as low as 12 electrons is even achieved.

6.3.6 Interpretation of the Results and Applications

The theoretically calculated and experimentally achieved noise performance and power consumption per pixel is an important step towards highly segmented X-ray detectors with very high energy resolution. To date, line detec-

TABLE 6.5 measurement of buffer-shaper circuit with photogate sensing device and optical stimulation

Parameter	Value
light source wavelength	555 nm
buffer-shaper supply voltage	3.3 V
buffer-shaper supply current (nominal)	2 μ A
sense node recharge voltage	3.3 V
source-gate bias of reset resistor MOS device	350 mV
high photogate bias voltage (external)	2 V
low photogate bias voltage (external)	3 V
photogate bias current	177 μ A
pad protection resistor per 2 (parallel) photogates	50 Ω
high photogate bias voltage (internal)	2.98 V
low photogate bias voltage (internal)	2.02 V
photogate polysilicon gate resistance	5.41 k Ω

**FIGURE 6.12** Measured input referred noise charge of the buffer-shaper circuit as a function of the high-pass filtering frequency

tors with several tens to a few hundred pixels and several comparators with adjustable thresholds are available on the market. Such detectors using efficient direct conversion sensing devices, e.g. made from Cadmium Telluride, achieve an energy resolution of a few tens of keV at detection efficiencies as high as 80% [87]. This corresponds to an equivalent noise charge of more than one thousand electrons. Obviously, this result should not be directly compared to the noise equivalent charge of the presented buffer-shaper charge pulse detector, since the sensing device capacitance might not be comparable and leakage current shot noise of direct conversion layers might have an important impact. However, the comparison shows the large potential for improvement of energy resolution of energy-sensitive detectors.

X-ray spectroscopy applications [88], [89] will require improved energy resolution for achievement of highly sensitive element-based material discrimination and will, therefore, take profit from detectors with improved noise performance.

The improved noise performance of the presented buffer-shaper charge pulse detecting circuit might as well be useful in order to compensate for the generally poor efficiency of scintillator layers in comparison to direct conversion layers. Using a scintillator-based sensing device in combination with a low to medium energy X-ray source might require detection of low charge amounts in order to enable photon counting, i.e. high-contrast X-ray absorption imaging without suffering from beam hardening effects.

Chapter 7

Summary and Outlook

In this thesis, circuit design techniques and novel circuit topologies have been developed in order to achieve progress in cutting-edge noise performance, i.e. the sensitivity, of *synchronous* CMOS image sensors and *asynchronous* energy-sensitive single-particle and X-ray photon imaging systems.

In the field of *asynchronous* single-particle and X-ray photon detectors, CSA-shaper circuits (Charge Sensitive Amplifier and Shaper circuits) are the traditional choice of charge pulse detecting circuits, mainly for the reason of their possibly high charge-to-voltage conversion factor which is independent of the sensing device capacitance. This CSA-specific property is crucial for implementations using discrete devices or for integrated CSAs combined with wire-bonded external sensing devices, i.e. in cases of high sensing device capacitance. However, the analysis presented in chapter 5 shows that the amplifier's transconductance, i.e. its power consumption, required to achieve a given noise performance strongly scales with the sensing device capacitance. Therefore, power-efficient low-noise asynchronous charge pulse detection with CSAs still requires low sensing device capacitance even with the conversion factor being independent of the sensing device capacitance. This consideration becomes increasingly important in the case of segmented detectors with high pixel number and, consequently, often restricted power budget per pixel. For such detectors either bump-bonded or monolithic sensing devices with low sensing capacitance are the preferred solutions. Probably the lowest sensing device capacitance is provided by the combination of scintillator layers and visible-wavelength sensing devices with area independent capacitance, such as photogates.

For such sensing devices, a buffer-shaper circuit, as presented in chapter 6, relying on charge-to voltage conversion on its total input capacitance achieves a good charge-to-voltage conversion factor. Under these circumstances, buffer-

shaper circuits outperform CSA-shaper circuits in terms of equivalent noise charge for a given power budget thanks to the absence of a feedback capacitor, low input capacitance of source-follower buffers, and reduced complexity for the implementation of a very-high-value reset resistor. Based on the excellent noise performance achieved with the implemented test circuits, buffer-shaper circuits are very interesting candidates of charge pulse detecting circuits for future highly segmented single-particle and X-ray photon detectors.

In the field of low-noise *synchronous* CMOS image sensors, a commonly used architecture using BPDs, pixel-level source-followers, and switched-capacitor column-level voltage amplifiers has emerged over the past decade. Besides flicker noise of the source-follower and leakage shot noise of the buried photodiode, thermal noise of the source-follower and, more importantly, of the column-level amplifier is a significant noise component in these sensors. Two novel circuit topologies able to reduce thermal noise in synchronous CMOS image sensors to an extremely low level are presented in this thesis.

The first approach, as discussed in chapter 3, uses pixel-level open-loop voltage amplification to virtually eliminate the impact of noise from column-level, chip-level, and board-level readout and processing circuits. At the same time, the thermal noise bandwidth of the pixel-level amplifier is effectively limited by the amplifier's own low-pass transfer function. Thanks to the effect of load capacitance multiplication due to the use of voltage gain, the described bandwidth limitation is achieved at low expense of column load capacitance and, therefore, low cost and compact package size. An attractive compromise between area-saving bandwidth limitation and decent swing, i.e. decent dynamic range, is found for moderate values of pixel-level voltage amplification. For example, at an amplification of about ten, a linear dynamic range of 73 dB is achieved. Compression characteristics of the open-loop amplifier can be employed to extend the useful region of the sense node voltage swing while applying voltage amplification for low illumination levels. A dynamic range of 90 dB has been demonstrated by use of the pixel-level amplifier's compression characteristics. Substantial spread of the compression characteristics will, however, necessitate pixel-by-pixel digital correction of the compressed region of the amplifier's characteristics. Even if such a correction is relatively substantial in terms of computation power, it could possibly be based on the simple readout of a frame of pixel reset levels at power-up of a camera system, rather than requiring a dark frame or any calibration frames under known illumination condition.

The second low-noise image sensor topology, as presented in chapter 4, uses conventional pixel-level source-follower buffers in conjunction with column-level open-loop degenerate common-source amplifiers. On one hand, the noise performance of image sensors based on this approach benefits from the lower sense node capacitance achieved with pixel-level source-followers in comparison

to pixel-level common-source amplifiers. On the other hand, more power consumption and silicon area on the column level of the image sensor are required than in the case of pixel-level amplification, since the noise of the column-level open-loop amplifier has to be minimized in absence of pixel-level voltage amplification. Single-branch degenerate common-source amplifiers are the preferred amplifier topology for low-noise open-loop amplifier implementation. As a matter of fact, they offer a substantially advantageous trade-off between noise performance and required capacitance per column in comparison to switched-capacitor OTA based amplifiers in conventional low-noise image sensors.

The results achieved with both presented approaches represent the current cutting-edge noise performance in synchronous CMOS image sensors. Less than 0.9 electrons of readout noise equivalent charge and an overall dark noise of 1.4 electrons including leakage shot noise of the BPD are achieved by the implemented image sensor with pixel-level voltage amplification. Less than 1.0 electrons of readout noise including a power supply noise component has been measured on a one-column implementation of the image sensor with open-loop column-level voltage amplification. Removal of this supply noise component by row noise correction is expected to improve the readout noise equivalent charge of such an image sensor topology to a level between 0.6 and 0.8 electrons. These characterization results as well as calculations and simulations indicate that the thermal noise components present in image sensors using the presented topologies have been reduced to deep sub-electron values of around 0.4 electrons depending on the exact implementation. The achieved overall dark noise is, therefore, predominantly defined by flicker and random telegraph signal noise from the pixel-level electronics and by leakage current shot noise of the BPD.

In comparison to thermal noise, leakage current shot noise and flicker noise are highly dependent on process technology. If future technology enhancements result in further reductions of leakage current density and flicker noise power spectral density, the advantage of the presented architectures over the conventional architecture will become even more pronounced thanks to the extremely low thermal noise component.

This final consideration actually gives a very interesting perspective towards practical single-photon detection with charge-integrating synchronous CMOS image sensors. For reliable detection of single photons, an RMS variation equivalent of about one third of a photon is required. The most realistic way to achieve this goal in the medium term is to combine deep sub-electron dark noise with near 100% product of quantum efficiency times fill factor, as achieved with backside illuminated image sensors. In this perspective, it is important to point out that the implementation versions of the image sensor with open-loop column-level voltage amplification using n-channel pixel-level transistors are immediately compatible with backside illuminated image sensors. The

implemented version of the image sensor with pixel-level voltage amplification would suffer from a severe loss of quantum efficiency, if operated with back-side illumination, due to the use of p-channel transistors in an n-well biased at a positive supply voltage. The concept of using a single-transistor pixel-level common-source amplifier can, however, also be implemented by exclusive use of n-channel transistors at the pixel level, possibly at the cost of losing the interesting compression characteristics of the pixel-level amplifier.

Based on these considerations and on the achievement of deep sub-electron thermal noise, the development of the proposed next-generation low-noise image sensor topologies is considered as a relevant step towards single-photon-detecting charge-integrating CMOS image sensors, to be complemented with future CMOS image sensor process technology enhancements.

To summarize, two novel readout circuit topologies for synchronous CMOS image sensors have been developed in the framework of this thesis. These readout circuits rely on pixel-level and column-level open-loop voltage amplification respectively. This key property has been shown to enable readout noise performance below the values achieved by prior art image sensors. The method of open-loop voltage amplification, which is not conventional in the field, has practically been proven to be applicable to CMOS image sensors without any significant compromises or disadvantages. Additionally, a novel charge pulse detecting circuit for asynchronous energy-sensitive detection of single massive particles or high-energy photons has been proposed in this thesis. This charge pulse detecting circuit based on a source-follower type buffer and a shaper circuit has been shown to provide an advantage in terms of noise performance over conventional charge pulse detecting circuits. The work presented in this thesis can, therefore, be considered as a relevant contribution to the ongoing improvement in noise performance of cutting edge synchronous and asynchronous imaging systems for visible light or high-energy radiation. Three patent applications covering the results of this thesis have been filed.

Appendix A

Formulae

A.1 Optimization of Gate Area in Pixel-Level Common-Source Amplifiers

This appendix section provides an analytical optimization of the gate area for minimum noise equivalent charge of common-source pixel-level open-loop amplifiers. The overall noise equivalent charge to be minimized, as given in (A.1), contains the components of flicker noise and thermal noise.

$$q_{n,cs}^2 = q_{n,cs,th}^2 + q_{n,cs,1/f}^2 \quad . \quad (A.1)$$

Inserting the flicker noise and thermal noise equivalent charge from (3.8) and (3.11), and replacing the sense node capacitance by expression (3.12) leads to expression (A.2) of the equivalent noise charge as a function of the gate area a_{cs} . In order to obtain this simple expression, the gate-drain overlap capacitance of common-source transistor C_{gd} is neglected and the gate-source capacitance C_{gs} is approximated by the gate-channel capacitance, i.e. gate-source overlap capacitance is neglected as well.

$$q_{n,cs}^2 = (C_{cst} + a_{cs}C_a)^2 \left(V_{cst}^2 + \frac{1}{a_{cs}} V_{1/a}^2 \right) \quad , \quad (A.2)$$

where

$$C_{\text{cst}} = C_{\text{jun,n}} + C_{\text{ovlp,tx}} + C_{\text{jun,p}} + C_{\text{ovlp,res}} + C_{\text{wire,vcst}} + C_{\text{wire,sncol}} (1 + A_{\text{pix}}) , \quad (\text{A.3})$$

$$C_a = \frac{2}{3} C_{\text{ox}} , \quad (\text{A.4})$$

$$V_{\text{cst}}^2 = \frac{2kT\gamma}{A_{\text{pix}} C_{\text{col,tot}}} , \quad (\text{A.5})$$

and

$$V_{1/a}^2 = \frac{K}{C_{\text{ox}}} \int_0^\infty |H_{\text{cds}}(f)|^2 \left| \frac{1}{1 + 2\pi f R_1 C_{\text{col,tot}}} \right|^2 \frac{1}{f} df . \quad (\text{A.6})$$

the extrema of the noise equivalent charge are found by setting the derivative of (A.2) equal to zero:

$$\frac{d(q_{\text{n,cs}}^2)}{d a_{\text{cs}}} = (C_{\text{cst}} + a_{\text{cs}} C_a) \left(a_{\text{cs}}^2 + a_{\text{cs}} \frac{V_{1/a}^2}{2V_{\text{cst}}^2} - \frac{V_{1/a}^2 C_{\text{cst}}}{2C_a V_{\text{cst}}^2} \right) = 0 . \quad (\text{A.7})$$

Analysis of the above polynomial equation's roots reveals only one minimum at positive gate area, as given in (A.8)

$$a_{\text{cs,opt}} \approx \frac{V_{1/a}^2}{4V_{\text{cst}}^2} \left(-1 + \sqrt{1 + \frac{8V_{\text{cst}}^2 C_{\text{cst}}}{V_{1/a}^2 C_a}} \right) . \quad (\text{A.8})$$

A.2 Optimization of Gate Width in Buffer-Shaper Circuits

This appendix section covers the analytical optimization of the source-follower transistor's gate width in buffer-shaper circuits for minimum electronic noise. As outlined in section 6.2.5, the high-pass filtering frequency f_{hp} , the low-pass filtering frequency f_{lp} , the high-pass filtering capacitance C_{hp} , and the low-pass filtering capacitance C_{lp} are defined by the used sensing device, available area and power, and the requirement of low ballistic deficit. It has also been shown, that the source-follower gain A_{sf} can be assumed constant in the case of an n-type source-follower transistor. This assumption greatly simplifies the analytical optimization. As discussed previously, the recharge resistor's noise component is independent of the source-follower's gate width. The equivalent noise charge expression to be minimized, as given in (A.9), is therefore obtained from (6.15) omitting the recharge resistor's noise equivalent charge component:

$$q_{\text{n,opt}}^2 = q_{\text{n,sf}}^2 + q_{\text{n,hp}}^2 + q_{\text{n,lp}}^2 . \quad (\text{A.9})$$

Inserting (6.9), (6.13), and (6.14) for the different components of the noise equivalent charge and replacing the total input capacitance C_{in} and the source-follower's input capacitance $C_{\text{in,sf}}$ by (6.5) and (6.6) respectively, the following expression for the noise equivalent charge is found:

$$q_{\text{n,opt}}^2 = \left(C_{\text{sen}} + C_{\text{par,in}} + C_{\text{gd,sf}} + C_{\text{gs,sf}} (1 - A_{\text{sf}}) \right)^2 \cdot \left(kT\gamma_{\text{sf}} \frac{2\pi f_{\text{lp}}}{g_{m,\text{sf}}} + \frac{kT\gamma_{\text{hp}}}{C_{\text{hp}}} + \frac{kT\gamma_{\text{lp}}}{C_{\text{lp}}} \right) . \quad (\text{A.10})$$

The source-follower's transconductance, gate-drain capacitance, and gate-source capacitance are expressed as a function of its gate width W_{sf} by (A.11), (A.12), and (A.13), where I_{sf} , L_{min} , c_{gdw} , and c_{gds} are the source-follower transistor's bias current, length, gate-drain overlap capacitance per unit width, and gate-source overlap capacitance per unit width respectively.

$$g_{m,\text{sf}} = \sqrt{2\mu C_{\text{ox}} I_{\text{sf}} \frac{W_{\text{sf}}}{L_{\text{min}}}} . \quad (\text{A.11})$$

$$C_{\text{gd},\text{sf}} = c_{\text{gdw}} W_{\text{sf}} . \quad (\text{A.12})$$

$$C_{\text{gs},\text{sf}} = \left(c_{\text{gds}} + \frac{2}{3} C_{\text{ox}} L_{\text{min}} \right) W_{\text{sf}} . \quad (\text{A.13})$$

Inserting these expressions into (A.10) leads to the following expression of the equivalent noise charge as a function of the gate width:

$$q_{\text{n,opt}}^2 = (C_{\text{cst}} + C_{\text{w}} W_{\text{sf}})^2 \left(V_{\text{cst}}^2 + \frac{n_{\text{w}}}{W_{\text{sf}}} \right) . \quad (\text{A.14})$$

where

$$n_{\text{w}} = \frac{kT \gamma_{\text{sf}}^2 2\pi f_{\text{lp}} \sqrt{L_{\text{min}}}}{\sqrt{2\mu C_{\text{ox}} I_{\text{sf}}}} , \quad (\text{A.15})$$

$$V_{\text{cst}} = \sqrt{kT \left(\frac{\gamma_{\text{hp}}}{C_{\text{hp}}} + \frac{\gamma_{\text{lp}}}{C_{\text{lp}}} \right)} , \quad (\text{A.16})$$

$$C_{\text{cst}} = C_{\text{sen}} + C_{\text{par,in}} , \quad (\text{A.17})$$

and

$$C_{\text{w}} = c_{\text{gdw}} + (1 - A_{\text{sf}}) \left(c_{\text{gsw}} + \frac{2}{3} C_{\text{ox}} L_{\text{min}} \right) . \quad (\text{A.18})$$

The optimum gate width is found by searching the minima of the noise equiv-

alent charge as a function of the gate width. The extrema of the equivalent noise charge are found at its points of zero derivative:

$$\frac{d \left(q_{\text{n,opt}}^2 \right)}{d \left(W_{\text{sf}} \right)} = 0 . \quad (\text{A.19})$$

In the resulting polynomial equation, a first extremum at negative gate width, as given in (A.20), can be factorized and discarded.

$$W_{\text{sf,ex0}} = -\frac{C_{\text{cst}}}{C_{\text{w}}} . \quad (\text{A.20})$$

Definition of a variable x as the square root of W_{sf} , allows expression of the remaining polynomial equation as a third-order polynomial of x , as given in (A.22).

$$x = \sqrt{W_{\text{sf}}} . \quad (\text{A.21})$$

$$ax^3 + bx^2 + cx + d = 0 , \quad (\text{A.22})$$

where

$$a = 2V_{\text{cst}}^2 C_{\text{w}} , \quad (\text{A.23})$$

$$b = \frac{3}{2} n_{\text{w}} C_{\text{w}} , \quad (\text{A.24})$$

$$c = 0 , \quad (\text{A.25})$$

and

$$d = -\frac{1}{2}n_w C_{cst} . \quad (\text{A.26})$$

The roots of (A.22) can be found by application of Vieta's formula. For application of this method, the polynomial discriminant Δ is determined according to (A.27):

$$\Delta = \left(\frac{q}{2}\right)^2 + \left(\frac{p}{3}\right)^3 = \frac{n_w^2 C_{cst}}{64V_{cst}^4 C_w} \left(\frac{C_{cst}}{C_w} - \frac{n_w^2}{4V_{cst}^4} \right) , \quad (\text{A.27})$$

where

$$p = \frac{c}{a} - \frac{b^2}{3a^2} = -\frac{3}{16} \frac{n_w^2}{V_{cst}^4} , \quad (\text{A.28})$$

and

$$q = \frac{2b^3}{27a^3} - \frac{bc}{3a^2} + \frac{d}{a} = \frac{n_w}{4V_{cst}^2} \left(\frac{n_w^2}{8V_{cst}^4} - \frac{C_{cst}}{C_w} \right) . \quad (\text{A.29})$$

The calculations are significantly simplified under the following assumption, which is verified for the design presented in section 6.3.3.

$$\frac{C_{cst}}{C_w} \gg \frac{n_w^2}{4V_{cst}^4} . \quad (\text{A.30})$$

In this case, the discriminant is positive. Furthermore p is non-zero in the case of any meaningful design. Under these conditions, (A.22) has one real root, which is found by calculation of another auxiliary variable u :

$$u = \sqrt[3]{-\frac{q}{2} + \sqrt{\Delta}} \approx \sqrt[3]{\frac{n_w C_{cst}}{4V_{cst}^2 C_w}} . \quad (\text{A.31})$$

The root value of x , and hence the optimum gate width, are finally found according to (A.32).

$$\begin{aligned} W_{sf,opt} &= (x_0)^2 = \left(-\frac{b}{3a} + u - \frac{p}{3u} \right)^2 \quad (\text{A.32}) \\ &\approx \left(-\frac{n_w}{4V_{cst}^2} + \frac{n_w^{1/3} C_{cst}^{1/3}}{2^{2/3} V_{cst}^{2/3} C_w^{1/3}} + \frac{n_w^{5/3} C_w^{1/3}}{2^{10/3} V_{cst}^{10/3} C_{cst}^{1/3}} \right)^2 . \end{aligned}$$

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Curriculum Vitae

Christian Lotto

Born April 12, 1979, swiss, single

e-mail: christian.lotto@a3.epfl.ch

2008 - present **Ph.D. Student**

CSEM SA, Zürich

2007 **R&D Engineer**

CSEM SA, Zürich

Applied research and development of CMOS image sensors

2004 - 2006 **Analog Design Engineer**

Micronas GmbH, Freiburg (Germany)

Development of hall-effect magnetosensor ICs

2003 - 2004 **Master Thesis Student**

Philips Research, Eindhoven (Netherlands)

Research on MEMS for radio-frequency applications

2002 **Intern**

Phonak Hearing Systems, Stäfa

Development of a DSP algorithm for sound scene classification

2002 **Teaching Assistant**

Federal Institute of Technology Lausanne (EPFL)

Assistant in assembler programming lectures

1999 - 2004 **MSc. Microengineering**

EPFL, Lausanne

Publication List

Peer Reviewed Publications:

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