University of Neuchâtel

Design, fabrication and characterization of piezoresistive pressure sensors, including the study of electrochemical etch-stop

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by

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Design, fabrication and characterization of piezoresistive pressure sensors including the study of electrochemical etch-stop

de Monsieur Benjamin Kloeck

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Abstract

Classical pressure sensors use a membrane that is deformed under the action of a differential pressure in a liquid or a gas. The deformation of the membrane can be detected by a variety of methods, one of which is to measure the resistance change of strain gauges.

The combination of this old idea with microelectronic fabrication processes and with recently developped silicon micromachining techniques, has lead to the creation of solid-state sensors which can be batch-fabricated and which have very small dimensions and reproducible specifications.

This text describes the development of a miniature piezoresistive pressure sensor. The thin membrane of the sensor was made by chemical etching of silicon in a potassium hydroxide solution. One of the most important objectifs of the research was the study of electrochemical etch-stop to control the thickness of the etched mebrane, and to show the compatibility of this etch-stop method with a standard bipolar fabrication process. Therefore, the main originality of this work lies in the investigation of some fundamental and practical aspects of electrochemical etching and etch-stop.

Contents

Abstract i

Contents ii

List of symbols, abbreviations and notations vi

1. Introduction 1

1.1 Objective and environment of the work 2
1.2 Overview of the technological evolution 2
1.2.1 History of piezoresistive pressure sensors 3
1.2.2 Membrane etching 3
1.2.2.1 Monocrystalline silicon membranes 3
1.2.2.2 Etch-stop 4
1.2.2.3 Polysilicon membranes 5
1.2.3 Readout techniques for membrane-based pressure sensors 6
1.2.4 Packaging techniques 8
1.2.5 On-chip electronic circuitry 9
1.3 Outline of the thesis 10

2. Piezoresistivity in monocrystalline silicon 11

2.1 Introduction 12
2.2 Mathematical model 12
2.2.1 Piezoresistance in a coordinate system aligned to the crystal axes 12
2.2.2 Transformation of axes 15
2.2.3 Longitudinal and transverse piezoresistance coefficients 16
2.3 Measurement of the piezoresistance coefficients 18
2.4 Quantum-physical explanation 22
2.5 Concentration and temperature dependence of the piezoresistivity 24
2.5.1 Doping concentration dependence 24
2.5.2 Temperature dependence 24
2.6 Piezoresistivity in diffused resistors 27
2.6.1 Effective diffused piezoresistance coefficient 27
2.6.2 Diffused piezoresistance coefficient as a function

of doping concentration 28
2.6.3 *Diffused piezoresistance coefficient as a function of temperature* 29
2.7 Conclusions 30

3. Design and fabrication of piezoresistive pressure sensors 32

3.1 General piezoresistive pressure sensor design 33
3.1.1 *General structure* 33
3.1.2 *Wheatstone bridge configuration* 33
3.13 *Resistance change as a function of stress* 35
3.2 Membrane stress calculation 36
3.2.1 *Basic equations* 36
3.2.2 *Simply supported rectangular plates* 38
3.2.3 *Rectangular plates with built-in edges* 39
3.2.4 *Computer simulation* 40
3.2.5 *Non-linearity and the Balloon effect* 41
3.3 Geometrical design of the piezoresistive structure 45
3.3.1 *General design considerations* 45
3.3.2 *Computer simulations* 46
3.3.3 *Cross-connection of the half-resistors* 48
3.3.4 *Wafer lay-out* 49
3.4 Technological design of the piezoresistors 50
3.4.1 *Implanted versus diffused resistors* 50
3.4.2 *Definition of the implanation parameters* 51
3.5 Fabrication process 53
3.6 Conclusions 58

4. Membrane fabrication by means of electrochemical etch stop 59

4.1 Introduction 60
4.2 Bias-dependent etching of silicon 61
4.2.1 *Introduction* 61
4.2.2 *Experimental* 62
4.2.2.1 *Sample preparation* 62

4.2.2.2 Electrochemical measurements 63
4.2.2.3 Etch rate determination 63
4.2.3 Results and discussion 64
4.2.3.1 Current-voltage characteristics 64
4.2.3.2 Silicon etch rate versus voltage 69
4.2.3.3 Oxide time-to-etch back 71
4.2.4 Conclusion 73
4.3 Electrochemical etch-stop on an epitaxial layer 74
4.3.1 Introduction 74
4.3.2 Experimental 75
4.3.3 Results and discussion 76
4.3.3.1 Etch-stop methodologies 76
4.3.3.2 Etch-stop process parameters 79
4.3.3.3 Electric al contact to the epitaxial layer 84
4.3.3.4 Etch-stop indicators 85
4.4 Conclusions 88

5. Characterization of the sensor 90

5.1 Introduction 91
5.2 Measurement set-up 91
5.3 Pressure response 93
5.3.1 Pressure sensitivity 93
5.3.2 Zero-pressure offset 96
5.3.3 Non-linearity 97
5.4 Temperature response 100
5.4.1 Temperature coefficient of the piezoresistors 100
5.4.2 Temperature coefficient of offset 101
5.4.3 Temperature coefficient of pressure sensitivity 103
5.4.4 Temperature hysteresis 106
5.5 Conclusions 109

6. Biomedical applications 119

6.1 Introduction 120
6.2 Pressure sensor for heart catheter 120
6.3 pH/pressure sensor for stomach catheter 121
6.3.1 Introduction 121

6.3.2 Sensor chip fabrication ... 122
6.3.3 Catheter encapsulation ... 123
6.3.4 Measurement set-up ... 124
6.3.5 Results and discussion ... 125
6.3.6 Conclusion ... 126
6.4 Force sensor for muscle catheter ... 126
6.4.1 Introduction ... 126
6.4.2 Chip fabrication ... 126
6.4.3 Measurement set-up ... 127
6.4.4 Results and discussion ... 128
6.4.5 Conclusion ... 129
6.5 Conclusions ... 130

7. Conclusions ... 132

Acknowledgements ... 137

Publications ... 138

References ... 140

List of symbols, abreviations and notations

Greek symbols:

ε_s	permittivity of silicon
γ_s	specific gravity of silicon
μ	mobility of an electron
ν	Poissons's ratio
π_{11}, π_{12}, π_{44}	piezoresistance coefficients in a Cartesian system aligned to the <100> silicon (or germanium) crystal axes
π_l	longitudinal piezoresistance coefficient
π_t	transverse piezoresistiance coefficient
ρ	electric resistivity.
σ	electric conductivity
σ	normal stress
τ	shear stress

Roman symbols:

a, b	side lengths of a rectangular membrane
D	flexural rigidity
E	electric field
h	thickness of a membrane
i	electric current
I_b	DC current applied to a Wheatstone bridge
j	(technological context) diffusion junction depth
j	(electrical context) current density
k	wave number of an electron
L_p	p-type side of a space charge region
M	bending moment
N	impurity concentration
O	offset of a Wheatstone bridge
p	pressure
R	electric resistance
S	pressure sensitivity of a sensor
T	temperature
V	electric voltage
V_b	DC voltage applied to a Wheatstone bridge

w	deflection of a membrane under pressure
W	width of the space charge region

Abbreviations:

BEP	energy band edge point
CVD	chemical vapour deposition
EC	epitaxial layer contact
EDP	a solution of ethylenediamine, pyrocatechol and water
FP	Flade potential
ISFET	ion-sensitive field-effect transistor
OCP	open circuit potential
OFP	oxide formation potential
PP	passivation potential
SC	silicon substrate contact
SCE	standard calomel electrode
SCR	space charge region
s.d.	standard deviation
SFB	silicon fusion bonding
TC	temperature coefficient
TCO	TC of Wheatstone bridge offset
$TC\pi$	TC of piezoresistance coefficient
TCR	TC of piezoresistor
TCS_i	TC of pressure sensitivity, with a constant current applied
TCS_v	TC of pressure sensitivity, with a constant voltage applied

Notations:

X α Y	variable X is proportional to variable Y
ΔX	small increase of the variable X
(100)	Miller indices for a crystal plane
{100}	Miller indices for a family of equivalent planes
[100]	Miller indices for a crystal direction
<100>	Miller indices for a family of equivalent directions

Chapter 1 Introduction

1.0 Summary
1.1 Objective and environment of the work
1.2 Overview of the technological development
1.3 Outline of the thesis

1.0 Summary

This chapter sketches the general environment in which this thesis is placed. It briefly reviews the evolution of the technology that was developed for the fabrication of pressure sensors, starting with silicon strips glued on a relatively big membrane and going through a chain of refinements to yield the present-day sensors with very small dimensions. Finally the structure of this manuscript is outlined.

1.1 Objective and environment of the work

6%, 10% and 6%, such are the relative parts of sessions concerning pressure sensors at the International Conference on Solid-State Sensors and Actuators, held in 1985, '87 and '89 respectively [1-3]. The conference is the main world event in the field of integrated sensors and actuators. Do these percentages mean that pressure sensor research is over its zenith ? The fact is that, especially for monocrystalline pressure sensors, the development has reached the point where purely academic input has become rare, and where most efforts are concentrated on various applications and industrial mass production. Symptomatic for this evolution is the majority of contributions from industrial R&D centra at Transducers 89, whereas in 1987 academic researchers were still ahead in number.A primary reason for the industrial take-over is the development of high-volume markets, mainly in process control, automotive and medical applications. According to prognosis reports on sensor technology [4], the expectation of a steadily growing market seems to be justified.

In the line of this evolution, the design and development of a piezoresistive pressure sensor that is reported in this text, has been undertaken in collaboration with an electronic company, Ascom Favag Microelectronics S.A. in Bevaix (Switzerland). The main objective was to find out if the bipolar technology that is in use at Ascom Favag, could be combined with the fabrication of piezoresistive sensors. In particular, an elegant process could be developped if the epitaxial layer required for bipolar circuits could serve at the same time for the fabrication of very thin membranes with precisely controlled thickness, which are necessary for the pressure sensors. The fundamental study of electrochemical etching and etch-stop on an epitaxial layer has allowed to realize this objective.

The available tools were computer aided design programs, the collaboration with the integrated-circuit laboratory of Ascom Favag Microelectronics, the integrated-circuit laboratory of the Institute of Microtechnology of the University of Neuchâtel, and the professional literature on the subject. To start with, an overview of the literature is given in the next section.

1.2 Overview of the technological evolution

This section briefly reviews the technological development of piezoresistive pressure sensors, wet etching of silicon membranes, other readout techniques for membrane based pressure sensors, packaging techniques, and on-chip electronic circuitry. Most subjects are only mentioned; for a more complete discussion, reference is made to the literature.

1.2.1 History of piezoresistive pressure sensors

Soon after the discovery of the piezoresistance effect in silicon and germanium three decades ago [5], the use of diffusion techniques for the fabrication of piezoresistive sensors for stress, strain and pressure was proposed by Pfann and Thurston in 1961 [6], and used for the first time on thin single-crystal silicon membranes by Tufte et al. [7]. The idea was rapidly adopted by others, thanks to the better performance of silicon resistors compared to classical strain gauges. Some of the practical advantages that have been recognized from the beginning are listed below:

- the gauge factor of semiconductors is more than an order of magnitude higher than that of metals;
- the integration of gauge and membrane suppresses the need to bond the two components together, which eliminates hysteresis and creep;
- the strain is transmitted perfectly from the membrane to the gauge;
- silicon is a very robust material;
- the resistors are limited to the very surface of the element in bending or torsion, i.e., where the stresses are maximal;
- good matching of the resistors can be achieved, which is particularly useful if Wheatstone bridges are used;
- the technique is very suitable for miniaturization of the sensors;
- mass fabrication is easy because it can profit from the available technology of integrated circuits;
- the sensors can be made very cheap;
- it is possible to integrate electronic circuitry directly on the sensor chip, for e.g. signal amplification and temperature compensation.

The very first semiconductor strain gauges used a homogeneously doped silicon strip attached to a membrane of other material. Here, only advantage was taken of the higher gauge factor of silicon. Later, a whole wafer was used as membrane under bending, and resistors were diffused in order to measure the maximum stress at the surface. Further refinement was introduced by etching away part of the silicon under the resistors until a thin membrane was left, so that higher stresses were created and the sensitivity increased. This configuration is generally used today.

1.2.2 Membrane etching

1.2.2.1 Monocrystalline silicon membranes

Many methods have been developed to fabricate silicon membranes. A possible classification of bulk silicon micromachining is the following:

Monocrystalline silicon micromachining:

Mechanical:	drilling	
Electromechanical:	spark erosion	
Chemical:	isotropic:	HF-HNO_3-CH_3COOH
	anisotropic:	KOH (and other hydroxides)
		EDP
		hydrazine
Electrochemical:	isotropic:	HF

Historically, the isotropic etchants were developed first. A typical isotropic etch solution is the system HF/HNO_3, with H_2O or CH_3COOH as diluents [8, 9]. An electrochemical etch system is the solution HF/H_2O [10]. In this case, silicon is oxidized anodically, and the oxide is continuously etched away by the dilute HF solution. A minimal current density is required, hence only conductive silicon, i.e. high doped can be etched. Evidently, the membranes that are obtained are circular. The lateral underetch of the etch mask is as large as the depth of the hole. Therefore, isotropic etchants have been combined with mechanical methods to improve the ratio of lateral dimensions to depth. Although still in use, these methods are not ideally suited for large mass production. Drilling is done on-wafer, but requires the handling of one membrane at the time. The anisotropic etchants, much more popular today, will be discussed in Chapter 4.

1.2.2.2 Etch-stop

The importance of automatic etch-stop will be explained in Chapter 4. Three methods are briefly compared here:

Chemical:	boron etch-stop	
Electrochemical:	isotropic	n^+/n etch-stop
	anisotropic	p/n junction etch-stop

Again, the isotropic etch-stop has been developed first [11]. A low doped n-type epitaxial layer is grown on a high doped silicon substrate. The substrate is etched electrochemically as mentioned before. However, the conductivity of the epitaxial layer is too low to reach the required current density and etching stops at the interface. To improve the depth to width ratio, this method has been combined with spark erosion, which is facilitated by the relatively high conductivity of the n^+ substrate [12]. The metal electrode of the spark machine can be shaped to drill several holes at a time.

The boron etch-stop method is based on the observation that highly doped silicon (particularly with boron) is etched very slowly by the mentioned anisotropic etchants [13, 14]. Thus, thin membranes can be fabricated by diffusing or implanting boron into a thin layer on one surface of a wafer and by etching the silicon away from the other side through a mask window. As soon as all the silicon is removed, etching is stopped at the diffused layer, which will stay as a free membrane connected to the thick silicon rim. It is a very versatile technique to make micromechanical devices. However, the high doping concentration precludes them from integrating electronic components.

The most appropriate method to make low-doped, monocrystalline silicon membranes of well controlled dimensions and thickness, is the electrochemical etch-stop on a diffusion or an epitaxial layer. This will be discussed extensively in Chapter 4.

1.2.2.3 Polysilicon membranes

The introduction of polysilicon as membrane material, has opened new possibilities. An etch-resistant film, e.g. silicon dioxide or silicon nitride, is grown or deposited on a silicon substrate. Polysilicon is then deposited on top of this film. One way to go now is to etch away the silicon from the back side of the wafer until etching is stopped at the inert layer. Smaller sensors can be obtained if the hole is not designed to delineate the membrane, but just to give access to the etch-resistant layer, which is then removed by e.g. a HF solution in the case of silicon oxide. The result is shown schematically in Figure 1.1 [15].

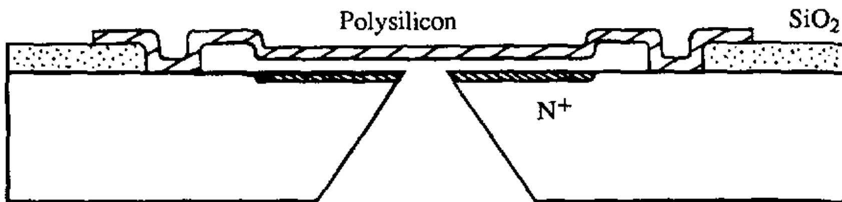


Fig 1.1 The combination of polysilicon and a sacrificial layer allows the fabrication of smaller chips than with anisotropic etching of monocrystalline silicon membranes, since less surface is lost by the {111} side planes of the hole.

A second way to go is surface micromaching technology [16]. In this approach the bulk silicon is not etched away, but only the sacrificial layer between the

silicon substrate and the polysilicon membrane is removed through via holes on the surface. In order to obtain a sealed cavity, the via holes are closed by oxidation [17]. It is noted that only absolute pressure sensors can be made this way. The dimensions of polysilicon membranes can be controlled very accurately, however, the mechanical stability of polysilicon is inferior to that of monocrystalline silicon. Although polysilicon is applied sucessfully to create a variety of geometries, it is rarely used for pressure sensor membranes.

1.2.3 Readout techniques for membrane-based pressure sensors

In the course of the evolution of the membrane etch methods, new techniques have emerged to detect the deformation of the thin membrane under the action of the applied pressure. Most methods detect the static deflection of the membrane, although also resonant membrane sensors have been reported. The readout methods can be classified as follows:

Static membrane:

Stress detection:	piezoresistive strain gauges (normal stress)
	transverse voltage gauge (shear stress) [6,18,19]
	piezojunction effect [20,21]
	polysilicon [22,23]
Deformation detection:	capacitance [24-27]
	optieal interferometry [28,29]
Resonant membrane:	piezoresistive strain gauges [30]
	optical [31]

In the class of static methods, the first set of elements are sensitive to the stresses in the membrane that are induced by its deformation. Devices that sense normal stress are the subject of this thesis. The second type of sensors, also called piezo-Hall sensors or X-ducers, is based on the observation that an electric field is developed perpendicular to the current flow if such devices are subjected to a shear stress. The maximum voltage occurs at an angle of 45° to the <110> directions of a (100) silicon substrate. No Wheatstone bridge is required here to eliminate the temperature coefficient of the resistors, so that only one element is needed, which can yield smaller sensors. The temperature coefficient of the pressure sensitivity, however, is the same as for Wheatstone bridge sensors. The piezojunction effect is based on the fact that the current gain and the base-emitter voltage depend on the applied stress. The sensor can be designed so that the dependence of the base-emitter voltage is linear.

At high temperatures, diffused resistors show pn junction leakage problems. To circumvent these problems, polysilicon resistors can be deposited on an isolated membrane of monocrystalline silicon or other material. Both Wheatstone bridge and transverse voltage sensors have been reported. These devices can be used to temperatures up to 250°C. However, the piezoresistance coefficients of polysilicon are about half as large as those for monocrystalline silicon. By laser recrystallization, they can be increased to 2/3 of the monocrystalline values [32].

A second static readout method is deformation detection. The membrane can be used as one electrode of a capacitor with a fixed second electrode. The second electrode is typically a thin metal film deposited on a glass or silicon substrate that is bonded to the rim of the membrane. The complete membrane surface contributes to the output signal. The pressure resolution and temperature behaviour of capacitive pressure sensors is better than for piezoresistive sensors, however, capacitance is more complicated to measure than voltage, and on-chip circuitry is recommended to avoid stray capacitances. As for the piezoresistive sensors, the on-chip electronics prohibits its use at higher temperatures.

Recent developments in optical interference readout are very promising for high temperature applications. Interference can be acheived between a semi-transparent optical flat and a thin silicon membrane. The fringes are measured with a photodetector. A laser beam is directed on this system either directly or via optical fibers. The laser and the readout equipment is at room temperature and only the fiber-end is close to the sensor, so that high temperature applications (> 200°C) are possible.

Finally the sensor can be designed as a resonant structure. The resonance frequency of a silicon membrane depends on the pressure that is applied. The membrane can be excited thermally or electrically by depositing a piezoelectric material such as zinc oxide. Reported readouts are piezoresistive and optical. Although a frequency signal is interesting from the point of view of data acquisition, there are other mechanical structures than membranes that reach higher Q-factors [33], and thus better measurement resolutions.

All the mentioned systems have their typical application fields, depending on parameters such as pressure range, resolution and stability, mass production and price, environment (especially temperature), required equipment and others. For high volume, low price and low temperature applications, piezoresistive pressure sensors are ideally suited.

1.2.4 Packaging techniques

Encapsulation of the sensors is a special problem that deserves attention. The way the silicon chip is fixed in its housing is subjected to two major conditions: the

encapsulation should introduce minimal mechanical stress and, more important, if mechanical stress can not be avoided, it has to be stable in time in order to limit the offset drift of the sensor. For some applications, also the temperature behaviour of the bond must be regarded. These conditions preclude the use of e.g. epoxies and other organic adhesives. Considering the thermal expansion coefficients, silicon to glass and silicon to silicon are the best combinations. A classification of the non-organic bond techniques for these materials is given here:

<u>Silicon to glass:</u>	anodic bonding
	eutectic bonds
<u>Silicon to silicon:</u>	sputtered glass
	spin-on glass
	glass frit seals
	eutectic bonds
	silicon direct bonding

An overview of these methods (except for the last one), including the required temperatures and typical applications, is given by Knecht [34]. The most widely used for the moment is anodic bonding of silicon to Pyrex 7740 borosilicate glass. The process involves temperatures of typically 400°C and voltages between 600 and 1000 V. The bond is completed in a few seconds.

Recently, new techniques have been developed to bond two silicon wafers together. In a first embodiment, intended to fabricate silicon-on-insulator structures, the wafers were bonded (and thus also isolated) by a silicon oxide layer [35-37]. Anthony [35] used a pair of oxidized wafers and bonded them anodically with 30-50 V applied, at 850-950°C and during one hour. Ohura et al. [36] used one oxidized and one bare wafer and bonded them by heat treatment at 1100°C during four hours. Li et al.[37] worked with pairs of oxidized/bare and oxidized/oxidized wafers, and bonding was carried-out at 1000°C during 30 minutes.

A very interesting new evolution, called silicon fusion bonding (SFB), is the bonding of bare silicon wafers together without any intermediate layer [38-39]. The quality of the interface is such that nearly perfect diodes are obtained with silicon wafers of opposite type. The process involves cleaning of the mirror-polished wafers, a hydrophilic surface treatment and heating to 1000-1100°C for two hours [38]. This method has been used to fabricate small piezoresistive pressure sensors, where the {111} slopes of the etched hole go inwards, instead of outwards as for the classical anisotropically etched sensors (cfr. Figure 1.2).

Thus, less chip surface is required for the same membrane dimensions. The process is illustrated in Figure 1.2 [39]. A pyramidal pit is etched in the base wafer. A second wafer with n-type epitaxial layer is bonded on the first by SFB. The substrate of the top wafer is completely etched away until only the epitaxial layer remains as a thin membrane. Then, piezoresistors are implanted in the membrane. This method allowed the fabrication of a catheter-tip sensor of only 0.4 mm wide.

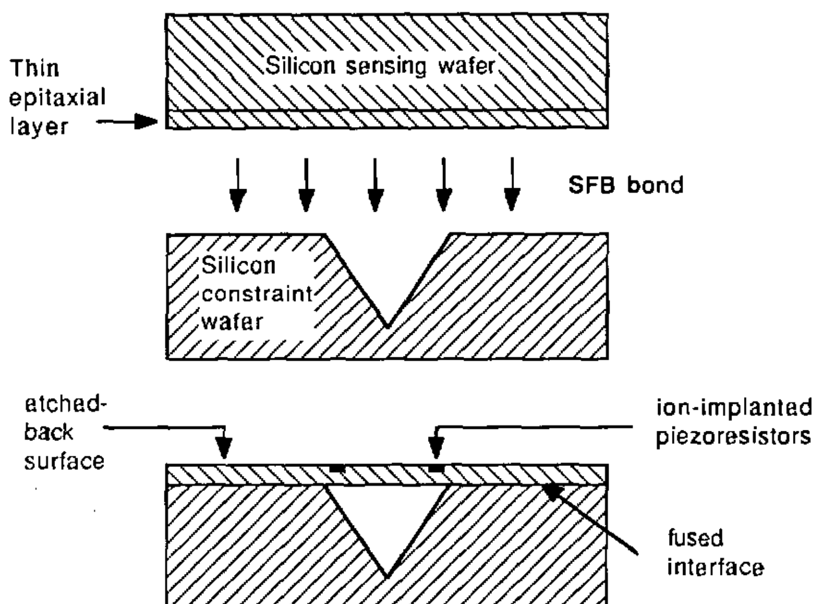


Fig 1.2 Fabrication process of a small piezoresistive pressure sensor by silicon fusion bonding (SFB) [39].

1.2.5 On-chip electronic circuitry

It was mentioned before that for a capacitive sensor, on-chip circuitry is desirable to avoid stray capacitances. For piezoresistive sensors, active on-chip signal conditioning is not a necessity, but a number of important advantages can be realized, such as signal amplification, offset compensation, common-mode voltage elimination, improvement of the linearity, temperature compensation, output lead count reduction and voltage-to-frequency conversion. A stable, low-impedance signal leaves the sensor chip and the requirements for the off-chip readout equipment are less severe than for a bare Wheatstone bridge sensor. On-chip circuit realizations have been published in bipolar technology with voltage [41,43] and with frequency output [40,42,43], and in MOS technology [44]. Also

Ascom Favag Microelectronics has developed and characterized a compatible bipolar process [45, Chapter 3 of this thesis].

1.3 Outline of the thesis

The theoretical and technological background required to understand and apply the piezoresistive effect in semiconductors is reviewed in **Chapter 2**. The piezoresistance coefficients are defined. The parameters that will be important for sensor design, such as crystal orientation dependence, temperature and doping concentration influences are discussed, for bulk silicon as well as for thin diffused layers.

Chapter 3 presents the general design of piezoresistive pressure sensors and the design rules that were considered in order to optimize the performance of the sensor. Special attention is paid to the position of the piezoresistors on the membrane and to their diffusion profile.

Chapter 4 is a fundamental study of one aspect of the sensor fabrication: the etching of the thin silicon membrane by electrochemical etch-stop. First the electrochemical behaviour of silicon as such in a potassium hydroxide solution is studied. Then this knowledge is applied to control the thickness of silicon membranes by etch-stop on an epitaxial layer, and the performance and characteristics of the method are explored.

Chapter 5 evaluates the output specifications of the fabricated pressure sensor and relates the observed results to the physical laws of the second chapter and to the fabrication parameters of the two previous chapters. The response to pressure is investigated with respect to sensitivity, offset and non-lineartity. The disturbing influence of temperature on resistance, offset and sensitivity is discussed.

Chapter 6 presents three applications of piezoresistive pressure sensors for biomedical purposes. Catheter systems for invasive in-vivo measurement in the heart, stomach and muscle tissue are described and commented.

Chapter 7, finally, summarizes the important conclusions of this thesis work.

Chapter 2
Piezoresistivity in monocrystalline silicon

2.0 Summary
2.1 Introduction
2.2 Mathematical model
2.3 Measurement of the piezoresistance coefficients
2.4 Quantum-physical explanation
2.5 Temperature dependence
2.6 Piezoresistivity in diffused resistors
2.7 Conclusions

2.0 Summary

The basic elements of piezoresistive pressure sensors are the stress-sensitive resistors. Probably all materials exhibit the piezoresistance effect in some degree. However, the effect is of particular interest in certain semiconductors, in which appreciable resistance changes occur. The most studied up to now are silicon and germanium. In this chapter an overview is given of the piezoresistance effect in monocrystalline silicon, based on the literature of the last 30 years [1 - 18].

2.1 Introduction

Semiconductors, and in particular silicon, are widely used for sensors for mechanical signals, e.g. pressure, force and acceleration. Monocrystalline silicon is particularly suited for the conversion of mechanical deformation to an electrical signal due to its excellent mechanical properties, combined with a high piezoresistance effect, i.e., the bulk resistivity (ρ) is influenced considerably by mechanical stress. Many materials exhibit stress dependence through the mobility or the number of charge carriers as a function of the volume of the material. Volume changes affect the energy gap between the valence and the conduction bands. Hence, the number of carriers and thus the resistivity change. For silicon, however, the piezoresistance effect is observed to be much larger than predicted by these mechanisms. This has been explained by means of the many-valley model.

In this chapter, the mathematical model that describes the phenomenon will be reviewed. A special feature is the anisotropy of the piezoresistance coefficients. We will give the results of measurements that have been carried out some 30 years ago to define the piezoresistance coefficients and then we will discuss the quantum-physical explanation of the mechanism. The dependence on doping concentration and on temperature are discussed, since they will be very important for sensor design.

The above mentioned properties will first be described for bulk material with homogeneous doping concentration. The situation becomes more complex when diffused resistors are involved, since the piezoresistance coefficients and their temperature behaviour depend on the doping concentration. Hence, we will discuss how effective values can be obtained by integrating over the doping profile.

2.2 Mathematical model

2.2.1 Piezoresistance in a coordinate system aligned to the crystal axes

The mathematical description of the piezoresistivity starts with the general three-dimensional relation between current and electrical field, and the influence of stress on this relation. The symmetry of the crystal lattice will help to simplify the complex mathematical model.

For a three-dimensional anisotropic crystal, the electric field vector (E) is related to the current vector (i) by a three by three resistivity tensor. Experimentally the nine coefficients are always found to reduce to six and the tensor is symmetrical:

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_5 & \rho_4 & \rho_3 \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{2.1}$$

Both silicon and germanium have a cubic crystal structure. If the Cartesian axes are aligned to the <100> axes of the crystal, then ρ_1, ρ_2 and ρ_3 define the dependence of the electric field along one of the <100> crystal axes on the current in the same direction. ρ_4, ρ_5 and ρ_6 are cross-resistivities, relating the electric field along one axis to the current in a perpendicular direction. For an isotropic conductor, e.g. unstressed silicon, $\rho_1 = \rho_2 = \rho_3 = \rho$, and ρ_4, ρ_5 and ρ_6 are equal to zero.

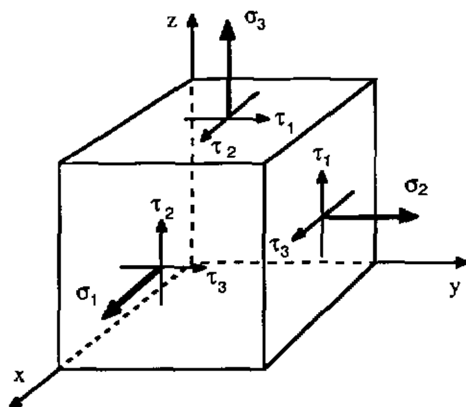


Fig. 2.1 Definition of the normal stresses σ_i and shear stresses τ_i

In a piezoresistive material, these six resistivity components depend on the stress situation of the material, which can also be decomposed into three normal stresses σ_1, σ_2 and σ_3, along the cubic crystal axes, and three shear stresses τ_1, τ_2 and τ_3, as defined in Figure 2.1, where the stresses are represented as acting on a cube of infinitesimal dimensions *dx*, *dy* and *dz*. If we reference the resistivities to the isotropic unstressed case, then we can write the six components as:

$$\begin{bmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{bmatrix} = \begin{bmatrix} \rho \\ \rho \\ \rho \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} \Delta\rho_1 \\ \Delta\rho_2 \\ \Delta\rho_3 \\ \Delta\rho_4 \\ \Delta\rho_5 \\ \Delta\rho_6 \end{bmatrix} \tag{2.2}$$

The piezoresistance effect can now be described by relating each of the 6 fractional resistivity changes $\Delta\rho_i/\rho$ to each of the 6 stress components. Mathematically this yields a matrix of 36 coefficients. The elements of this matrix are called piezoresistance coefficients, expressed in Pa^{-1} (1 cm^2/dyne = 10 Pa^{-1}). In order to define the matrix, it is not necessary to carry out 36 independent measurements. Since the matrix represents properties of a crystal, it must be invariant under the symmetry operations of the crystal lattice under study. Hence the form of the matrix can be found theoretically for each class of crystals belonging to the same crystallographic point group. The symmetry conditions lead to certain relations between the different matrix components which reduce the number of independent, nonvanishing components to considerably less than 36. For the cubic crystal structure of silicon and germanium, three different coefficients remain, π_{11}, π_{12} and π_{44}, and the matrix takes the following form :

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_1\\ \Delta\rho_2\\ \Delta\rho_3\\ \Delta\rho_4\\ \Delta\rho_5\\ \Delta\rho_6\end{bmatrix} = \begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix} \cdot \begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \tau_1\\ \tau_2\\ \tau_3\end{bmatrix} \tag{2.3}$$

Combining formulas (2.1), (2.2) and (2.3), we obtain an expression for the electric field in a cubic crystal lattice under stress:

$$\begin{aligned} E_1 &= \rho\, i_1 + \rho\, \pi_{11}\, \sigma_1\, i_1 + \rho\, \pi_{12}\, (\sigma_2 + \sigma_3)\, i_1 + \rho\, \pi_{44}\, (i_2\, \tau_3 + i_3\, \tau_2) \\ E_2 &= \rho\, i_2 + \rho\, \pi_{11}\, \sigma_2\, i_2 + \rho\, \pi_{12}\, (\sigma_1 + \sigma_3)\, i_2 + \rho\, \pi_{44}\, (i_1\, \tau_3 + i_3\, \tau_1) \\ E_3 &= \rho\, i_3 + \rho\, \pi_{11}\, \sigma_3\, i_3 + \rho\, \pi_{12}\, (\sigma_1 + \sigma_2)\, i_3 + \rho\, \pi_{44}\, (i_1\, \tau_2 + i_2\, \tau_1) \end{aligned} \tag{2.4}$$

The first term in Eq. (2.4) is the contribution of unstressed conduction. The second term, containing π_{11}, represents the piezoresistance effect as it is known from wire and foil gauges; it is the effect of a stress in the direction of current flow, on the potential drop in that direction. The other terms reflect the more complicated piezoresistive behaviour of the stressed semiconductor lattice. These

coefficients are properties of the material and hence they vary from one material to another.

It is noted that the expressions of (2.4) are only valid for uniform bulk material. For devices with finite dimensions, the influence of dimension changes ought to be added, although in general this is negligible in comparison with the larger effect due to the change in resistivity. It is also important to notice that the piezoresistance coefficients can be either negative or positive, and that in general they vary with doping concentration and temperature, as will be explained in more detail later. For non-uniform materials, as e .g. the diffused or implanted silicon strain gauges that will be discussed in the last section of this chapter, the formulas have to be integrated over the complete structure.

2.2.2 Transformation of axes

With the knowledge of the three parameters π_{11}, π_{12} and π_{44}, which were defined in a coordinate system aligned to the <100> axes of the silicon crystal, all the piezoresistance properties of silicon can be calculated. In order to calculate the stresses and the electric field expressed in an arbitrary Cartesian system, the <100> axes can be transformed into the given coordinate system by means of the direction cosines written in terms of Euler angles as defined in Figure 2.2. A vector (x, y, z) referred to the crystal axes is transformed into a vector (x*, y*, z*) using:

$$\begin{bmatrix} x^* \\ y^* \\ z^* \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \cdot \begin{bmatrix} x \\ y \\ z \end{bmatrix} \qquad (2.5)$$

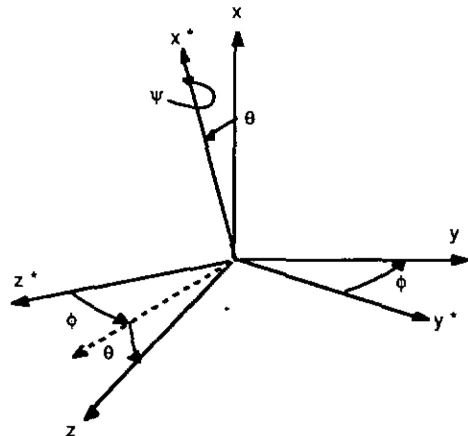


Fig. 2.2 Euler angles for Cartesian axes transformation.

In Eq. (2.5), the transformation matrix is the product of three matrices which represent three consecutive three-dimensional rotations given by:

$$\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \qquad (2.6)$$

$$\begin{bmatrix} \cos\phi \cos\theta \cos\psi - \sin\phi \sin\psi & \sin\phi \cos\theta \cos\psi - \cos\phi \sin\psi & -\sin\theta \cos\psi \\ -\cos\phi \cos\theta \sin\psi - \sin\phi \cos\psi & -\sin\phi \cos\theta \sin\psi + \cos\phi \cos\psi & \sin\theta \cos\psi \\ \cos\phi \sin\theta & \sin\phi \sin\theta & \cos\theta \end{bmatrix}$$

2.2.3 Longitudinal and transverse piezoresistance coefficients

In view of the use of the piezoresistance effect for sensor devices, two common situations will be examined here. They are represented schematically in Figure 2.3. The first one concerns a uniaxial state of stress σ^*, electric field E^* and current i^*, all in the same direction, but not necessarily along a crystal axis (Fig. 2.3a). In this case, the relation between stress and change of resisitivity is called longitudinal piezoresistance coefficient, noted π_l. In order to calculate π_l as a function of the three basic piezoresistance coefficients, the axis transformation of Eq. (2.5) is applied to Eq. (2.4), yielding:

$$E^* = \rho\, i^* + \rho\, i^* \left[\pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_1^2 m_1^2 + l_1^2 n_1^2 + m_1^2 n_1^2)\right] \tag{2.7}$$

and hence the longitudinal piezoresistance coefficient can be written as:

$$\pi_l = \pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})(l_1^2 m_1^2 + l_1^2 n_1^2 + m_1^2 n_1^2) \tag{2.8}$$

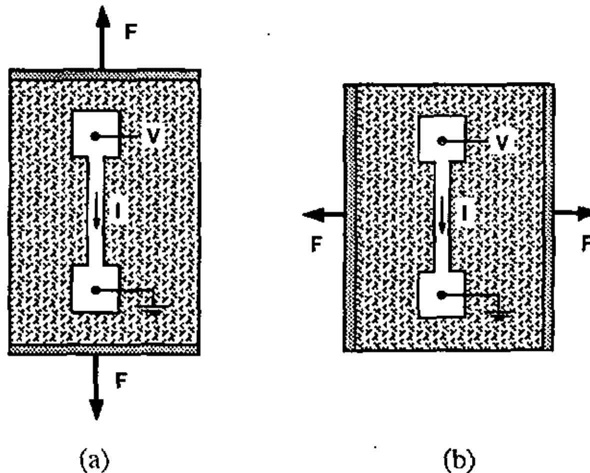


Fig. 2.3 Schematic representation of the stress/current situations that are ruled by the longitudinal piezoresistance coefficient (a) and by the transverse piezoresistance coefficient (b). F represents a force applied to the sample. It is noted that for clarity resistors are represented here, but the theory in the text is discussed for bulk material.

In another commonly used embodiment (very often combined with the previous case), the electric field and current are colinear, and the uniaxial stress is perpendicular to both (Fig. 2.3b), giving rise to a transverse piezoresistance coefficient, π_t, which is calculated likewise. The result is:

$$\pi_t = \pi_{12} - (\pi_{44} + \pi_{12} - \pi_{11})\,(l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2) \tag{2.9}$$

It is easily shown that the factor $(l_1^2 m_1^2 + l_1^2 n_1^2 + m_1^2 n_1^2)$ is a maximun in the directions making equal angles with the crystal axes, i.e., in the <111> directions. It follows that, if $(\pi_{44} + \pi_{12} - \pi_{11}) \neq 0$, the longitudinal coefficient has either a maximum or a minimum in the <111> directions, depending on the relative magnitudes of π_{11}, π_{12} and π_{44}. Materials with a minimum in the <111> directions have their maximum π_l along the crystal axes. The value of the <111> π_l is obtained from Eq. (2.8) by setting $l_1^2 = m_1^2 = n_1^2 = 1/3$:

$$(\pi_l)_{<111>} = \frac{1}{3}(\pi_{11} + 2\,\pi_{12} + 2\,\pi_{44}) \tag{2.10}$$

Calculated similarly using expressions (2.8) and (2.9), Table 2.1 lists longitudinal and transverse piezoresistance coefficients for various practically useful directions in cubic crystals.

Table 2.1 *Longitudinal and transverse piezoresistance coefficients for various directions in cubic crystals.*

Longitudinal Direction	π_l	Transverse Direction	π_t
1 0 0	π_{11}	0 1 0	π_{12}
0 0 1	π_{11}	1 1 0	π_{12}
1 1 1	$1/3\,(\pi_{11} + 2\,\pi_{12} + \pi_{44})$	$1\,\bar{1}\,0$	$1/3\,(\pi_{11} + 2\,\pi_{12} - \pi_{44})$
$1\,1\,\bar{0}$	$1/2\,(\pi_{11} + \pi_{12} + \pi_{44})$	1 1 1	$1/3\,(\pi_{11} + 2\,\pi_{12} - \pi_{44})$
$1\,1\,\bar{0}$	$1/2\,(\pi_{11} + \pi_{12} + \pi_{44})$	0 0 1	π_{12}
1 1 0	$1/2\,(\pi_{11} + \pi_{12} + \pi_{44})$	$1\,\bar{1}\,0$	$1/2\,(\pi_{11} + \pi_{12} - \pi_{44})$

It is noted that during device fabrication careful alignment to the crystal axes is required to realize maximum stress sensitivity, because of the high anisotropy of the piezoresistance coefficients. Pfann [12] made the interesting observation that

the piezoresistance coefficients would be independent of orientation for a semiconductor with $(\pi_{11} - \pi_{12} - \pi_{44}) = 0$. He showed that, in principle, it was possible to meet this requirement by an alloy of the silicon-germanium system, with still a usably large piezoresistance effect. He calculated that the coefficients of his isotropic alloy would be:

$$\pi_{11} = -49 \quad \pi_{12} = +21 \quad \pi_{44} = -70 \quad (10^{-11}\,Pa^{-1})$$

However interesting this idea is from a theoretical point of view, a description of a device based on this alloy was never published.

2.3 Measurement of the piezoresistance coefficients

In order to measure the piezoresistance coefficients, a small known stress has to be applied and the resistivity change measured. Two types of stress can conveniently be applied to a solid: hydrostatic pressure and uniaxial tension or compression. The effect of pure hydrostatic pressure p is obtained by setting $\sigma_1 = \sigma_2 = \sigma_3 = -p$ and $\tau_1 = \tau_2 = \tau_3 = 0$ in Eq. (2.4), which gives:

$$E_i = \rho\, i_i\,[1-p(\pi_{11} + 2\,\pi_{12})] \qquad (i = 1, 2, 3) \qquad (2.11)$$

Two other independent measurements are required to determine the three coefficients, which will give three linear combinations of the coefficients. C.S. Smith, who was the first to measure the coefficients π_{11}, π_{12} and π_{44} for different doping concentrations at room temperature, used the three independent arrangements presented in Figure 2.4 [2]. He applied a uniaxial tensile stress to a single crystal rod by hanging a weight on a string, and measured the voltage drop. The first set-up (Figure 2.4a) performs a longitudinal measurement on a [100] sample, yielding a value for π_{11}. The second (Fig. 2.4b) is a transversal measurement on the same sample, giving π_{12}. Finally a longitudinal measurement on a [110] sample (Fig. 2.4c) determines, in accordance with Table 2.1, a value for $1/2\,(\pi_{11} + \pi_{12} + \pi_{44})$. If the length of the specimens is large compared to the transverse dimensions, there will be a region in which the stress field is not perturbed by the grips used at the ends to apply the stress. The directly observed quantities, dR/R, have to be corrected for dimensional changes to obtain the required $d\rho/\rho$, although these corrections are small. In general the measurements are performed under adiabatic conditions, i.e. the measurement is completed in a short time compared to the time required for thermal equilibrium between the sample and its environment to be established after the stress is applied. The

correction that is needed to convert the measured constant to an isothermal constant is quite negligible [8].

Table 2.II lists the results that Smith published in 1954. It is seen that the values are considerably larger than the the typical values of 2 to 4 for commercially available strain gauges of other types. The largest coefficients for silicon are π_{11} in n-type silicon and π_{44} in p-type silicon, about $-102 \cdot 10^{-11}$ Pa^{-1} and $138 \cdot 10^{-11}$ Pa^{-1} respectively.

With the values of Table 2.II, Equations (2.8) and (2.9) can now be calculated. It was mentioned before that the maximum longitudinal piezoresistance coefficient π_l occurs either in the <111> or in the <100> directions, depending on the relative magnitudes of the main piezoresistance coefficients. Using the data of Table 2.II it is seen that p-type silicon and both types of germanium have maxima in the <111> directions, whereas n-type silicon has a maximum longitudinal effect along the crystal axes. The expressions of Table 2.1 give as maximum values for low doping concentrations and at room temperature:

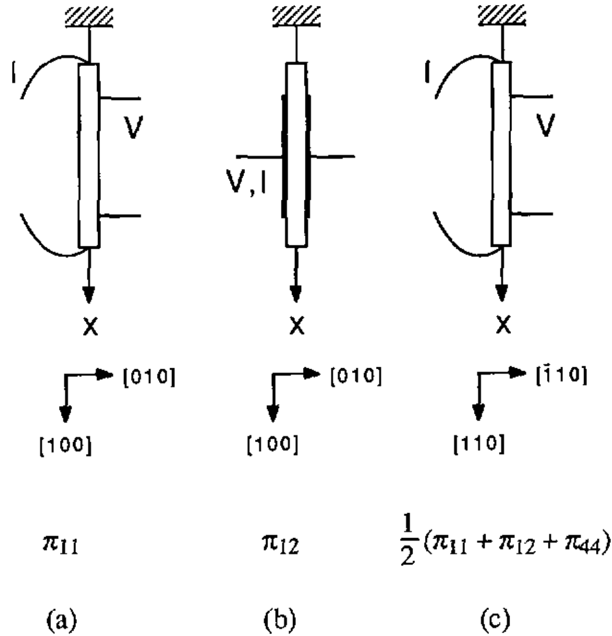


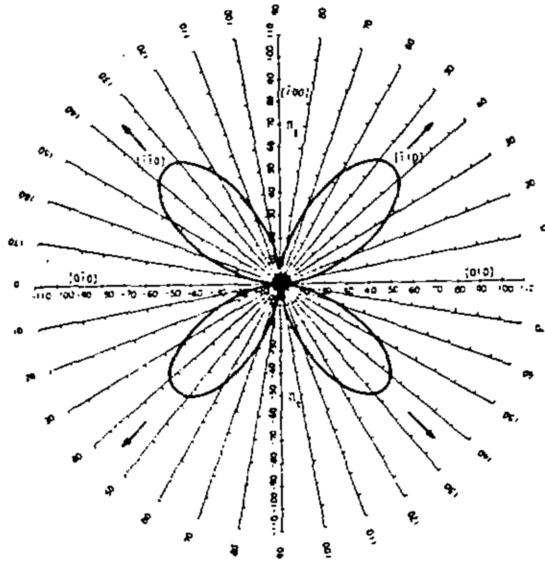
Fig. 2.4 Schematical set-up for the measurement of the piezoresistance coefficients by C.S. Smith [2], and (combination of) the coefficients that are obtained.

$$\begin{aligned} &\text{p-Si: } \pi_{l<111>} = 93.5 \cdot 10^{-11}\ \text{Pa}^{-1} \\ &\text{n-Si: } \pi_{l<100>} = -102.2 \cdot 10^{-11}\ \text{Pa}^{-1} \end{aligned} \tag{2.12}$$

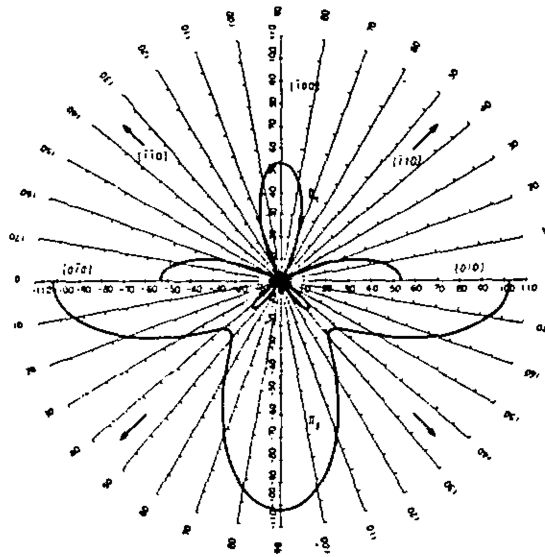
Figure 2.5 [17] shows a graphical plot of Eq. (2.8) and (2.9) in a <100> plane, with the sample orientation as parameter. Although Fig. 2.5 and Eq. (2.12) indicate that a higher piezoresistivity can be obtained with n-type silicon, piezoresistors in pressure sensors are generally of p-type because of orientation limitations. This will be explained in chapter 3.

***Table 2.II** Adiabatic piezoresistance coefficients at room temperature [2].*

Material	ρ	π_{11}	π_{12}	π_{44}
	Ω cm	10^{-12} cm²/dyne or 10^{-11} Pa^{-1}		
Silicon				
(p-type)	7.8	+6.6	-1.1	+138.1
(n-type)	11.7	-102.2	+53.4	-13.6
Germanium				
(p-type)	1.1	-3.7	+3.2	+96.7
	15.0	-10.6	+5.0	+46.5
(n-type)	1.5	-2.3	-3.2	-138.1
	5.7	-2.7	-3.9	-136.8
	9.9	-4.7	-5.0	-137.9
	16.6	-5.2	-5.5	-138.7



(a)



(b)

Fig. 2.5 Longitudinal and transverse piezoresistance coefficients in a <100> plane, as function of orientation. (a) p-type silicon; (b) n-type silicon [17].

2.4 Quantum-physical explanation

To begin the discussion with n-type silicon, let us consider the energy state of an electron in or above the conduction band [7,9,10,15,18]. Quantum mechanics permits us to associate separate wave numbers k_1, k_2 and k_3 with the components of the motion of the electron in the directions 1, 2 and 3. In some media (e.g. a silicon lattice), it is possible for an electron to achieve the minimum energy which it requires to remain in the conduction band, by several combinations of k_1, k_2 and k_3. These combinations are referred to as band edge points, since they constitute lower bounds for the energy required for a free electron. Figure 2.6 shows such points in k-space for n-type silicon, where this space is expressed in components corresponding to the directions of the crystal axes. An electron with slightly more energy than is required at a band edge point may possess such energy by a variety of combinations in (k_1, k_2, k_3) that describe a constant energy surface around the band edge point.

A family of such surfaces, centered on a band edge point, describes a so-called energy valley in k-space. In the case of silicon, these families consist of prolate ellipsoids of revolution that are aligned with the crystal axes.They are the projections in k-space of the energy band edge of the first Brillouin zone, as also illustrated in Figure 2.6. As there are several band edge points, we speak of a many-valley model. Since the valleys can be transformed into one another, they are identical except for orientation. Figure 2.6 draws two of the six valleys aligned with the six <100> directions (or three if only positive directions are considered). The fact that the constant energy surfaces possess principal axes of unequal lengths, may be interpreted to mean that the components of effective mass and mobility, μ_1, μ_2 and μ_3, of an electron in such a valley are different in the three principal directions. In Figure 2.6 the mobility is lowest in the valley direction (i.e. <100>) and highest normal to that direction. Consequently, these electrons make anisotropic contributions to the total conductivity of the lattice. If, however, all ellipsoids have the same properties and all valleys are equally populated with electrons, which is the case for silicon in the unstressed state, then the over-all conductivity of the lattice will be isotropic.

The application of an anisotropic stress condition now changes the relative energies, and hence changes the populations in these valleys. Traction in a valley direction removes electrons from that valley and transfers them to valleys lying normal to the traction. Compression has the opposite effect. In Figure 2.6 the stress-induced shifts of the band-edge energies are illustrated by dashed lines, for the case of traction in the [010] direction or compression in the [100] direction.

The energy decreases with a value ΔE in the [100] direction, hence more electrons have enough energy to enter the conduction band. In the [010] direction, the minimum required energy increases by ΔE and less electrons satisfy that condition. Thus the average mobility becomes lower in the direction of traction (longitudinal effect) and higher in directions transverse to the traction axis (transverse effect).

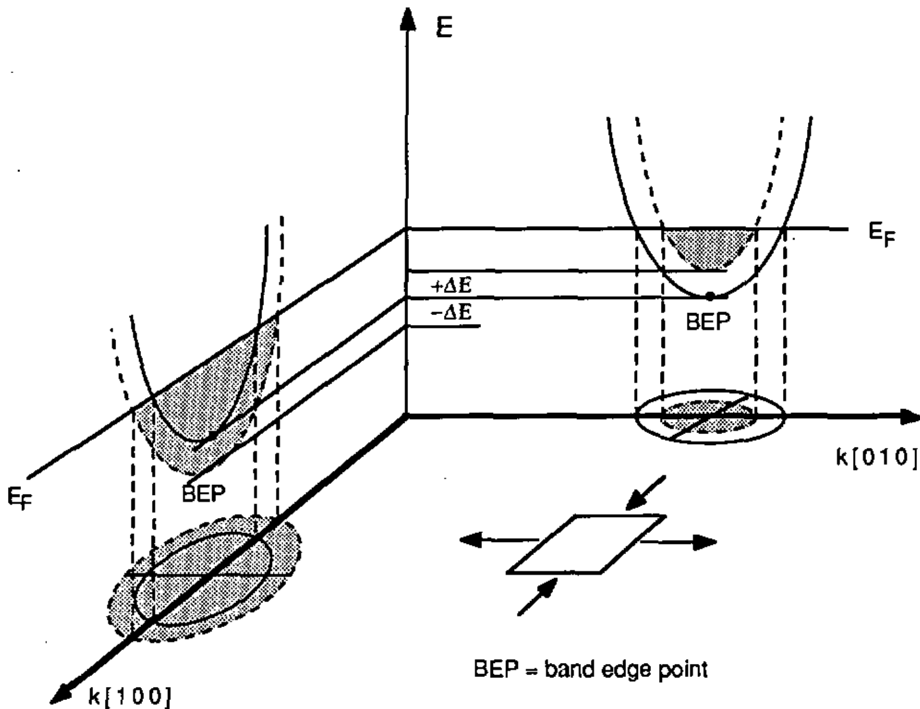


Fig. 2.6 Two n-type silicon valleys in k-space, aligned with the <100> axes, and energy shifts when stress is applied as indicated on the square sample [9].

The more the stress on the lattice destroys the symmetry of the valley structure, the larger piezoresistance effect is produced. The fact that for n-type silicon the valleys are aligned to the <100> axes explains thus that π_{11} is the largest coefficient for n-type silicon, since stress in a <100> direction significantly disturbs the symmetry. If, on the other hand, the crystal is stressed in a <111> direction, or if the resistance change is measured in a <111> direction, there is a negligibly small effect, because this direction is symmetrical to the three valleys.

Based on the many-valley model, the piezoresistance coefficients can be calculated explicitly [3, 8, 17]. For each ellipsoid, the conductivity is expressed as

a function of the population, given by the Fermi distribution function, and the relaxation time. The influence of stress on these two functions is calculated, and the total conductivity change is obtained by adding the contribution of each ellipsoid. The mathematical treatment and the resulting expressions for the piezoresistance coefficients yield relative magnitudes that are essentially in agreement with measured values. In reverse, piezoresistance measurements have been useful to obtain more detailed information on the band structure and scattering processes of semiconductors, and to verify the theoretical models.

For p-type silicon, the many-valley model is found to be less accurate. Still some general conclusions can be drawn using the model. The symmetry of the piezoresistance coefficients is assumed to be that of a <111>-valley material. They are imagined as lying in four valleys, one along each <111> direction. Stress in this direction will have an important impact on the symmetry of the valleys, resulting in a large coefficient π_{44}.

The mathematical expressions that are obtained by quantum physics contain terms that depend on temperature and on the doping concentration. Hence, the influence of these two parameters can be studied. This is discussed in the next section.

2.5 Concentration and temperature dependence of piezoresistivity

2.5.1 Doping concentration dependence

For the low doped silicon samples that he used (about 10^{15} cm^{-3} for the values listed in Table 2.II), Smith [2] observed no dependence on zero-stress resisitivity in his longitudinal measurements and thus concluded that the piezoresistance coefficients were independent on impurity concentration. For germanium on the other hand, he did find a doping concentration dependence: the piezoresistance coefficients decrease with increasing impurity concentration (see Table 2.II). Later measurements showed that at higher impurity concentrations, also for silicon this decrease is observed. Based on quantum physics the doping concentration dependence can be calculated. As an example, Figure 2.7 shows calculated and measured values for π_{11} for p-type silicon at 27°C and for impurity concentrations ranging from 10^{16} to 10^{20} at/cm^{-3} [16].

It is clear that for practical use, the doping concentration should not be chosen too high in order to keep a reasonably high gauge factor.

2.5.2 Temperature dependence

Mathematical calculations based on the many-valley model predict a decrease of the piezoresistance effect with increasing temperature [3,4,8], as illustrated

schematically in Figure 2.8, where the logarithm of any piezoresistance coefficient is plotted against the logarithm of temperature. At very low temperatures, this relation is linear with slope -1. In other words, the

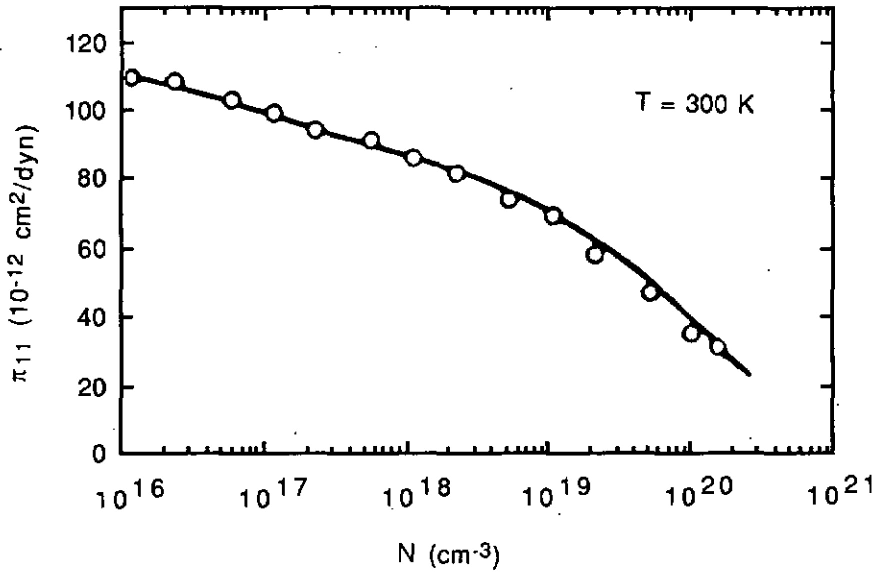


Fig. 2.7 π_{11} versus impurity concentration in n-type silicon, calculated (——) and measured values (o) [16].

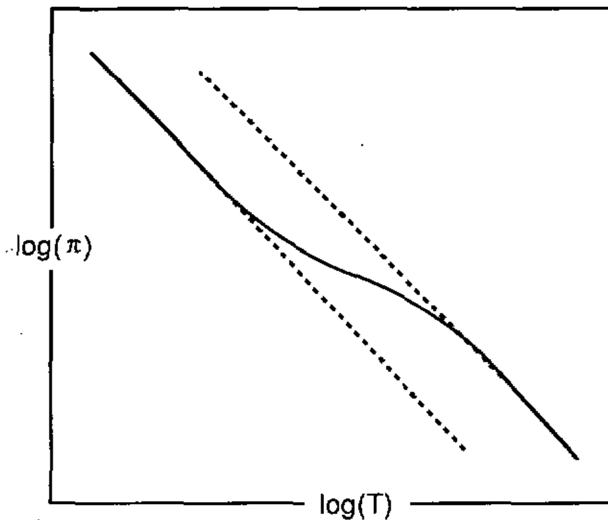


Fig. 2.8 Schematic variation of any piezoresistance coefficient with temperature.

piezoresistance coefficients increase linearly with the inverse of the temperature. At these temperatures, the scattering from electrons from one valley to another is frozen out. With increasing temperature, inter-valley scattering becomes more and more important. Since inter-valley scattering produces a larger assymmetry than intra-valley scattering, a larger piezoresistance is associated with the latter. Hence, the piezoresistance reducing effect of increasing temperature is partly cancelled by the enhancing effect of growing inter-valley scattering and the slope in Figure 2.8 is less steep in this transition area. At higher temperatures (including room temperature), the 1/T behaviour is restored again.

The 1/T relation predicted by the many-valley model was investigated by Morin et al. [4]. His measurements showed that for n-type silicon, linearity was followed for a large temperature range, about -200 to 80 °C (the highest temperature that he has used in his measurements). For p-type silicon, the relation was observed to be valid in a more restricted range, from -100 to 80 °C.

In general, any piezoresistance coefficient can be expressed by its low doped room temperature value, π_0, multiplied by a dimensionless factor which is a

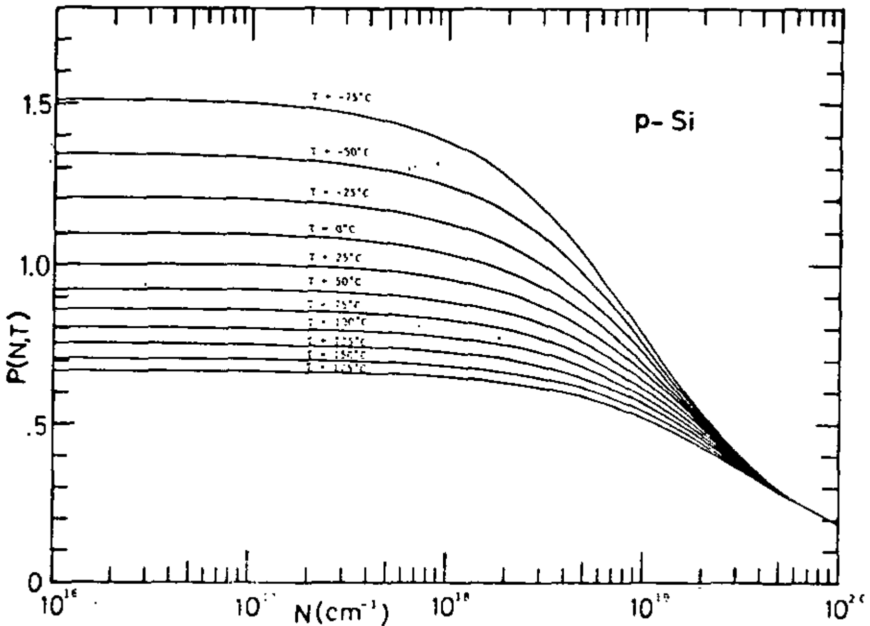


Fig. 2.9 Piezoresistance factor P(N,T) as a function of impurity concentration and temperature for p-type silicon [17].

function of doping concentration (N) and temperature (T), as proposed by Kanda [17]:

$$\pi(N,T) = \pi_0 \cdot P(N,T) \tag{2.13}$$

The piezoresistance factor P(N,T) based on mathematical calculations, is shown for p-type silicon in Figure 2.9. This figure graphically summarizes the discussion of this section: the piezoresistance decreases with increasing doping concentration and with increasing temperature. Moreover, the temperature coefficient of the piezoresistivity is seen to decrease with increasing doping concentration. It is reminded that this figure is only valid for uniform bulk material.

2.6 Piezoresistivity in diffused resistors

2.6.1 Effective diffused piezoresistance coefficient

An important advantage of semiconductors for pressure sensor applications, is that very thin layers can be fabricated by means of standard microelectronic technology, so that the current is limited to the surface of the element under bending or torsion, where stresses are maximum. Moreover, the geometry of the piezoresistors can easily be defined. If doping elements are either deposited on, or implanted in a silicon substrate of opposite doping concentration, and then diffused into it, a piezoresistive layer of typically 0.5 to 3 μm is obtained. In this section it will be assumed that the diffused layers are very thin compared to the substrate thickness, so that the stresses in the layer can be considered independent of depth.

In the previous sections, the physical properties of the piezoresistivity in silicon were described for uniform bulk material. There it was shown that the piezoresistance coefficients decrease with increasing impurity concentration (Figures 2.7 and 2.9). In diffused or implanted resistors the impurity concentration decreases with depth, hence, the piezoresistance coefficients show an increasing profile. If the (unstressed) impurity profile as a function of depth (z) is known, the piezoresistance profile $\pi(z)$ can be determined. (The Z-axis points from the surface into the silicon bulk.) For each piezoresistance coefficient, an average value $\bar{\pi}$ can now be defined as an effective coefficient that would yield the same electromechanical behaviour for the given doping profile. Obviously, a higher contribution to the average coefficient has to be given to layers where the current flow is higher. Hence the local coefficient $\pi(z)$ is weighed by the conductivity $\sigma(z)$, which is, again, a function of the doping profile:

$$\bar{\pi} = \frac{\int_0^j \pi(z)\, \sigma(z)\, dz}{\int_0^j \sigma(z)\, dz} \tag{2.14}$$

where j is the junction depth. It is assumed that the current distribution does not change significantly with applied stress. Although the deeper layers of the resistor are less doped and thus exhibit a higher piezoresistivity, their contribution is limited by the higher resistivity. Figure 2.10 schematically presents the piezoresistivity as function of depth and a typical profile of the contribution of each resistor layer to the effective piezoresistance coefficient of Eq.(2.14).

It is evident that the shown piezoresistivity profile has to be multiplied by the stress profile, if the latter is not constant as was assumed before, i.e. if the resistor depth is not negligible compared to the thickness of the substrate under stress in which it is diffused. For very thin silicon membranes, used in piezoresistive pressure sensors, this situation is not uncommon, as will be discussed in Chapter 3.

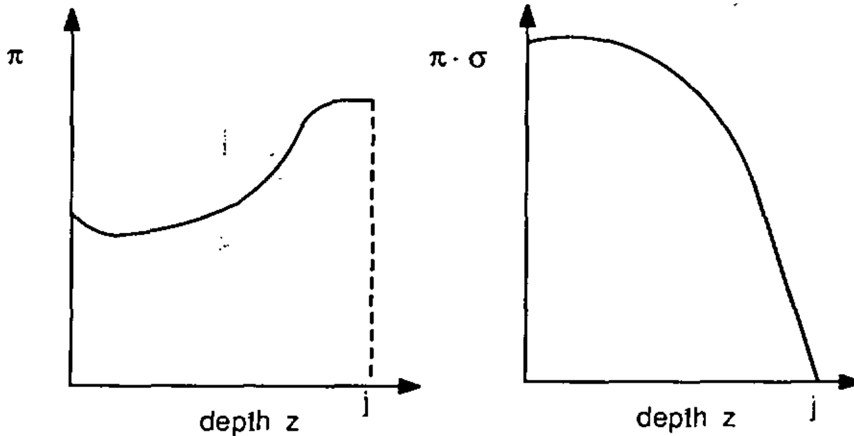


Fig. 2.10 (a) Schematic representation of the piezoresistivity π as a function of depth for a diffused resistor; (b) effective piezoresistivity, obtained by multiplying π(z) with the conductivity σ(z) as weighing function.

2.6.2 Diffused piezoresistance coefficient as a function of doping concentration

Kerr et al. [14] have shown that, for a given mathematical form of the impurity distribution function, the piezoresistance coefficients defined in expression (2.14) depend only on the surface concentration of impurities and not on the junction depth. Hence, the piezoresistance coefficient can be expressed as a function of the

surface concentration. Kerr has calculated this function for a complementary error profile (diffusion from a source which maintains a constant surface concentration) and for a Gaussian profile (diffusion from a thin planar deposit of impurities)for p-type silicon with <111> orientation. The results are presented in Figure 2.11. For comparison, the figure gives the concentration dependence of uniformly doped material. The diffused coefficients are systematically higher than the uniform coefficient because of the (small) contribution of deeper layers with higher piezoresistance. The longitudinal piezoresistance coefficient in p-type silicon has been measured for different surface concentrations by Tufte et al. [13] for doped layers that were diffused from a source which maintains a constant surface concentration (erfc profile). The measured values were in good agreement with the calculated coefficients.

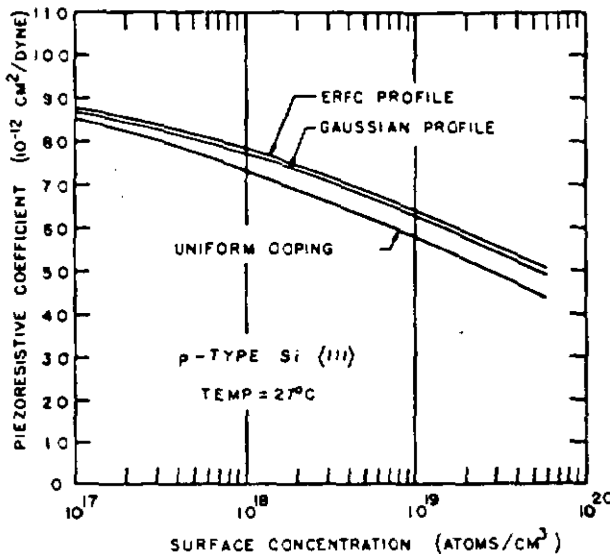


Fig. 2.11 Bulk piezoresistance coefficient versus impurity concentration in p-type silicon with <111> orientation, and diffused coefficients for erfc and Gaussian profiles of p-type impurities [14].

2.6.3 Diffused piezoresistance coefficients as a function of temperature

To calculate the average temperature dependence of the piezoresistance of diffused resistors, integration over the depth profile is, again, required. Hence, a relatively high surface concentration does not necessarily result in a very low temperature dependence, as Figures 2.8 and 2.9 (which are valid for uniform bulk material) would suggest, since the deeper and thus lower doped layers exhibit a

higher temperature coefficient. For this reason, shallow implanted resistors with a very sharp doping concentration decline can reach lower temperature dependencies than deep diffused resistors with equal sheet resistance.

Tufte et al. [13] have shown that, as was the case for the doping concentration dependence, it is possible to express the temperature behaviour of resistors with equal concentration profiles, as a function of only the surface concentration. Figure 2.12 plots the temperature dependence of two diffused p-type resistors with the same surface concentrations, but different depths, measured by Tufte. As for bulk material, the diffused piezoresistance coefficient is seen to decrease with increasing temperature. It is noted that the surface concentration of the samples that Tufte used was very high (2 10^{21} cm^{-3}), so that the temperature coefficient was very low: about -0.05 %/°C estimated from Figure 12.

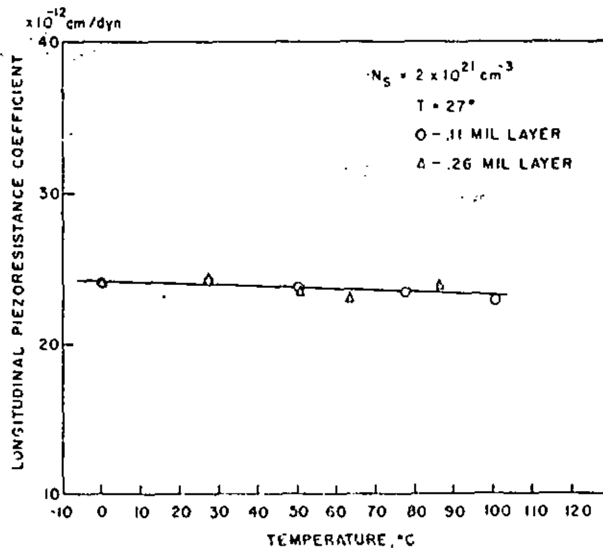


Fig. 2.12 Longitudinal piezoresistance coefficient versus temperature for two p-type diffused layers having the same mathematical inpurity profile function and the same surface concentration but different layer thicknesses [13].

2.7 Conclusions

In this chapter, an overview was given of the piezoresistance effect in monocrystalline silicon, which was seen to be highly anisotropic. The phenomenological description was supported by a mathematical model, to derive

expressions for all crystal directions. A physical explanation was given, based on the assymmetry of the three-dimensional band structure of silicon as described by the many-valley model. This model allows to calculate the dependence of piezoresistance on doping concentration and temperature. The piezo-resistance effect decreases with increasing doping concentration and with increasing temperature. Moreover, at higher doping concentrations, the temperature coefficient at room temperature decreases, and this effect is more significant than the loss of stress sensitivity due to the higher doping concentration.

The calculations and measurements mentioned above are valid for homogeneous silicon layers of constant doping concentration. To apply them to diffused resistors, they have to be integrated over the doping profile of the resistor. It was seen that the described tendencies remain valid , but are reduced, because they are averaged out over layers with different doping concentrations. For very steep junctions (obtained by ion implantation e.g.), the contribution of deeper layers with low concentration becomes less important, and the resistors approach the characteristics of bulk material.

In the next chapter, the knowledge of the piezoresistance coefficients for the different crystal orientations, and their dependence on doping concentration and temperature, will be used to design resistors for piezoresistive pressure sensors.

Chapter 3
Design and fabrication of piezoresistive pressure sensors

3.0 Summary
3.1 General design
3.2 Membrane stress calculation
3.3 Geometrical design of the piezoresistive structure
3.4 Technological design of the piezoresistors
3.5 Fabrication sequence
3.6 Conclusions

3.0 Summary

In this chapter, general design considerations of piezoresistive pressure sensors will be discussed. This study will focus on the position of the piezoresistors on the silicon membrane and on the fabrication technology of the piezoresistors as applied to our sensors. For all these considerations, the knowledge of the stress field in a membrane under pressure is required. Hence, this chapter includes a review of the methods that allow to calculate the membrane stress. Finally the fabrication sequence of our sensors with implanted resistors will be treated.
Parts of this chapter have been published in ref. [1, 2, 3, 4].

3.1 General piezoresistive pressure sensor design

3.1.1 General structure

In its most general embodiment, a piezoresistive pressure sensor consists of a thin silicon membrane supported by a thicker silicon rim. On the membrane, typically close to the edges, piezoresistors are integrated. The membrane is fabricated by etching away the bulk silicon on a defined region until the required thickness is reached. In the beginning of pressure sensor history, isotropic etchants were used, yielding round membranes. Today, anisotropic etch solutions are more popular, because a much better definition of the membrane dimensions can be achieved. The etched holes are defined by the silicon crystal structure and have thus rectangular or square borders. The etch technique that we used, and especially the etch-stop technique to control the thickness of the membranes that we optimized, are extensively described and studied in chapter IV.

Figure 3.1 presents a schematic cross-section of a piezoresistive pressure sensor. When a pressure difference is applied across both sides of the device, the thin membrane will bend downward or upward, inducing traction or compression on the resistor. The resistance change caused by this stress can easily be measured.

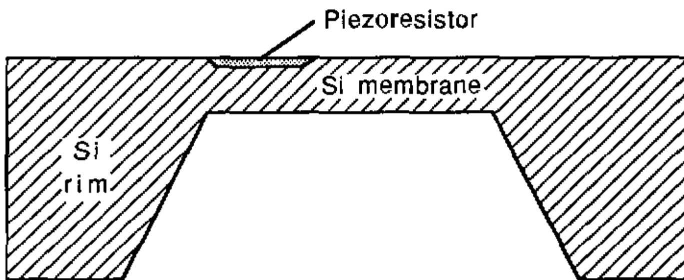


Fig. 3.1 Schematic cross-section of a piezoresistive pressure sensor

3.1.2 Wheatstone bridge configuration

In general, not one piezoresistor is used but four, as shown in Figure 3.2a. Two are placed parallel to opposite edges of the membrane, and the other two perpendicular to the other two edges. The two perpendicular resistors sense stress in the direction of their current axes and undergo thus an increase in resistance for positive pressure (membrane bend downward, causing traction on the membrane surface at the edge). The parallel resistors are under lateral stress and show a resistance decrease under the same condition. For negative pressure (membrane bend upward), the resistance changes are of opposite sign. If the resisors are correctly positioned with respect to the stress field over the membrane, the

correctly positioned with respect to the stress field over the membrane, the absolute value of the four resistance changes can be made equal. The resistors are connected as a Wheatstone bridge, as presented schematically in Figure 3.2b Equally positioned resistors form opposite arms of the bridge so that, under applied pressure, the left and right output nodes of the bridge deviate from zero with opposite signs.

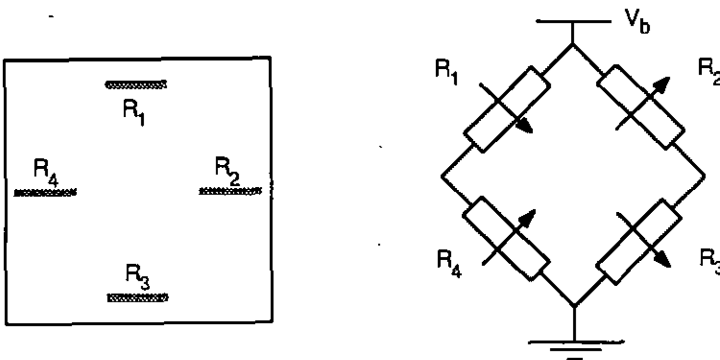


Fig. 3.2 Schematic view of the basic position of the piezoresistors on the membrane (a) and connection in a Wheatstone bridge (b). The arrows indicate resistance changes when the membrane is bend downward.

The Wheatstone bridge configuration has some distict advantages. It converts the resistance change directly to a voltage signal. Power can be supplied to the bridge by applying either a constant voltage or a constant current. It is easily calculated that the differential output voltage (ΔV) of an ideally balanced bridge with assumed identical (but opposite in sign) resistance changes ΔR, in response to a differential pressure change ΔP, is given by:

$$\Delta V = \frac{\Delta R}{R} V_b \tag{3.1}$$

where R is the zero-stress resistance and V_b the voltage over the bridge. For a constant supply voltage, the pressure sensitivity (S) is defined as the relative change of output voltage per unit of applied differential pressure (expressed in e.g. mV/V bar):

$$S = \frac{\Delta V}{\Delta p} \cdot \frac{1}{V_b} = \frac{\Delta R}{\Delta p} \cdot \frac{1}{R} \tag{3.2}$$

Here an important advantage of the Wheatstone bridge configuration shows up: the output voltage is, in first order, independent of the absolute value of the piezoresistors, but appears to be determined by the relative resistance change and the bridge voltage.

If a constant bridge current (I_b) is applied, then the pressure sensitivity is defined as the change of differential output voltage per unit pressure and per unit bridge current (expressed in e.g. mV/mA bar):

$$S = \frac{\Delta V}{\Delta p} \cdot \frac{1}{I_b} = \frac{\Delta R}{\Delta p} \tag{3.3}$$

In the ideal case, the total resistance of each half-bridge and thus also of the total bridge is independent of pressure since the resistance changes cancel one another. Moreover common-mode effects, in particular temperature influences, are not felt at the differential bridge output. Indeed, a temperature rise increases the resistance of all piezoresistors equally, so that the output of the bridge remains zero. It is noted that this is only the case for a perfectly balanced bridge. It is also interesting to notice that at constant bridge voltage, the total current will vary with the temperature or, more practical to measure, for constant current bridge supply, the total bridge voltage will vary, so that a built-in temperature sensor is available for further compensation of temperature effects.

3.1.3 Resistance change as a function of stress

Based on the theory and data of chaper II, the resistance change can be calculated as a function of the membrane stress. It was shown that there is a contribution to resistance change from stresses that are longitudinal (σ_l) and transverse (σ_t) with respect to the current flow. Assuming that the membrane stresses are constant over the resistors, the total ΔR is thus calculated by

$$\frac{\Delta R}{R} = \sigma_l \pi_l + \sigma_t \pi_t \tag{3.4}$$

where π_l and π_t are the longitudinal respectively transverse piezoresistance coefficients. It is noted that dimensional changes are not taken into account in Eq.(3.4).

The orientation of the membrane is determined by its anisotropic fabrication (see chapter IV). The surface of the membrane is a <100> plane and the edges are intersections of <100> and <111> planes and are thus (110) directions. Hence, the orientation of the piezoresistors with respect to the silicon crystal is also (110). Table 2.1 tells us that the longitudinal piezoresistive coefficient in the (110) direction is $\pi_l = 1/2\,(\pi_{11} + \pi_{12} + \pi_{44})$ and the corresponding transverse coefficient is $\pi_t = 1/2\,(\pi_{11} + \pi_{12} - \pi_{44})$. From table 2.II we know that, for p-type resistors, π_{44} is by far more important than the other two coefficients. Equation (3.4) is thus approximated for p-type resistors by:

$$\frac{\Delta R}{R} = \frac{\pi_{44}}{2}\,(\sigma_l - \sigma_t) \tag{3.5}$$

For n-type resistors, π_{44} can be neglected, and we obtain:

$$\frac{\Delta R}{R} = \frac{\pi_{11}+\pi_{12}}{2} (\sigma_l + \sigma_t) \quad (3.6)$$

It is noted that expressions (3.5) and (3.6) are only valid for uniform stress fields or if the resistor dimensions are small compared to the membrane size. For small pressure sensors the stresses will vary over the resistors and have to be integrated. That is done by simulation programs like SENSIM which will be discussed later.

Considering the values of the piezoresistive coefficients (Table 2.II), it is easily calculated from Eq. (3.5) and (3.6) or seen in Figure 2.5 that for the crystal orientations (110), which are imposed by the membrane fabrication, a two to three times higher pressure sensitivity is reached with p-type than with n-type resistors. For low doping concentrations and at room temperature, the exact values are 72 and 31 respectively for the longitudinal piezoresistance coefficients, and -66 and -18 respectively for the transverse coefficients (all coefficients are expressed in 10^{-11} Pa^{-1}). Hence, in spite of the fact that the maximum longitudinal coefficient in the <100> plane (Fig. 2.5) is larger for n-type than for p-type silicon, p-type resistors are preferable since their coefficients have a maximum in the (110) direction, whereas the n-type coefficients have exactly a minimum in that direction.

3.2 Membrane stress calculation

3.2.1 Basic equations

In chapter II and in the previous section, the transduction from membrane stress to electrical signal was explored. Now the transformation from applied pressure to membrane stress will be discussed, to complete the pathway from pressure to electrical signal, via expressions (3.5 or 3.6). The standard reference for this purpose is the book from Timoshenko "Theory of Plates and Shells" [8]. This section summarizes some useful basic calculation tools from this book and gives important conclusions for the fabrication of pressure sensors.

Timoshenko's book includes the treatment of pure bending of uniform plates under lateral loads, e.g. pressure. If the deflections are very small compared to the membrane thickness, the problem can be solved analytically for some situations. The following assumptions have to be adopted :

- There is no deformation in the middle plane of the plate. This plane remains neutral during bending.
- Points of the plate lying initially on a normal-to-the -middle plane of the plate remain on the normal-to-the-surface after bending. In other words, the

effect of shear forces on the deflection of the plate are not considered.

- The normal stresses in the direction transverse to the plate can be disregarded

The solution of the problem starts with the calculation of the deflection of the plate in function of the position on the membrane w(x,y), under a given pressure p. Based on Hooke's law, the differential equation describing this situation can be derived for an infinitessimal part of the membrane, which is shown in Figure 3.3. The result is:

$$\frac{\partial^4 w}{\partial x^4} + \frac{\partial^4 w}{\partial x^2 \partial y^2} + \frac{\partial^4 w}{\partial y^4} = \frac{p}{D} \tag{3.7}$$

D is the flexural rigidity defined as

$$D = \frac{E\,h^3}{12\,(1-\nu^2)} \tag{3.8}$$

E is Young's modulus, ν is Poisson's ratio and h the membrane thickness. The first step is thus to solve Eq. (3.7) for the boundary conditions that are imposed by the configuration under study.

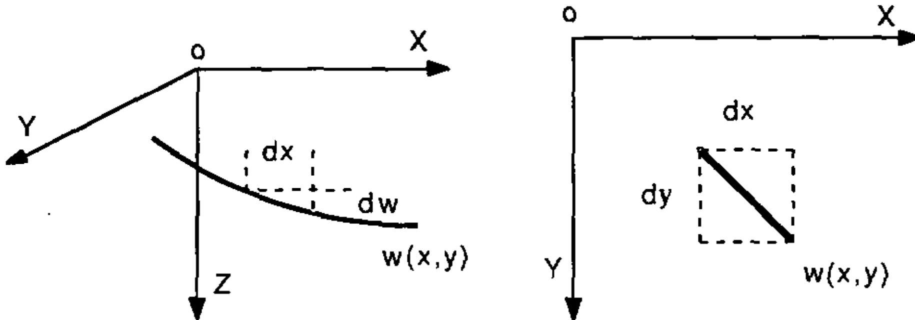


Fig. 3.3 Definition of the differentials used in the calculation of the deflection of the membrane.

The second step is the calculation of the bending moments based on the expression for the deflection calculated in the first step:

$$M_x = -D\left(\frac{\partial^2 w}{\partial x^2} + \nu\,\frac{\partial^2 w}{\partial y^2}\right) \qquad M_y = -D\left(\frac{\partial^2 w}{\partial y^2} + \nu\,\frac{\partial^2 w}{\partial x^2}\right) \tag{3.9}$$

Finally the knowledge of the bending moments allows to calculate the stress distribution. The stress profile in the z-direction is triangular: stress is zero at the middle plane and rises linearly to its maximum value at the surface. This maximum value is calculated for each position as:

$$(\sigma_x)_{max} = \frac{6\,M_x}{h^2} \qquad (\sigma_y)_{max} = \frac{6\,M_y}{h^2} \tag{3.10}$$

For any given situation, the stresses can be calculated by applying these three steps: membrane deflection / bending moments / stress. We are interested in the calculations for a membrane with built-in edges. This a rather complicated problem. However, an elegant solution exists, based on the calculation of simply supported plates. Therefore, the solution of this problem is first discussed here.

3.2.2 Simply supported rectangular plates

The equations (3.7) to (3.10) can be solved analytically for circular membranes. For rectangular or square membranes, which are obtained by anisotropic etching of silicon and which we are interested in here, the situation becomes more complex. For simply supported rectangular plates, Timoshenko proposes a semi-analytical solution to calculate the defection $w_{ss}(x,y)$ as a function of position on the membrane.

The boundary conditions for this case are:

$$w_{ss} = 0 \qquad \text{and} \qquad (M_x = 0 \quad \text{or} \quad M_y = 0) \tag{3.11}$$

Using Eq.(3.7) Timoshenko first calculates the deflection of a rectangular plate under a sinusoidal load instead of a uniform pressure. Then he represents the uniform pressure load in the form of a double trigonometric series (Navier solution). The deflection of the plate takes the form of a double series of trigonometric functions, each of which is the solution of one of the sinusoidal functions that constitutes the uniform pressure. The double series for a pressure p is:

$$p = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} a_{mn} \sin \frac{m\pi x}{a} \sin \frac{m\pi y}{b} \tag{3.12}$$

with a and b the side lengths of the membrane and

$$a_{mn} = \frac{16\,p}{\pi^2 mn} \tag{3.13}$$

An analytical solution for the deflection of a rectangular membrane under pressure is then given by

$$w_{ss}(x,y) = \frac{16\,p}{\pi^6 D} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\sin \frac{m\pi x}{a} \sin \frac{n\pi y}{b}}{mn \left(\frac{m^2}{a^2} + \frac{n^2}{b^2}\right)^2} \qquad (m,n = 1, 3, 5, \dots) \tag{3.14}$$

The stresses are further calculated by means of Eq. (3.9) and (3.10). It is reminded that, in order to apply the superposition prinicple, linearity and thus small deflections have to be assumed to apply this method.

Alternatively, for simply supported rectangular plates the simple-series method of Lévy can be used in stead of the double-series of Navier. The solution is a priori defined as a series of the form

$$w_{ss}(x,y) = \sum_{m=1}^{\infty} Y_m(y) \sin \frac{m\pi x}{a} \tag{3.15}$$

and the functions $Y_m(y)$ are determined so that Eq. (3.15) satisfies the equation of the deflection surface Eq. (3.7) and the boundary conditions of Eq. (3.11). The result is:

$$Y_m(y) = \frac{4pa^4}{\pi^5 D} \frac{1}{m^5} \left(1 - \frac{\alpha_m \tanh \alpha_m + 2}{2 \cosh \alpha_m} \cosh \frac{2\alpha_m y}{b} + \frac{\alpha_m}{2 \cosh \alpha_m} \frac{2y}{b} \sinh \frac{2\alpha_m y}{b} \right) \tag{3.16}$$

where $m = 1, 3, 5, \ldots$ and $\alpha_m = \frac{m\pi b}{2a}$

3.2.3 Rectangular plates with built-in edges

For rectangular plates with built-in edges, the deflection of simply supported plates, $w_{ss}(x,y)$ given by the double-series method (Eq. 3.14) or by the simple-series (Eq. 3.15), is superposed on the deflection of the plate by moments distributed along the edges, $w_m(x,y)$, schematically shown in Figure 3.4:

$$w(x,y) = w_{ss}(x,y) + w_m(x,y) \tag{3.17}$$

These moments are adjusted so as to satisfy the boundary conditions for clamped plates:

$$w = 0 \qquad \text{and} \qquad \frac{\partial w}{\partial n} = 0 \tag{3.18}$$

n is the direction perpendicular to the edge.

With this method, the bending moments along the clamped edges are calculated. For a square membrane, the maximum of the absolute value af these moments is at the middle of the sides of the square. The result is given by

$$M_{max} = \mu_m \, p \, a^2 \tag{3.19}$$

where a is the membrane side length and μ_m depends on the number of series terms that are taken into account. For m=7, $\mu_m = 0.0517$.

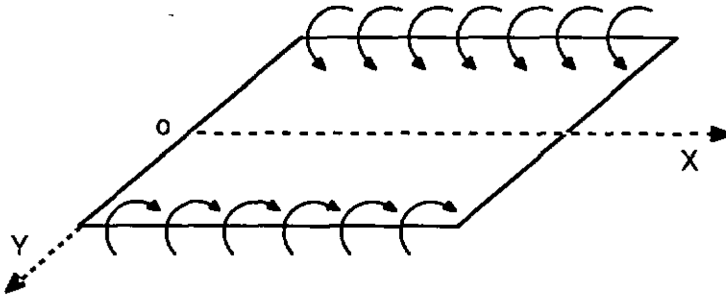


Fig. 3.4 Schematic representation of a plate deflected by moments that are uniformly distributed along the edges.

Combining Eq. (3.10) and (3.19), it is found that the surface stress in the middle of the sides of the membrane is (for m=7):

$$(\sigma_x)_{max} = 0.31\, p \frac{a^2}{h^2} \qquad (3.20)$$

The very important conclusion form Eq. (3.20) is that the stress and thus the pressure sensitivity of piezoresistive pressure sensors are proportional to the square of the ratio membrane side to membrane thickness. For maximum sensitivity, a/h should be chosen as high as possible. If very small sensors are required, the sensitivity loss due to the reduced membrane dimensions can be compensated by making the membrane thinner. Further, it will be very important to control both the side length and the thickness precisely in order to limit sensitivity variations from sensor to sensor.

3.2.4 Computer simulation

All the foregoing calculations are suitable for computer simulations. If the silicon membrane is covered with one or more layers of other material (an oxide or passivation layer e.g.), which is very common for pressure sensors, it is more convenient to solve the basic differential equations numerically by means of the finite difference method. A computer program, SENSIM, was written for this purpose by K.W. Lee [9, 10]. The program uses the finite difference method for general cases and the faster double-series method for the special case where the membrane is a single layer. In order to obtain the resistance change as a function of applied pressure, the deflection and stress are calculated as a function of the position on the membrane, and the stress is integrated over the region defined by

position on the membrane, and the stress is integrated over the region defined by the piezoresistor, which yields an average longitudinal and transverse stress. These stresses are then combined with the corresponding piezoresistance coefficients according to Eq. (3.3).

As shown in Figure 3.1, the transition between membrane and rim is not abrubt, so that the border of the rim will also undergo some deformation when pressure is applied. Hence the boundary condition of the membrane is something between simply-supported and built-in. SENSIM introduces a variable in the stress equations to take this condition into account. Large and thin membranes will approach the simply-supported condition; small and thick membrane are closer to the built-in situation. Finally it is noted that SENSIM also provides the possibility to calculate temperature effects and additional stress conditions caused by packaging.

SENSIM only uses the linear theory, i.e. only small deflections can be calculated adequately. For thin membranes, normal membrane stresses become important, as discussed in the next section, and the surface stress is no longer linear with applied pressure. Recently, powerful general purpose finite-element software has appeared on the market, which could be adapted for sensor design. An example for capacitive sensors is given in [11]. Such programs could include a non-linear stress analysis for accurate mechanical simulation.

Eq. (3.4) has indicated that, at first approximation, (σ_l - σ_t) determines the resistance change for p-type resistors. Figure 3.5 gives an idea of the distribution of this stress difference as a function of postion on a square silicon membrane. If the resistor position of Fig. 3.2 is kept in mind, Fig. 3.5. confirms that resistance changes are equal at opposite edges and opposite in sign between touching edges. It is also clear that the maximum stress is in the middle of the edges and that the stress decreases rapidly (concave slope) towards the center of the membrane and less rapidly (convex slope) towards the corners.

3.2.5 Non-linearity and the Balloon-effect

In the previous section it was shown that the sensitivity of pressure sensors can be increased by designing membranes with a high ratio of side length to thickness. The upper limit of this ratio is imposed by the required linearity of the pressure response. For very thin membranes, the deflections will no longer be small compared to the membrane thickness, and the first assumption of 3.2.1 is no longer valid, i.e. the middle plane of the membrane will no longer be neutral. This situation is referred to as "Balloon effect" [7, 8, 13], since the middle plane is stretched like a balloon. Apart from the linearity, the Balloon effect also affects

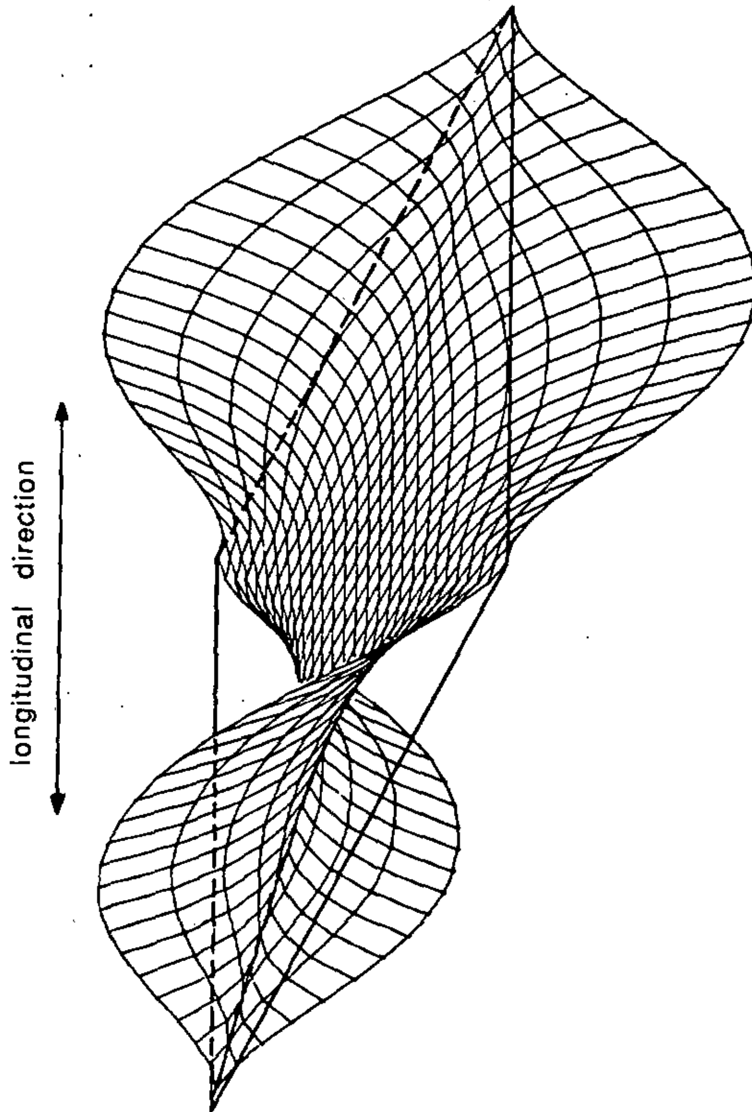


Fig. 3.5 (σ_l - σ_t) *stress distribution as a function of position on a square membrane that is bent down and for the indicated resistor orientation [17].*

the symmetry of the pressure response for positive or negative pressures, as illustrated by Figure 3.6. The tensile s tress from the Balloon effect has to be added to the stress caused by pure bending. This increases the response when the membrane is bent down (traction) and decreases the total stress on the piezoresistor when the membrane is bent up (compression). Hence, there is a difference in sensor output when the same (relatively large) pressure is applied to either side of the membrane. The difference in surface stress between the two cases is twice the stress due to the Balloon effect.

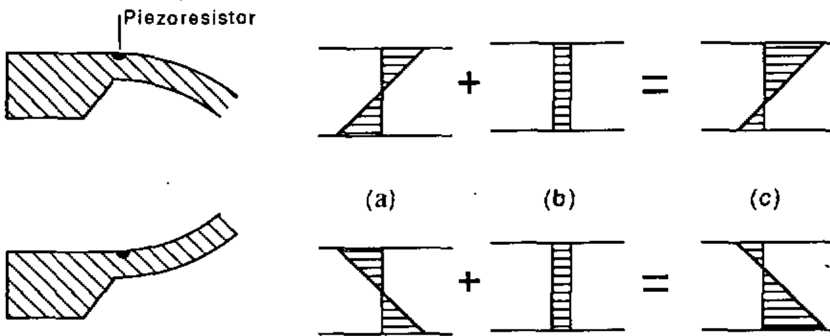


Fig. 3.6 Schematic representation of the assymmetry introduced by the Balloon effect for pressure differences across the membrane that are equal in amplitude, but opposite of sign. (a) Stress profile in the cross-section of the piezoresistor for pure bending, (b) Tensile stress caused by the Balloon effect, (c) Total stress; the difference at the membrane surface between both situations is twice the tensile stress caused by the Balloon effect.

Timoshenko calculated the deformation of large plates with clamped edges by means of the method of virtual displacements [8]. Figure 3.7 shows the resulting stress as a function of pressure, at the middle of the side of a square membrane with side length a, compared to the linear stress dependence given by the theory for small deflections. The pressure is expressed as a dimensionless load factor pa^4/Dh, and the stress is normalized to $\sigma a^2(1-\nu^2)/Eh^2$. Departure from linearity is seen to occur at a load factor of roughly 50. If this number is taken as guideline, and using Eq. (3.8), a maximum a/h ratio can be calculated to design a pressure sensor for a given pressure range, with maximum sensitivity:

$$\left(\frac{a}{h}\right)_{max} = \left(4.2\frac{E}{1-\nu^2}\frac{1}{p_{max}}\right)^{1/4} \tag{3.21}$$

If 1.69 10^{11} Pa is taken for Young's modulus for (110) silicon and 0.279 for Poisson's ratio [12], then Eq. (3.21) is approximated by:

$$\left(\frac{a}{h}\right)_{max} = 935\ p_{max}^{-1/4} \qquad (p_{max} \text{ in Pa}) \qquad (3.22)$$

For a pressure sensor for e.g. 1 bar (10^5 Pa), the optimal a/h ratio would be about 50. This ratio was adopted as design rule to determine the thickness of the silicon membrane, the side lenth being imposed by the intended application. Indeed, the pressure sensor was designed to be mounted in a heart catheter of diameter 5F (outer diameter: 1.67 mm). The chip width was therefore limited to 1.1 mm. Taking into account the width that is lost by the <111> slopes of the etched hole, the membrane side was defined at 520 μm. Respecting the a/h ratio of 50, the membrane thickness was designed to be 10 μm. In Chapter 5 it will be shown that this thickness gives a non-linearity of 0.2 % to 0.8 bar.

It is noted that also the piezoresistance coefficients show non-linearity with applied pressure [13,14]. However, this effect has not been considered here.

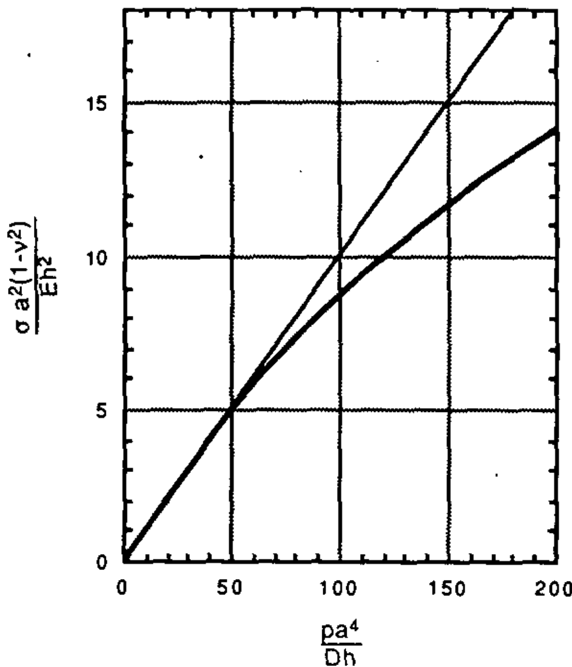


Fig. 3.7 Stress at the middle of the edge of a square membrane with side a. Comparison between the linear theory for small deflections and the calculations that take the Balloon effect into account [8].

3.3 Geometrical design of the piezoresistive structure

3.3.1 General design considerations

In this section, the dimensions of the piezoresistors and their position on the thin silicon membrane will be discussed. These will be chosen as a compromise between maximum pressure sensitivity and an other requirement that is important to consider, i.e. the expected fabrication reproducibility.

Most pressure sensors with square membranes [15-17] have four piezoresistors disposed at the four edges of the membrane, as schematically shown in Figure 3.2. The exact lay-out however varies. The first design rule is evidently to locate the resistors as close as possible to the middle of the membrane edges, since that is where the stresses are maximal (cfr. Fig. 3.5). From this central point, stress decreases more rapidly towards the center of the membrane than towards the corners, so that the perpendicular resistors are likely to be less pressure sensitive than the parallel ones. To preserve the Wheatstone bridge symmetry, the parallel resistors have to be removed from the edge until equal sensitivity is obtained, giving rise to a certain sensitivity loss. For very small membranes, the sensitivity loss can be quite important. In that case it is advisable to cut the perpendicular resistors in two parts, as shown in Figure 3.8 (D1). Alternative lay-outs are possible where both the perpendicular and the parallel resistors consist of two or three parts (Fig. 3.8 D2, D3 and D4).

A second design consideration is the minimum allowable distance between the resistors and the membrane edge. This parameter is limited practically by the fabrication reproducibility of the membrane. Normal commercially available three inch silicon wafers have a thickness reproducibility of ± 8 μm. Since electrochemical etch-stop is used, all membranes are etched from the backside to exactly the same thickness. However, because of wafer thickness variations, the etched holes will be deeper for some membranes than for others, and the

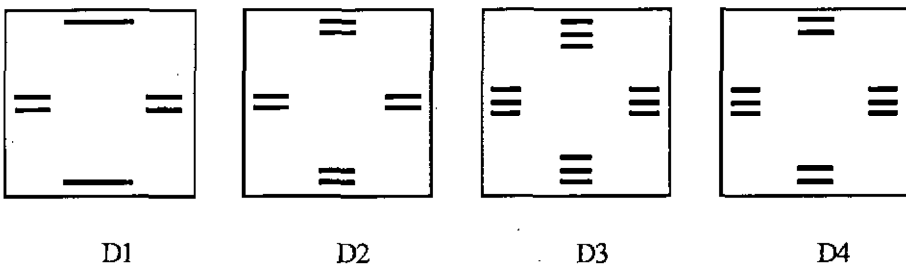


Fig. 3.8 Alternative lay-outs of the piezoresistors, used for computer simulations.

pyramidal structure formed by the <111> slopes of the holes will be more or less closed, depending on the etched depth. Together with alignment errors of the etch mask with respect to the silicon crystal orientation, the membrane side variation was experimentally found to be typically ±10 µm. Thus the nomininal distance between membrane edge and piezoresistor has to be at least 10 µm, especially for the piezo-resistors that are placed paralel to the membrane edge.

3.3.2 Computer simulations

With the dimensional restrictions of the previous section, the four proposed designs of Figure 3.8 have been simulated with SENSIM. Each alternative was calculated for two distances between membrane edge and resistors: 10 µm and 20 µm (groups 1 and 2 in Table 3.1 respectively). All dimensions and distances are defined in Figure 3.9 and listed in Table 3.1.

The width of the resistors was fixed at 10 µm, and the length was calculated so as to obtain 10 squares for all resistors. The resistance was defined to be 2000 kΩ, which corresponds to a sheet resistivity of 200 Ω/square (see section 3.5). The sensitivity calculated for each lay-out by SENSIM is listed in the last row of Table 3.1. Comparing group 1 to group 2, it is seen that a displacement of 10 µm towards the middle of te membrane reduces the sensitivity by about 20 %. The first design (D1 in Fig. 3.8) was about 17 % more sensitive than the other three lay-outs, for both groups. Hence the design with two parallel resistors and two times two perpendicular half-resistors was chosen for further development.

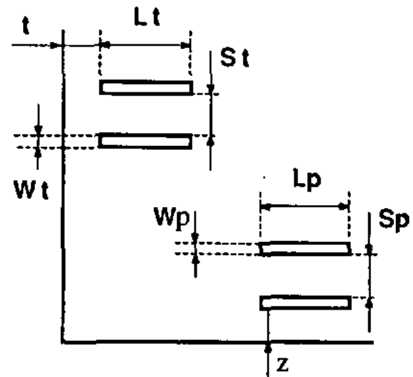


Fig. 3.9 Definition of the distances and dimensions for the different piezoresistor lay-outs shown in Fig. 3.8 and listed in Table 3.1

Three variations of this design were realized, in order to investigate the influence of dimensional parameters on the reproducibilty of the sensor specifications. The three designs are given here; the effects on the specifications will be discussed in Chapter 5, Sensor Characterization. The dimensions and distances of the three lay-outs are summarized in Table 3.II. The first topic to investigate was the influence of the resistor dimensions. Therefore, in design A, the resistor width was set to 20 µm instead of 10 µm. The parallel resistors are 20

Table 3.1 Position and dimensions for the simulated piezoresistor lay-outs. D1, D2, D3 and D4 refer to the lay-outs presented in Fig. 3.8; the symbols in the first column refer to Fig. 3.9. All dimensions are in micrometer. In Group 1, the distances between resistors and membrane edge are 10 µm; in Group 2 they are 20 µm. The last row gives the pressure sensitivity as calculated by SENSIM, in mV/V bar.

	Group 1				Group 2			
	D1	D2	D3	D4	D1	D2	D3	D4
z	10	10	10	10	20	20	20	20
t	10	10	10	10	20	20	20	20
W_p	10	10	10	10	10	10	10	10
W_t	10	10	10	10	10	10	10	10
L_p	100	50	50	75	100	50	50	75
L_t	50	50	50	50	50	50	50	50
S_p	-	30	30	30	-	30	30	30
S_t	20	30	30	30	40	30	30	30
Sens.	17.6	15.1	14.9	15.0	14.3	12.3	12.2	12.2

µm from the membrane edge. Evidently, this lay-out produces a lower pressure sensitivity, since the perpendicular half-resistors are so long (100 µm) that they come rather close to the center of the membrane. In order to limit the sensitivity loss they are allowed to touch the edge (t=0). Designs B and C keep the smaller resistors (10 µm wide).

A second question was the actual influence of the distance between membrane edge and the resistors on the reproducibility of the output parameters. Therefore, designs B and C have equal resistor dimensions but they are closer to the edges in design C, which results in a higher sensitivity. It was expected, however, that design C would be more sensitive to variations of the membrane size. In fact, in Chapter 5 it will be shown that the reproducibility of pressure sensitivity is not

much different for the three designs, so that, for this criterion, design C would be the preferred configuration because of its higher pressure senitivity.

Table 3.II Position and dimensions of the piezoresistor lay-outs that have been fabricated based on design D1

	A	B	C
z	20	20	10
t	0	15	5
W_p	20	10	10
W_t	20	10	10
L_p	200	100	100
L_t	100	50	50
S_t	40	40	40
Sens.	13.1	15.1	18.3

3.3.3 Cross-connection of the half-resistors

The perpendicular half-resistors have to be connected at their "internal" ends This section describes the different lay-outs that have been realized for this connection. The incentive to develop successive lay-outs was mainly the reduction of Wheatstone bridge offset, i.e. the improvement of resistor matching. Therefore the discussion on the characterization of the sensor (Chapter 5) is anticipated here for this parameter in order to explain and motivate the lay-out adjustments.

The cross-connections of the perpendicular half-resistors should not be stress-sensitive since, being oriented at a right angle to the rest of the resistor, it would decrease the pressure sensitivity of the total resistor. Therefore, in the first sensor generation, it consisted of a high boron diffusion covered by aluminum. After fabrication, the Wheatstone bridge outputs for zero pressure for designs A, B and C were measured to be typically 20, 40 and 60 mV/V respectively (mV differential output voltage per volt applied to the bridge). This large offset was evidently caused by a mismatch of the piezoresistors. This mismatch was found to be due to the small additional resistance of the cross-connection between the two perpendicular half-resistors. A new cross-connection was then designed as illustrated in Fig. 3.10 (only design A is shown here). The half-resistors were connected by a large p-doped region of the same concentration as the piezoresistors. To keep the same total resistance as the parallel resistors (10 squares), the p-connection was made of one large square and the two half-resistors of 4.5 squares. Computer simulations with SENSIM showed that, without changing anything else, the sensitivity would decrease by only 1.5 %. This new design was implemented in a second generation of pressure sensors, without succes however: the offsets for designs A, B and C were worse than before: 50, 70 and 70 mV/V respectively. It is indeed not evident to estimate the effective

resistance of the U-structure presented in Fig. 3.10, since no design rules exist for this situation.

It was, of course possible to adapt the U-design until all resistors would be equal, but, rather than optimizing this approach, it was decided to keep the cross-connections of the first generation of sensors and to introduce them also in the parallel resistors, in order to obtain a symmetrical lay-out for all resistors. This third-generation layout is shown in Fig. 3.11. The paralel resistors are cut in two parts, but still placed on one line (and not side by side) so as to keep them on high membrane stress regions. With this lay-out, the offset was reduced to about 5 mV/V for the three designs, which was an enormous improvement compared to the previous generations. The obtained offset will be discussed in more detail in Chapter 5.

3.3.4 Wafer lay-out

The sensors were fabricated on three-inch wafers which were divided in 54 cells. Each cell contained a sensor of each design type of Table 3.II and a test structure for membrane fabrication control, i.e. a supplementary membrane without resistors, on which the etched depth and resulting membrane thickness could be measured.

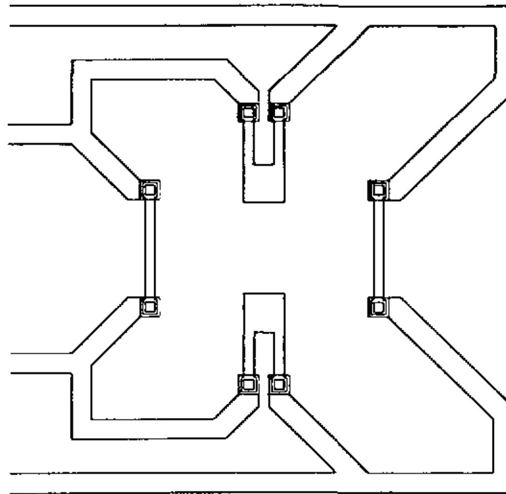


Fig. 3.10 Lay-out of the second generation of pressure sensors.

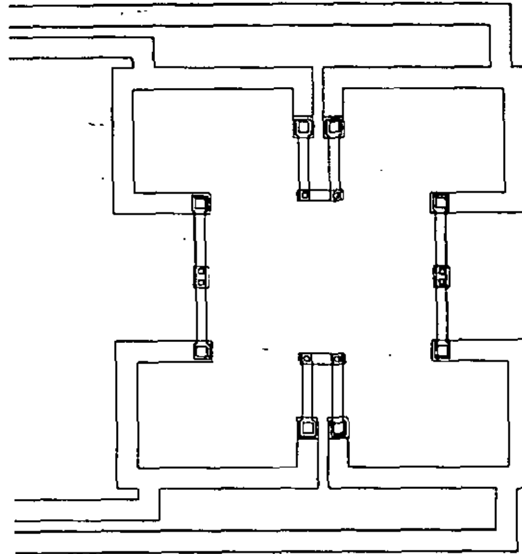


Fig. 3.11 Lay-out of the third generation of pressure sensors.

3.4 Technological design of the piezoresistors

3.4.1 Implanted versus diffused resistors

The piezoresistors can either be diffused or implanted into the silicon membrane. The difference lies in the depth and the shape of the concentration profile. By ion implantation, the resistors can be made more shallow and with a steeper concentration profile. Advantages of implanted resistors are:

- better control over the processing parameters and thus better reproducibility of the resistors
- higher sensitivity to applied pressure, due to the shallow junction
- better control of temperature behaviour

The first advantage is known from electronic circuit technology and will not be further treated here. It is just reminded that good matching of the piezoresistors is important to reduce the offset of the Wheatstone bridge output. The sensitivity improvement is especially notable for thin membranes. For a 10 μm thick membrane, stress decreases from its maximal value at the surface to zero at the middle plane (linear theory), which is 5 μm under the surface. This is so small that the decrease of stress as a function of depth over the resistor junction is not negligible. Hence, much sensitivity is gained if the resistor is limited to the layers of maximal stress close to the surface. It is known that, for equal sheet resistance,

implantation can yield a more shallow junction than deposition and diffusion, giving thus a higher pressure sensitivity for implanted resistors. The temperature effect finally has been discussed in the previous chapter and is related to the concentration profile. In a deep profile, there is a more important contribution of resistor layers with low concentration and thus high temperature dependence. Where for Gaussian doping profiles the temperature coefficient only depends on the surface concentration (see Chapter 2 and Fig. 2.12), a lower temperature is obtained with a doping profile that decreases more rapidly than the Gauss function. This, again, is the case for implanted resistors. For all these reasons it was decided to fabricate the piezoresistors by ion implantation.

3.4.2 Definition of the implantation parameters

Boron was used as dopant, since it was shown in section 3.2.3 that p-type resistors yield a higher pressure sensitivity for the given silicon crystal orientation. A doping concentration of 10^{19} atoms/cm^3 was chosen for the piezoresistors, as a compromise between high piezoresistance coefficient and low temperature coefficient (see Chapter 2 and Fig. 2.9). The sheet resistance was chosen 200 Ω/square. With 10 squares per resistor, as proposed in the previous section, the total resistance will be 2 kΩ for each piezoresistor.

To determine the fabrication parameters for the implantation, computer simulations were carried out using SUPREM and ICECREM. Based on these simulations, six samples were prepared on three-inch wafers. The wafers were phosphorous doped and had a resistivity of 3 to 5 Ωcm. Boron was implanted with an implantation energy of 40 keV and three different implantation doses. One set of samples had no oxide before implantation and one set had an oxide of 440 Å. Table 3.III summarizes the fabrication parameters of the six samples.

Table 3.III Fabrication parameters of six test wafers for boron implantation

Wafer nr.	Oxide before implantation (Å)	Energy (keV)	Dose (at/cm^2)	Thermal treatment after implantation
81	no	40	$8.0\ 10^{14}$	at 950 °C: 30 min. dry oxide 16 min. wet oxide
101	no	40	$1.0\ 10^{15}$	
121	no	40	$1.2\ 10^{15}$	
081	440	40	$8.0\ 10^{14}$	at 950 °C: 30 min. dry oxide 16 min. wet oxide
0101	440	40	$1.0\ 10^{15}$	
0121	440	40	$1.2\ 10^{15}$	

In order to compare the computer simulations to the effective specifications, the junction profiles of the samples have been measured by spreading-resistance. This method involved polishing the sample under a small angle so that the whole junction came at the surface, spread out over a large strip, and then measuring the resistivity with two or four probes on consecutive points on a line at a right angle to this strip. The measured resistivities were calculated back to the doping concentration profile. This method allowed to determine the junction depth very accurately. Alternatively, the junction depth was determined by a Calotest (i.e. wearing out a spherical hole by means of a metal ball covered with diamond paste, staining the sample, measuring the diameters of the obtained ring structure with an optical microscope and calculating the corresponding junction depth). Finally the sheet resistance has been measured on several spots on each wafer by a four-point-probe and avaraged.

Table 3.IV displays the results of all these measurements and calculations for four samples: the three without oxide before implantation and one with oxide. The measurements were seen to be in reasonable agreement with the computer simulations. Figure 3.12 shows the doping profiles calculated by SUPREM and measured by Spreading Resistance for sample 81. The maximum concentrations corresponded very well: about 1.5 10^{19} at/cm^3. The decrease in boron concentration at the surface was less pronounced than predicted by SUPREM. The measured junction depth, 0.55 μm, was less than calculated by SUPREM, and the

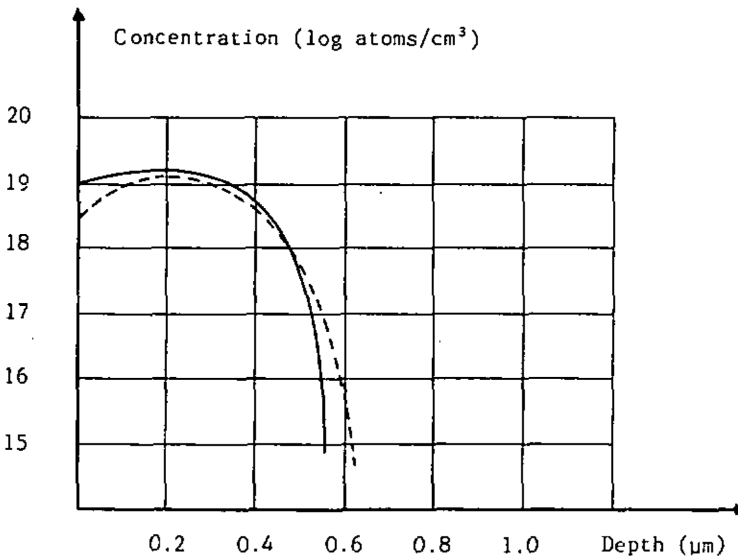


Fig. 3.12 SUPREM simulation (- - -) and spreading-resistance measurement (——) of the doping profile of sample 81.

junction profile was even steeper than calculated, which, as discussed before, was an advantage. The implantation type of sample 81 corresponded best to the required specifications: 200 Ωcm resistivity, 10^{19} at/cm^3 boron concentration and a shallow junction. Hence, the parameters used for the boron implantation of the piezoresistors were an energy of 40 keV and a dose of 8 10^{19} at/cm^2 , without oxide before implantation.

3.5 Fabrication process

The pressure sensors were fabricated on double-side polished, three inch wafers of 380 μm thick. They were boron doped and had a resistivity of 3-5 Ωcm. First a 10 μm thick epitaxial layer was grown. This layer had a low phoshorous doping concentration (10^{15} at/cm^3). It was required to fabricate the membranes by electrochemical etch-stop, as will be explained in Chapter 4. The wafers were thermally oxidized to 1.5 μm (wet oxide) to serve as masking material for the etching of the membranes from the back side (see also Chapter 4). After diffusion of the p^+ regions, the top oxide was removed and a new oxide was grown and patterned for boron implantation of the piezoresistors into the n-type epitaxial layer, according to the specifications given in the previous section. Electrical connections were made using standard aluminum metallization. The chips were protected with a passivating CVD oxide.

In Chapter 4 it will be proved necessary to provide an electrical contact to the n-type epitaxial layer in order to provide an electrochemical etch-stop. This was realized by a high phosphorous diffusion and Al contact. Alternatively, the additional processing steps for this contact could be avoided by using the metallization of the sensor itself. For electrochemical etch-stop, a positive voltage was applied to the epitaxial layer; the diode formed by the p+ diffusion for the piezoresistors and the n-type substrate was in forward bias mode when a positive voltage was applied. Thus it formed no barrier for the etch-stop current. The voltage drop across this diode merely had to be added to the passivation potential that was applied. In addition, an electrical contact to the p-substrate was needed for four-electrode etch-stop. For this purpose, 2 holes of 5 mm x 5 mm were etched through the epitaxial layer and aluminum was deposited and alloyed. Alternatively boron was diffused through the epitaxial layer and covered with aluminum to provide an electrical contact to the p-type substrate.

After completion of the piezoresistive structure, 1050 μm x 1050 μm square openings were patterned and etched in the back-surface oxide. Alignment of the openings to the top resistors was accomplished by means of a double-sided mask

Table 3.IV Measurements and computer simulations for boron implantation on four test wafers. The listed parameters are junction depth (x_j), sheet resistivity (ρ_s), surface concentration (C_s) and implanted dose (Q_A). Measurements were done by spreading-resistance (SR), Four-Point-Probe (FPP) and Calotest (CT).

	x_j (μm)	ρ_s (Ω/□)	C_s (cm^{-3})	Q_A (cm^{-2})
Sample 81, dose = 8.0 10^{14} cm^{-2}, no oxide				
Suprem	0.64	181	3.3 10^{18}	4.8 10^{14}
Icecrem	0.72	179	3.1 10^{18}	5.1 10^{14}
SR	0.55	151	8.9 10^{18}	6.1 10^{14}
CT/FPP	0.54	218-230	-	-
Sample 101, dose = 1.0 10^{15} cm^{-2}, no oxide				
Suprem	0.67	151	4.1 10^{18}	6.0 10^{14}
Icecrem	0.73	150	3.8 10^{18}	6.3 10^{14}
SR	0.66	114	1.1 10^{19}	8.4 10^{14}
CT/FPP	0.54	182-190	-	-
Sample 121, dose = 1.2 10^{15} cm^{-2}, no oxide				
Suprem	0.69	129	4.8 10^{18}	7.2 10^{14}
Icecrem	0.75	129	4.5 10^{18}	7.5 10^{14}
SR	0.64	111	1.4 10^{19}	8.8 10^{14}
CT/FPP	0.54	167-170	-	-
Sample 0101, dose = 1.0 10^{15} cm^{-2}, 440 Å oxide				
Suprem	0.54	148	1.1 10^{18}	6.4 10^{14}
Icecrem	0.62	146	5.3 10^{18}	6.7 10^{14}
SR	0.55	130	3.3 10^{18}	7.6 10^{14}
CT/FPP	0.54	198-205	-	-

aligner. The size of the openings was calculated so that the final membrane geometry after etching was 520 µm x 520 µm. The membranes were etched anisotropically in potassium hydroxide, while protecting the front-side from the KOH by clamping the wafer in a chuck that only leaves the back-side exposed to the etch solution. The etch process will be explained in detail in Chapter 4.

Table 3.V summarizes the fabrication sequence of the pressure sensors. The process requires 7 masks. It is noted that the fabrication procedure is completely compatible with standard microelectronic processes, except for the last step: the etching of the membranes. Figure 3.13 shows a picture of both sides of the sensor, fabricated with this process.

At Ascom Favag Microelectronics, a bipolar process in (100) silicon has been developed and characterized, to integrate the piezoresistive sensor and electronic circuitry on one chip. The process steps are illustrated in Figure 3.14 [18].

Fig. 3.13 Photograph of both sides of the sensor chip.

Table 3.V Fabrication sequence of the piezoresistive pressure sensors

Step	Process	Mask
1	Epitaxial layer growth, 10 μm, P-doped 10^{15} at/cm^3	
2	Wet oxidation, 1.5 μm	
3	Photolithograpy and oxide opening for p^+ regions	Mask 1
4	Predeposition boron (p^+ conductors)	
5	Removal of oxide layers	
6	Boron diffusion + oxidation (5000 Å)	
7	Photolithograpy and oxide opening for n^+ regions	Mask 2
8	Predeposition + diffusion n^+ (phosphorous)	
9	Photolithograpy and oxide opening for piezoresistors	Mask 3
10	Boron implantation	
11	Anneal piezoresistors + oxidation	
12	Photolithograpy and oxide opening for contacts	Mask 4
13	Aluminum evaporation	
14	Photolithography + etching Al	Mask 5
15	Aluminum anneal	
16	deposition of CVD passivation oxide	
17	Photolithography + oxide opening pads	Mask 6
18	Photolithography + oxide opening for membranes (back)	Mask 7
19	Membrane etching in KOH	

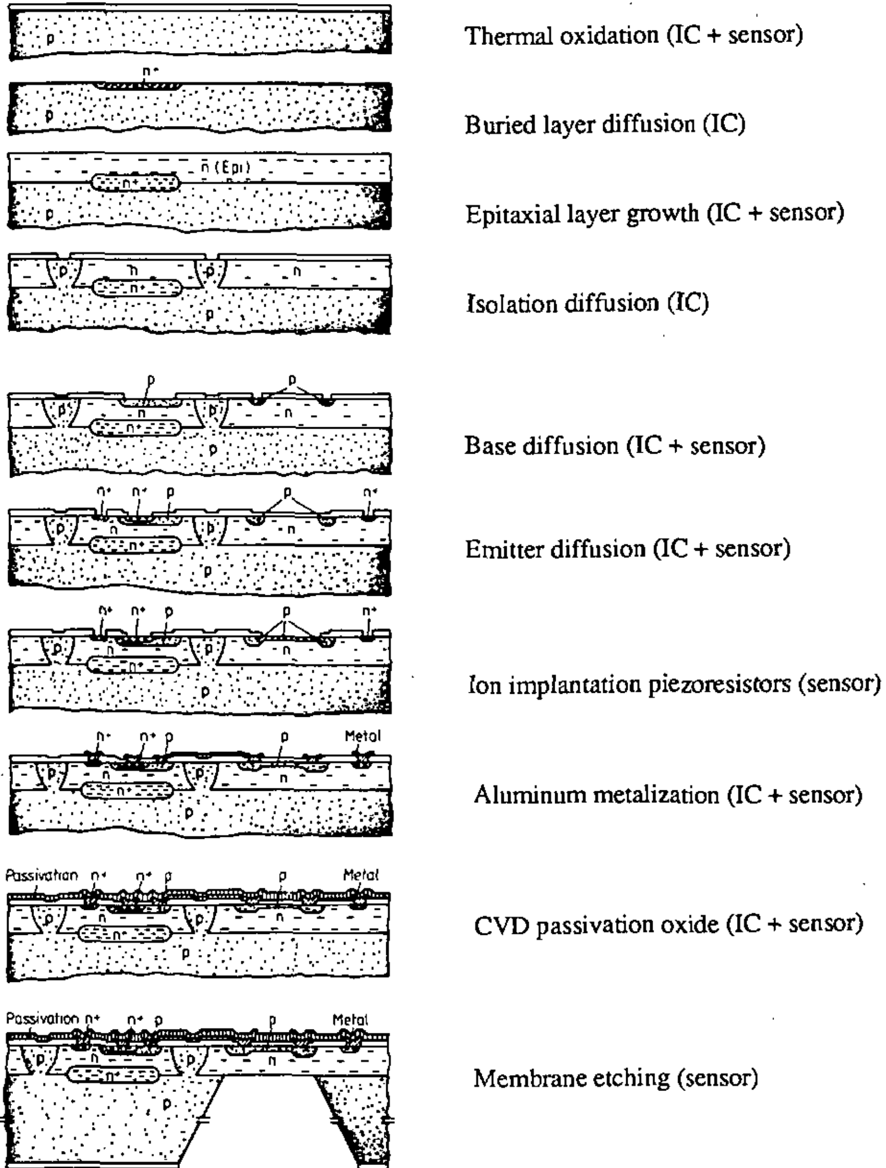
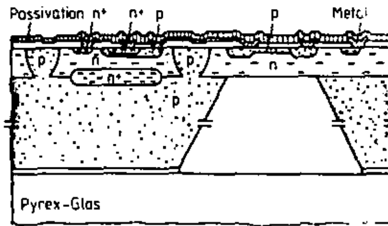


Fig. 3.14 Process sequence for the simultaneous integration of piezoresistive sensors and bipolar electronics [18] (continued on next page).



Bonding (sensor)

Fig. 3.14 Process sequence for the simultaneous integration of piezoresistive sensors and bipolar electronics [18] (continued from previous page).

3.6 Conclusions

In this chapter, the lay-out of the piezoresistive pressure sensor was presented: basically it consists of four piezoresistors disposed at the edges of a square silicon membrane. It was shown how the mechanical stress in the membrane can be calculated. An important conclusion could be drawn, that is, the stress in the middle of the membrane edge is proportional to the square of the membrane side (a) and inversely proportional to square of the membrane thickness (h). Hence, for maximum pressure sensitivity, the ratio a/h should be chosen as high as possible. The limit on this ratio is imposed by the non-linearity requirement. For very thin membranes, the stress will no longer be linear with applied pressure because of stretching of the membrane. This is called the Balloon effect. For a given membrane side of 520 μm, a thickness of 10 μm was taken as a compromise between pressure sensitivity and non-linearity. Aided by computer simulations, the position of the resistors on the membrane has been optimized. Three different designs were proposed and fabricated. The specifications of these three versions will be compared in Chapter 5. It was explained that better performances can be obtained with resistors fabricated by ion implantation than by deposition and diffusion. The optimal implantation parameters have been determined by computer simulations and by the fabrication and measurement of test samples. Based on these design features, the fabrication sequence has been presented and discussed. Etching of the membranes is the last fabrication step of the pressure sensors. Since a square relationship was found between the pressure sensitivity and the membrane dimensions, it is very important to achieve an accurate control of the membrane dimensions. The next chapter will explain how this goal is reached by electrochemical etch-stop.

Chapter 4
Membrane fabrication by means of electrochemical etch stop

4.0 Summary
4.1 Introduction
4.2 Bias-dependent etching of silicon
4.3 Electrochemical etch-stop on an epitaxial layer
4.4 Conclusions

4.0 Summary

Among the recently developed techniques for machining microscale mechanical components out of silicon, electrochemical etch-stop on a p/n junction shows some distinct advantages: it allows an easy and precise control of the dimensions of the fabricated devices without compromising the excellent mechanical properties of silicon. The thin membranes, and all related structures that can be conceived and created, are monocrystalline, robust and stress-free. Moreover they are low doped, so that integration of electronic components directly into them is feasible. This chapter consists of two parts. The first explores the electrochemical behaviour of silicon under electrical biases. The second part shows how the technique can be put into practise and reports its performance. Electrochemical etch-stop on an epitaxial layer results in better thickness control over the silicon membranes (±0.2 μm s.d.) and hence, improves the reproducibility of, in this particular application, piezoresistive
Parts of this chapter have been published in ref. [1, 2, 3, 4].

4.1 Introduction

Miniature mechanical components are fabricated in silicon for a wide variety of applications [5, 6], of which sensors and actuators take a large part. Silicon is sculptured using chemical etch products such as potassium hydroxide [7, 8], ethylenediamine/ pyrocatechol [9, 10] or hydrazine solutions [11, 12]. These etchants being anisotropic, well controlled three-dimensional shapes are obtained. Very often, however, etch times can be rather long, so that small variations in etch rate give rise to dimensional incertitude when only the chronometer is used to control the fabrication process. If very narrow fabrication tolerances are imposed on miniature mechanical components, the introduction of one or other etch-stop technique is imperative, i.e. a mechanism should be built in that stops the etch process when the required dimensions are reached, even if the devices remain exposed to the etchant. Several methods have been conceived and exploited successfully for this purpose, by either bulk or surface micromachining. In Chapter 1 it was mentioned that, apart from electrochemical etch-stop, two other methods are frequently used today: etch-stop on a highly doped layer [13] and sacrificial layer technology [14].

Many applications, including diffused or implanted piezoresistive pressure sensors, require the integration of electronic components on the microfabricated structure. This is excluded when using the high boron concentration etch-stop, since the layer is already too conductive. It is frequently done with the polysilicon approach, but then some of the excellent mechanical properties of monocrystalline silicon have to be traded off. Efforts have been reported to create inert layers burried into monocrystalline silicon. However, it is impossible to grow a good-quality epitaxial layer on top of high doped silicon, since the crystal lattice is too disturbed by the abundant presence of doping elements. Other experiments were carried out, not only for micromachining purposes, but also for the electrical isolation of electronic components in integrated circuits, e.g. the implantation of oxygen into monocrystalline silicon to obtain silicon-insulator-silicon structures. None of these techniques has, as yet, penetrated into micromachining technology, because some problems remain to be solved; especially the high concentration of lattice defects in the monocrystal. Moreover, the general philosophy in micromachining - for the moment and as long as micromechanical components are fabricated in microelectronic production lines - is to use as much as possible the standard processes that are available in integrated circuit labs.

The one method among the three that were mentioned, which allows accurate microfabrication of low doped, monocrystalline membranes and related

structures, is the electrochemical etch-stop on a p/n junction. This method works with low doped diffusions and epitaxial layers, technologies that are well established in the micro-electronic world. The first part of this chapter discusses the influence of an electric voltage on the etch behaviour of silicon. In the second part, it will be shown how this can be used to selectively etch structures with p/n junctions. Further, the required equipment will be discussed, and finally some typical performance characteristics of electrochemical etch stop will be presented.

4.2 Bias-dependent etching of silicon

4.2.1 Introduction

Anisotropic silicon etchants are used to produce three dimensional mechanical and electronic microstructures. The three most common anisotropic silicon etchants are:

- potassium hydroxide + isopropanol (optional) + water [7, 8]
- ethylenediamine + pyrocatechol (EDP) + water [9, 10]
- hydrazine + water [11, 12]

These etchants have different etch rates for the various silicon crystal planes. The <111> plane etches slowly compared to both the <100> and <110> planes. The structures that are obtained are delimited by the surface of the wafer, by a set of well defined <111> planes and by a plane that is parallel to the wafer surface, in general defined by the moment when the etch process is stopped. Electrochemical etch-stop allows to control exactly the position of this bottom plane.

This section describes and discusses the phenomena that occur when an electric potential is applied to silicon. Waggener using KOH [15] and later Jackson et al. using EDP [16], demonstrated that a sufficiently high positive bias applied to the silicon could prevent it from etching. These authors suggested that the anodic etch-stop of silicon is due to the growth of passivating oxides, as are known to form on positively biased metals. However, primarily because of this passivating oxide, the electrochemical study of silicon has proven very difficult [17].

In recent years, Palik and others [18 - 22], have reported this bias dependent behaviour of silicon etching and passivation in KOH, and have discussed their results in terms of oxide layers of varying stoechiometry. Their work was performed mainly at room temperature, where etch rates are very low. In KOH, the <100> and <110> etch rates increase with temperature, while the ratio of silicon etch rate to that of thermal SiO_2 etch mask decreases with temperature [8]. Therefore, practical silicon micromachining in KOH is commonly performed between 40 and 80 °C, where both the silicon etch rate and the mask selectivity are

between 40 and 80 °C, where both the silicon etch rate and the mask selectivity are large enough to be useful, e.g. >> 1 µm/h and 100, respectively. This chapter examines silicon etching and passivation at 60 °C. A new method of preparing accurately oriented <111> surfaces for electrochemical studies is used.

4.2.2 Experimental

Three different experiments are presented here:

- the current-voltage behaviour and its sweep-rate dependence,
- the bias dependence of etch rate,
- the time to etch back anodically grown oxides.

Each experiment was performed on four different samples: phosphorous- or boron-doped <100> or <111> oriented silicon surfaces.

4.2.2.1 Sample preparation

All samples were prepared from commercial 3-7 Ωcm <100> oriented 7.65 cm wafers. The backsides of the wafers were heavily doped with either phosphorous or boron, to ensure ohmic contact. A layer of 1.4 to 1.8 µm of thermal oxide was grown. This oxide served as an etch mask and defined the silicon area which was exposed to the KOH solution. The <100> surfaces were obtained by simply removing the oxide from a photolithographically defined 2 mm x 2 mm square. Each sample consisted of a 1 cm x 1 cm square cut from the <100> wafers. For measurements on <111> wafers, a different technique was used. The <111> samples were prepared by etching an array of 100 µm x 100 µm squares into the oxide, exposing <100> surfaces. Square 1 cm x 1 cm samples, each containing such an array, were cut from the wafer and placed in KOH at 60 °C. Each sample was then allowed to etch until the etch terminated along the <111> crystal planes, resulting in an array of 25 square pyramidal pits with <111> oriented surfaces, yielding a total area per sample of approximately 0.004 cm^2. The advantage of this method over using commercial <111> oriented wafers is that such wafers are known to be misaligned on the order of 1° [23], and therefore, etch results are dominated by faster etching <100> surfaces which are exposed along step dislocations [21], as schematically shown in Figure 4.1.

Electrical contact to the silicon was provided through aluminum or gold, electron-beam evaporated onto the back side of the wafers. The 1 cm x 1 cm silicon samples were clamped into a plexiglass (PMMA) and stainless steel chuck, using Viton O-rings to seal the sample. The chuck was then placed in a polyethylene lined thermostated reaction vessel containing approximately 100 ml of aqueous KOH at 60 °C. The KOH solutions were prepared by the dissolution of

solid KOH in 18 MΩ deionized water and stored under nitrogen. The KOH concentration was determined by titration with HCl, and found to be 39.84%. Nitrogen was continuously passed over the solutions during all the tests, and the solutions were routinely changed prior to each test. All experiments were performed in the dark.

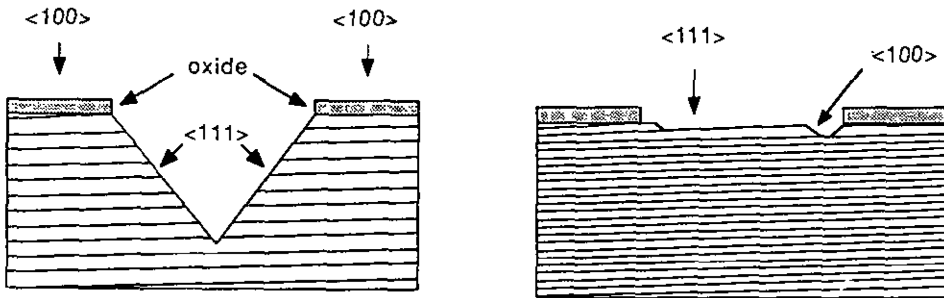


Fig. 4.1 Schematical representation of (a) square pyramidal pits with true <111> silicon planes, fabricated for electro-chemical studies, and (b) commercially available <111> wafers, with <100> planes exposed on step dislocations (exaggerated in this figure).

4.2.2.2 Electrochemical measurements

All electrochemical data were obtained using a modified IBM Voltammetric Analyzer, Keithley 617 Electrometer, and Metrohm 654 pH Meter. Current versus voltage (i-V) experiments were performed in a triple electrode configuration using a platinum counter-electrode and a saturated calomel electrode (SCE) with ceramic junction as reference. No particular care was taken to prevent chloride diffusional losses from contaminating the test solutions, i.e. no double junction reference was used. All potentials are referenced to the SCE at 60 °C, 0.253 V [24]. The i-V curves were obtained by linearly sweeping the potential either positive or negative of the open circuit potential, OCP. Sweep rates were varied from 0.15 to 200 mV/s.

When a sample was initially placed in the KOH, some time was required before a stable OCP was obtained. This was presumably due to slow removal of residual surface oxides by the KOH. In all experiments care was taken to obtain a stable OCP before performing any electrochemical measurements. When this procedure was followed, a particular sample could be used for any of the experiments in any order, without affecting reproducibility of results.

4.2.2.3 Etch rate determination

Etch rates of silicon in KOH at fixed bias were measured. After undergoing a dip in a solution of 1 part HF to 50 parts water, and a rinse in deionized water, samples were biased and placed in KOH. After etch times up to 10 h, the etch rate

was determined. On <100> samples, the rate was determined from the change of depth using a CaryCompar thickness comparator (Le Locle Switzerland), which electronically reads the displacement of an inductive stylus. On <111> samples, the width and depth of the pyramidal pits were measured using a high resolution optical microscope. To within the 2 μm resolution of the microscope, no <111> etch was observable, even after 10 h in the etch solution. Therefore, for <111> silicon samples, only an upper limit of the etch rate could be determined.

The potential dependence of oxide formation was also studied by performing anodic oxidation at various potentials, followed by etch-back of the oxide in the KOH. After achieving a stable OCP, the potential was stepped to various positive potentials. The potential was held at the new value until a steady-state current was reached. Then, the potential was removed, and the time until etching resumed was determined. The return of etching was indicated by a characteristic minimum in the OCP which precedes the steady-state OCP. This minimum was correlated with the onset of etching by direct observation of hydrogen gas evolution.

4.2.3 Results and discussion

4.2.3.1 Current-voltage characteristics

We start the discussion with a semiconductor that does not show electrochemical etch-stop in KOH, for instance germanium. If a voltage sweep is applied to a p-type germanium sample in a KOH solution, then a diode-like behaviour is observed, as presented schematically in Figure 4.2. For positive potentials, many majority charge carriers are available, and the current increases; for negative potentials the sample is more or less depleted, and the current saturates. For n-type germanium the diode is reversed. If a voltage sweep is applied to silicon, however, the current initially shows the same increase as for germanium, but at a certain potential the current drops, indicating that a current barrier is formed at this potential.

The measured i-V characteristics of n- and p-type <100> silicon are presented in Figure 4.3. These curves were obtained by sweeping the voltage linearly at 1 mV/s either positively or negatively from the open circuit potential, OCP (defined as the potential at which i=0). Both curves show an increase in the current at potentials positive of the OCP, until at some point the current drops off sharply. The potential at which the current is a maximum is classically denoted as the passivation potential (PP) and the potential at the bottom and positive of the peak, the Flade potential (FP). The steep decline in the current following PP, is usually interpreted to be where the formation of a passivating oxide inhibits further faradaic processes.

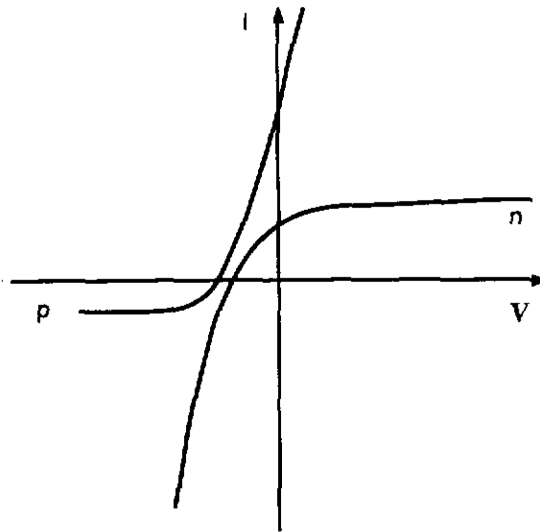


Fig. 4.2 Schematical representation of the i-V curves for n- and p-type samples of germanium .

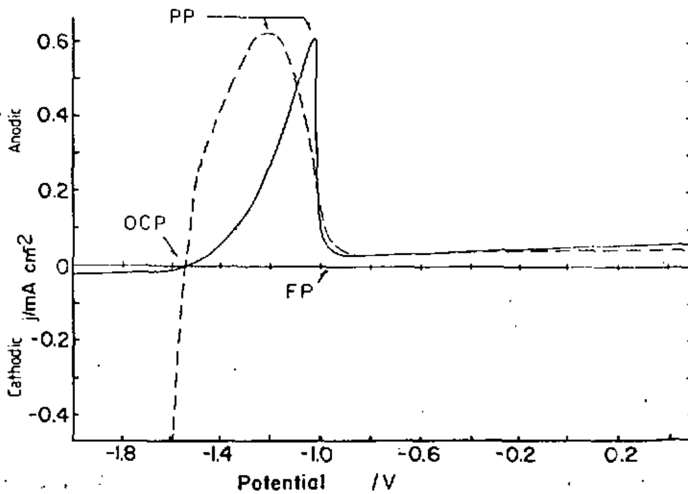
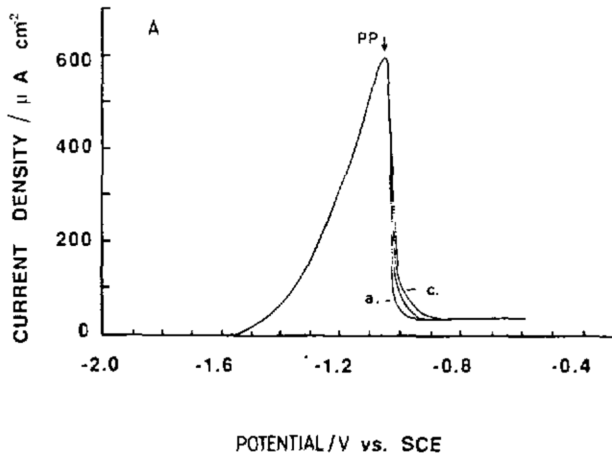


Fig. 4.3 The electrochemical i-V characteristics of p- (——) and n-type (- - - -) <100> oriented silicon, in 40% KOH aqueous H_2O solution at 60 °C at a sweep rate of 1 mV/s.

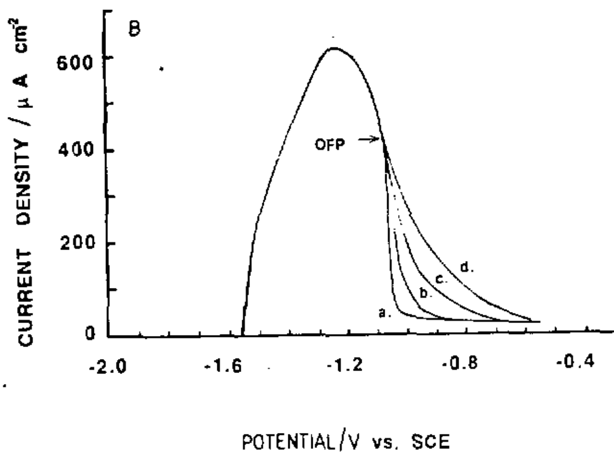
It was noted that the kinetics of passivation for silicon at 60°C were relatively slow, usually requiring several minutes for complete passivation to occur. Generally, p-type silicon showed an easier passivation than n-type silicon for the same crystal orientation, and <100> was more facile than <111> for the same doping type. Variations in the i-V characteristics with different potential sweep rates are shown in Figure 4.4 (A) and (B) for p- and n-type silicon. The i-V characteristics of p-type <100> silicon show little PP dependence upon voltage sweep rates up to 200 mV/s. However, between the PP (current maximum) and the FP, where passivation by oxide formation has been proposed to occur, the current does show sweep rate dependence. The n-type <100> silicon samples also show no potential sweep dependence of PP. However, unlike p-type <100>, the n-type i-V characteristic remains insensitive to sweep rate beyond the current maximum, until a potential of about -1.080 V has been reached. For this reason, passivation by oxide formation is proposed to occur at that potential where the kinetics become slow, -1.080 V, rather than at the potential of the current peak, -1.230 V. This potential is hereafter referred to as the oxide formation potential, OFP, and is so indicated on Figure 4.4 (B).

Typical i-V characteristics, obtained from the specially prepared n- and p-type <111> silicon samples are shown in Figure 4.5. Unlike other reported studies [18, 20], no indication of double current peaks were ever observed for any of the silicon samples studied as long as the tests were performed while under nitrogen and in the dark. The sweep-rate dependence of the i-V characteristic for the <111> crystal face was notably different from that of the <100> crystal face. The sweep rate dependence of an n-type <111> silicon sample i-V characteristic is shown in Figure 4.6. The p-type <111> samples showed similar behaviour. Generally, the entire current peak is shifted to more positive potentials with a corresponding increase in the peak current as the sweep rate is increased. This behaviour is typical of a kinetically slow transformation of a fixed amount of surface-bound electroactive material. In order to determine the amount of charge involved in the reaction, the area under each current peak was divided by the sweep rate. This is equivalent to transforming Figure 4.6 to a current-versus-time graph and integrating the current function, since voltage increases linearly with time. Areas were estimated manually using a hand-drawn baseline, linearly interpolated beneath each peak. Within the error of this method, all three peaks in Figure 4.6 gave a value of $(2.4 \pm 0.5)\ 10^{-3}$ C/cm^2.

Since the passivation potential for <111> silicon depends on the sweep rate, is not unambiguously defined. Figure 4.7 shows the PP versus sweep rate for the n- and p-type silicon samples. The values for PP, obtained by extrapolating linearly



(A)



(B)

Fig. 4.4 Variations in the i-V characteristics in 40% KOH at 60 °C of (A) p-type and (B) n-type, <100> oriented silicon with sweep rate: (A): (a) 0.15, (b) 1.0, (c) 30 mV/s; (B): (a) 0.15, (b) 1.0, (c) 10, (d) 30 mV/s.

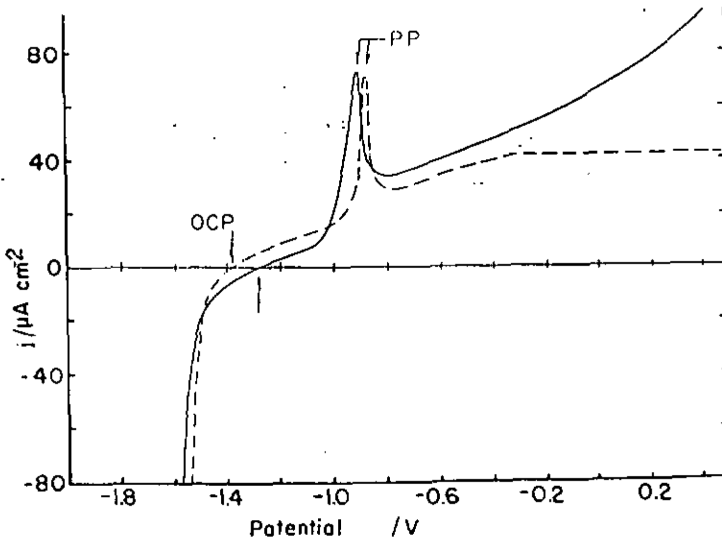


Fig. 4.5 The electrochemical i-V characteristics of p- (——) and n-type (-----) <111> oriented silicon, in 40% KOH aqueous H_2O solution at 60 °C at a sweep rate of 1 mV/s.

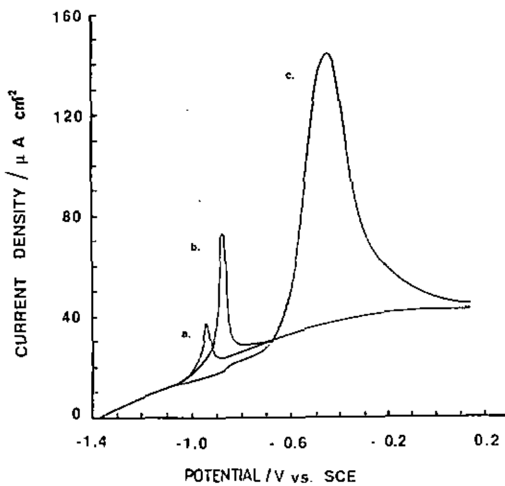


Fig. 4.6 Sweep rate dependence of the i-V characteristics of n-type <111> oriented silicon (40% KOH, 60 °C). (a) 0.15, (b) 1.0, (c) 10 mV/s.

to zero sweep rate, are nearly identical. These values are chosen to represent the potential of oxide formation for the <111> surface.

Average values for OCP, PP and FP, determined as described above, from at least six samples of each type, are shown in Table 4.1. Interestingly, the values for the OCP and oxide formation are the same for either dopant type and vary only according to crystal orientation.

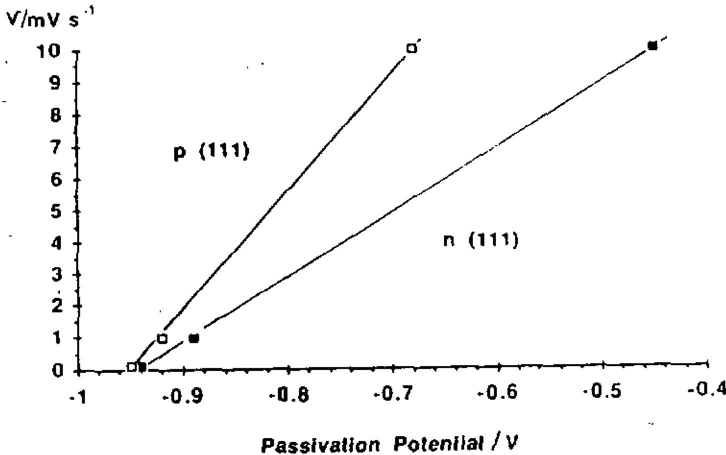


Fig. 4.7 Plot of passivation potential (potential at current peak) versus sweep rate for n- and p-type <111> silicon (40% KOH, 60 °C).

4.2.3.2 Silicon etch rate versus voltage

Since the <111> sample pit geometries changed less than 2 µm over the term of the experiments, the etch rates of the <111> samples are inferred to be of the same order or less than the etch rate of the thermal oxide mask, approximately 36 nm/h. No measurable voltage dependence of etch rate was observed. This is in contrast to the data presented by Glembocki et al. [21], who measured a considerable etch rate and etch rate bias dependence of the <111> crystal plane at 20°C. However, as was pointed out by Glembocki et al., the <111> silicon samples they used to obtain etch rates were only oriented to within 1° of the <111> crystal plane, and the etch rates given could reflect the faster etching of exposed <100> or <110> crystal planes along step dislocations (see Figure 4.1). This same interference would also affect their reported <111> current-voltage characteristics, since current magnitudes obtained on <100> silicon are generally 10 times greater than for <111>.

The potential dependent etch rate of p- and n-type silicon is shown in Figure 4.8. It is evident that the dissolution of <100> silicon in KOH can be controlled

*Table 4.1 Average values of open circuit potential (OCP), passivation potential (PP) or oxide formation potential (OFP, indicated by *), and Flade potential (FP) obtained from the electrochemical i-V characteristics of the four sample types.*

Sample	OCP (V)	PP / OFP (V)	FP (V)
p-type Si			
<100>	-1.547 ± 0.012	-1.040 ± 0.013	-0.985 ± 0.011 [1]
<111>	-1.280 ± 0.035	-0.955 ± 0.008 [1]	-0.873 ± 0.008 [1]
n-type Si			
<100>	-1.541 ± 0.013	-1.080 ± 0.016 *	-1.030 ± 0.012 [1]
<111>	-1.380 ± 0.030	-0.959 ± 0.009 [1]	-0.958 ± 0.008 [1]

[1] Linearly extrapolated to zero sweep rate. Error values represent the standard deviation of values obtained at a sweep rate of 1mV/s

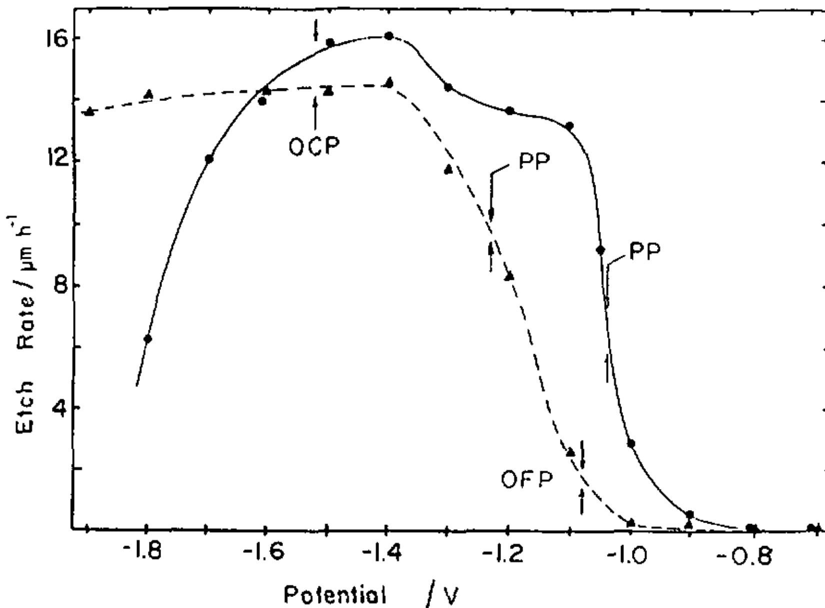


Fig. 4.8 Potential dependence of the etch rate of <100> p-type (—•—) and n-type (-▲-) silicon in 40% KOH at 60°C.

selectively by the application of the appropriate voltage. In agreement with other reports [20-22], etch stopping was observed on both n- and p-type material for biases sufficiently positive of the OCP. For p-type <100> silicon, etching slows down at roughly the same potential as is classically designated as PP. However, for n-type <100> silicon, the etch rate begins to decrease considerably negative of both OFP and the classically defined PP, at about -1.4 V. In fact, the silicon etch rate at the OFP is only about 8 % of the OCP value. This indicates that the etching of n-type silicon is not only affected by the presence of the oxides which are formed at the OFP, but also by an other mechanism. A slight dip in the p-type <100> etching curve in the same potential range, -1.4 to -1.1 V, could be related to the same mechanism. A prepassivation oxide has been suggested by others to account for such decreases in n-type silicon etch rate at potentials between the OCP and PP [19]. At potentials negative of the OCP, p-type <100> silicon is seen to decrease its etch rate while that of n-type <100> silicon is relatively unaffected. This is again in contrast to the observations of Glembocki et al. [21]. In fact, the general shapes of the potential dependent etch rate curves presented here are opposite, with respect to n- and p-type, to those presented by Glembocki. These surprising results were confirmed by repeated experiment and sample type measurements. There is perhaps a temperature dependence in the bias dependent etch behaviour which would account for the observed differences, but this has not been investigated. It is noted that the mentioned research group published a study which compares different etch-stop methods [22]. Here they report that efforts to achieve cathodic etch-stop on a p-n diode junction (based on the difference in etch rates of p- and n-type silicon at potentials negative of the OCP) have failed, which would confirm the biased etch rate measurements presented in Figure 4.8. Cathodic etch-stop could be used, though, to etch n-type silicon and protect p-type, the opposite configuration as generally used for anodic etch-stop.

4.2.3.3 Oxide time-to-etch back

To support the claim that the passivation potentials given in Table 4.1 actually correspond to the formation of a passivating oxide, the potential was stepped from the OCP to various potentials positive of the PP. The potential was held at the new voltage until a steady state was reached, at which time it was released, and the time until etching resumed was monitored. Since silicon oxides are etched slowly in KOH, the time required to resume etching should be a function of the thickness and type of passivating oxide present. The oxide etch-back time, plotted as a function of voltage, is shown in Figure 4.9. Conversion of the time-to-resume-etching into equivalent oxide thickness was done by using the measured etch rate

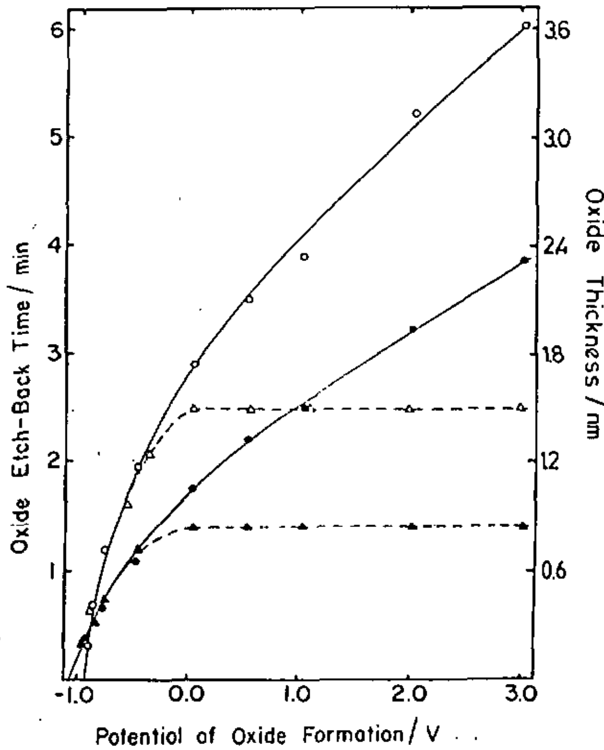


Fig. 4.9 The oxide time-to-etch-back as a function of oxide formation voltage. The left vertical axis indicates the time required to resume silicon etching once the applied voltage is removed. The right vertical axis indicates the oxide thickness derived from the etch-back time and an assumed etch rate equal to that of thermal oxide (40% KOH, 60 °C). (○) p-type <111> oriented, (Δ) n-type <111> oriented, (•) p-type <100> oriented, (▲) n-type <100> oriented.

of thermal oxide, 36 nm/h. It is possible that the anodic oxides etch at somewhat different rates from the thermal oxide, but comparisons between the various samples are still valid.

The extrapolation to zero time (no oxide) gives potential values of -1.10 ± 0.07 V for the <100> and -0.96 ± 0.07 V for the <111> crystal orientation, which coincide nicely with the respective values listed in Table 4.1 for the potentials of oxide formation (PP and OFP). It was noted that the oxide etch-back times for <111> and <100> surfaces have similar bias dependence, but different absolute values. This could be a result of either different oxide thicknesses (a consequence

of differing oxidation rates [25]) or different oxide etch rates (a consequence of the formation of oxides of differing stoichiometry). It was also noted that the oxide formed on n-type silicon, of either <111> or <100> orientation, does not continue to grow as does the oxide on p-type silicon. Further, if the oxide on n-type silicon is grown under illumination, the oxide etch-back time continues to increase. This is an indication that the mechanism for the formation of the passivating oxide requires the presence of holes, as has been proposed by others [26].

4.2.4 Conclusion

In this section, the potential dependent etching and passivation behaviour of silicon in KOH at 60 °C was investigated. The i-V characteristics of the <100> and <111> surfaces and their sweep rate dependence were examined. A new sample preparation technique was employed, which ensured an accurately oriented <111> surface exposed to solution for measurement.

The observed sweep rate dependence of the i-V characteristics for n-type <100> samples required a different definition of passivation potential than that where the current peak is maximum. The potential where the kinetics became slow, reflected by the onset of a dependence of current on sweep rate, was chosen and identified as Oxide Formation Potential, OFP. For <111> samples, the entire i-V curve was affected, with the current peak shifted dramatically with sweep rate. Therefore the PP values for <111> samples were obtained by extrapolating linearly the potential of the current peak to zero sweep rate. The oxide etch-back results confirm that the potential where oxide is formed on the silicon surfaces corresponds to the extrapolated PP values and OFP values determined from the i-V characteristics.

The OCP and potential where oxide formed on the silicon surfaces were found to be independent of dopant type for both <100> and <111> samples. However, the i-V and etch rate versus bias behaviour did show dopant type dependence on <100> silicon. This indicates that more than one mechanism, i.e. not only passivation, is involved in the bias dependence of <100> silicon etching.

The i-V characteristics of <111> surfaces did not show any dopant type dependence until after an oxide began to grow. Increasing sweep rate shifted the PP and increased the current peak in a manner corresponding to the presence of an active surface bound layer with charge density of 2.4 10^{-3} C/cm^2. This surface bound layer is proposed to be responsible for the observed dopant type-independent electrochemical behaviour of the <111> surface before passivation. At passivation, this layer was converted to oxide. The continued growth of this

oxide then became dependent on the silicon surface dopant type, as in the case of the <100> surface. The oxide etch-back experiments confirmed that oxide is grown on both <100> and <111> surfaces, and that both showed a similar dependence on dopant type. These results also indicate that the oxide stoichiometry and/or the oxide growth rate was different for <100> and <111>.

4.3. Electrochemical etch-stop on an epitaxial layer

4.3.1 Introduction

The etch-stop technique combines the above described anodic passivation characteristics of silicon with a reverse biased p/n junction to provide a large etching selectivity of p-type silicon over n-type in anisotropic etch solutions. Dimensional definition of micromachined structures can be controlled precisely by taking advantage of standard silicon diode fabrication technologies. This technique was first proposed by Waggener in 1970 [15] and has, since, been sucessfully applied to the fabrication of several different microstructures [16, 27-30]. The result is that etching can be stopped at a well defined p/n junction. To achieve this, a positive voltage is applied directly to the n-type silicon via an ohmic electrical contact while the electrical contact to the p-type silicon is accomplished via the etch solution with an appropriate counter electrode. Under sufficiently anodic biases (cfr. Figure 4.8) silicon passivates as a result of anodic oxide formation and etching stops. Since the majority of the potential drop is across the reverse biased p/n junction, the p-type silicon remains essentially at Open Circuit Potential (OCP) and etches. With the complete removal of the p-type silicon, the diode is destroyed and the n-type silicon becomes directly exposed to the etch solution. The positive potential applied to the n-type silicon then passivates it and etching terminates. Many silicon microstructures may be fabricated this way by selectively etching away p-type silicon and leaving the n-type silicon passivated. Definition of the microstructure morphology is precisely determined by the definition of the n-type silicon sections under anodic biasis.

In this section, a characterization of the electrochemical etch-stop in KOH is presented. Emphasis will be placed on the evaluation of different electrochemical fabrication methodologies, as well as the pertinent process parameters that control the physical nature of the etch-stop. The advantages of increased microstructural control become clear when the electrochemical etch-stop is applied to the fabrication of thin silicon membranes for use in piezoresistive pressure sensors. In chapter 5, the device characteristics and lot reproducibilities of these pressure sensors will be compared with other sensors fabricated without the aid of the electrochemical etch-stop.

4.3.2 Experimental

All experiments used boron-doped (2 x 10^{15} at/cm^3), three-inch silicon wafers with an approximately 10 μm thick n-type epitaxial layer deposited on the top surface. The epitaxial layer was phosphorous doped at 5 Ωcm. To etch the membranes, the wafers were mounted in a chuck of plexiglass and stainless steel using Perbunan 65 o-rings to seal the sample from the solution. The chuck was immersed in a 40 % KOH solution at 60 ± 0.5 °C (see Figure 4.10 or 4.11). The required potentials were applied using an IBM EC/225 Voltammetric Analyser with a Saturated Calomel Electrode (SCE) and a platinum counter electrode. Unless specified otherwise, all electrochemical potentials are referenced to the SCE at 60 °C (see also section 4.2.2.2). Membrane thicknesses were measured mechanically using a CaryCompar (Le Locle, Switzerland). The surface roughness was recorded by means of a Talystep profilometer.

For the electrochemical studies, the n-type epitaxial layer surface was degeneratedly doped and a thick thermal oxide layer (1.5 μm) was grown to serve as a KOH etch mask for the back surface. After oxide patterning, the epitaxial layer was etched away except for a 5 by 5 array of 3 mm x 3mm squares, thus forming 25 mesas of p-type silicon with the n-type epilayer on top of it. A schematic cross-section of the wafer is shown in Figure 4.10. This was done to isolate the 25 diodes from each other and to have the possibility to make an electrical contact to the p substrate. In the oxide on the back (p-type substrate), openings of 2 mm x 2 mm were aligned to the mesas to define the future geometry of the silicon membranes. An aluminium layer was deposited by e-beam

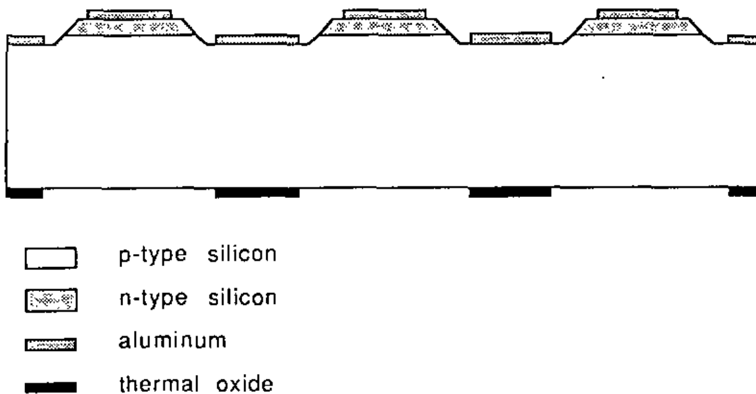


Fig. 4.10 Schematic cross section of the wafers for etch-stop experiments, containing 25 isolated junction diodes.

evaporation and patterned to contact the epitaxial layer areas and the substrate. The aluminum was then alloyed at 450 °C for 15 min. For some experiments the wafer was diced into individual diodes.

4.3.3 Results and discussion

In the next sections, some practical, process relevant parameters of commonly used electrochemical etch-stop configurations are discussed in detail and a modified setup, the four-electrode configuration, is proposed for improved fabrication facility. The etch-stop technology will be evaluated by a detailed characterization of process parameters such as surface smoothness, membrane thickness reproducibility and the influence of the applied passivation voltage. It will be shown that electrochemical etch-stop is very suitable for process automation.

4.3.3.1 Etch-stop methodologies

In its simpliest embodiment, the required passivating potential can be applied between the epitaxial silicon and a single inert metal electrode in the etch solution. Since any potential sufficiently anodic of the Oxide Formation Potential (OFP = -1.080 V at 60 °C, see Table 4.1) will passivate the n-type silicon, any sufficiently large reverse bias will assure an etch-stop. However, the solution potential is ill defined and current dependent, which results in the lack of precise control over the fabrication parameters. Therefore, the use of a single metal electrode is not a viable process technique.

A three-electrode configuration, as shown in Figure 4.11, overcomes the afore-mentioned limitations of a two-electrode configuration and is the preferred electrochemical arrangement. A potentiostat, in conjunction with a reference electrode, e.g. an SCE, and an inert counter-electrode, maintains a constant and reproducible solution potential with respect to the reference electrode. In order to establish the required voltage between the working electrode, i.e. the silicon wafer, and the SCE, the voltage between the working electrode and the SCE is measured and compared to the required voltage, and the current through the counter-electrode is adjusted so as to null the readings. In this way the reference electrode remains currentless (high impedance input) and its interface potential with the solution is stable. In reality the working electrode is grounded, but all electrochemical potentials are referenced to SCE.

By using three electrodes, the n-type epitaxial layer is kept at a well defined passivation potential, but an additional shortcoming of both the two- and the three-electrode configurations is that the substrate potential is not under direct

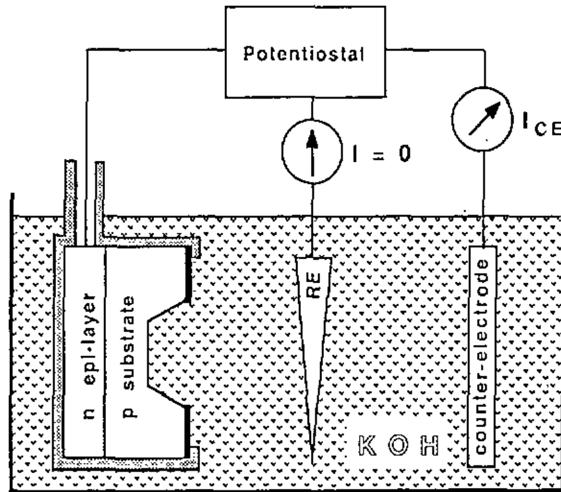


Fig. 4.11 Standard three-electrode system for etch-stop. RE is the Standard Calomel Reference Electrode.

electrical control. In the ideal case it "floats" to OCP and is etched. In practice, however, the diode junction can be short-circuited and, since little current is required to passivate silicon, even a high resistance short circuit will prevent the p-type substrate from etching. The substrate potential, which in that case is defined by the total impedance of all electrical connections, will move to the right in Figure 4.3, and if it becomes more anodic than the PP for p-silicon (-1.04 V, see Table 4.1), the substrate will be passivated. Common sources of p/n junction shorts are point defects in the junction and leakage at the border of the wafer, since the diode covers the entire surface of the wafer, about 45 cm^2. Thus for practical application of etch-stop, a three-electrode configuration may not be sufficient.

Rather than to impose more stringent requirements on the epitaxial layer fabrication, it was preferred to modify the etch-stop arrangement so as to deal effectively with these problems. The new configuration uses four electrodes: an electrical connection to the substrate is added, as shown in Figure 4.12. Whereas in the three-electrode method, the potentiostat was connected to the n-type epitaxial layer, it is now connected to the p-substrate. A suitable voltage is applied directly to the p-type substrate to assure that it maintains a controlled etching potential, close to the OCP of p-type silicon (-1.5 V to SCE, see Table 4.1),

independent of the magnitude or variations in the junction shorts. A second voltage supply, V_E in Figure 4.12, is connected between the epitaxial layer and the substrate to bias the epitaxial layer at a passivating potential, i.e. more anodic than the OFP for n-type silicon (-1.08 V with respect to SCE, see Table 4.1), and thus more than + 0.4 V with respect to the substrate. In practice, V_E is set at about 1.5 V, which puts the epitaxial layer at 0 V with respect to SCE. In Figure 4.12, a diagram of the potential distribution is sketched for the four-electrode arrangement. All potentials so applied are "hard" low impedance connections, and the effects of unpredictable and fluctuating impedance pathways are eliminated. This method gave excellent results even with reverse-diode leakage currents as large as 10 mA per wafer from p/n junction defects. It is noted here that,

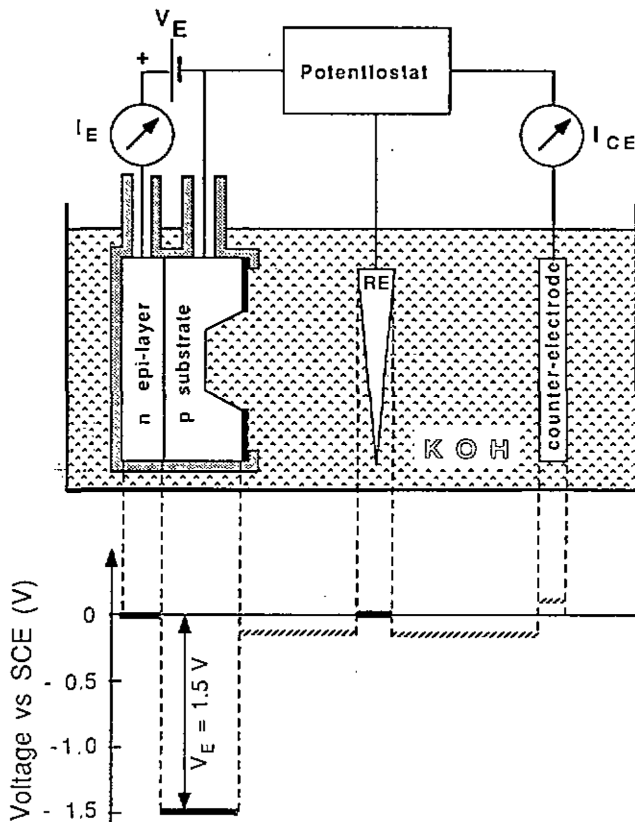


Fig. 4.12 Four-electrode electrochemical etch-stop configuration and voltage distribution with respect to the SCE reference electrode (RE). The standard three electrode configuration of Figure 4.11 is used with the addition of a potential, V_E, between the epitaxial layer and the substrate to externally maintain the substrate at etching potentials.

compared to the three-electrode method, the four-electrode configuration does not improve the surface quality of the etch-stopped membranes, but it allows etch-stop to be successful on every wafer, no matter how poor the junction quality is.

4.3.3.2 Etch-stop process parameters

In this section the smoothness of etch-stopped surfaces and the thickness reproducibility of the membranes will be presented. These are major requirements for the mass production of high quality micromechanical devices. Furthermore the influence of the Space Charge Region (SCR) on etch-stop will be investigated in order to find out if the applied reverse bias can be used to vary the obtained membrane thickness according to the fabrication needs. Indeed, the width of the SCR is a function of the reverse-bias potential. Variations in the reverse-bias voltage could affect the thickness of the resulting membranes if the etch-stop is SCR dependent.

Smoothness of the membrane surface is important to increase the yield strength and the fatigue resistance. Figure 4.13 shows a cross-sectional view of a cleaved silicon membrane fabricated using etch-stop. The approximately 10 µm thick membrane is seen at the bottom of the picture and two anisotropically etched <111> planes to the back and right. Despite an unpolished initial back-side wafer

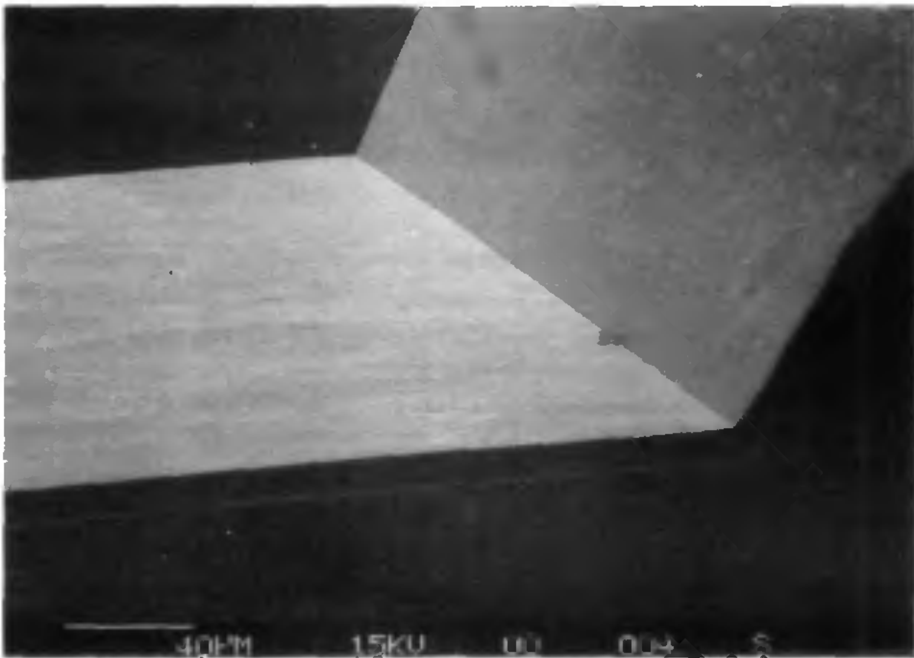


Fig. 4.13 SEM photograph of an etch-stopped membrane surface.

surface, the smoothness of the etch-stopped membrane surface approaches that of the extremely smooth <111> planes. Figure 4.14 shows a profilometer scan of the etch-stopped surface and the initial wafer surface from which the membrane was etched. The initial surface roughness of about 5 μm was smoothed to less than ± 0.1 μm after etch-stop. This is a significant improvement over conventional timed etches which at best demonstrate a steady state limit roughness of 0.4 to 0.5 μm, even for initially polished wafers of less than 0.02 μm roughness [32].

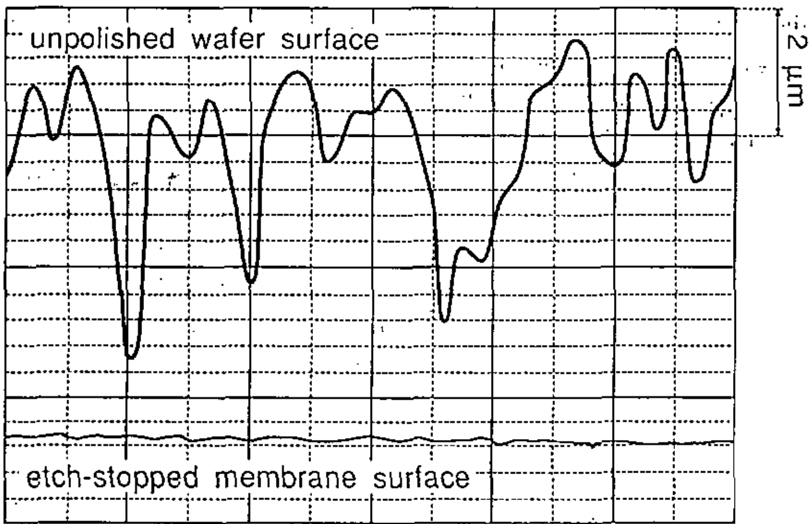


Fig. 4.14 Profilometer scan of an unpolished silicon wafer surface (upper) and of an etch-stopped membrane (lower).

For mass production, all devices should have identical mechanical properties. Hence, the reproducibility of the membrane thickness is another important fabrication feature. In order to study the thickness reproducibility across a wafer, 52 membranes were fabricated, equally spaced over a three-inch wafer. After etch-stop by means of the four-electrode method at a reverse diode bias of 1.5 V, the thickness of the membranes was measured. Figure 4.15 shows a histogram of the measurements obtained for the membranes of one wafer. The membrane thickness was 10.7 μm ± 0.2 μm s.d. This distribution reflects the thickness variation of epitaxial silicon for the wafers used in these experiments, which is about 0.2 μm. Between different wafers, the thickness of the epitaxial layer can vary more than 0.5 μm, yielding a larger membrane thickness variation.

Figure 4.16 shows a SEM photograph of a cleaved membrane. The photo was taken while a reverse-bias potential was applied to the diode junction, so that

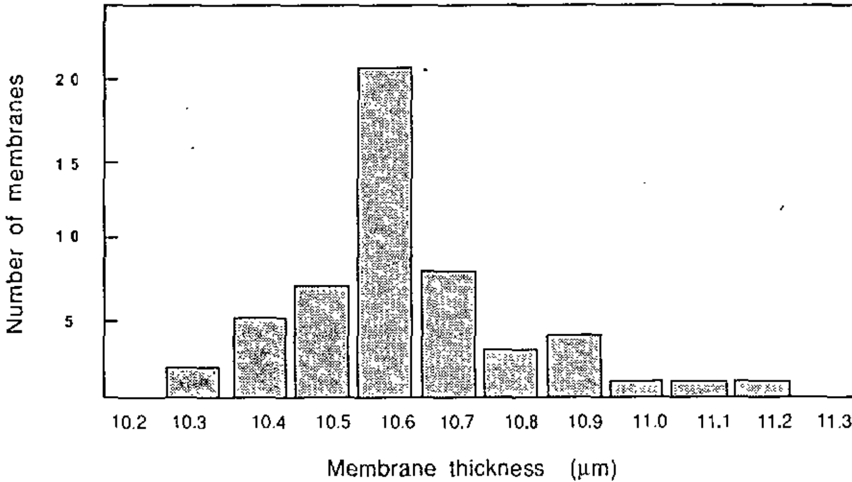


Fig. 4.15 Histogram of the membrane thickness obtained by four-electrode etch-stop.

electrons impinging on the p/n space charge region (SCR) were absorbed by electron-hole recombination. Hence, the SCR appears as a black line on the picture and is seen to coincide exactly with the etch-stopped membrane surface. This confirms that etching is stopped at the diode junction. Therefore the etch-stop reproduciblibility is shown to be limited only by the reproducibility of the epitaxial layer growth process.

The SCR width can be an important process parameter for membrane thickness control if etch-stop is SCR dependent. To determine how the SCR affects etch-stop, membranes were fabricated by applying different epitaxial layer potentials. The resultant thickness was compared with the SCR width, W, which is calculated by Eq. (4.1) for abrupt junctions [33]:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_{D\cdot}}\right)(V_{bi} + V_E)} \tag{4.1}$$

where N_A is the substrate boron concentration ($N_A = 2 \cdot 10^{15}$ at/cm^3), N_D is the epitaxial layer phosphorous concentration ($N_D = 10^{15}$ at/cm^3); ε_s is the permittivity of silicon ($1.0536 \cdot 10^{-12}$ F/cm [33]), V_{bi} the built-in diode potential (0.7 V) and V_E the externally applied bias voltage. For the above mentioned dopant concentrations, the width of the p-type side of the SCR can be reduced to:

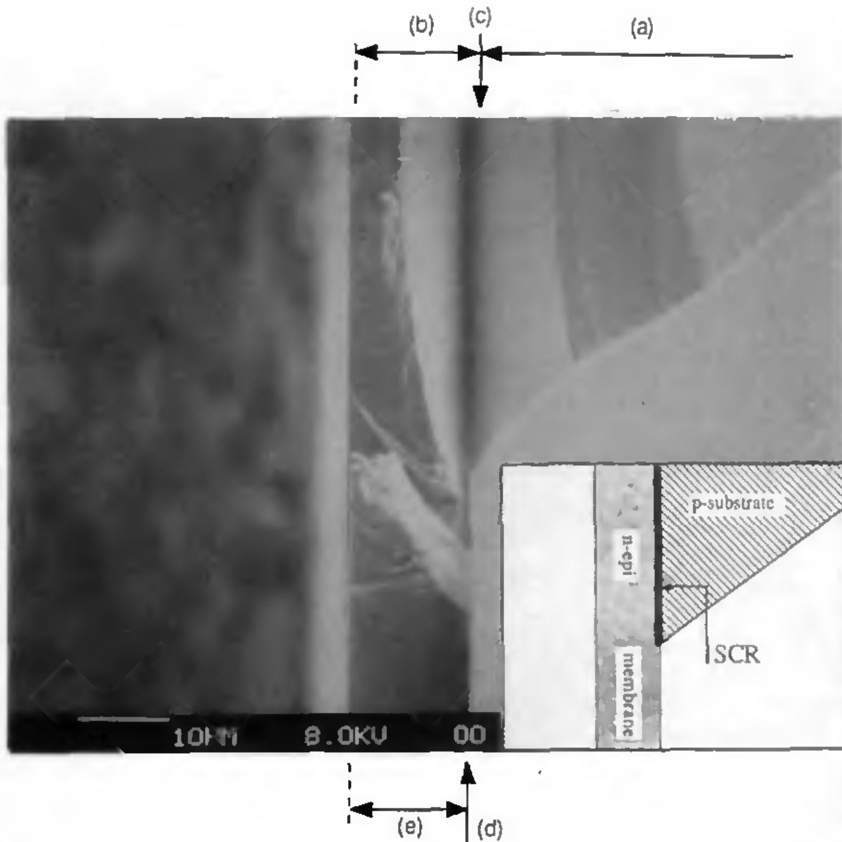


Fig. 4.16 Photograph of a cleaved membrane, showing that etching is stopped at the diode SCR. The inset indicates the relevant features of the picture; other lines are caused by imperfect cleavage of the sample. (a) p-type substrate, (b) n-type epitaxial layer, (c) Space Charge Region, (d) etch-stopped membrane surface, (e) membrane.

$$L_p = \frac{1}{3} \cdot W = 0.47 \cdot 10^{-6} \sqrt{0.7 + V_E} \qquad (4.2)$$

An array of 25 electrically isolated diodes, reverse biased at 8 different voltages, were etch-stopped on a single wafer. Applied voltages ranged from -0.80 V to + 4.00 V. The substrate was held at a potential of -1.5 V, so that bias voltages between 0.7 V and 5.5 V were established across the diode junction. According to Eq. (4.2), L_p ranged from 0.55 µm to 1.17 µm. The difference between these two SCR widths, 0.6 µm, should be reflected in the obtained membrane thicknesses if any SCR influence is involved in etch-stop chemistry. In Figure 4.17, the thickness of each of the membranes is shown. The left-hand side

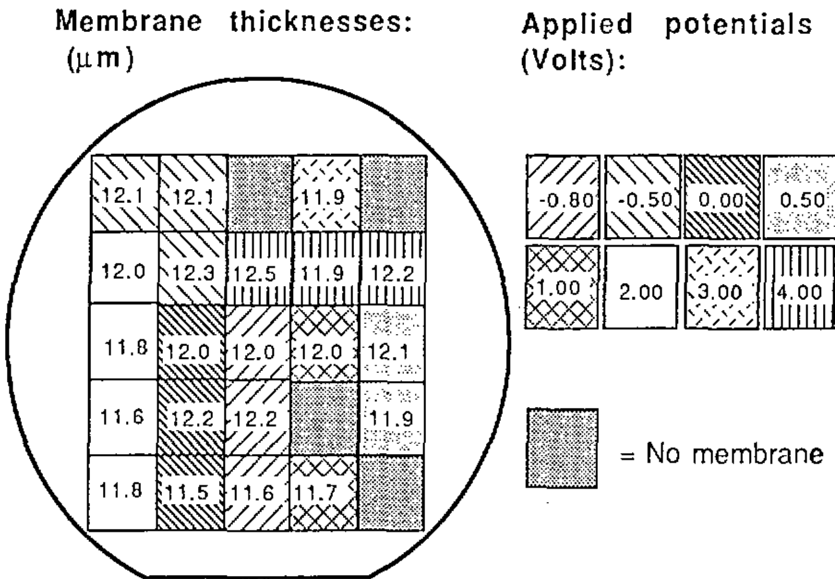


Fig. 4.17 Correlation investigation between membrane thickness and applied passivation potential: spatial distribution of the measurements.

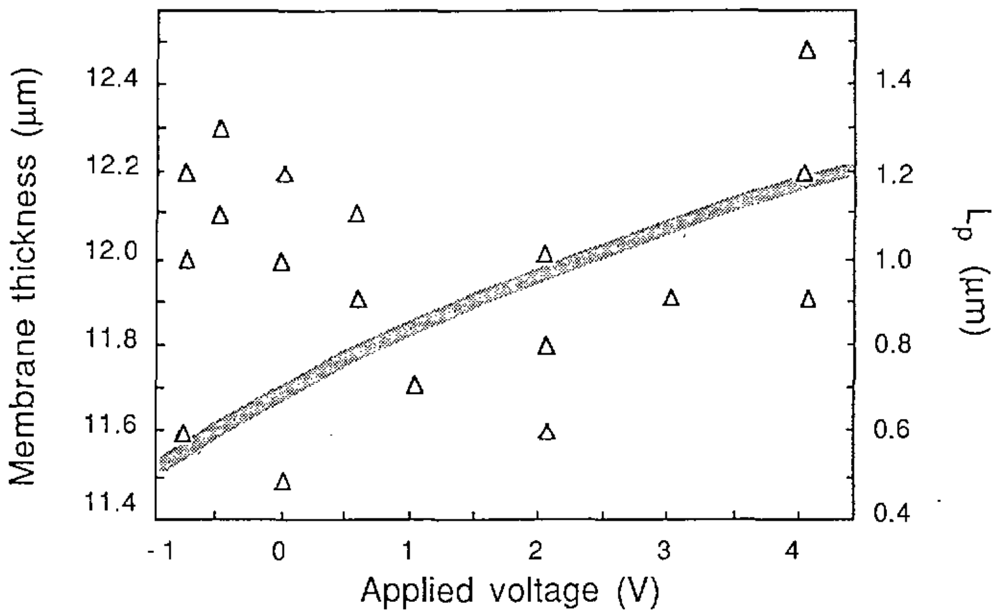


Fig. 4.18 Correlation investigation between membrane thickness and applied passivation potential : measured membrane thicknesses (Δ) and calculated L_p — the p-type substrate side of the SCR — (line) as function of the applied voltage.

of the figure schematically represents the wafer location of the membranes and their thicknesses; the shadings give the applied voltage on each membrane, as indicated on the right-hand side. The average thickness of 21 samples was 12.0 μm and the standard deviation was 0.25 μm. Figure 4.18 plots the membrane thicknesses measured in this experiment and the calculated L_p as a function of the potential as given by Eq. (4.2). No obvious correlation between the membrane thickness and the SCR could be observed. If, nevertheless, the SCR does have an effect, then it is negligible compared to other influences, such as cpilayer thickness. Thus it may be concluded that it is not possible to adapt the thickness of the membranes according to the fabrication needs, by changing the magnitude of the applied reverse bias voltage.

4.3.3.3 Electrical contact to the epitaxial layer

Since the potential applied to the epitaxial layer does not influence the thickness of the fabricated membranes, the way how the electrical contact to the epitaxial layer is made should not be critical. It was investigated if it was possible to succeed etch-stop with only one contact to the epitaxial layer and one contact to the substrate on a three inch wafer. Using a hand-drawn mask, the contacts were placed 4.5 cm apart from one another, as shown in Figure 4.19. A mask with 54 oxide openings was used for this experiment. A V_E of 1.5 V was applied to the

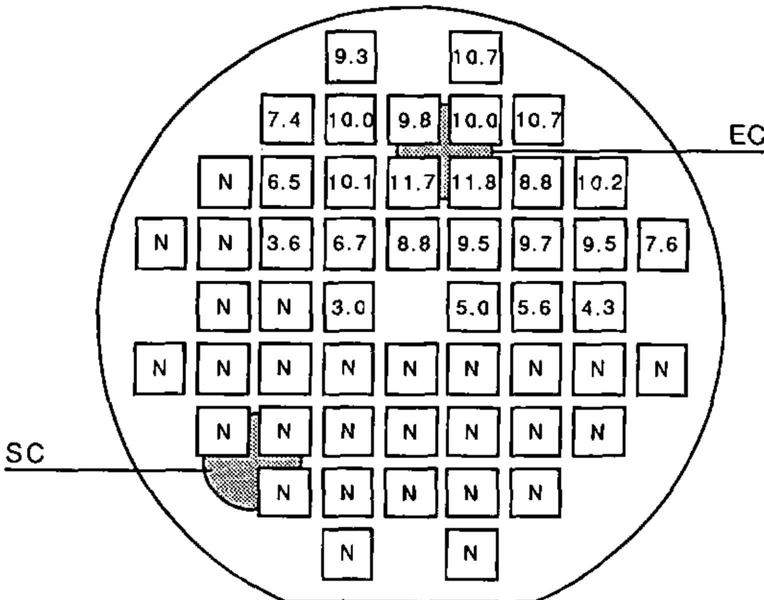


Fig. 4.19 Membrane thicknesses (in μm) obtained with only one electrical contact to the epitaxial layer (EC) and one to the substrate (SC). N indicates a perforated membrane.

epitaxial layer, so that it was nominally at 0 V with respect to the SCE. Figure 4.19 shows the thickness of the obtained membranes after etch-stop. It was found that only the membranes in the neighbourhood of the epitaxial layer contact had stopped correctly. Further away from this contact the membranes were thinner than the epitaxial layer and even completely etched away.

This result is explained by the resistance of the epitaxial layer. With a resistivity of 5 Ωcm and a thickness of 10 μm, the resistance of the epitaxial layer between the two regions of contact in Figure 4.19 is of the order of 10 kΩ. A leakage current of 1 mA flowing through the epitaxial layer can cause a voltage drop of 1 V. According to Figure 4.8, the applied potential to the epitaxial layer is then close to the OFP. The etch rate will then no longer be zero and will be higher as the effectively applied voltage approaches OCP. It is noted that in the case of a good diode junction, this problem does not occur since there is a negligible current and voltage drop. It is concluded that it is important to provide several epitaxial layer contacts across the wafer in order to succeed etch-stop under any circumstances.

4.3.3.4 Etch-stop indicators

During a fabrication run it is useful to have an indicator that allows one to follow the process evolution and that automatically signals its completion. The current through the system is very well suited to perform this task. Figure 4.20 shows current waveforms recorded as a function of time during four-electrode membrane etching. The current levels can be explained by examinating the working points of the etch process on Figure 4.3. For clarity, Fig. 4.3 is taken again here as Figure 4.21. Curve 4.20 (a) represents the ideal case where the reverse-biased diode current is negligible. The working point during substrate etching is at OCP and is indicated by S in Figure 4.21. Hence, the counter-electrode current (I_{CE} in Figure 4.12) is zero. As soon as the etch front reaches the n-type epitaxial layer, the current is seen to increase and form a peak. As a fabrication tool this peak signals the onset of the etch stop. The existence and shape of the current peak follow naturally from the two dimensional nucleation kinetics of oxide passivation [34] and from the wafer thickness taper and surface roughness. A complete explanation of this phenomenon is given in [35]. When the etch-stop process is finished across the entire wafer, a new steady-state current is reached at point E in Figure 4.21, the working point for the passivated n-epitaxial layer, corresponding to a current through the counter-electrode of about 0.1 mA. In practice, the final passivation current is higher, 0.2 mA/cm^2 in Figure 4.20 (a) (j_{ox}), because of the interaction between the two voltages applied by the potentiostat and V_E.

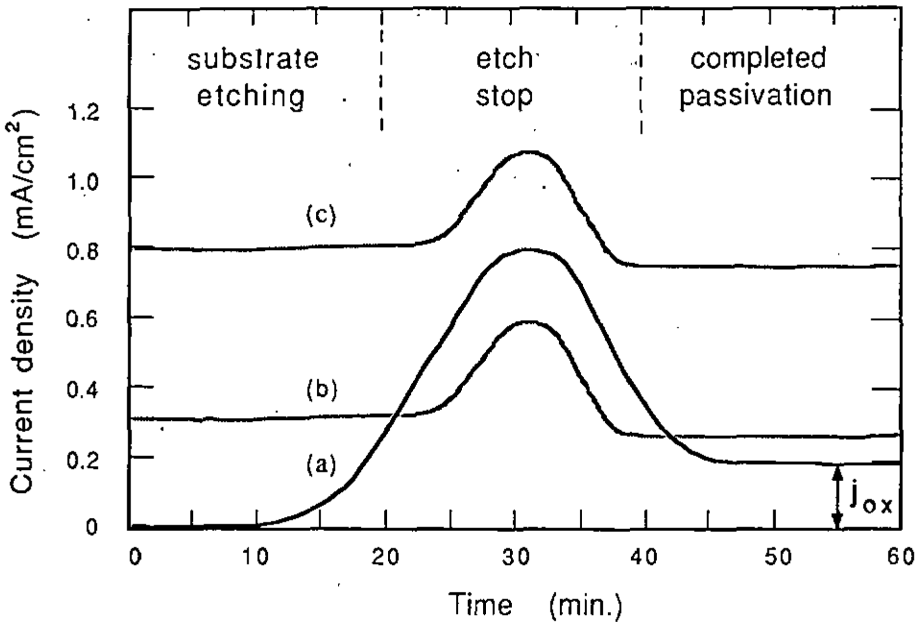


***Fig. 4.20** Currents recorded during four-electrode etch-stop:*
(a) Counter-electrode current of a wafer with minimal p/n diode leakage. j_{ox} is the current through the passivation oxide.
(b) Counter-electrode current of a wafer with a large p/n diode leakage current;
(c) Epitaxial layer current recorded simultaneously with (b).

As the current reflects the magnitude of the etch rate of the passivation oxide in KOH, the steady-state etch rate of the passivated n-type epitaxial layer (E_p) can be calculated by Faraday's law.

$$E_p = \frac{j_{ox} \cdot A \cdot AMU}{4 \cdot e \cdot \gamma_s} \tag{4.3}$$

In Eq.(4.3) it is assumed that all the current on a passivated membrane is used for the tetravalent oxidation of silicon (Si^0 to Si^{+4}); j_{ox} is the measured current density, A is the atomic weight of silicon (A = 28), AMU the atomic mass unit (1.6606 10^{-27} kg), e the elementary charge (1.60207 10^{-19} C) and γ_s the specific gravity of silicon ($\gamma_s = 2.33$). For a current density of 0.2 mA/cm^2, the etch rate is calculated to be 3.7 nm per minute. Thus, leaving the wafer in the KOH will hardly etch the membranes anymore and there is no danger of overetching or perforating the membranes.

For wafers where the diode leakage current is not negligible, a typical simultaneous recording of counter-electrode current and epitaxial layer current

(I_{CE} and I_E in Figure 4.12) is shown in Figure 4.20 (b) and (c) respectively. The discussion above still holds, except that the counter-electrode current during substrate etching is no longer zero. Even though the externally applied voltage to the substrate is still -1.5 V, a steady-state situation is established across the network of interdependent interfacial and bulk impedances such that the actual potential at the exposed substrate surface is more anodic than OCP. The working point has moved up to S* in Figure 4.21, and there is current flowing through the substrate/KOH interface. The substrate etch rate is slightly lower than in the ideal case (14 μm/h at -1.2 V as opposed to 16 μm/h at OCP, as can be read from Figure 4.8), but the etch process is not inhibited as long as the substrate surface potential stays sufficiently cathodic of the PP. If the diode leakage current is not too high, the voltage drop in the structure can be compensated for, by adjusting the external substrate potential applied by the potentiostat to values that are more negative than -1.5 V, until the counter-electrode current is tuned to zero and the etch rate is again maximal. The shapes of curves (b) and (c) are essentially identical; the

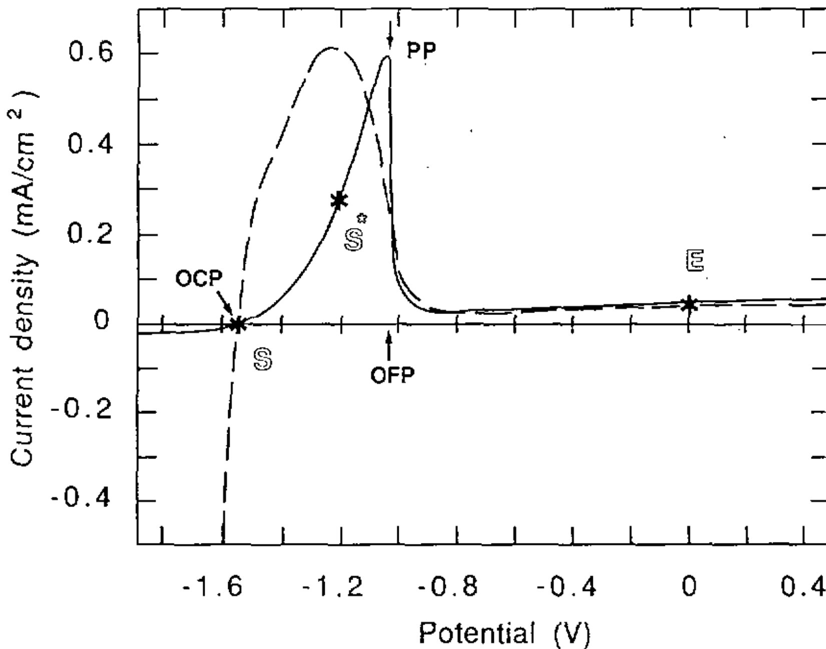


Fig. 4.21 Working points for four-electrode etch-stop, indicated on the i-V characteristics of p- and n-type <100> silicon (see Figure 4.2). S: (at OCP) working point for the p-substrate in the ideal case, S: working point for the p-substrate in case of a high diode leakage current, E: working point of the n-epitaxial layer.*

difference is the part of the diode leakage current that does not flow through the solution but goes through the substrate back to the negative lead of voltage supply V_E. Three-inch wafers with a total diode leakage current as high as 10 mA were etched successfully with the four-electrode etch-stop.

4.4 Conclusions

A large class of sensors and actuators use micromachined silicon structures as sensing or active elements. The miniaturization of these devices to an ever smaller scale increases the requirements for dimensional control of micromachined components such as membranes, cantilever beams, suspended masses, etc. An important method that has been employed in the fabrication of microstructures is the electrochemical etch-stop at a reverse biased p/n junction. In this chapter, this method has been studied.

In the first part of the chapter, the potential dependent etching and passivation behaviour of silicon in KOH at 60 °C was investigated. The i-V characteristics of the <100> and <111> surfaces and their sweep rate dependence were examined. A new sample preparation technique was employed, which ensured an accurately oriented <111> surface exposed to solution for measurement. There are many differences between the results of this work and those found in the literature. Still, in agreement with other researchers, our results suggest that more than one type of oxide may be involved. Of particular interest for the practical application of etch-stop was the determination of the passivation and oxide formation potential for p- and n-type silicon, and the etch rate for for both types as a function of applied potential.

In the second part of the chapter, the potential dependent etch behaviour of low doped silicon, was used to fabricate thin silicon membranes by p/n junction etch-stop. The original method was modified by controlling the potentials of both the epitaxial layer and the silicon substrate. All wafers that were etched with this four-electrode technique showed a successful etch-stop, including wafers with a large diode leakage current. In the latter case, the substrate was passivated when no substrate contact was provided (i.e., with two- or three-electrode methods), and no etching occured.

The performance of four-electrode etch-stop was characterized in detail. It was shown that the surface of etch-stopped membranes was very smooth (± 0.1 μm pp) and that their thickness can be controlled to within ± 0.2 μm s.d. The influence of the diode SCR width on etch-stop was investigated and it was concluded that it had no relevant effect on the membrane thickness. It was demonstrated that four-

electrode etch-stop is an easy-to-handle, yet powerful fabrication tool, which is extremely suitable for integration in an automatic fabrication control system: any wafer can be processed, no matter how poor its diode quality is; the presence of the current peak allows automatic end point detection and the overetch protection makes it an uncritical, and thus easy to handle, but still very well controlled process step.

Four-electrode etch-stop was used to fabricate membranes for piezoresistive pressure sensors. In the next chapter it will be shown that the pressure sensitivity of the devices could be controlled more accurately than when no etch stop is used.

It is noted that the advantage of electrochemical etch-stop is not only the thickness control of membranes and related structures; it also opens now possibilities that could not be realized with time etching. A three-dimensional diffusion pattern, for instance, can be etched out of silicon to remain as a free-standing structure by protecting it electrochemically from etching.

Chapter 5
Characterization of the sensor

5.0 Summary
5.1 Introduction
5.2 Measurement set-up
5.3 Pressure response
5.4 Temperature response
5.5 Conclusions

5.0 Summary

In this chapter, the output specifications of the fabricated piezoresisistive pressure sensor are presented and discussed. The response to differential pressure and the interference of temperature effects are treated. Wherever possible, a relation is established between the observed characteristics and the underlying physical principles (Chapter 2) and technical parameters (Chapters 3 and 4).

Parts of this chapter have been published in ref. [1-4]

5.1 Introduction

A major concern of future sensor research will be the elimination or reduction of drift and hysteresis of the sensor output parameters. Since the trend is to integrate sensor elements in computerized control systems, all reproducible imperfections and non-linearities of the complete system can be dealt with by one in-situ calibration cycle. By executing the calibration in-situ, the measurement system as a whole is calibrated, without making distinction between the individual elements that constitute the given configuration, of which the sensor chip is only one link in the chain. Thus time consuming individual calibration will no longer be needed, the only requirement being that each element satisfies a set of minimum-quality specifications that are reliable and stable in time. It is evident that such a strategy can only work if the fabrication processes guarantee a high reproducibility of the required specifications.

In this chapter, the output characteristics of the sensor will be presented and discussed. Although this chapter is not meant as an extensive statistical study, emphasis will be placed on the reproducibility of the parameters, obtained with the processes presented in the two previous chapters for the fabrication of the piezoresistive structure and of the thin silicon membrane. The first section treats the equipment that has been used to determine the sensor specifications, in particular a measurement station that has been developed to study the pressure response of the sensors on wafer, i.e. before dicing them into individual chips. The second section deals with the response of the sensor to applied pressure, and the differences between the three designs that have been realized. The zero-pressure offset, the pressure sensitivity and the linearity will be discussed. To evaluate the electrochemical etch-stop, the reproducibility of pressure sensitivity will be compared for wafers fabricated with or without electrochemical etch-stop. The last section, finally, discusses the temperature dependence of the output characteristics, which is a particular problem for piezoresistive pressure sensors. The temperature coefficient of the offset and of the sensitivity, as well as their hysteresis will be treated.

Note: in order to avoid too much cutting of the text, the tables with the results of the measurements that have been carried out have been grouped at the end of the chapter.

5.2 Measurement set-up

In microelectronic industry, the main functions of integrated circuits are tested on wafer in order to eliminate malfunctioning circuits before sending them through the packaging procedure. In the same way, a production line of sensors

has to provide a means to avoid the cost and time consuming encapsulation manipulations for sensor chips that would proof unusable afterwards. In this work, the basic elements for such a system have been developed and tested, not however by concern of mass production testing, but in order to have a means to test the bare silicon sensors and to avoid occasional influences of mechanical tensions introduced by packaging. An important part of the data presented in the next section were obtained on this system, in particular the results on pressure sensitivity and offset.

The goal was to build a regular wafer tester with needle contacts, and to extend it with equipment to apply a differential pressure to the sensors. For this purpose a hollow wafer holder was fabricated to form a regulated-pressure room. Holes were drilled from the surface to the cavity, aligned with the membrane positions of the wafer. One hole was provided for each cell of three pressure sensors. A grid of parallel canals on the top side of the holder allowed to keep the wafer on place by vacuum. The surface of the holder was polished to obtain a sufficiently hermetic seal when the (also polished) wafer was placed on it. It was found that extreme care and cleanness was required to maintain a constant pressure in the pressure circuit, which made the method rather unpractical. For convenience, only one hole in connection with the pressure cavity was maintained, and the wafer was shifted over this hole, for individual sensor measurements. The wafer was aligned to the hole by means of a stereomicroscope Zeiss DV4.

The pressure circuit consisted of the wafer holder cavity, connected with flexible tubes to a manual pressure regulator (Huber OM 120) and a high precision calibrated pressure balance (Huber PRD 3012.032.S). The electrical set-up consisted of a constant current source (HP 6177C) and a high impedance multimeter (HP 3478A). Both the pressure balance and the multimeter were interfaced to a computer (HP 9000 series 216) and an automatic data acquisition program was written.

Pressure sensitivity measurements were carried out by pumping the pressure circuit to the required maximum pressure, and introducing a small leakage in the system. While the pressure was allowed to decrease slowly, simultaneous pressure and voltage readings were recorded at regular pressure intervals. With this on-wafer system, sensor specifications were measured at room temperature.

For the temperature measurements, the wafers were diced and the sensors were mounted on a perforated TO-5 holder. The sensor was glued with the membrane positioned above the hole. Before sealing the cap hermetically onto the holder, it was also perforated and connected to a flexible tube which was introduced in the pressure circuit. The packaged sensors were then placed in a

ventilated oven with both heating and cooling equipment, allowing thus the measurement of the temperature coefficient of offset and pressure sensitivity.

5.3 Pressure response

5.3.1 Pressure sensitivity

In Chapter 3, Design and Fabrication, it was shown by Eq. (3.17), that the surface stress in the middle of the sides of the membrane is the square of the ratio membrane side (a) to membrane thickness (h). Since the resistance change and thus the pressure sensitivity is proportional to the stress in the membrane for an equal pressure (p) it was concluded from Eq. (3.2) and Eq. (3.18) that the pressure sensitivity (S) is also proportional to this ratio:

$$S = \frac{\Delta V}{V_b} \cdot \frac{1}{\Delta p} \quad \alpha \quad \frac{a^2}{h^2} \tag{5.1}$$

From Eq. (5.1) it is concluded that a good control of the membrane dimensions is required in order to obtain a reproducible sensitivity.

For the first generations of pressure sensors that have been fabricated in the course of this work, no automatic etch-stop was used to control the thickness of the etched membranes. After a long etch time, the wafers were taken out of the etch solution in order to determine the exact etch rate and the remaining etch time that was required. Although this method was rather laborious, reasonable results could be obtained if the taper of the wafers was not too important. A taper of 6 μm causes a thickness incertainty of about ± 3 μm. For a nominal thickness of 10 μm, this means a variation of ± 30 % (worst-case). According to Eq. (5.1), a pressure sensitivity variation of ± 60 % can then be expected. Table 5.1 shows the sensitivities of pressure sensors from one wafer, fabricated without etch-stop. The measurements were carried out on-wafer, with the equipment described in the previous section, at room temperature, with a constant voltage applied to the sensor bridges and for a pressure range from 0 to 300 mbar. The average sensitivities for Designs A, B and C (see Chapter 3) were 20.2, 22.4 and 25.8 mV/V bar respectively. Although the membranes were about 10 μm thick, the sensitivities were higher than the simulated values of Table 3.11. For the limited number of samples that have been measured (6 per design type), the standard deviation (σ) was about 20 %. If we roughly take 3σ to delineate the worst-case limits, then these measurements are in agreement with the 60% predicted by Eq. (5.1).

To show how these results can be improved when electrochemical etch-stop is applied to fabricate the membranes, let us first calculate the sensitivity variation that can be expected theoretically. In the previous chapter, a thickness standard deviation of 0.2 μm (2 %), as was measured. According to Eq. (5.1), this should cause a variation in pressure sensitivity of 4 %. However, the expected sensitivity variation is higher than 4 %, because etch-stop implies also a variation of the membrane side length if the taper of the wafer is taken into account. In regions where the wafer is thicker, etching will continue longer until the epitaxial layer is reached; the pyramidal structure formed by the <111> oriented side walls of the holes will be deeper and thus the resulting membrane area smaller. It is noted that this side length effect does not exist when no etch-stop is used, since in that case all etched holes have the same depth.

To determine the pressure sensitivity variation experimentally, pressure sensors were fabricated by means of four-electrode etch-stop. For 42 sensors the output characteristics were recorded on wafer, again at room temperature and for a pressure range from 0 to 300 mbar. Table 5.II presents the results of the measurements. The average sensitivities for the three designs were now 14.4, 16.9 and 19.9 mV/V bar, with standard deviations of only 1.2 mV/V bar. The epitaxial layer, and thus also the membranes, were 11.4 μm thick, which explains that the values were lower than the sensitivities of Table 5.I. Figure 5.1 gives a histogram of the results per design type.

The average values of the sensitivities given in Table 5.I (fabricated without etch-stop) indicate that design A would be the least sensitive and design C the most sensitive. However, the differences are of the order of 10 % and the standard deviation on the measurement is 20 %, so that we can not affirm this statement statistically. For the results of pressure sensors fabricated with etch-stop the same difference in sensitivity between the three designs is observed. In contrast to Table 5.I, however, the differences between the average values are now twice the standard deviation of the measurements so that the statistical evidence is stronger for these results. The differences are explained by the geometrical design specifications which were discussed in Chapter 3, section 3.4.2, and shown in Table 3.II. Design A uses larger resistors that reach out further away from the maximum stress region in the middle of the membrane side, whereas the other two designs are half as large, and thus more concentrated on high stress fields. In Design C, the nominal distance between the parallel resistors and the edge of the membrane is only 10 μm, as opposed to 20 μm for the two other designs, giving thus a higher pressure sensitivity. It was expected that, because of this smaller distance, Design C would be more sensitive to membrane side variations, and thus

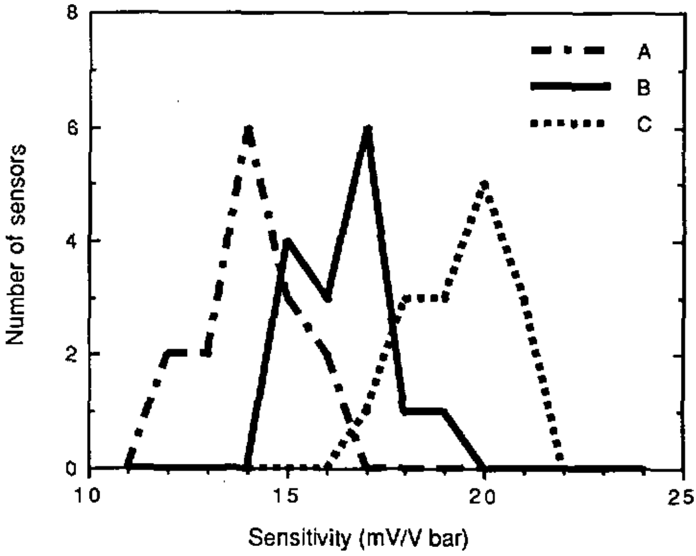


Fig. 5.1 Histogram of the pressure sensitivities in Table 5.II, per design type. The sensors were fabricated with electrochemical etch-stop.

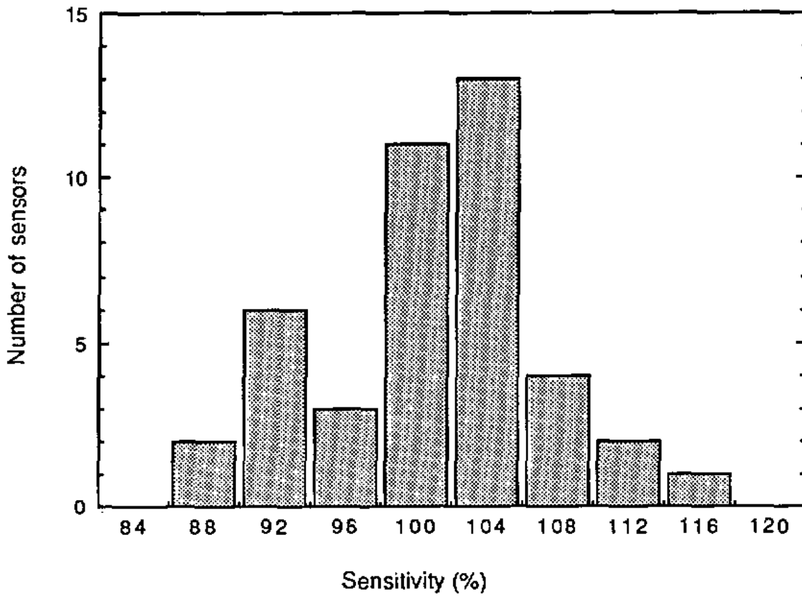


Fig. 5.2 Histogram of the pressure sensitivities in Table 5.II (sensors fabricated with etch-stop). Per design type the sensitivities are expressed relative to their average value.

result in less reproducible output characteristics. In the design phase, these three design alternatives with increasing pressure sensitivity and supposedly decreasing reproducibility were introduced to evaluate the best trade-off between these two specifications. Surprisingly, however, we learn from Table 5.I that the reproducibility of pressure sensitivity is comparable for the three designs; hence, Design C is concluded to be the preferred piezoresistor lay-out as far as pressure sensitivity is concerned.

To give an overall view of the reproducibility of pressure sensitivity, Figure 5.2 shows a histogram of the sensitivity of the 42 sensors, relative to the average value of the design type that the sensor belongs to. The combined effect of membrane thickness and side length variation is seen to give a standard deviation of the measured pressure sensitivities of only 7 %. This is three times better than the results of Table 5.1 and an even more important improvement compared to other series of piezoresistive pressure sensors, where the membranes were fabricated without electrochemical etch-stop and the sensitivity on one wafer could vary by a factor of 2 from one sensor to the other [1].

5.3.2 Zero-pressure offset

In Chapter 3 it was mentioned that in the first sensor designs, the bridge output for zero pressure applied was very large: about 20, 40 and 60 mV/V for designs A, B and C respectively. This offset was found to be due to the additional resistance from the cross-connection between the two perpendicular half-bridges. Through a series of new designs the offset could be reduced to lesser values. Table 5.III shows the offsets for sensors from the same wafer as those in Table 5.II, but the offsets were measured before the membranes were etched. Thanks to good resistor matching, the average offsets are very low for designs A and B. Design C, however shows an average offset of 4.2 mV/V. Table 5.IV gives the offsets of the same wafer again, but now after etching of the membranes. The results are visualized in the form of a histogram in Figure 5.3. Now the offsets of design A and B are around - 4 mV/V, and that of design C is less: - 1.4 mV/V. Interestingly, a systematic decrease of offset was observed between the measurements before and after etching of the membranes: -3.3, - 4.7 and - 5.6 mV/V for designs A, B and C respectively. Apparently, after etching the stress situation is changed by the interaction of stress in the membrane layers (thin silicon membrane, thermal oxide, aluminium, passivation oxide). For designs A and B, the offset introduced by residual membrane stress is much larger than the offset due to resistor mismatch and for design C they are of the same order of magnitude. Hence, better matching of the resistors will not decrease the offset anymore.

The standard deviation of the measurements is lower for design A, as is seen in both Table 5.III and Table 5.IV, and also in Figure 5.3. In Chapter 3, section 3.4.2 it was explained that the resistors of design A are twice as wide and long as the other two designs. It can now be concluded that an advantage of larger resistors is a better reproducibility of zero pressure offset, although the difference is probably not worth the loss of sensitivity, which is almost 30 % for design A compared to design C.

It is clear that the zero-pressure offset of the Wheatstone bridge can be turned down to zero by passive components or by an active circuit, as long as it is stable in time. The offset drift of the pressure sensors has been measured at the ETH Zürich [5] and was found to be less than 0.5 μV/V per hour for Design C.

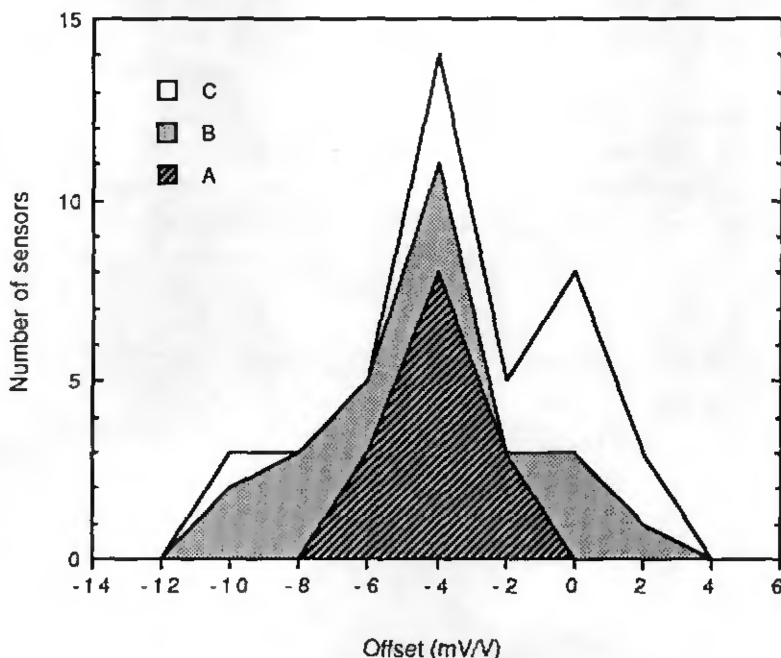


Fig. 5.3 Histogram of the zero-pressure offset of sensors from one wafer, per design type. The histogram is additional, i.e. the numbers of sensors of the three design types are added.

5.3.3 Non-linearity

The main source of non-linearity for piezoresistive pressure sensors is the increasing tensile stress on the membrane at high pressures. This is called the Balloon-effect, as explained in Chapter 3, section 3.3.5. For low pressure ranges, this effect is negligible. The sensors were designed so as to show no Balloon effect

to pressures up to 1 bar, a reasonable maximum for biomedical use. Figure 5.4 shows a typical calibration curve for the pressure sensors. A straight line was drawn through the measurements by means of the least square approximation and the correlation factor between applied pressure and sensor output was calculated to be 1.

Non-linearitiy can be defined in many ways. In this work, the definition illustrated in Figure 5.5 was used: the sensor output was measured for five pressures, including zero and the maximum pressure (P0 to P4). A straight line was drawn through P0 and P3. The diffences between this line and the actual readings at P1, P2 and P4 were divided by theoutput at P4. The absolute value of the maximum of these three relative differences was defined as the non-linearity of the pressure response. Table 5.V shows the non-linearities for 8 pressure sensors measured at Keller AG für Druckmesstechnik [6], for the pressure ranges 0 - 400 mbar and 0 - 800 mbar. The average four-point non-linearities defined as discussed before, were 0.07 % and 0.2 % respectively.

Figure 5.6 shows the four-point non-linearity as a function of the pressure range for one pressure sensor. When the pressure range mounts up to 16 bar, the non-linearity is seen to increase to almost 4 %. As pointed out in Chapter 3, the maximum pressure for which a sensor is designed is limited by the required

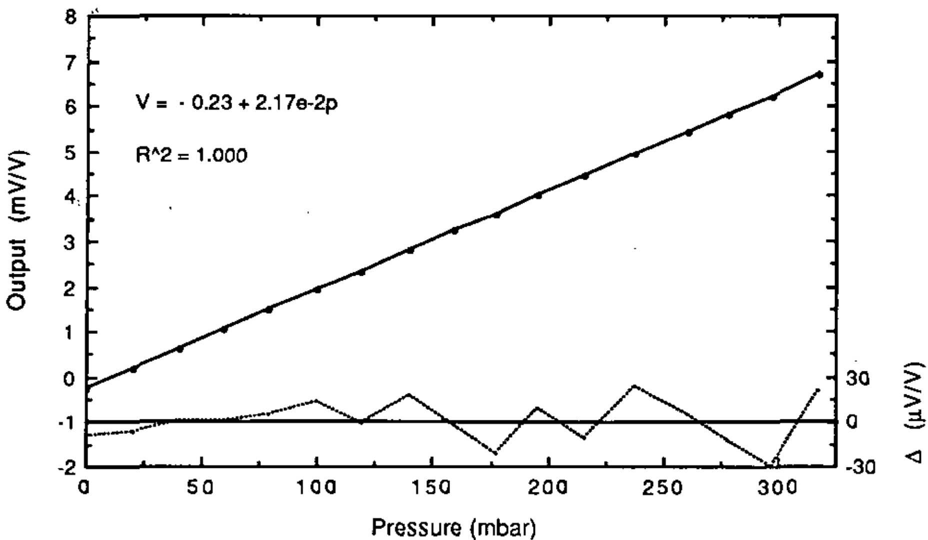


Fig. 5.4 Wheatstone bridge output versus applied pressure for the fabricated piezoresistive pressure sensors.

linearity in the range of operation, and not at all by rupture of the silicon membrane. For the present sensors with 520 μm membrane side length and 10 μm thickness, pressures up to 20 bar were applied without breaking the membrane. It is evident, however, that at this pressure the response is no longer linear because of the Balloon-effect. It is noted that non-linearity, like the zero-pressure offset discussed before, is one of these specifications that could easily be compensated for with a digital control system. This would increase the useful pressure range significantly, without loss of sensitivity.

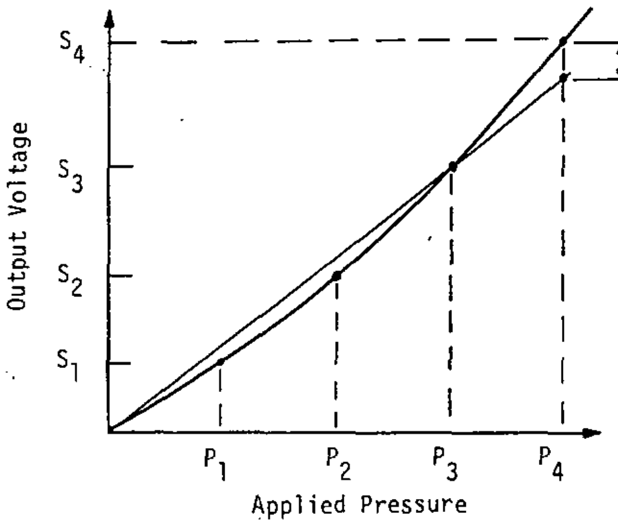


Fig. 5.5 Definition of non-linearity used in this section.

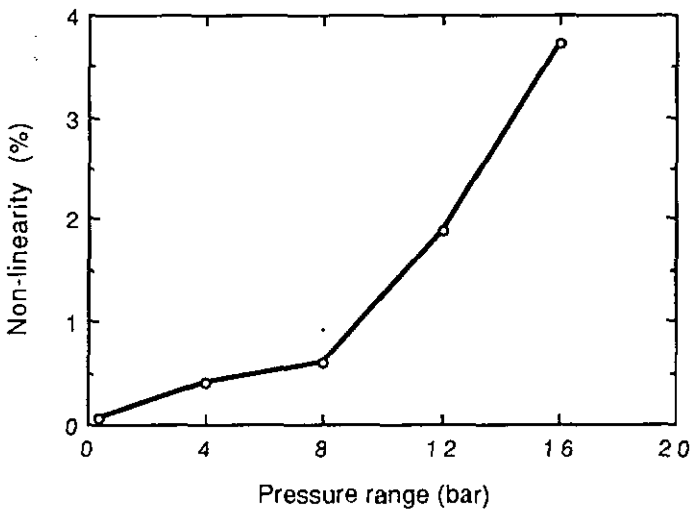


Fig. 5.6 Non-linearity of the pressure response as a function of pressure range.

5.4 Temperature dependence

5.4.1 Temperature coefficient of the piezoresistors (TCR)

In this section, the temperature dependence of the pressure sensors will be discussed. First, the temperature behaviour of individual resistors (TCR) is considered, then the temperature coefficient of the Wheatstone bridge offset when no pressure is applied (TCO), and finally the dependence of the pressure sensitivity (TCS).

Figure 5.7 shows a typical measurement of the resistance of one piezoresistor as a function of temperature, from 20 to 80 °C. A parabolic curve fit is drawn through the measurement points. Also shown are the equations and correlations of the linear and the parabolic curve fit obtained by least-square approximation. The correlation is seen to be better for the parabolic approximation, from which it is concluded that the curve is slightly parabolic. The temperature coefficient of this resistor (TCR), calculated from the linear approximation, was 707 ppm/°C. Table 5.VI presents the temperature coefficients of eight resistors from different sensors. The measurements were done at Ascom Favag S.A. [7]. The TCR at 20 °C was calculated from the derivative of the parabolic curve fit at 20°C, divided by the resistance at that temperature; the "average" TCR was the slope of the linear approximation, divided by the resistance at 20 °C. The average temperature

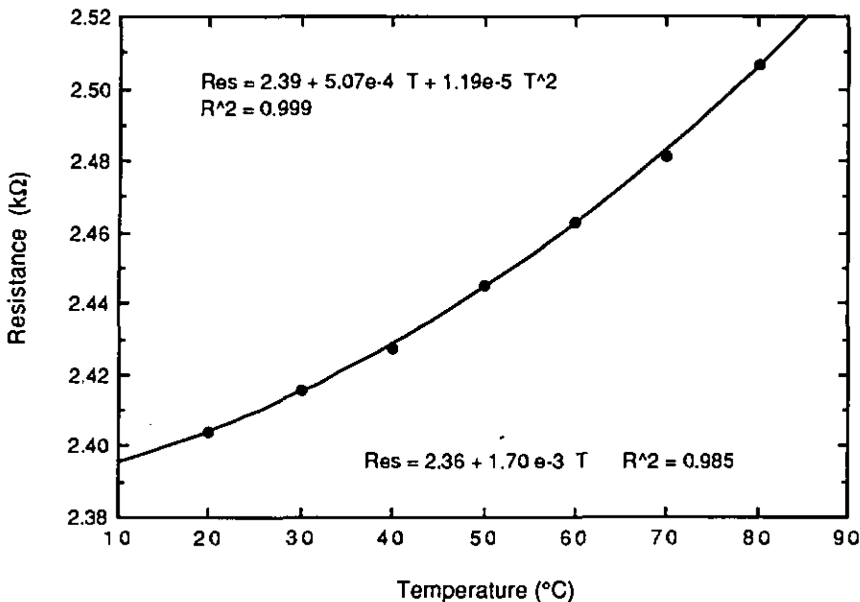


Fig. 5.7 Typical recording of the resistance of a piezoresistor as a function of temperature, and the linear and parabolic least-square approximations.

coefficient at room temperature was low, about 410 ppm/°C or less than 0.5 %/°C. Over the entire temperature range (20 to 80°C), the average TCR of the 8 resistors was 658 ppm/°C ± 87 ppm/°C (s.d.).

5.4.2 Temperature coefficient of offset (TCO)

In theory, the Wheatstone bridge output at zero pressure is independent of temperature if the four resistors have equal (not necessarily zero) temperature coefficients. Indeed, in this ideal case, temperature variations have a common-mode effect but do not influence the differential output of the bridge. We show this here for the simplified (but realistic) case where resistors in opposite arms of the Wheatstone bridge (opposite sides on the membrane) are equal, but different from resistors in touching arms by a value r, as shown in Figure 5.8. For this configuration, the offset (V_o) per volt applied to the bridge (V_b) is:

$$O = \frac{V_o}{V_b} = \frac{r}{2R+r} \qquad (5.1)$$

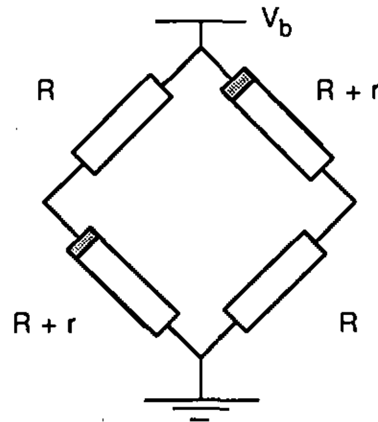


Fig. 5.8 Wheatstone bridge with symmetrical mismatch of the resistors.

The temperature dependence is easily calculated to be:

$$\frac{\partial O}{\partial T} = \frac{2(\dot{r}R - r\dot{R})}{(2R+r)^2} \qquad (5.2)$$

where a point on the variable denotes the derivative with respect to temperature. Now, if the resistors have equal temperature coefficients, then

$$\frac{\dot{r}}{r} = \frac{\dot{R}}{R} \qquad (5.3)$$

and Eq. (5.2) becomes zero, i.e. the offset is insensitive to temperature changes, no matter how large the mismatch (r) is.

In reality, however, the offset is temperature dependent, partly because the temperature coefficients of the resistors are not equal and partly because stress is introduced by thermal expansion of the different layers that constitute the membrane. Since in the discussion about the offset in the previous section, it was found that residual membrane stress largely contributes to the room temperature offset, it is expected that thermal expansion will also determine the TCO.

Figure 5.9 presents a typical recording of offset versus temperature. The offset is seen to decrease as a parabolic function. Table 5.VII lists the temperature coefficients of five different sensors. The TCO at 20°C is the derivative of the parabolic least-square curve fit. Also listed are the linear temperature coefficients for the interval 0°C to 75°C. The first sensor in Table 5.VII has both a higher offset and a higher TCO than the following four. It is possible that this correlation occurs systematically. Although, if a sensor has a low offset because the residual stress effect and the resistor mismatch cancel one another, the TCO will not necessarily be low. However, no measurements have been carried out to study this statistically. The average of the linear TCO's of the four sensors with comparable offset was 25 μV/V °C. With a pressure sensitivity of 20 mV/V bar, this is equivalent to 1.25 mbar/°C. This temperature dependence is not negligible, and for accurate measurements passive or active compensation circuitry is required.

Table 5.VII includes the TCO of two chips where the membranes were not etched. As discussed before, the offset itself is lower than that of the etched sensors, in this case about an order of magnitude better. But what is more important here, the TCO is seen to be less than 1 μV/V °C or 30 to 40 times smaller than for the sensors with membranes. This observation confirms that the TCO is basically due to the deformation of the thin silicon membranes and not to the temperature coefficient of the resistors.

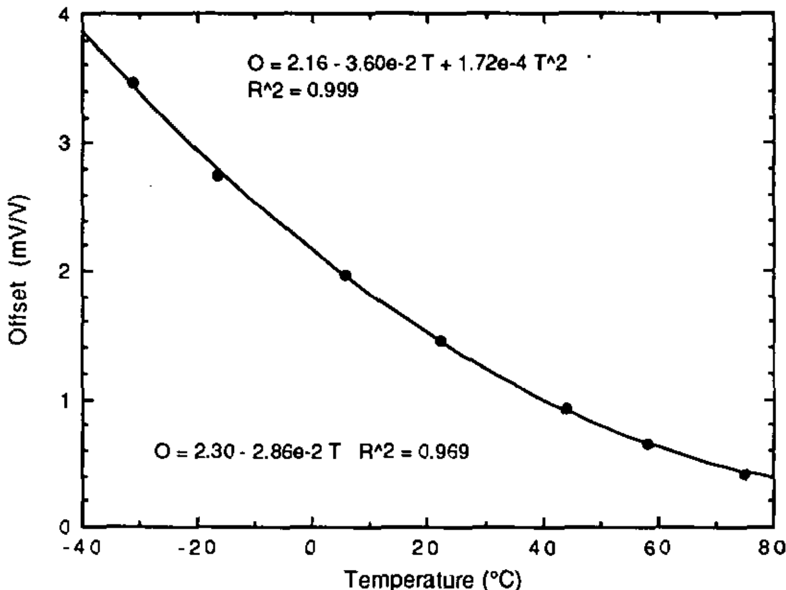


Fig. 5.9 Typical recording of the zero-pressure offset as a function of temperature, and the linear and parabolic least-square approximations.

5.4.3 Temperature coefficient of pressure sensitivity (TCS)

The pressure sensitivity depends on temperature, if not by anything else, then at least through the temperature dependence of the piezoresistance coefficients discussed in Chapter 2. The temperature coefficient of the sensitivity has been measured with a constant current applied to the Wheatstone bridge (TCS_i) and with a constant voltage applied (TCS_V). The measurements were carried out on four sensors. At temperature intervals ranging from -30°C to 90°C, the pressure response was recorded from 0 to 300 mbar. For each sensor two tables were then established giving the temperature and the corresponding sensitivity at constant current and at constant voltage. Figure 5.10 shows typical recordings for the two cases. From these tables, the temperature coefficients were calculated. The results are shown in Table 5.VIII. At constant current, the temperature dependence was observed to be parabolic, at constant voltage, the linear correlation was much better. Therefore the TCS_i was calculated as the derivative of the parabolic curve fit at 20°C, divided by the pressure sensitivity at 20°C. For the TCS_v, the slope of the linear approximation was divided by the pressure sensitivity at 20°C.

The values in Table 5.VIII show that the TCS_i at room temperature is systematically lower than the TCS_v. The average values are - 0.17%/°C and - 0.20%/°C respectively. It is noted that at higher temperatures, the TCS_i becomes even smaller because of the parabolic shape of the function. The difference is explained by the fact that, at constant bridge current, the voltage over the bridge increases with temperature due to the positive TC of the resistors. This effect enhances the pressure sensitivity and thus partly compensates for the loss of sensitivity due to the negative TC of the piezoresistance coefficients. At constant voltage, this internal negative feedback does not occur. It is noted that this effect also explaines the more parabolic shape of the TCS_i, since theresistors were seen to have a parabolic dependence of temperature. Mathematically the temperature coefficients can be derived as follows:

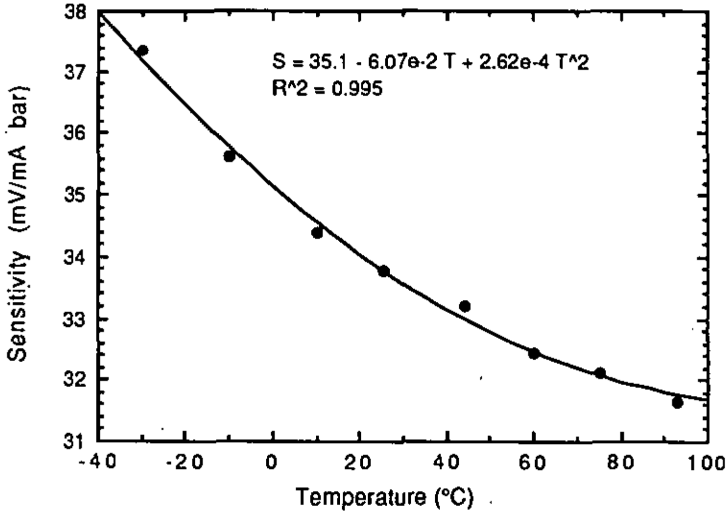
For constant bridge voltage:

Combining Eq. (3.2) and (3.5) gives the following expression for the pressure sensitivity:

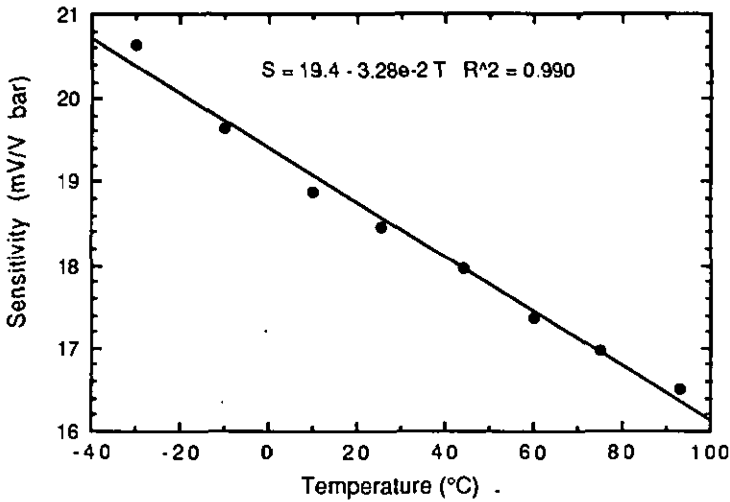
$$S = \frac{1}{2\,\Delta p}\,\pi_{44}\,(\sigma_l - \sigma_t) \tag{5.4}$$

Temperature dependence of S:

$$\frac{\partial S}{\partial T} = \frac{\sigma_l - \sigma_t}{2\,\Delta p}\,\frac{\partial \pi_{44}}{\partial T} + \frac{\pi_{44}}{2\,\Delta p}\,\frac{\partial(\sigma_l - \sigma_t)}{\partial T} \tag{5.5}$$



(a)



(b)

Fig. 5.10 Pressure sensitivity of the piezoresistive pressure sensors as a function of temperature. (a) Measurement at constant Wheatstone bridge current; (b) measurement at constant voltage.

Hence: $$TCS_v = \frac{1}{S}\frac{\partial S}{\partial T} = \frac{1}{\pi_{44}}\frac{\partial \pi_{44}}{\partial T} + \frac{1}{\sigma_l - \sigma_t}\frac{\partial(\sigma_l - \sigma_t)}{\partial T} \tag{5.6}$$

Eq. (5.6) means that the TC of the pressure sensitivity is determined by the TC of π_{44}, and by thc temperature dependence of the membrane stress. Since the latter has proven to be of importance for the TCO, the influence cannot be excluded a priori from the calculations.

For constant bridge current:

For a constant current, the pressure sensitivity was defined as the change of output voltage per unit bridge current and per unit pressure. Eq.(3.3) and (3.5) are then combined to:

$$S = \frac{1}{2\,\Delta p}\, R\, \pi_{44}\, (\sigma_l - \sigma_t) \tag{5.7}$$

In Eq. (5.7), R appears, and thus the temperature coefficient of the piezoresistors will occur in the expression for TCS_i:

$$TCS_i = \frac{1}{S}\frac{\partial S}{\partial T} = \frac{1}{\pi_{44}}\frac{\partial \pi_{44}}{\partial T} + \frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{\sigma_l - \sigma_t}\frac{\partial(\sigma_l - \sigma_t)}{\partial T} \tag{5.8}$$

The first two term in Eq. (5.8) are of opposite signs (the TCπ is negative and the TCR is positive) so that they compensate each other. The effect of the compensation depends on the relative magnitudes of the terms. Table 5.VIII gives an average value of - 0.20 %/°C for TCS_V and -0.17 %/°C for TCS_i. The compensating effect of the bridge resistance is thus +0.03 %/°C, which is not very high. This value compares well with the temperature coefficient of the resistors (TCR) which was found to be +0.04 %/°C at 20°C (Table 5.VI). It is noted that it is possible to realize a low TCS by choosing the doping concentration and junction profile of the piezoresistors so as to achieve a better matching of the two involved temperature coefficients. If they are exactly equal, they completely cancel each other.

In order to evaluate the contribution of membrane stress to the TCS, we have to compare it with the temperature coefficient of the piezoresistive coefficients (TCπ - the first term in both Eq. (5.6) and (5.8)). For a doping concentration of 10^{19} cm^{-3}, the literature mentions a TCπ of -0.19 %/°C [8], from which is concluded that the influence of thermal stress on the TCS is minimal. Apparently, the stresses introduced by thermal expansion define the pre-stress situation at each temperature, and thus the zero-pressure offset, but have no influence on the pressure sensitivity.

If the temperature behaviour of the pressure sensitivity is predominantly determined by the piezoresistance coefficients (in particular for constant bridge

voltage), then the shape of the temperature curves should be similar for both. In Chapter 2 it was said that, around room temperature, the piezoresistance coefficients vary with 1/T (section 2.5.2). Therefore, Figure 5.10 (b) is redrawn, with the sensitivity expressed as a function of 1000/T (T in Kelvin). This is illustrated in Figure 5.11, which shows a R^2 of 0.997 for the linear curve fit. Although more data are required to support this statistically, Fig. 5.11 tends to confirm the thesis that the TCS of the sensors can be described mainly in terms of the TCπ, and that, in contrast to the TCO, thermal stress is less important.

It is concluded from this discussion that the temperature coefficients of the pressure sensitivity measured at constant bridge voltage are in good agreement with the theoretical value, and that the TCS is reduced if the Wheatstone bridge is operated at constant current, although this effect is rather small for a piezoresistor doping concentration of 10^{19} cm^{-3}.

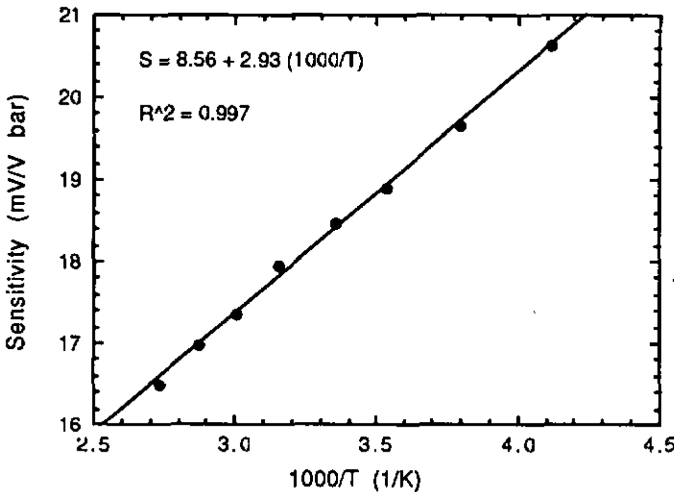


Fig. 5.11 Pressure sensitivity as a function of the inverse of the temperature, for the same data as presented in Fig. 5.10(b).

5.4.4. Temperature hysteresis

During the temperature characterization of the sensors, an unwelcome characteristic was revealed, that is temperature hysteresis in the Wheatstone bridge output, especially in the resistance and the zero-pressure offset. The latter is illustated in Figure 5.12. When the temperature was increased from room temperature, the zero-pressure offset was observed to decrease with a slight parabolic curvature, as discussed earlier. After cooling down the sensor, the

room-temperature offset was larger than before. Then, while further cooling down, the values increased with, again, a parabolic curvature, but now convex in the other direction. To characterize the hysteresis, four sensors were put in a furnace and the temperature was stepped up and down between four temperatures and the offset was measured, after a stabilization time of at least 6 hours at each temperature. The results for one sensor are shown in Figure 5.13. In the beginning , the temperature was stepped from 22°C to 56°C, further to 80°C and then back, passing again over 56°C. No appreciable hysteresis was observed. However, when the maximum temperature was 100°C instead of 80°C (right half in Fig. 5.13), a clear hysteresis occured, shown by the offset values at 56°C, which were alternatively reached after increasing and decreasing temperature. The difference between the two values was 3% of the offset at 56°C.

Since in general the thermal history of a sensor is not known, temperature hysteresis is a highly undesirable feature. The explanation must be sought in the plastic deformation of one of the layers on the membrane. The material with the lowest yield strenght that is involved is aluminum. Gardner et al. [9] discuss the mechanical stress in aluminum as a function of temperature. The authors stated that film deformation is difficult to avoid since the difference in the linear expansion coefficients is large for aluminum versus silicon. They found that

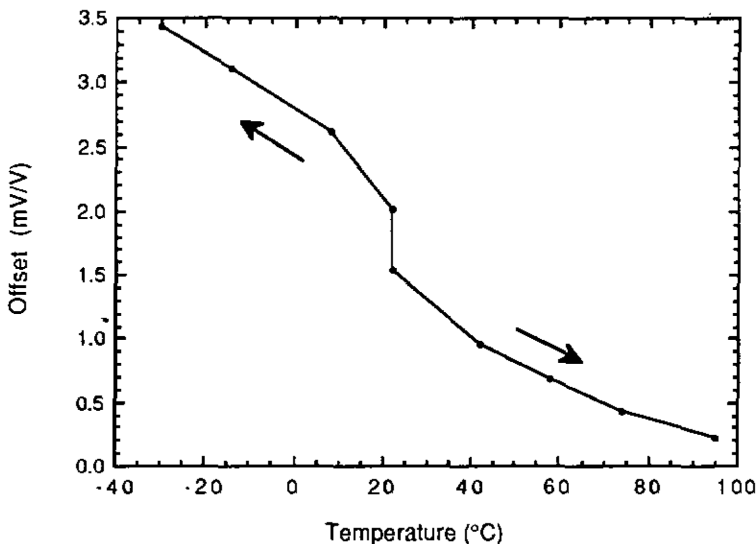


Fig. 5.12 Hysteresis, demonstrated by the measurement of the offset as a function of temperature. The arrows indicate the direction of the temperature changes.

thermally activated dislocation glide occured at 100°C.

Based on this knowledge, three solutions are possible to eliminate the hysteresis. The first is to harden the aluminum film to increase its yield strenght and extend the region of elastic deformation to stresses higher than the ones that occur by thermal expansion. This could be done by doping or by quenching the aluminum. Such treatments hinder the movement of dislocations by blocking them at the impurities or at the small grain boundaries. A second possibility is to use another metal or alloy with higher yield strength. The third solution finally is to remove the aluminum layer from the membrane and replace it by diffused silicon conductors. By applying this last method in a new sensor generation designed and fabricated by Ascom Favag Microelelectronics, the problem of hysteresis was effectively dealt with.

It is noted that, since thermal hysteresis, just like thermal expansion, is a prestress effect, it was observed to have repercussions on the resistor values and on the offset, but not on the pressure sensitivity.

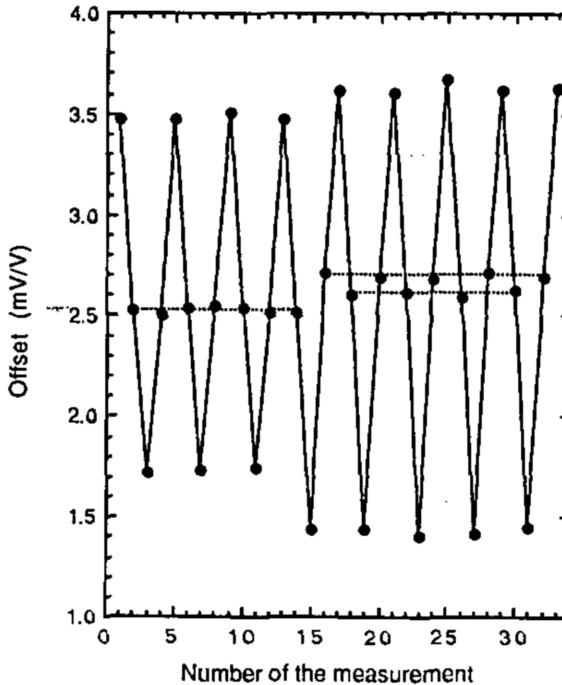


Fig. 5.13 Hysteresis measurements by stepping the temperature between 0°C, 56°C and 80°C (left half - without hysteresis) and 0°C, 56°C and 100°C (right half - with hysteresis).

5.5 Conclusions

The output characteristics of piezoresistive pressure sensors were evaluated. Attention was paid to the influence of the lay-out differences and of the electrochemical etch-stop on the specifications.

The different lay-outs gave different pressure sensitivities, as predicted by computer simulations. The only advantage of the version with the largest resistors was a better reproducibility of the offset (but not a lower offset). However, this is not worth the loss in sensitivity inherent of this lay-out. Design C, with the resistors closest to the membrane edge, gave the best sensitivity and the lowest offset. Hence this is the preferred lay-out. The specifications of desing C are summarized in Table 5.IX.

The benefits of the etch-stop for the thickness control of the thin membranes were demonstrated by the reduction of the pressure-sensitivity variations across the wafer. Without etch-stop, the sensitivity on one wafer could vary by a factor of 2 from one sensor to the other. With etch-stop the pressure sensitivity of devices fabricated on the same wafer could be controlled to within ± 7 % s.d.

The non-linearity of the response was less than 0.2 % for the pressure range 0 to 800 mbar, and was found to increase rapidly for pressure ranges higher than 8 bar.

In the discussion of the influence of temperature on the sensor specifications, the temperature coefficients of the resistors (TCR), the zero-pressure offset (TCO) and the pressure sensitivity (TCS) were investigated and discussed. The TCR and the TCO, as well as the TCS when measured at constant bridge current, were observed to be parabolic. Moreover, the TCO was concluded to be determined mainly by the pre-stress introduced by the thermal expansion of the different membrane materials, whereas the TCS was solely dependent on the TC of the piezoresistive coefficients.

Table 5.1 Pressure sensitivity (in mV/V bar) measured on wafer, for the three sensor designs discussed in chapter 3, belonging to one cell. The membranes of these sensors were fabricated without electrochemical etch-stop.

Cell	Design type		
	A	B	C
23	25.3	24.4	27.0
25	19.2	24.6	25.3
44	25.3	28.7	33.7
48	20.3	22.2	26.6
67	15.8	16.6	19.1
69	15.2	17.8	23.3
Average	20.2	22.4	25.8
σ	4.4	4.6	4.8

Table 5.II Pressure sensitivity (in mV/V bar) measured on wafer, for the three sensor designs discussed in chapter 3, belonging to one cell. The membranes of these sensors were fabricated with electrochemical etch-stop.

Cell	Design type		
	A	B	C
1	12.4	15.2	18.0
2	13.6	15.4	18.2
3	15.3	17.8	21.1
4	14.2	17.1	20.8
5	15.6	17.3	20.2
6	15.1	17.5	21.7
7	16.7	18.4	20.9
8	14.6	17.4	20.7
9	13.2	15.2	21.1
10	14.4	16.9	17.9
11	14.1	16.7	20.8
12	14.3	16.8	19.5
13	16.0	19.4	19.6
14	14.7	17.7	19.9
Average	14.4	16.9	19.9
σ	1.2	1.2	1.3

***Table 5.III** Zero-pressure offset (in mV/V) per design type, measured on wafer before etching the membranes.*

Cell	Design type		
	A	B	C
1	- 3.93	3.17	- 0.38
2	- 1.10	- 0.70	5.40
3	- 0.73	- 4.46	4.24
4	0.00	-6.41	-2.80
5	- 2.14	- 3.47	1.70
6	- 1.45	-3.36	7.47
7	0.55	1.54	7.27
8	- 1.67	0.00	- 4.92
9	- 3.54	- 5.17	4.79
10	0.00	2.74	15.83
11	4.69	- 0.38	10.35
12	0.19	4.61	8.50
13	- 0.99	- 3.49	4.04
14	0.75	3.88	4.48
15	0.55	5.88	- 2.98
Average	- 0.59	0.07	4.20
σ	2.0	3.9	5.5

Table 5.IV Zero-pressure offset (in mV/V) per design type, measured on wafer after etching of the membranes. The bottom row (Δ) gives the difference of the average values with the corresponding values of Table 5.III (offset before etching of the membranes).

Cell	Design type		
	A	B	C
1	-2.2	-5.2	-3.2
2	-5.3	-11.0	-3.2
3	-3.3	+0.5	-3.7
4	-5.2	-6.9	-9.8
5	-5.0	-10.5	+0.3
6	-3.5	-3.5	-0.2
7	-2.9	+0.9	-2.8
8	-3.3	-7.5	+2.0
9	-5.4	-7.2	+1.0
10	-4.6	-4.0	+0.7
11	-2.5	+1.7	-1.7
12	-3.9	-7.7	+2.0
13	-4.4	+0.9	+0.7
14	-3.2	-4.9	+105.4
Average	-3.9	-4.6	-1.4*
σ	1.1	4.2	3.2*
Δ	-3.3	-4.7	-5.6

* For the average offset and the standard deviation of bridge C, the extremely deviating value of cell 14 is not considered.

Table 5.V Non-linearity of the pressure response according to the definition given in Fig. 5.5.

Sensor	Non-linearity (%)	
	0- 400 mbar	0-800 mbar
14B	0.09	0.35
37B	0.08	0.19
37C	0.04	0.07
46C	0.03	0.13
67B	0.07	0.19
73B	0.10	0.42
83C	0.09	0.05
92B	0.05	0.17
Average	0.07	0.20
σ	0.03	0.13

Table 5.VI Temperature coefficients of eight piezoresistors from different sensor bridges, calculated from resistance measurements between 20 and 80 °C. The TCR at 20 °C is the derivative of the parabolic approximation divided by the resistance at that point. The "average" TCR (third column) is the slope of the linear approximation, divided by the resistance at 20 °C.

Sensor	Temperature coefficient (ppm/°C)	
	TCR (20°C)	TCR (av.)
1	265	659
2	553	777
3	409	707
4	441	565
5	215	515
6	414	715
7	474	616
8	512	711
Average	410	658
σ	116	87

Table 5.VII Offsets and temperature coefficients of offset (TCO), calculated from offset measurements between -30 and 75 °C. The TCO at 20 °C is the derivative of the parabolic approximation. The "average" TCO is the slope of the linear approximation between 0 and 75 °C. The last two rows are data from chips on which the membrane was not etched.

Offset (mV/V)	Temperature coefficient (μV/V°C))	
	TCO (20°C)	TCO (av.)
12.3	- 50	- 44
3.5	- 33	- 27
3.4	- 31	- 25
2.0	- 29	- 23
3.7	- 32	- 25

Unetched chips:

- 0.38	-	- 0.8
0.41	-	- 0.6

Table 5.VIII Pressure sensitivities of four sensors and their temperature coefficient, measured with constant Wheatstone bridge current (I = ct) and with constant voltage (V = ct).

Sensitivity (mV/V bar)	Temperature coefficient (%/°C)	
	TCS (V=ct)	TCS(I=ct)
15.0	- 0.20	- 0.17
15.1	- 0.19	- 0.16
16.8	- 0.22	- 0.18
18.7	- 0.17	- 0.15
Average	- 0.20	- 0.17

Table 5.IX Summary of the output specifications of Design C. Error values represent the standard deviations of the measurements.

Chip dimensions:	1.1 mm x 3 mm x 0.4 mm
Membrane dimensions:	520 μm x 520 μm x 10 μm
Piezoresistors:	4 x 2 kΩ
Pressure sensitivity:	(20 ± 1.3) mV/V.bar
Output offset:	(- 1.5 ± 3) mV/V
Non-linearity:	less than 0.1% to 400 mbar
	less than 0.2% to 800 mbar
Membrane rupture:	more than 20 bar
Temperature coefficients:	
of resistors (TCR):	(658 ± 87) ppm/°C
of offset: (TCO):	-1.2 mbar/°C
of sensitivity: (TCS):	- 0.2 %/°C

Chapter 6
Biomedical applications

6.0 Summary
6.1 Introduction
6.2 Pressure sensor for heart catheter
6.3 pH-pressure sensor for stomach catheter
6.4 Force sensor for muscle catheter
6.5 Conclusions

6.0 Summary

In this chapter, three catheter devices are discussed that use the piezoresistive effect to measure pressure or force for medical diagnosis purposes. In the first application, the pressure sensor described in the previous chapters is built in a heart catheter. The second example concerns a new sensor containing a pressure and a pH sensitive part combined on one chip, for esophageal studies. The third sensor is a force-sensitive beam structure for use in a muscle catheter.
Parts of this chapter have been published in ref. [1-3]

6.1 Introduction

Mainly because of their size, a typical application field for integrated sensors is the biomedical world, and more precisely the in-vivo determination of physical and physiological parameters. One important parameter is the pressure of body fluids. To define the place of piezoresistive pressure sensors in this specific area, as opposed to capacitive sensors, three specifications have to be considered, i.e. size of the sensor chip, ease of read-out and power consumption. Capacitive pressure sensors require on-chip read-out circuitry, but they have a low power consumption. Therfore, they are suited for long term implantation, where the chip cost is of less concern then the load of the battery. Piezoresistive sensors on the other hand generally consume more power, but they are cheap to fabricate in mass and easy to read-out. Moreover the dimensions of piezoresistive sensors can be made smaller, because capacitive sensors need a rather large area for the capacitor. Therefore, the future of piezoresistive pressure sensors is in cheap disposable catheters for invasive measurements with external power supply. The first section of this chapter shows how the pressure sensor discussed in this work can be applied for that purpose by mounting it in a 6F heart catheter.

Two more applications are presented in this chapter concerning catheters that contain sensor chips which are based on the technology developed in the previous chapters and where also other criteria as those mentioned above are involved. The first is an 8F double-lumen catheter for the investigation of the esophageal function. A new sensor chip was designed for this application, using a double-side integration technique specially developed for this purpose, and the back-side contact technology. It consists of a pressure sensing part and a pH sensing part. The advantages of the sensor design with back-side contacts are outlined. In-vitro and preliminary in-vivo experiments are presented, which show satisfactory results for simultaneous pressure and pH measurements.

The second example is a 4F muscle catheter, developed to measure pressures and forces in the muscle tissue. Here the special feature is the very small lateral dimension of the sensor chip.

6.2 Pressure sensor for heart catheter

Classical heart catheters are essentially tubes filled with a physiological solution that is in contact with the blood through a flexible membrane in the catheter tip. The pressure is measured externally at the other end of the catheter. This system works well for static pressures, but fast pressure changes are damped by the pliancy of the catheter walls. Evidently, this problem does not occur if the

pressure is measured and transformed to an electrical signal, directly in the catheter tip [4-8].

The pressure sensor presented in this work was mounted in a 6F catheter (2 mm outer diameter) by Keller AG für Druckmesstechnik (Winterthur). The catheter tip was made of stainless steel and the tube of polyurethane. The catheter head without polyurethane tube is shown in Figure 6.1. The piezoresistors are turned toward the inside of the catheter, and only the membrane cavity is exposed to the external environment.

The catheter has been tested in-vitro, dry and in physiological salt solutions. The stability was proven to be satisfactory: less than 1 mbar drift in 42 hours. So far the catheter has not been used for in-vivo experiments.

Fig. 6.1 Piezoresistive pressure sensor mounted in a 6F heart catheter.

6.3 pH-pressure sensor for stomach catheter

6.3.1 Introduction

At present, esophageal catheters only allow the measurement of either pH (acidity) or pressure separately. For some studies and diagnoses however, the measurement of both simultaneously is felt as a need to obtain a more complete image of the pysiological phenomena involved [9-11]. One important application is the investigation of the lower esophageal sphincter (the ring-shaped muscle that by contraction closes the acces to the stomach), and in particular the reflux of

stomach acid into the esophagus that occurs if this muscle is malfunctioning. Diagnosis is complicated by the fact that the symptoms are often intermittent and are triggered by stimuli like stress or temperature extremes. Another interesting application for medical and pharmacological research is the dynamic and chemical activity of certain medicines and drugs. The advantage of having a pressure sensor at the same time, is that also informations about the movement of the esophageal tract are obtained.

Today's commercially available esophageal catheters for pH monitoring, use either antimony or glass electrodes. Antimony electrodes have the advantages that they are small and very cheap, and thus suited for disposable use. On the other hand, however, they are inexact and suffer from ageing and hysteresis, since their electrode reaction is essentially a corrosion process. Moreover, at low pH values there is an accumulation of reaction products around the electrode, which causes false pH readings. Glass electrodes are exact to a tenth of a pH or better, and stable. The disadvantages are that they are fragile and that they have a high impedance. Still, for the moment the glass electrodes are the most reliable devices that are on the market, but if they have to be combined with pressure sensors, their size increases, causing thus a lot of discomfort for the patient who recieves the catheter through his nose. Compared with these existing systems, the silicon based sensor has the advantages of small dimensions, good accuracy and stability, and above all, a vast flexibility to integrate two or more sensors on one chip and on more sites in the catheter. In this section, a silicon based pH-pressure catheter (double-lumen), with the possibility for the integration of a reference electrode in one lumen, is discussed.

6.3.2 Sensor chip fabrication

The sensor chips are fabricated by standard microelectronic and micromachining processes on double-side polished, 3 inch wafers (boron-doped, 3-5 Ωcm, 380 μm thick). A very special feature of this chip is that components are integrated on both sides. This is because one of the major design goals was to locate all the contact pads on the back side of the chip, since it has to be mounted in a catheter. Therefore the pressure sensor is integrated on the back side and the pH ISFET, which must be exposed to the solution, on the front side, but with contact feed-throughs through the chip, as is shown schematically in Figure 6.2. The dimensions of the chip are 1.5 mm by 4.0 mm.

The pressure sensor consists of four boron-diffused piezoresistors at the edges of a thin membrane and connected in a Wheatstone bridge configuration. The output voltage is proportional to the pressure difference across the membrane and

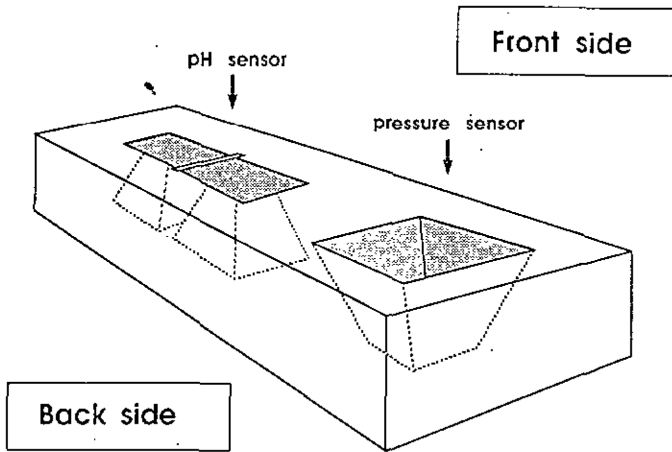


Fig. 6.2 Transparent scheme of the combined pH-pressure sensor .

to the applied bridge voltage. The membrane is etched in potassium hydroxide from the front side of the wafer and its thickness is controlled by a four-electrode electrochemical etch-stop, as described in Chapter 4. A 10 μm thick epitaxial layer of n-type silicon is grown on a p-type silicon substrate. The p-type substrate is etched and etching is stopped at the epi-layer/substrate junction by applying a passivating potential to the epi-layer. The thickness of the remaining silicon membrane is thus defined exactly by the thickness of the epitaxial layer and not influenced by the taper of the wafer.

The pH ISFET fabrication resembles the standard fabrication process [12] with one exception, i.e. the location of the drain and source contacts. Under the source and drain regions, holes are etched from the back side of the wafer, leaving a membrane of about 10 μm thick. A high phosphorous diffusion through this membrane, covered with aluminum establishes the electrical contacts to the source and drain from the back side of the chip.

6.3.3 Catheter encapsulation

The pH-pressure chip is mounted in a double lumen 8F catheter (2.7 mm diameter). Figure 6.3 shows the important advantage of the back-side contacts: this approach allows the sensitive part to be almost at the same level as the outside surface of the catheter, avoiding thus the presence of a cavity in the tip, where local pH could differ from the effective pH in the stomach. The gate of the pH sensor and the back side of the pressure membrane are directly in contact with the solution. The catheter contains seven wires: four wires to contact the pressure

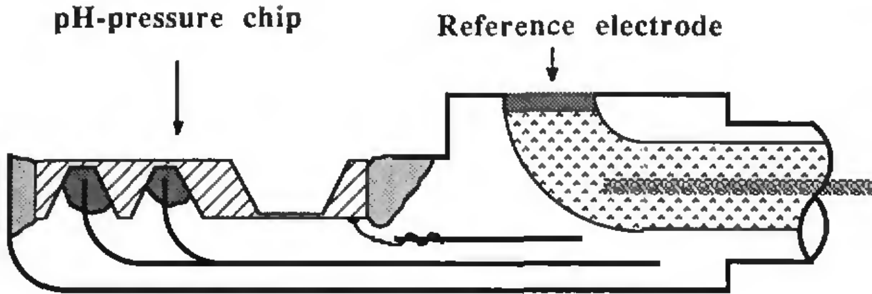


Fig. 6.3 Cross-section of the catheter tip, showing the chip encapsulation.

sensor, two for the pH ISFET and one for possible integration of an Ag/AgCl reference electrode in the second lumen. The chips were mounted in the catheter by Keller AG für Druckmesstechnik (Winterthur). Figure 6.4 Shows a photo of the catheter tip.

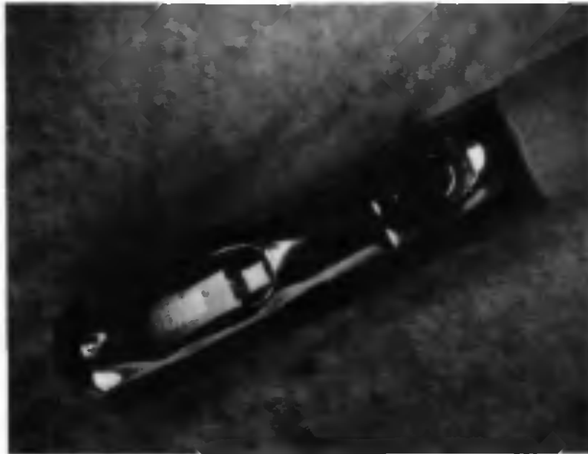


Fig. 6.4 Photograph of the pH-pressure chip mounted in the catheter.

6.3.4 Measurement set-up

For the in-vitro measurements the catheter was inserted in a vertical flexible tube that was consecutively filled with different pH buffer solutions. The upper liquid level was varied to yield pressure variations in the order of 100 mbar. Thus pressure and pH could be measured simultaneously. Merck pH buffer solutions were used. The pH was measured with an in-house built ISFET amplifier: a feedback control system that applies a constant V_{DS}, measures I_{DS} and adjusts V_{GS} through an Ag/AgCl reference electrode, in order to keep this I_{DS} constant. V_{GS}

is then proportional to the pH of the solution. The pressure was measured with a Wheatstone bridge amplifier supplied by Keller AG.

For the in-vivo measurements only battery powered equipment was used: a portable in-house built ISFET amplifier with skin reference electrode, a Keller DPM 80 Wheatstone bridge amplifier and MIC GastrograpHs to obtain digital recordings of the measurements. The sensors were routinely calibrated before use.

6.3.5 Results and discussion

In-vitro measurements have shown that the pressure sensor had good linearity and a sensitivity of 8 mV/V.bar. The pH sensor had a sensitivity of 56 mV/pH and a stability better then 0.2 mV/h. Preliminary in-vivo measurements were carried out at the Insel Spital in Bern, in the stomach of a normal volunteer. A typical simultaneous recording of pressure and pH is shown in Figure 6.5. At the same time a glass pH-electrode (Ingold) was inserted in the stomach and the readings were observed to be parallel, with only slight differences between both electrodes caused by their different positions in the stomach. One of the advantages of the

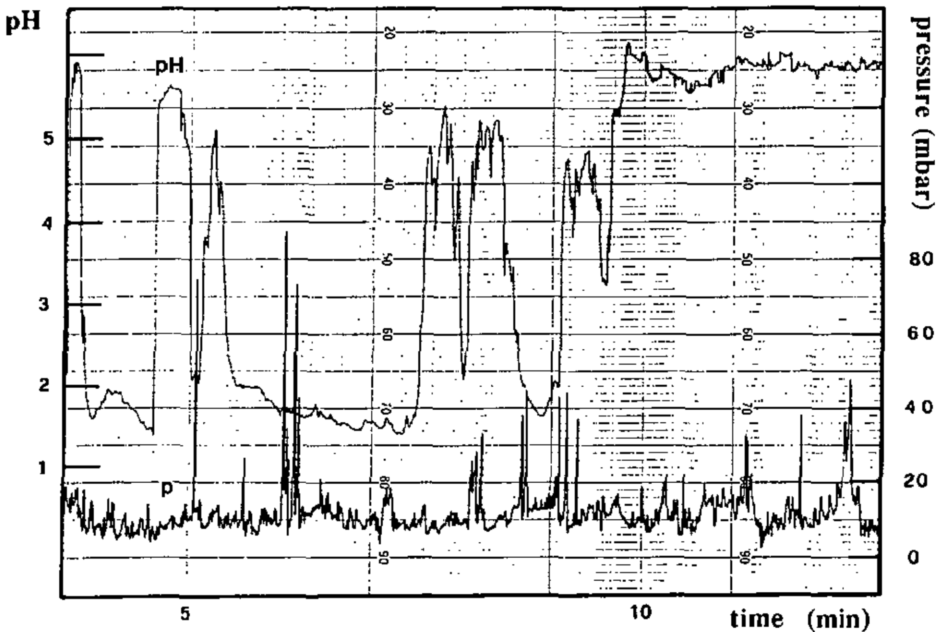


Fig. 6.5 Simultaneous recording of pressure and pH in the stomach of a normal volunteer.

pressure recording is that the moment when the catheter passes through the sphincter can be determined exactly.

6.3.6 Conclusion

The in-vitro characteristics of the pH-pressure sensor are comparable to equivalent single transducers. The integration of pH and pressure sensors on one chip, with back-side contacts, enables an easy catheter mounting and adequate encapsulation. To obtain better spatial information, more measuring sites in the catheter are feasible. The integration of a reference electrode has been tested in-vitro. The first in-vivo tests with skin electrode showed good response for both pH and pressure recordings.

6.4 Force sensor for muscle catheter

6.4.1 Introduction

The activity of muscles can be investigated by inserting a thin catheter longitudinally into the muscle bundle. A force sensor in the side-wall of the catheter gives information on the lateral action of the muscle. A sensor chip was designed to replace an older system where minuscule strain gauges were glued on a beam. Its fabrication involved individual assembling of each sensor and laborious handling of the microscopic parts. Evidently this application is a typical challenge for integrated sensor technology. This section presents a first generation of this type of sensors, to show the feasibility of fabricating silicon integrated force sensors with very small lateral dimensions.

6.4.2 Chip fabrication

The chip had to be designed to be mounted in a 4F catheter (1.3 mm outer diameter). Its dimensions were limited at maximum 0.6 mm width and 6 mm length. A mesa was required on one end of the chip, to touch the thin membrane in the catheter opening, as shown schematically in Figure 6.6. The chip thickness was 0.2 mm, and the total thickness of the chip and the mesa was 0.4 mm. The operational range was 40 mN and the maximum allowed deflection of the beam 0.05 mm. If the beam deflects too much, then the muscle tissue presses on the border of the catheter opening, and not on the mesa anymore. To increase the force sensitivity, a cavity was etched under the resistors. It is easily calculated that the sensitivity is proportional to the inverse of the square of the remaining thickness. The only restriction is the deflection at maximum force. It was

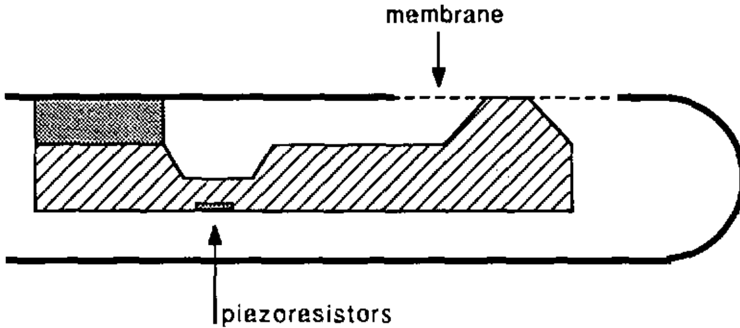


Fig. 6.6 Cross-section of the force sensor and the catheter encapsulation.

calculated that a thickness of 100 μm would give a beam deflection at 40 mN of less than 50 μm.

The sensors were fabricated on three-inch phosphorous doped silicon wafers of (100) orientation. The nominal thickness was 381 μm and the resistivity 1 - 10 Ωcm. The fabrication sequence was similar to that of the pressure sensors (cfr. Chapter 3), with the exception of the doping concentration of the piezoresistors. Since no Wheatstone bridge configuration was used for these sensors, the doping concentration was chosen high, $2 \cdot 10^{20}$ cm^{-3} at the surface, in order to reduce the temperature dependence of the piezoresistance coefficients (cfr. Figure 2.9). The sheet resistivity was 20 Ω per square. After fabrication of the piezoresistors, the wafers were etched in 40% potassium hydroxide at 60°C, to obtain the chip profile that is illustrated in Figure 6.6. The etching was done in two steps: first the aforementioned cavity was etched, and then the oxide mask was removed, except on the mesas, to etch the chip to the required thickness of 200 μm. Finally the wafers were diced into individual sensors. Figure 6.7 shows the design of two sensor types that were realized; one was 0.6 mm wide and the second only 0.3 mm.

6.4.3 Measurement set-up

For in-vitro measurement, the sensors were glued on a PCB in a way that allowed vertical deflection of the beam. A special measurement set-up was developed to measure simultaneously the force applied on the mesa, the deflection of the beam and the resistor change. For this purpuse, an 1-DIM displacement sensor (Cary Compar, Le Locle) was mounted vertically on a support. In the sensor head, an inductive stylus was suspended on two horizontal spring blades with a precisely known spring constant. The 1-DIM head could move vertically,

and a second discplacement sensor allowed to measure its movement. When the stylus just touched the beam, the applied force was zero and the reading of the displacement of the stylus (caused by its own weigth) was set to zero. When the I-DIM head was moved down, the applied force and the stylus displacement were read from the display. The deflection of the beam was the difference of the readings of the I-DIM and the second discplacement sensor. In this way increasing forces were applied and the corresponding resistance changes and deflections were measured.

For the temperature characterization, the PCB-mounted force sensors were placed in a furnace. The sensitivity was measured by a two-point calibration, using a known weigth.

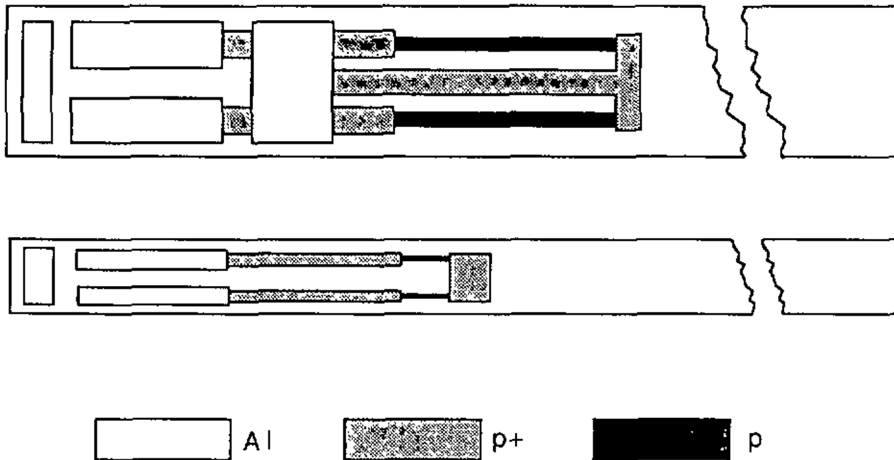


Fig. 6.7 Two designs of the force sensor: one with a chip width of 0.6 mm (upper), and one of 0.3 mm (lower).

6.4.4 Results and discussion

This paragraph summarizes the results of the measurements on four sensors. No functional differences were observed between the two sensor types (0.6 mm and 0.3 mm). Figure 6.8 shows a typical recording of the resistance change and the deflection of the beam as a function of applied force. The sensitivity was 0.5 Ω/kΩ mN. For a range of 40 mN, this results in a full scale resistance change of 20 Ω/kΩ. The deflection at 40 mN was 34 μm, which is within the required specification limit of 50 μm. It is noted that the sensitivity could be increased by taking a lower doping concentration for the resistors. For the used concentration the longitudinal piezoresistance coefficient in the <110> direction was $30 \cdot 10^{-11}$

Pa^{-1}, as opposed to e.g. $50{\cdot}10^{-11}$ Pa^{-1} for a doping concentration of 10^{-19} cm^{-3}. However, that would be at the expense of a higher temperature coefficient. In the interval from room temperature to 70°C, the temperature coefficient of the resistors (TCR) was measured to be 1400 ppm/°C and of the sensitivity (TCS) - 1700 ppm/°C.

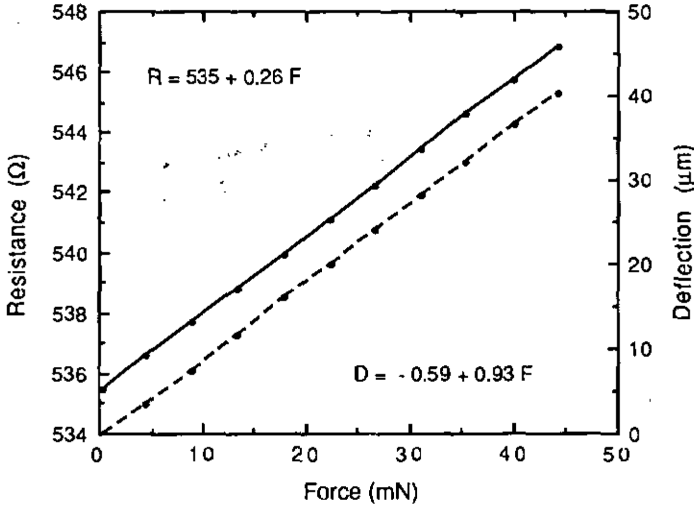


Fig. 6.8 Resistance change (——) and beam deflection (- - -) as a function of applied force.

6.4.5 Conclusion

The chip presented in this section was mainly a feasibility study as a first step towards a more sophisticated device. In particular temperature compensation was completely lacking on this chip. Because of the small dimensions (especially for the 0.3 mm chip), it is hardly possible to integrate two supplementary transverse piezoresistors and build a Wheatstone bridge as for the membrane pressure sensors described in Chapter 3. A full bridge would require the two transverse resistors to be placed on one line and besides the longitudinal ones, in order to sense the same mechanical tensions.

A valuable solution of this problem that requires only longitudinal resistors and still includes temperature compensation is proposed here. If two identical pairs of longitudinal resistors are integrated on both sides of the chip, as schematically shown in Figure 6.9, then deflection of the chip causes the two resistors on one side to increase and the two on the other side to decrease. As for the pressure sensors, the four resistors can be connected in a Wheatsone bridge configuration,

and temperature changes will in first order be a common mode effect and will not appear at the differential output of the bridge. Using the double-side integration and back-side contact technologies which were developed for the pH-pressure chip, such a force sensor can easily be fabricated with very small lateral dimensions. To decrease the size of the contact feed-throughs, very thin wafers should be used (100 to 150 μm thick).

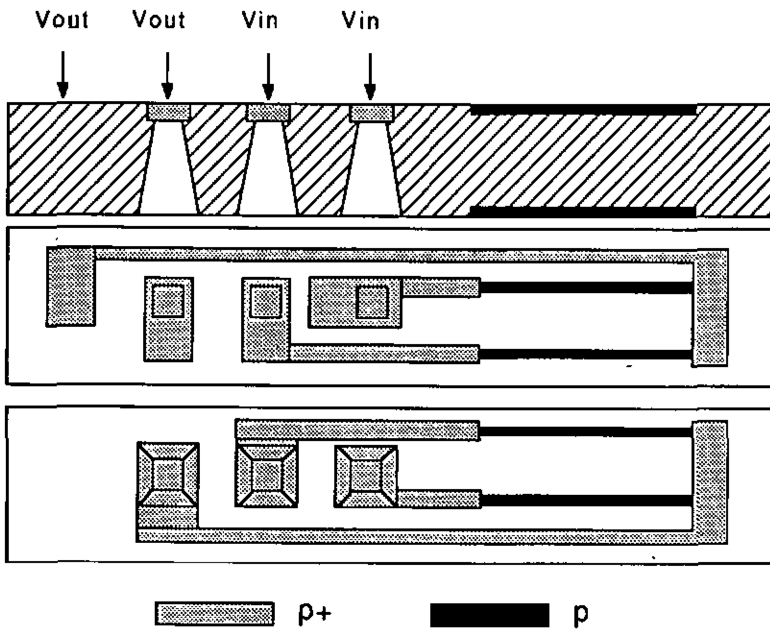


Fig. 6.9 Design proposition for a very narrow force sensor, using double-side integration and back-side contact technologies (the figure does not show the Al contact pads).

6.5 Conclusions

Many classical systems for medical diagnosis can be miniaturized effectively by the introduction of silicon integrated sensors. Moreover, the performance of the sensors is often better than that of the classical devices, and even new possibilities are created. This has been shown in this chapter by three examples of sensors that were mounted in catheters for invasive use in the human body. Common features of the three sensors are miniaturization, mass production and low cost.

A piezoresistive pressure sensor in the tip of a heart catheter improves the dynamical performance compared to classical systems. Mass production makes the sensor chip very cheap.

Integration in silicon allows the combination of more than one sensor of different type on one chip. Collaboration with pH-sensor specialists has lead to the realization of a combined pressure-pH sensor for esophageal studies. The device has been tested in-vivo giving very satisfactory results. The double-function catheter causes less discomfort to the patient than the insertion of two catheters. Moreover new information can be obtained, e.g., the moment when the pH-sensitive part crosses the sphincter can be determined accurately.

It is noted that this chapter was not concerned with the technique of building the sensor chips into the catheter. This still requires individual and often laborious treatments, where a number of problems remain to be solved, especially the lifetime of the encapsulations.

Chapter 7
Conclusions

The goal of this thesis was the study and the design of piezoresistive pressure sensors, and the compatibility study of the fabrication process with the electrochemical etch-stop technique. The conclusions at the different stages of the development have been summarized at the end of each chapter. An overview of the most interesting conlusions is given here. In addition, some improvements are suggested that could be introduced in the sensor design, and by the integration of on-chip circuitry. Applications of the developed technologies are briefly discussed, and the last word is given to the ever growing possibilities of silicon micromachining.

Piezoresistive sensor fabrication and characterization

The discussion started with an overview of the piezoresistance effect in monocrystalline silicon. The consequences for sensor design concerned the choice of doping impurity type, concentration and profile. For the crystal orientation imposed by anisotropic etching of the membranes, p-type resistors showed a higher longitudinal piezoresistance coefficient than n-type. Further, the choice of the concentration was determined by the magnitude and the temperature dependence of the piezoresistive coefficients. Higher concentrations yield a lower pressure sensitivity, but at the same time a lower temperature dependence. As a compromise, a boron concentration of 10^{19} at/cm^3 was chosen. Finally it was pointed out that shallow implanted resistors resulted in better sensitivity than diffused, especially if very thin membranes were used. By means of computer simulations and test samples, the implantation parameters were determined to fit the desired piezoresistor specifications: 10^{19} at/cm^3, 200 Ω per square and 0.6 μm junction depth.

The positions of the piezoresistors on the membrane were studied by means of computer simulations. The resistors are located near the middle of the membrane edges, since that is where mechanical stresses are maximal. For maximal

sensitivity, the perpendicular resistors were designed as two half-resistors, placed parallel to each other. For symmetry reasons, also the parallel resistors were cut in two, but placed on one line. Three configurations were fabricated with slightly varying lay-outs, in order to investigate experimentally the influence of resistor dimensions and distance to the membrane edge on the sensor specifications and especially their reproducibility.

An important parameter is the thickness of the silicon membrane. Serious effort has been spent on the study of thickness control by electrochemical etch-stop. A preliminary investigation on the etch behaviour of low doped silicon under electric bias has allowed to determine open-circuit potential, passivation potential and Flade potential for <100> and <111> oriented n- and p-type silicon in 40% KOH at 60°C. Other interesting results were revealed, some of which were in contradiction to the literature. For <100> silicon it was found that the formation of a passivating oxide occurs beyond (i.e. anodic of) the classically defined passivation peak, and this new potential was called oxide formation potential (OFP). Cathodic of the open circuit potential, the etch rate dropped down for p-type silicon, but not for n-type silicon. This property opens the possibility to perform etch-stop on a p-type epitaxial layer deposited on an n-type substrate. For <111> silicon, the i-V curves were sweep rate dependent even before passivation, which indicated the presence of a surface bound layer with fixed charge density. That layer was proposed to convert to oxide after passivation.

The knowledge of the etch behaviour of silicon was applied to the fabrication of thin silicon membranes by electrochemical etch-stop at a reverse biased p/n junction between an n-type epitaxial layer and a p-type silicon substrate. The commonly used three-electrode method was extended with a fourth electrode to control the potential of the substrate, and this set-up was characterized in detail. The smoothness of the etch-stopped surfaces was ±0.1 μm peak-to-peak, and the thickness was controlled to ± 0.2 μm s.d. It was found that the width of the diode space charge region had no influence on the thickness of the membranes. Further, the advantages of electrochemical etch-stop as a fabrication technique were pointed out: easy to carry-out, high fabrication yield, excellent thickness reproducibility, automatic end-point detection and overetch protection.

The study of the pressure response of the sensors has shown that neither the dimensions of the resistors, nor the distance to the membrane edge had a relevant influence on the output specifications or on their reproducibilities, except, of course, on the pressure sensitivity. Hence, the design with the smallest resistors which were closest to the edges was concluded to be the preferred configuration.

Owing to the etch-stop of the membranes, the reproducibility of the pressure sensitivity was better than ± 7% s.d. on a wafer, as opposed to a factor of two or more if no etch-stop was used. The temperature characterization of the sensors has proven that the temperature coefficient of the sensitivity was only determined by the inevitable TC of the piezoresistance coefficients, whereas the TC of the zero-pressure offset was mainly due to thermal expansion of the different layers that constitute the membrane. It was also confirmed that a constant bridge current allowed to reduce the TC of the sensitivity compared to constant voltage supply, although for the given doping concentration and junction profile, the improvement was only minor: less than 20%. A complete overview of the measured output specifications was given in Table 5.IX.

Improvements to be studied

At this stage, the performance of the pressure sensors is very satisfactory, but it is evident that improvements can always be conceived of, especially to reduce the temperature coefficients, the major problem for piezoresistive pressure sensors. Two (not mutually exclusive) paths can be followed. One is to work further on the design and the technology of the sensors, and the other is to integrate electronics on the sensor chip. The choice of whether or not the improvements are worth the effort depends on the intended application. If the sensor will be part of a complete automatic control system, then its imperfections can easily be compensated for off-chip, as long as they are known (calibrated), and stable in time. If, however, the sensor is meant for independent use, the recommended way to go is to get the best out of the technology and to adjust the last imperfections by on-chip circuitry.

Concerning the temperature effects, it was mentioned that thermal expansion of the membrane layers was responsible for the temperature coefficient of the zero-pressure offset, even if the offset itself is very small at room temperature. A detailed study of the thermomechanical behaviour of the layers, now thermal and CVD oxides, and of technological design alternatives should allow to reduce the TCO. Further, modifying the junction profile of the resistors should permit to decrease the TC of the sensitivity, although this will probably be at the expense of the magnitude of the sensitivity itself.

At the end of chapter 3 it was mentioned that Ascom Favag Microelectronics has developed and characterized a bipolar process in (100) silicon, compatible with the sensor fabrication. In the course of this work, the first ideas for on-chip electronics have been worked out. In particular, an operational amplifier with very low offset and temperature coefficient of the offset was designed and

fabricated [1], and thick film circuits have been designed. More work is required here to adapt the circuit to the sensor specifications.

Applications

Piezoresistive pressure sensors can be applied in many domains. The last chapter has presented three applications where the sensors were mounted in the tip of a catheter for biomedical diagnosis purposes. It was pointed out that in this field, solid state sensors, and in particular piezoresistive sensors incorporate important advantages: the measurement site is in the tip of the catheter, which eliminates the transfer function of the catheter tube which deforms the measurements in systems were the pressure is registrated outside of the cathteter. Further they can be fabricated in high volumes and very cheap, which makes them suitable for disposable use. Finally it was shown that it is possible to integrate more than one sensor type in the catheter tip, which allows the recording of different physiological parameters simultaneously, without causing much supplementary discomfort for the patient.

Silicon micromachining

The fabrication of thin membranes for pressure sensors is only a basic example of the possibilities silicon micromachining. Armed with a broad set of technologies for both monocrystalline silicon (isotropic and anisotropic etching, boron and electrochemical etch-stop, silicon fusion bonding) and polysilicon (sacrificial layer technolgy), the micromechanical design engineer has a large freedom to conceive and realize microscopic mechanical parts for a variety of applications. It is expected that new developments in microengineering will continue to show up, leading to exciting realizations that were never possible before.

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