

## MICRO POWER “RELATIVE PRECISION” 15-BIT A/D CONVERTER

L. Grisoni, A. Heubi, S. Grassi, P. Balsiger, F. Pellandini

Institute of Microtechnology  
University of Neuchâtel  
CH-2003 Neuchâtel-Serrières  
Switzerland

A. Schaub

Audiosys AG  
Sunnenbergstr. 20  
CH-8633 Wolfhausen  
Switzerland

### ABSTRACT

State of the art A/D converters are still critical in power-sensitive, battery-operated equipment like hearing aids. In this article, a new approach is presented that features excellent signal quality, 85 dB dynamic range equivalent to a 15-bit output word, 16 kHz sampling rate, 25  $\mu$ W power consumption, and 0.54 mm<sup>2</sup> chip area. Compared to standard components, the enormous power savings result from a sophisticated circuit design which limits the signal to quantization noise ratio to roughly 40 dB. Subjective listening tests prove, however, that the resulting signals are hardly distinguishable from their unprocessed versions, a remarkable fact due to masking effects inherent in the human auditory system.

### 1. INTRODUCTION

Research of digital hearing aids has been a topic of growing interest for more than two decades. Although the high flexibility inherent in digital signal processing algorithms looks promising, technological constraints have prevented a breakthrough so far. A major reason is the increased power requirements of a digital signal processing unit. Finally, there is a need for additional A/D and D/A converters which also require careful design with respect to power consumption.

A concept for a “floating point” or “relative precision” A/D converter was published in [1] in 1992. The main idea was to adaptively scale the input signal in such a way that most of the time, it would fit well to the fixed conversion range of a rather coarse quantizer. Scaling gain and quantizer output were subsequently combined in order to properly represent the signal sample within the full dynamic range of the acoustic input signal.

The emphasis of the former design clearly lay on saving as many bits in the quantizer as possible while still maintaining an adequate signal quality. Recent studies aiming at a hardware realization reveal that it is advantageous to provide for a finer quantization, thus improving the resulting signal to quantization noise ratio. But at the same time, a much simplified combinatorial circuit (combining scaling gain and quantizer output) is introduced, and the overall minimum power requirements are thus preserved.

This paper is organized as follows: parts of the converter published in [1] are quickly reviewed in Section 2. Section 3 explains the improvements that have been accomplished in the meantime. Sections 4 and 5 deal with particular aspects of hardware realization, and Section 6 concludes the discussion.

### 2. SCHAUB’S A/D CONVERTER

Figure 1 shows the front end stage of Schaub’s “relative precision” A/D converter. The converter produces 14-bit output words, thus covering a signal range of approximately 80 dB as required for hearing aids.

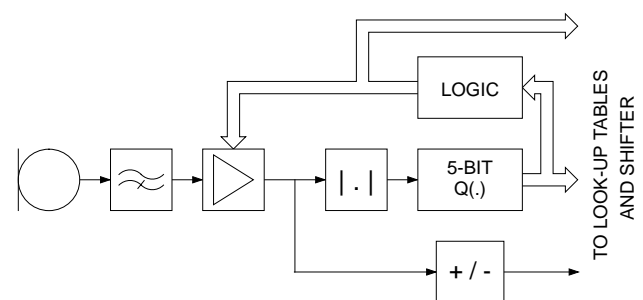


Figure 1: Front end stage of Schaub’s A/D converter

The microphone signal first passes a preemphasis filter in order to flatten the overall spectrum of the speech signal. Digital filtering in a subsequent DSP unit is expected for restoration of the original sound. The preemphasized signal is fed to a programmable amplifier with gain settings ranging from 0 to 46.5 dB in steps of 1.5 dB. They are set by an adaptation logic which therefore provides a 5-bit control word. The amplified signal is applied to a 6-bit quantizer (5-bit magnitude plus sign).

The five bits representing the magnitude of the quantized sample serve as the input to the adaptation logic which updates the gain of the programmable amplifier according to Table 1. The adaptation table is inspired by N.S. Jayant’s paper [2] on adaptive quantization of PCM signals. The multipliers are just restricted to powers of  $2^{1/4}$ , corresponding to approximately 1.5 dB steps.

Thus, a 14-bit A/D word can be assembled from the 5-bit control word and the 6-bit quantizer output by reference to one of four look-up tables and subsequent shifting operations.

Simulations using male and female speech as well as music have been performed. The input level of the test signals has been adjusted to -30 dB with respect to the full range of the converter, thus corresponding to realistic conditions in an application. Typical SNR values around 26 dB resulted from these experiments.

magnitude codeword	gain increment / decrement
0 ... 15	+ 1.5 dB
16, 17	-1.5 dB
18, 19	- 3 dB
20 ... 23	-4.5 dB
24 ... 27	-6 dB
28, 29	-7.5 dB
30, 31	-9 dB

**Table 1:** Gain adaptations for 6-bit quantizer

Comparative listening tests using headphones revealed noticeable differences between original and processed signals. Even though the amplified signal exceeds the fixed quantizer range in only a small fraction of time, the resulting clipping effect was clearly perceived. Another effect is due to quantization noise. Its spectral distribution with respect to the short time spectrum of the input signal is often too far away from ideal conditions which would let it optimally profit from well-known masking effects. Therefore, additional experiments were started that finally led to the results presented in the next section.

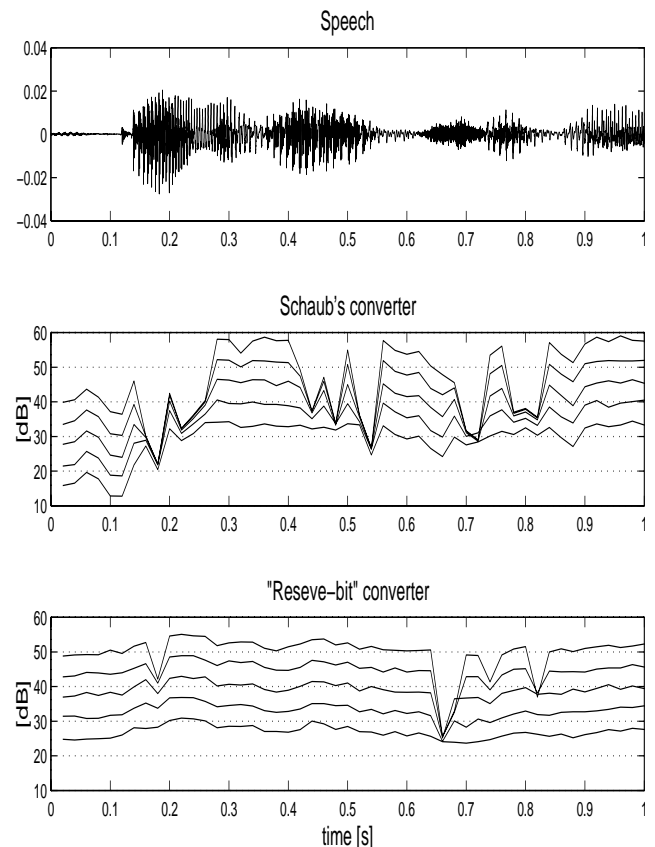
### 3. IMPROVEMENTS

Improving the signal to quantization noise ratio seemed straightforward at first glance. In a series of experiments the number of bits in the quantizer was repeatedly increased and the adaptation table was extended as required. The performance of the converter was observed by means of segmental SNR values computed for subsequent time intervals of 20 ms each. As long as the amplified input signal was within the range of the quantizer, improved SNR values were observed as expected. When the maximum amplitude of the quantizer was exceeded, however, i.e. in intervals of rapidly increasing signal level, the additional quantizer bits failed to improve the segmental SNR.

These effects are illustrated in Fig. 2. At the top a speech segment of 1 s duration is shown. Segmental SNR curves for Schaub's converter with an increasing number of quantizer bits are shown in the middle.

A closer look on the adaptation scheme summarized in Table 1 (and those directly derived from it to cope with the longer code-words) made the effect understandable. As a matter of fact, the adaptation circuit is a feed-back control loop setting a target value  $\theta$  that equals half the maximum amplitude of the quantizer. This is readily seen from the fact that the amplifier gain is increased whenever the magnitude of the amplified signal is below  $\theta$  and decreased otherwise.

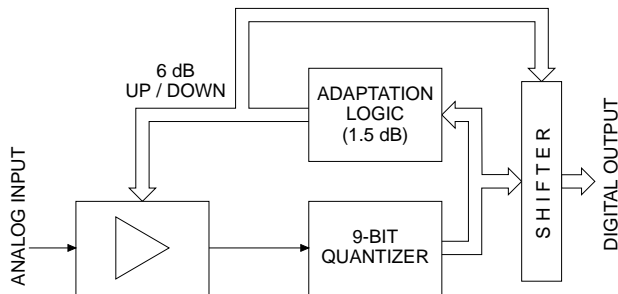
A new series of experiments was thus started with the concept of a so-called "reserve bit". For a quantizer with a given number of bits, the idea was to reduce the target value  $\theta$  from half to a quarter of the maximum amplitude. As an example, the adaptation table for a 7-bit quantizer was chosen as in Table 1 for magnitude code-words 0 to 31, whereas the maximum decrement of -9 dB was also applied to the codewords 32 to 63. In this way, a larger margin to protect against clipping was introduced. Segmental SNR values as well as comparative listening tests confirmed the expected improvement. The improvements correspond to the SNR curves at the bottom of Fig. 2.



**Figure 2:** Segmental SNR for 6 to 10-bit quantizers

From the beginning of the project, the intention was to develop a self-contained converter unit. With respect to the adaptive input stage this means that its counterpart should also be included, i.e. a time-varying alignment of the quantizer codeword to the output word in accordance with the applied gain in the input amplifier. To cope with 1.5 dB steps, multiplication with  $2^{-1/4}$ ,  $2^{-1/2}$ , and  $2^{-3/4}$

is required besides shifting operations that compensate 6 dB steps. However, integrating a digital multiplier on the converter chip was always considered out of scope.



**Figure 3:** 15-bit micro power A/D converter

In his former design, Schaub proposed to use look-up tables with pre-multiplied codewords. Look-up tables of size 64 were sufficient for a 6-bit quantizer. Unfortunately, the size of the look-up tables grows exponentially with the number of quantizer bits. Therefore, the look-up table approach is not very attractive in the case of quantizers with a higher number of bits. Of course, multiplications could be avoided completely, if the adaptation used coarser minimum steps of 6 dB. A few initial experiments showed, however, that this does not lead to the desired performance.

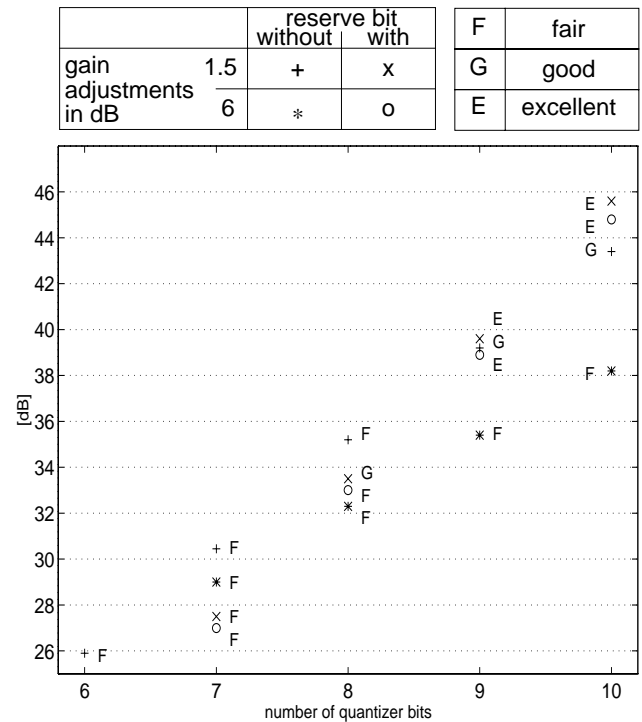
At that point of time it seemed as though the improvements accomplished with finer quantization and the need for simple codeword alignment were completely contradictory. Yet, an elegant solution was found which led to the final design of the revised “relative precision” converter: the changes in input gain are still computed in 1.5 dB steps as before. As to the input amplifier, however, changes are brought to effect only when they have accumulated to 6, -6, or -12 dB. Hence, shifting operations are sufficient for codeword alignment at the back end.

Simulations showed that segmental SNR values dropped by only 1 dB typically compared to the case where the amplifier gain is actually changed in 1.5 dB steps. Obviously, the previously introduced “reserve bit” was quite helpful in this situation as well. To be precise, the performance curves at the bottom of Fig. 2 actually reflect the converter design with the coarse 6 dB gain adjustments already taken into account.

The block diagram of the final design is depicted in Fig. 3. At the end of a series of comparative listening tests it was decided to use a 9-bit quantizer and to set the maximum gain to 36 dB. In this case, the 9-bit quantizer codeword can be shifted to six more positions in accordance with the amplifier gain, thus yielding a dynamic range of a 15-bit output word. Of course, a further extension to provide for an even larger dynamic signal range could now easily be realized by simply allowing a higher maximum gain value.

The results of the various listening tests are summarized in Fig. 4. The simulations included converter designs with and without “reserve bit”. The effective gain adjustments were also applied in

either fine 1.5 dB or coarse 6 dB steps. The figure shows mean segmental SNR values vs. number of quantizer bits. The identification marks used in the figure are explained on top of figure 4, as well as the meaning of the additional labels indicating subjective mean opinion scores.



**Figure 4:** Mean segmental SNR values

## 4. ANALOG DESIGN

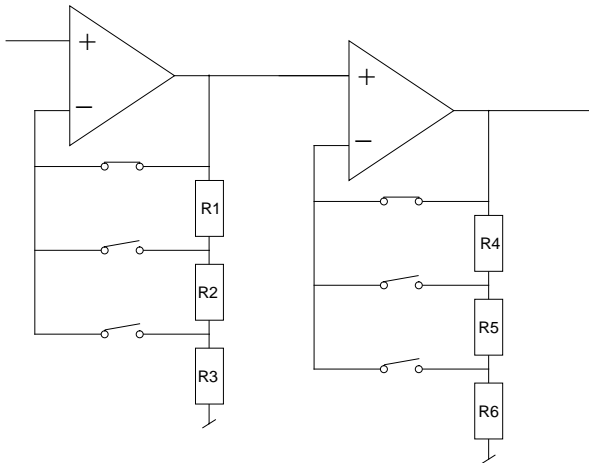
Both the programmable input amplifier and the 9-bit quantizer have been designed according to the ALP2 Low Voltage technology of EM Microelectronics-Marin, Switzerland. This 2  $\mu\text{m}$  technology has been developed primarily for watch ASICs. Minimum supply voltage is 1.5 V.  $V_{t0}$  values are typically -0.411 V and 0.605 V for a PMOS and a NMOS transistor, respectively.

The circuits have been simulated using ELDO. Estimations regarding power consumption and chip area have been worked out for both units.

The 9-bit quantizer is realized as a switched capacitor successive approximation converter. Its output is in two’s complement number format. Its design has been optimized with respect to minimum power consumption, using innovative techniques for which a patent will be applied. Therefore, no further detail regarding this part is revealed in this paper. Estimates for power consumption and chip area are 11.7  $\mu\text{W}$  at a  $\pm 1.3$  V supply voltage and approximately 0.15  $\text{mm}^2$ , respectively.

The programmable input amplifier is realized in a two-stage struc-

ture as depicted in Fig. 5. Gain selections are 0, 12, or 24 dB for the first stage. Those of the second stage are 0, 6, or 12 dB. In this way, gain settings in 6 dB steps, from 0 to 36 dB, are provided. The stages are implemented as non-inverting op amps. The required resistor ratios thus are:  $R_1 = 12 R_3$ , and  $R_2 = 3 R_3$ , for the first stage;  $R_4 = 2 R_6$ , and  $R_5 = R_6$ , for the second stage.

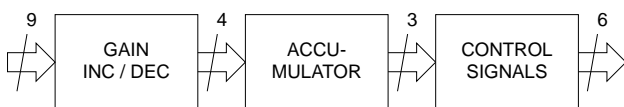


**Figure 5:** Programmable input amplifier

A simple RC low pass filter follows the programmable input amplifier. Its cutoff frequency is set to 10 kHz and thus eliminates higher frequency noise at the input of the quantizer. Estimates for power consumption and chip area for both programmable amplifier and low pass filter are  $12.8 \mu\text{W}$  and  $0.09 \text{ mm}^2$ .

## 5. DIGITAL DESIGN

Digital design has been performed using standard cells from the CSEL\_LIB library for the ALP2 Low Voltage technology. The library is supplied by CSEM Neuchâtel, Switzerland. Estimations regarding chip area and power consumption have been worked out using COMPASS.



**Figure 6:** Structure of the adaptation logic

The adaptation logic consists of three different sub-units, as shown in the block diagram of Fig. 6. The first sub-unit has the 9-bit quantizer output word as its input. It derives the required gain increment / decrement from the magnitude of the input word. The gain adaptation is computed in multiples of 1.5 dB, with incremental changes ranging from -9 dB to +1.5 dB. Four bits are thus required to represent these values, including the sign bit.

The incremental changes are accumulated in the second sub-unit. This accumulator is 6-bit wide, including a sign bit. The latter is

only required for detecting (and subsequently correcting) erroneous gain settings below the minimum of 0 dB. Additional circuitry is also required for detecting (and subsequently correcting) gain settings exceeding the allowed maximum of 36 dB. For correct accumulation, the incremental gain values need to be properly sign-extended.

The third sub-unit determines the control signals for the gain-selection switches in the programmable input amplifier. It therefore needs the accumulator word of the second sub-unit at its input. The admissible gain settings of 0, 6, 12, 18, ..., 36 dB are actually provided by the three more significant accumulator bits (excluding the sign bit). In this way, the gain adjustments of the input amplifier and the corresponding number of shifts to align the quantizer word are brought to effect with the required modulo 6 dB constraint. The shifter finally provides proper alignment of the 9-bit quantizer word into the 15-bit A/D word. Estimates regarding power consumption and chip area are  $0.54 \mu\text{W}$  and  $0.3 \text{ mm}^2$  for the whole digital circuit.

## 6. CONCLUSIONS

An extremely low power A/D converter intended for the conversion of audio signals has been designed. It operates at 16 kHz sampling rate and produces 15-bit wide output words. A dynamic signal range of approximately 85 dB is thus provided. The performance of the converter is limited to a signal to quantization noise ratio of approximately 40 dB. However, comparative listening tests using headphones yielded excellent subjective judgements. The signals were hardly distinguishable from their unprocessed versions, a remarkable result due to masking effects inherent in the human auditory system.

Fortunately, the admissible limitation in signal to quantization noise ratio allows drastic reductions in hardware requirements, thus leading to enormous savings in power consumption. Consequently, digital processing of audio signals in power-sensitive, battery-operated equipment like hearing instruments may become a realistic alternative.

## REFERENCES

1. Schaub A., "Micro Power A/D Converter for Audio Signals", *Digital Signal Processing*, Vol. 2, pp. 110 - 114, 1992
2. Jayant, N.S., "Adaptive Quantization with One Word Memory", *Bell Syst. Tech. J.*, pp. 1119 - 1144, September 1973.