

Wafer sawing processes: from microscopic phenomena to macroscopic properties

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Wafer sawing processes: from microscopic
phenomena to macroscopic properties

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Abstract

Keywords

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Mots clés

sciage à fil, wafer en silicium, résistance à la rupture, fissure

The majority of the solar modules are based on crystalline silicon (c-Si) wafers. Whereas the c-Si technology can offer a high efficiency, its main drawback (compared to traditional means to produce electricity) is the cost. The wafers account for one third of the total module cost, as high purity (thus expensive) silicon is required. One way to decrease the solar electricity cost is to decrease the amount of silicon needed for a wafer, for instance by sawing thinner wafers. Another way is to increase the solar cell production line yield by producing stronger wafers and hence reducing the breakage rate. From a technological point of view, both ways are equivalent, as thinner wafers have to be comparatively stronger to sustain the processing stresses.

The core of this work is the analysis and understanding of the impact of wire-sawing parameters on the wafer's mechanical properties with the aim of sawing thinner and stronger wafers. Wafer wire-sawing consists of a wire transporting a slurry, made of abrasive silicon carbide particles and lubricant, through a silicon brick. Such a process is complex, as it involves dynamic processes, fracture mechanics, fluid dynamics as well as tribological aspects on various length-scales.

In the first part of the work, characterisation methods were developed to quantify the wafer quality: roughness, crack depth distribution, breakage stress, wafer thickness and Raman measurements were carried out. Furthermore, a TEM study was made to get a precise view of the silicon just below the wafer surface, and the surface at the top of the sawing groove was analysed to get a fundamental understanding of the material removal mechanisms.

Two parametric studies were carried out to get insight into the influence of the sawing parameters on these wafer properties. The parameters that were studied were the abrasive size distribution, the slurry density, the wire tension and the feed rate. The first campaign focused on large parameter variations in order to have a global view of the variables determining wire-

sawing, whereas the second campaign concentrated on lower variations and a more thorough study of these parameters closer to their standard values. From these data, mechanisms of crack creation are proposed and a novel semi-analytical model describing the wafer strength as a function of the sawing parameters is given. It is based on physical interactions and allows a deeper understanding of the sawing mechanisms. Furthermore, the effect of the sawing parameters on the wafer thickness is analysed. From these campaigns, it is seen that stronger wafers are obtained by using a fine abrasive, a low wire tension and a slow feed rate.

A third study about the silicon debris impact on the wafer quality was carried out. It is found that below a given debris amount, they have no effect, but over this threshold, saw-marks appear and the wafer strength quickly decreases. This is put in relation with the findings from the two first sawing campaigns and a novel mechanism explaining the saw-mark creation is proposed: the debris prevents the abrasive particles from removing silicon as fast as required by the feed rate. This makes the wire pressure on the particle increase, until a second material removal mechanism appear. This mechanism is faster than the usual one and allow the wire bow (as well as the pressure on the particles) to decrease so that the sawing proceeds in fits and stops.

From all the analysis done, a better general picture of the sawing process was gained. Differences between the top and the side of the sawing groove are explained, as well as differences between the wire entrance and exit side of the ingot. At the top of the groove, the roughness is lower and presents more facets and sharp angles than at the side (which is also the wafer surface). This is explained by a faster material removal rate at the top of the groove and by a lower maximal pressure on the particles. At the side, the particles can apply large pressure on the silicon when there is not enough room for the wire and several large particles overtaking each other. On the other hand, the slow material removal rate at the groove side leaves the smaller particles enough time to smooth the angles. The particles are progressively ejected from the groove side, which accounts for a roughness diminution and a wafer thickness increase in the first half of the wafer length. In the second half of the wafer length, the roughness is constant but the thickness still increases, indicating that the abrasive particle volume fraction in the slurry diminishes, without a notable change in particle size. Finally, near the wafer edges, the wire vibrations outside the silicon also account for a thickness decrease.

In the last part, diamond-wire wafering was studied as an alternative to the standard slurry sawing. The wafer surface characteristics were analysed and compared with slurry-sawn wafers. On the diamond-wire sawn wafer, a thick layer of amorphous silicon was found. It has repercussions on topography, as smooth grooves are forming the surface, but also on the internal stress near the wafer surface: large stress has been measured by Raman spectroscopy and by EBSD, over 1 GPa.

By applying the conclusions from this work, it is possible to saw thin and strong wafers. This study brings a better understanding of the material removal process at the micrometer level, helping the optimisation of the sawing. Furthermore, the developed semi-analytical model giving the impact of the sawing parameters on the wafer strength is a useful tool for producing stronger wafers. Finally, the presented study on diamond-wire sawn wafers brings relevant insights into the challenges that have to be faced before this technology can be successfully used by the industry.

...
There are cities underneath cities
Cities beneath the sea
In deserted towns and burial mounds
There is beauty that no-one will see
And the magic of stones when taken back home
Is left on the beach
...

Gravenhurst, *Cities beneath the sea*, 2005

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Chapter 1

Introduction

Photovoltaic electricity (the electricity produced directly from the sunlight) has many advantages. It can be abundant, available everywhere, and renewable. But all these advantages are balanced by its high cost in comparison with non-renewable sources. Despite its fast growth, the photovoltaic (PV) industry still has to decrease its production costs, as well as to improve the efficiency of the cells produced, to reach the point where it will be economically sound to use solar modules to produce electricity.

The approximate cost of electricity in 2005 was around 4–6 €/kWh for traditional sources and around 20–40 €/kWh for PV electricity^{59,98}. Predictions for 2030 indicate that the costs for non-renewable energy should rise to 4–7 €/kWh, while the cost of PV electricity should drop down to 5–10 €/kWh^{59,98}. This implies a major cost decrease of solar modules fabrication. To achieve such a goal, every fabrication step is strongly solicited for cost reduction.

During the last decade, the PV industry has been enjoying fast growth (Fig. 1.1), as solar cell production worldwide increased by more than 40 % yearly⁵⁹, thanks to governments setting up incentives to promote (and make it worthwhile economically) the installation of PV modules. There are several different means to set up incentives: voluntary mechanisms (where the consumer is willing to pay more for renewable energy than for traditional energies), quotas (set up by the government), investment support and feed-in tariffs (during a certain amount of time, the owner is paid a pre-defined rate for the produced energy, covering the higher generation cost of the PV system), which is said to be the most efficient means of promoting PV energy production³⁶. These incentives support the fast market growth, which induces a decreasing cost of solar module fabrication, by allowing lower cost mass-production. At the same time, the efforts accomplished by the research and development should be continued until PV energy is competitive with the other electricity production methods.

One of the reasons explaining the high cost of solar cells is the price of raw materials.

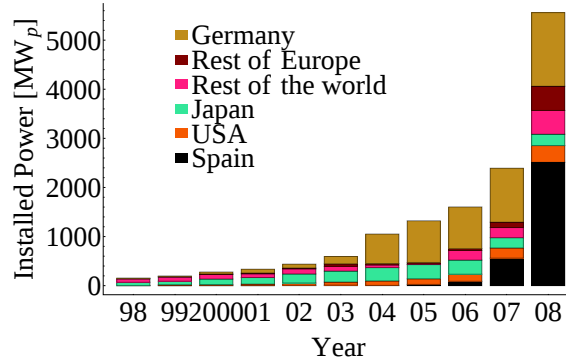


Figure 1.1: Newly installed photovoltaic power in the world. From the *European Photovoltaic Industry Association*³⁷.

Nowadays, most of the solar cells are silicon wafer-based (86–88 % of the market in 2008⁶³). But as the silicon required has to have a high purity, its production costs are expensive (long term silicon contracts are priced at \$50–80 kg^{−1}). Furthermore, the fast expansion of the PV industry induced, from 2003 to 2008, a stress on the material availability, increasing its price even more. In 2005, the PV module production required around 9.1 g/W_p of silicon³¹ whereas in 2009, this amount decreased to 6.5 g/W_p³². Indeed, diminishing the amount of silicon needed to produce a given surface of solar cells — i.e. the wafers thickness, but also the amount of silicon sawn away and the breakage rate in the production line — is of major importance for decreasing the production cost. Another way to reduce costs is to decrease the amount of silicon needed per W_p by improving the efficiency of the solar cells. Thus, the wafer surface needed to produce a certain amount of power diminishes, which will in turn diminish the cost of module manufacturing (less modules are needed for the same power), the cost of installation (less modules to install and connect), and the area needed. A third means to reduce the costs of solar cells is to reduce the cost of silicon refinement or using cheaper silicon. This has led to the research on “upgraded metallurgical grade” silicon, but is only partially compatible with increasing the cells efficiency as most of the high efficiency cell concepts need high purity silicon. Finally, automation of the cell and module production lines provides a more constant handling of wafers (inducing a more predictable breakage, so that wafer breaking rate improvement is easier to achieve) and savings in workforce expenses, both of which allow for a reduction of the module production cost.

Once the solar modules are installed, the last parameter determining the cost of energy production is the longevity of the modules. Since they are installed outdoor, they are subject to wind, rain, hail, moisture and UV-degradation. As the amount of energy produced by a module depends on the illumination time, a module working longer will produce more energy

and thus diminish its cost. Degradation of the panel can decrease the module efficiency drastically, even if only one cell is damaged, and as modules are designed to work for more than 20 years, even the smallest degradation speed will have major impact on the final amount of energy produced. Many module designs exist, but all of them consist of a transparent front material to protect the cells and let the light shine through, the cells, which are connected together to provide the desired operating voltage and current, and finally a back panel and a frame enclose the module and are used to fix the modules on the mounting system. In some cases, the frame is not present and the waterproofness is made by the glue between the front and back panels. The non-standardization of mounting systems is also a cause of higher installation prices, as every plant is specifically designed for a chosen type of solar panel.

1.1 General objective of this work

The wafer cost (from silica to wafer) accounts for around one third of the total module production costs, as shown in figure 1.2. The wafering step (from a multi-crystalline ingot) represents about 11 % of the total module production costs³¹. It is one of the important cost factors, so that decreasing the wafering cost is indispensable for diminishing the solar electricity production cost. This is done by increasing the wire-saws' productivity, increasing the wafer yield and decreasing the amount of silicon per wafer (i.e. decreasing the wafer thickness and the kerf loss). However, thinner wafers are inherently "weaker", so that for a given breakage strength, a lower force is needed to break a thin wafer. Furthermore, the wafering step has repercussions throughout the subsequent production steps as it defines most of the wafer strength. By

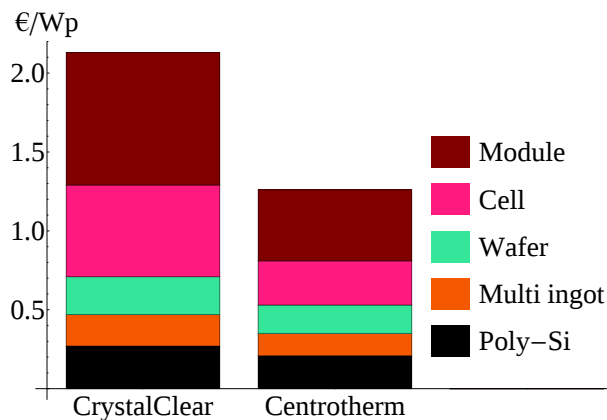


Figure 1.2: Cost structure reported from the European project *CrystalClear*³¹ in 2005 and a 2009 estimation from *Centrotherm*²⁴ for a 350 MW integrated factory with Poly-Si and casting in Canada and wafering, cell and module fabrication in Germany.

producing stronger wafers, the amount of wafers breaking in the cell and module lines can be decreased, consequently decreasing the module production costs.

Consequently, the decrease of wafering costs is linked with the capacity to produce stronger wafers. To do so, the understanding of the sawing process has to be improved and the effect of the different sawing parameters has to be better understood. The aim of this work is to gain knowledge of the sawing process and to have a better view of the impact of different sawing parameters, from a material science point of view, by studying the mechanical characteristics of sawn wafers cut with different sawing parameters.

1.2 Crystalline silicon solar cells

At its working point, a solar cell generates a tension and a current flows between its two electrodes. In practice, the classical crystalline silicon solar cells are designed as described in the simplified cross-section in figure 1.3. They are made out of a metallic grid at the front side contacting the emitter through the SiN anti-reflection coating. The emitter (a highly doped n layer) and the base (the p-doped bulk of the silicon wafer) form a p-n junction. The rear contact at the back of the wafer forms a p+ back-surface field. The metal back contact ensures internal reflection of the light and current collection. When light shines on the cell, some photons are entering inside the silicon. Other photons are reflecting at the surface, but this is minimised by the anti-reflection coating and the surface texture. Inside the cell, the photons can, if their energy is larger than the band-gap, generate electron-hole pairs. As long

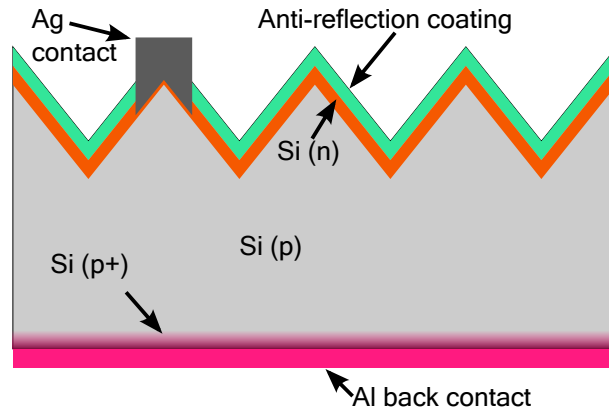


Figure 1.3: Cross-section of a screen printed solar cell. The wafer surface is etched to remove the defects and add a topography (for improving the light trapping). The wafer at the base of the cell is p-doped, and a n-doped layer is diffused at its surface. Then an anti-reflective and conductive coating is deposited at the surface; the front, rear contact and the back-surface field (p+ doped region) are printed and diffused into the cell.

as the photons have not been absorbed in the silicon, they continue through the cell, eventually reflecting at the rear side, or again at the front side (they can escape the cell at both surfaces, but the surface texture tends to reduce the number of escaping photons by promoting internal reflections). When a the minority carrier (an electron if the pair was created inside the base, a hole if it was created in the emitter) reaches the depletion region of the p-n junction, it is swept by the electric field to the other side of the junction, contributing to the photo-current. As long as the minority carrier has not reached the p-n junction, it can recombine with one of the majority carriers and the energy from this recombination is dissipated into heat. The time before such a recombination is measured by the minority carrier lifetime.

The minority carrier lifetime, and the associated diffusion length, depends on the silicon purity, but also on the defects (e.g. cracks, grain boundaries or dislocations). As the sawing process induces many defects at the wafer surface, the wafers are etched to remove the damaged layer. At the same time, this etching step creates a surface texture reducing the primary reflections by increasing the amount of multiple reflections at the cell surface, and inducing “light-trapping” for the photons that were reflected by the back reflector. This light-trapping mechanism allows the fabrication of a thinner solar cell, as the light can travel distance much larger than the actual cell thickness. With the right cell design, it is possible to decrease the cell thickness down to around 50 μm ¹²³ without dramatically decreasing the efficiency.

In practice, two parameters limit the wafer thickness decrease. Firstly their strength, as they have to endure mechanical and thermal solicitations during the cell and module production. Secondly, as contacts are printed on both surfaces of the cell and fired, differences in dilatation coefficients of the metals used will induce thermal dilatation mismatch that bend the wafers. This bending depends on the thickness of the wafer — as thinner wafers bend more for a given applied force — and can induce problems during the modules’ manufacturing, as wafers are laminated between two protective panels, implying that bent wafers are flattened back, thus increasing the stress level the wafers have to sustain and breaking the weaker wafers. In all, to lower the costs of PV, thin wafer and c-Si usage reduction will be a must, requiring improved mechanical properties and adapted production processes.

1.3 Silicon ingot production

Silicon is the second most abundant element on earth, but it is only present in the form of oxides. To produce crystalline silicon, these oxides have to be heated up to around 1900 °C and reduced with the help of carbon-based materials. From this reaction, so-called metallurgical grade silicon is obtained. Its purity attains around 98 %, and it can be used for alloying metals, e.g. for cast aluminium alloys. Most of the silicon produced is actually used for metal

alloying, and only a small part is further refined to produce electronic grade silicon or solar grade silicon. This refinement is typically done by reacting silicon with hydrochloric acid to produce trichlorosilane. This compound has a low boiling point and can easily be purified by distillation¹²⁴. The trichlorosilane is then decomposed with hydrogen to form high-purity silicon using the Siemens process¹⁷. This decomposition is done at the surface of pure silicon rods at around 1150 °C. This purification route requires a lot of energy (in the range of 100–200 kWh/kg^{17,25}).

Due to the rapid growth of solar cell production, high-purity silicon became rare, inducing a large increase in its price during the years 2006–2008. At the same time, the incentive to diminish the price of solar-grade silicon promoted research towards less-expensive silicon, mainly by avoiding the Siemens process step, for instance by using a fluidized bed reactor, which is a continuous process that is said to require much less energy than the Siemens process²⁵. Another possibility to purify silicon is through a metallographic route, with several methods of purification¹⁷. Much less energy is needed to produce silicon purified via the metallurgical route and it is cheaper, but the downside of such lower-quality material is that it includes more doping element and, for a given conductivity, it has a lower minority carrier lifetime.

After the purification process, the rods are broken in pieces that are ready for melting and crystallisation, either as a mono-crystal using the Czochralski process⁴⁶ (Fig. 1.4(a)), or as a multi-crystalline ingot using directional solidification⁸⁹ (Fig. 1.4(b)). There are several differences between mono- and multi-crystalline silicon. As their name indicates, the main difference resides in the number of crystals forming an ingot. Mono-crystalline silicon consists of one very large crystal, multi-crystalline is made of many columnar grains that grew perpendicularly to the crucible bottom. The cells produced from mono-crystalline silicon have a higher efficiency than multi-crystalline wafer based cells (for a similar structure). This is explained by several features of mono-crystalline silicon. First of all, the crystallographic orientation can be chosen so that an anisotropic etching that produces random pyramids on the wafer surface can be used, consequently reducing the cell optical reflection. Second, the grain boundaries and dislocations are prime hole-electron recombination sites that are only present in multi-crystalline cells. Finally, a higher purity level can be attained with the Czochralski process⁴⁷. Higher purity plays a role for basic design cells and can play an even more important role in the efficiency of more complex cells, such as interdigitated back-contact cells. Due to the solidification process, mono-crystalline ingots present themselves in the form of a rod of diameter — depending on the solidification parameters — up to 400 mm and around 1–2 meters long. The PV industry mostly uses smaller wafers than the micro-electronic industry, and most ingots have a diameter under 230 mm. To increase the amount of solar cells on the

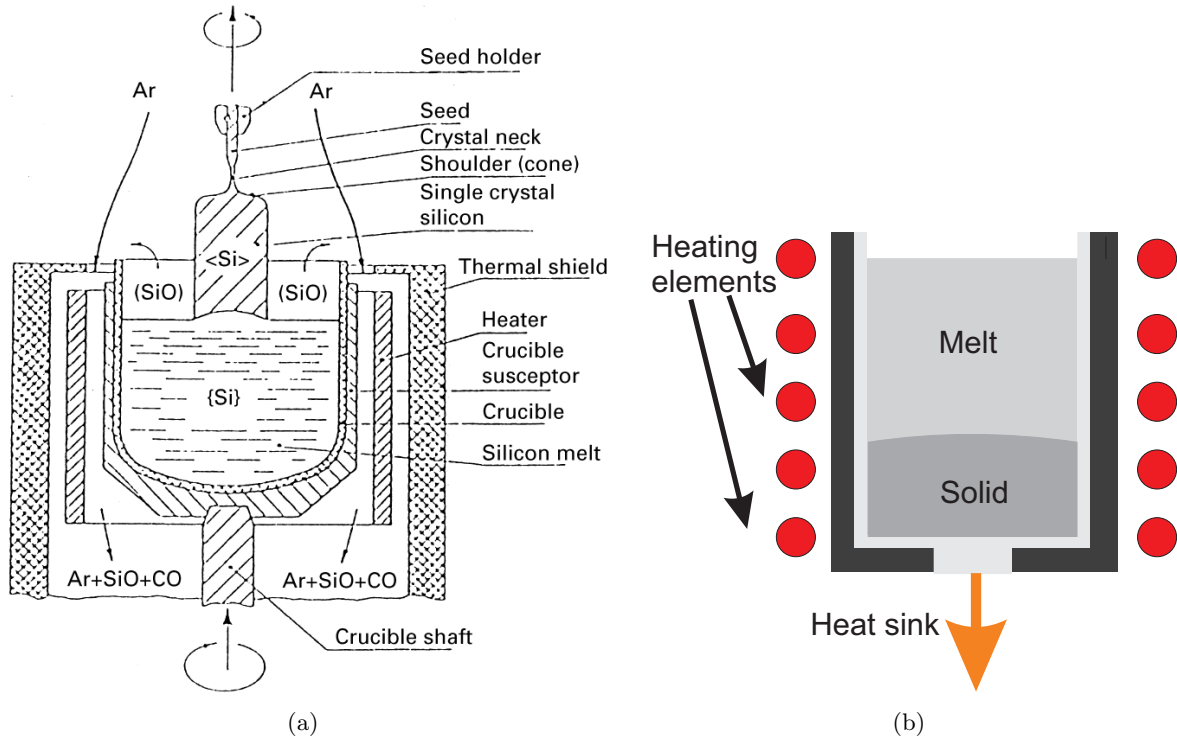


Figure 1.4: (a) Principle of Czochralski single-crystal pulling technique. Starting from a mono-crystalline seed dipped in the silicon melt, the seed is slowly pulled while rotating. By controlling the pulling speed, the size of the ingot can be varied. First, a small neck is made to remove any defects, then the crystal is made larger. The crucible is heated to keep the silicon melted and turned in the opposite direction of the crystal. After Goetzberger et al⁴⁶. (b) Multi-crystalline ingot casting. The silicon is solidified from the bottom to the top to favour large grains without much internal stress.

modules, these rods are sawn into square or pseudo-square (a square with rounded corners) ingots before being cut into wafers. The silicon cut out during this step can be once more molten to form a new ingot, but it increases the production cost of mono-crystalline wafer, a process that is already inherently more expensive than multi-crystalline ingot casting.

The Czochralski process consists in filling a rotating crucible with silicon and melting it. Then, a mono-crystalline silicon seed is dipped into the molten silicon and slowly taken out while rotating (in the opposite direction of the crucible). The upwards speed of the seed as well as its cooling rate are controlled to adjust the diameter of the silicon ingot produced. A small starting diameter and the right solidification parameters ensure a defect-free mono-crystalline ingot. The most important type of foreign atom found in Czochralski grown crystals is oxygen (at a concentration of 10^{17} – 10^{18} cm⁻³)⁴⁷. Oxygen is detrimental to the solar cell efficiency, as it can form boron–oxygen defects that are efficient recombination centres activated by

illumination, thus decreasing the cell efficiency after it is installed. Oxygen diffuses from the crucible (made of silica) into the molten silicon and is incorporated inside the crystal. This effect is only seen on boron, p-doped silicon and can reduce the cell efficiency by up to 10 % (relative)^{47,109}.

There are several ways of solidifying a multi-crystalline ingot, e.g. with a Bridgman oven, or in a directional solidification mould (Fig. 1.4(b)). As for the Czochralski process, impurities are incorporated through the contact with the crucible and through the ambient air. The aim of this solidification is to obtain an ingot with columnar crystals as large as possible, with a minimal amount of internal stress and homogeneous doping. For efficiency purposes, the industry is going towards larger ingots to decrease the impact of the crucible contamination and to increase the productivity. Multi-crystalline ingots have, apart from grain boundaries, dislocations and internal stresses due to the cooling of the ingot. They can also contain SiC and Si₃N₄ inclusions that may diminish the wafer quality or the solar cell efficiency.

Once the silicon is solidified, the ingot has to be cut to the right dimensions. For mono-crystalline material, it means cutting a square brick from the cylindrical ingot and for multi-crystalline material, cutting (pseudo-)square bricks from the large ingot (in production, the ingots are cut in up to 5×5 bricks of $156 \times 156 \text{ mm}^2$, forming ingots weighting more than 600 kg⁶⁷). On top of that, the sides of the multi-crystalline ingots have to be sawn off, as impurities from the mould have diffused into the silicon. The top and bottom of both multi- and mono-crystalline ingots have also to be removed as their doping and impurity levels are not suitable for solar cell production. This process can create structural defects on the brick sides that are later found on the wafer edges. For this reason — and to have a better dimensional precision of the bricks — the sides and the edges of the bricks may be polished before being cut into wafers. The wafering step is then made with multi-wire saws.

1.4 Description of the wire-saw

A standard wire-saw is made of a steel wire wound around two or four so-called wire-guides, in order to make a web of parallel and regularly spaced wires (Fig. 1.5). The wire is unwound from a spool and is driven into a tension control circuit before forming the web^{87,88}. At the exit of this wire web, a second tension regulating circuit is present before the take-up spool. The wire length is around 400–800 km, depending on its diameter (generally between 100 and 160 μm). Both spools are driven, as well as the wire guides. The wire is not structured and is just used to transport the cutting liquid into the cutting zone.

This cutting liquid — the slurry — typically consists of a mixture of poly(ethylene glycol) — PEG — and silicon carbide (SiC) particles^{87,88}. The slurry is poured on the wire web



Figure 1.5: (a) A wire-saw from Applied Materials Switzerland SA. (b) Schematic description of a multi-wire slurry saw. The wire-saws usually have two or four wire guides. After Québatte et al⁹⁹. Both images are courtesy of Applied Materials Switzerland — printed with permission.

on both sides of the ingots and collected at the bottom of the sawing chamber, then carried to the slurry tank until it is pumped again on the wires. As the silicon carbide particles are heavier than the PEG, the particles tend to sink, making the slurry inhomogeneous. To prevent this, the slurry in the tank is constantly being mixed and the PEG has to be viscous enough. Apart from transporting the abrasive particles, the slurry plays two other major roles: removing silicon debris and heat from the cutting zone.

The typical brick size is $125 \times 125 \text{ mm}^2$ or $156 \times 156 \text{ mm}^2$, and has a length of around 300 mm. Several bricks are sawn together: up to 2 metres of silicon brick length can be cut at the same time in the largest saws. This means that one single cut produces approximately 6000 wafers at a time, assuming that the pitch (the distance from one wire centre to the next wire centre) is $300 \mu\text{m}$. It might look like an important number of wafers, but taking into account that one run needs about eight to twelve hours to finish⁹⁰, the production is only in the range of 500 wafers per hour.

During the cut, the silicon blocks have to be held in place. The challenge consists in being able to cut through the brick and still hold the wafers at the end of the cut. The usual set-up is based on a steel holder clamped to the saw, as presented in figure 1.6. A steel plate is screwed to this holder. On it, a glass plate is glued (with an epoxy) and finally, the bricks are glued on the glass plate (with another epoxy). The glass plate is needed because part of it has to be sawn to be sure that the whole silicon bricks are cut. Indeed, as the wire is only

supported by the wire-guides, it bends when the silicon is pressed through the wire web. This bow implies that the sides of the bricks are cut faster than the middle so that to cut the whole brick, part of the glass plate has to be sawn as well. Furthermore, as the cutting produces heat, the glass plate is used to limit the effect of thermal stress on the silicon. After the cut, the whole assembly is taken out of the saw and put into warm water to unglue the wafers. Once the wafers are unglued, the steel plate is unscrewed from the holder and unglued from the glass plate. If the glue is not strong enough, wafers might fall and break at the end of the cut but, at the same time, it has to be easy enough to remove the wafers from their support once they are sawn, without breaking them.

During sawing, silicon debris are introduced into the slurry, changing its properties and lowering its sawing efficiency⁶. This implies that the slurry has to be changed, either during the cut with a slurry management system or by completely replacing it at the end of the cut. For cost decrease purposes, the slurry is recycled, either in-house or in an external factory. This recycling consists in separating the abrasive SiC from the slurry, and then in removing the silicon debris from the PEG. Finally, a new slurry is prepared by mixing the recycled PEG with the SiC and completing the mix with new component.

The wire also plays a major role in the sawing. It determines most of the kerf (the width of the cutting groove, i.e. the amount of silicon lost as debris during sawing), but using a thinner wire is not without its problems. The wire has to sustain high tensions throughout the sawing, so that the presence of any inhomogeneity can decrease its strength, which may lead to its rupture. As the relative importance of a small inhomogeneity increase with a diameter decrease, the risk of having a wire breakage increases as well. Furthermore, the wire is worn during sawing. Sawing thinner wafers means also sawing more wafers out of an ingot, which implies that the wire has to saw a longer distance of silicon (i.e. it wears more) before reaching the take-up spool. The same applies when a thinner wire is used: as the kerf is less important, more wafers (of comparable thickness) can be sawn from a given brick, which

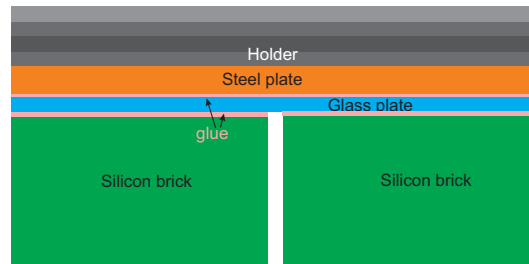


Figure 1.6: *Simplified view of the brick holding system. The holder on top is clamped to the saw, and the steel plate is screwed on it. The glass plate and the silicon bricks are glued.*

means more wear. The more the wire is worn, the less tension it can bear and the more prone to failure it is. Once used, the wire cannot be used a second time and thus should saw as much silicon as possible during one cut. But if the wire cuts too much silicon, it is too worn and the risk of breakage increases. The tension of the incoming wire is set by a device located between the spool and the first wire-guide. The wire has to sustain this defined tension along the whole cutting path plus any variation due to the cutting process. The tension of the wire is an important factor controlling the vibration of the wire, and it holds the wire inside its groove on the wire-guide.

At the end of the cut, the whole assembly (saw beam, glass plate and wafers) have to be lifted up from the wire web before being removed from the saw. This operation has to be done carefully, as the wafers are only held by a small ridge of glue that has been damaged by the sawing. Once the wafers are out of the wire-saw, they are unglued from the glass plate and cleaned before being characterised and processed into solar cells. The cleaning must remove all trace of PEG and SiC particles, but also the glue, without damaging the wafers as they are in the most fragile state of the solar cell production process⁷³.

There are several means of diminishing the amount of silicon needed for a wafer. The easiest is to decrease the wafer thickness by decreasing the distance between the sawing wires. Thus, it is possible to saw more wafers out of a given ingot. Another way is to decrease the amount of silicon removed by the wires, either by decreasing the wire diameter, or by decreasing the size of the sawing abrasive. Finally, decreasing the number of wafers breaking during the sawing process or during the subsequent production steps also decreases the amount of silicon needed per solar cell. Unfortunately, none of these measures are easy to achieve, as decreasing the wafer thickness produces weaker wafers, thus decreasing the production yield, decreasing the wire diameter makes it more sensitive to wear and increases the risk of rupture, and decreasing the abrasive size has only a limited impact and can lead to sawing problems¹¹².

The efforts of the industry in the last few years has lead to a decrease in the wafer thickness of about 10–20 μm every year. Thus, at the beginning of this study (in 2006), the mean thickness of the wafers was about 240 μm and it should be about 160 μm at its end (2010). Diminishing the wafer thickness implies that the whole cell process line has to be rethought, as the handling of wafers itself becomes more and more critical, from gluing the ingot on its holder for sawing to the separation and cleaning after sawing to the cell processing and the inter-connexion into modules. Thus, even if sawing thin but fragile wafers is easily done, the breakage rate during sawing — and more importantly after it — would increase so much that the costs saved by sawing thinner wafers would be overrun by the higher costs due to wafers breaking during the subsequent production steps. In consequence, increasing the mechanical strength of the wafers is of prime importance for diminishing the costs.

1.5 Alternative means to produce wafers

Although wire-sawing is used to produce most of the wafers used in the PV industry, there are several alternatives. The major drawback of wire-sawing is that almost half the silicon is lost in the kerf. Therefore, the alternative means to produce wafers concentrate on avoiding the sawing step by directly solidifying silicon in foils or wafers (like the EFG or the ribbon growth), or to separate silicon wafers without kerf loss by ion implantation followed by cleavage.

The edge-defined film-fed growth (EFG) uses a graphite mould in the shape of an octagon or a dodecahedron to solidify a hollow octagon (respectively a dodecahedron), the walls of which have the wafer width and a thickness around 200–300 μm ¹⁵. Silicon is pulled through the mould until the hexagon height is around 6 meters. Then the walls are separated by laser and wafers are cut from these foils. One drawback of this method is that silicon is contaminated by carbon, which can lead to a diminution of the charge carrier mean free length. Another problem is that, in order to have a production speed fast enough, large thermal gradients have to be used. This results in thermal stresses and fine, elongated silicon grains⁸⁹. It seems possible to produce thinner wafers²⁸ (around 140 μm), but reducing the thickness emphasises the buckling and internal stress, making the production more complicated¹⁵. This process was used at industrial scale by Schott Solar AG, but they stopped this production at the end of 2009.

Another method is the string ribbon growth used by Sovelo AG and Evergreen Solar Inc. Ribbons of silicon are grown between two supporting shafts that are slowly pulled through a crucible as presented in figure 1.7. The ribbons are about 8 cm wide and 200 μm thick. They are cut with a laser into a wafer of 15 cm length. The challenge of this method, like for EFG silicon, is to reduce the wafer thickness while keeping the ribbon width.

A third production method is the ribbon growth on substrate (RGS) initiated by Bayer and then further developed by the Energy Research Centre of the Netherlands^{21,77}. This method is still experimental and no industry is currently using it for production. Substrate plates are slid under a casting frame containing molten silicon. The exit side of the frame is higher than the others, so that a thin molten silicon layer is deposited on the substrate and solidified. After cooling, the silicon wafer is detached from the substrate and ready for the cell production. The resulting wafers suffer from an important defect density (due to the fast cooling) and contamination from the crucible and the substrate¹¹³. Nevertheless, its fast production rate and low silicon consumption makes it a plausible alternative to wire-sawing.

Another method focuses on cleaving a silicon ingot (thus without kerf) and is developed by Silicon Genesis. First, highly energetic hydrogen ions are implanted under the silicon ingot surface^{55,56}. Then, the brick follows a thermal treatment in which the hydrogen atoms

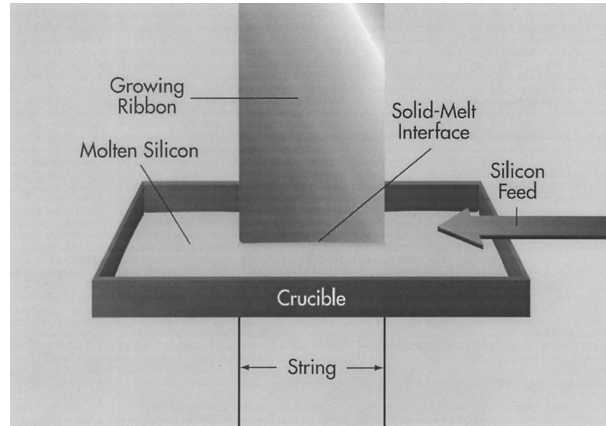


Figure 1.7: *Simplified view of String Ribbon growth. After J. Hanoka⁵².*

coagulate into pores at the depth where they were implanted. Then, the silicon is cleaved along these pores, giving a thin wafer. Once the wafer is removed, the implantation and thermal treatment processes are repeated to produce another wafer. It is possible to produce wafers with a thickness of 50–150 μm with a lower roughness and a much higher bending stress than wire-sawn wafers^{55,56}. This process is not yet used at an industrial scale and it not yet clear that an economic industrialisation is feasible. Noticeably, the wafer have to be monocrystalline, with a 111 orientation — to allow cleaving — which does not allow an anisotropic etching like the one currently used for monocrystalline wafers.

1.6 Main contributions of this work

The major results of this thesis will be placed in the context of research done by other groups later, only the key contributions of this work are summarised here:

- A characterisation methodology was developed to allow insight into the wafer mechanical characteristics. Our analyses showed that the roughness measurement is a good indication of the wafer strength, linking the surface roughness with crack depth¹⁰. Wafer surface roughness thus provides a fast and non-destructive measurement of the wafer strength. Furthermore, it shows that indentation mechanics, as it predicts such a correlation, is a useful tool for understanding the sawing process.
- The global picture of the sawing process was refinded. Roughness and sub-surface crack depth differences were measured between the wire entrance and its exit, as well as between the top of the wire groove and the wafer surface¹². From these results, the

differences of material removal conditions at the wafer surface compared to the top of the groove are analysed: the top of the groove is sawn fast and relatively small loads are applied by the abrasive particles whereas the wafer surface is sawn slowly and much larger loads can be applied by the abrasive particles. The wafer surface also shows differences between the wire entry and its exit: the thickness decreases and the average roughness is higher near the wire entrance. The roughness reaches a plateau after around one half of the brick width whereas the wafer thickness monotonely increases from the wire entrance to its exit, although this increase is faster near the wire entrance. It is explained by a decrease in the active particle diameter and by a decrease of particle volume fraction. Finally, wire vibrations outside the bricks explain thickness variations in the first few millimetres from the wafer edges.

- An original and extensive parametric testing of wafer sawing was made, leading to the development of a semi-analytical model for the wafer strength. The work presented here is based on a unique set of wafers sawn with different parameters in a production-like environment. The studied parameters were the abrasive grit size, the slurry density, the wire tension, and the feed rate. The influence of each parameter was analysed, as well as the interactions between them. A novel semi-analytical sawing model was then developed that describes the wafer strength using the sawing parameters. The sawing parameters influence on the wafer thickness was also studied and modelled. It was found that wafers sawn with a finer abrasive were stronger¹⁰ and that a lower slurry density also produces stronger wafers¹¹. The developed model showed that using a low wire tension and a slow feed rate increases the wafer breakage strength and that the sawing parameters had more influence on the wafers sawn with a fine abrasive. This model gives insight into the sawing process, in order to increase the wafer strength or to saw thinner wafers.
- A novel model for the apparition of saw marks is given. The effect of silicon debris inside the slurry was investigated by sawing several bricks with a different amount of debris in the slurry. The impact on the wafer quality was quantified and for the first time, a model describing the progress of saw marks is proposed¹³. This model allows the optimisation of slurry usage by knowing the amount of debris produced during one cut and the maximal amount of debris admissible.
- A first analysis of the diamond-wire sawn wafer surface is carried out⁹. New methods for characterising the wafer surface were developed, such as the use of Raman spectroscopy to quantify the amount of amorphous silicon on the wafer surface and measure the crystalline silicon internal stress, the use of electron backscattered diffraction to measure

the stress on a wafer section, and the use of optical micrographs to assess the amount of chips on the wafer surface. An important quantity of amorphous silicon was found on the wafer surface and its effects were investigated. The so-produced wafers were compared with slurry sawn wafers and the processability of diamond-wire sawn wafers into solar cells on existing industrial lines was analysed. It was found that diamond-wire sawn wafers can be used to make solar cells that are as efficient as reference cells, provided that the saw damage etching step is correctly adapted to the specific surface features of diamond-wire sawn wafers.

1.7 Outline of the thesis

In the next chapter, the response of silicon to mechanical solicitation is explained. The different deformation modes (i.e. dislocation generation and slip, phase transformation and cracking) are described together with the mechanical loading conditions needed to observe them. Based on that, Chapter 3 first describes general wear models that can be applied to wire-sawing and ends with a description of the existing wire-sawing models and some of the current research trends. In Chapter 4, the experimental tools used for this work are described and the experimental details are given. These methods are illustrated by giving typical results obtained and the chapter closes with a description of the important wafer characteristics for solar cell processing. In Chapter 5, the results of wafers sawn with different sawing parameters are shown, leading to insight to the wafering process and to an improved sawing model. Chapter 6 is focused on the impact of debris on the sawing quality, and a model describing this effect is given. Chapter 7 focuses on wafers sawn with a diamond-plated wire, their characteristics and their processability into solar cells. Finally, Chapter 8 gives the general conclusions of this study.

Chapter 2

Modelling the response of silicon to mechanical loading

The process of sawing wafers from a silicon block corresponds to wearing the silicon in the saw grooves. Thus, tribological models can give insights into the wafering process. To understand these models, the response of silicon to external solicitations has first to be described. One of the methods to study the properties of a brittle material like silicon is the indentation. In the case of silicon sawing, indentation processes are most likely to be responsible for material removal: indentation is nothing more than pushing a hard tip into the sample, while controlling the applied force and measuring the displacement of the tip. This induces cracks inside the sample. The crack propagation is in turn described by the tools developed for fracture mechanics.

This chapter will first focus on the fracture mechanics of silicon. From that, elements of indentation are introduced and some insight into the mechanisms of plastic deformation is given. The silicon scratching is discussed as it can give helpful information for diamond-plated wire-sawing. Finally, the anisotropy of silicon is discussed: sawing monocrystalline silicon can be improved by taking into account that the properties change with the crystallographic orientation.

2.1 Fracture mechanics

Crack generation and propagation is of paramount importance for treating the problem of indentation. The cracks are not only the deepest defects created — at least under a large load — but they are also detrimental for the wafer mechanical stability. Indeed, the cracks are stress concentrators, and when a small stress is applied to a cracked sample, the stress

level is much larger near the crack tip. The cracks introduced in the wafers during sawing are potential failure points of the wafers, either during the subsequent photovoltaic cell production, or during its lifetime. A perfect sample without any crack on its surface or in its bulk should be able to sustain a really large stress, up to the limit imposed by the inter-atomic bonds (roughly given by $E/10$, E being the Young's modulus). In practice, such a case is not realistic, as even the smallest defect on the surface of the sample will strongly decrease its fracture strength, but a carefully prepared sample can almost reach limit, e.g. freshly drawn glass fibres or metallic whiskers. The first crack propagation model was developed by Griffith in 1920⁵⁰ to explain the failures of aircraft parts, despite the fact that they were built much stronger than what was thought to be needed at the time. He stated that the elastic energy stored in a sample under tensile stress relaxes when the crack propagates. This release of energy has, in order for the crack to propagate, to be at least equivalent to the amount of energy needed to create the two free surfaces forming the sides of the crack. The elastic energy released when a crack of length c propagates a length dc , as shown in figure 2.1, is:

$$dE_{el} = -\frac{\sigma^2}{4E}\pi cdc \quad (2.1)$$

where E is the Young's modulus and σ is the applied stress. The amount of energy required to increase a crack of a length dc is:

$$dE_s = 2\gamma dc \quad (2.2)$$

where γ is the surface energy (dependent on the material). Thus, a crack propagates when $\frac{dE_{el}}{dc} \geq \frac{dE_s}{dc}$:

$$\frac{\sigma^2 \pi c}{E} \geq 2\gamma \quad \text{or} \quad \sigma \sqrt{\pi c} = \sqrt{2\gamma E} = \sqrt{EG_c} \quad (2.3)$$

where G_c is the toughness of the material considered.

This approach provides an easy method to determine when a crack propagates. But it can be hard to apply in practice. A second way, that was originally developed by Irwin in the 1950s is based on stress calculation around the crack tip and is the root of the linear elastic fracture mechanics (LEFM). A crack can be loaded in three different fracture modes (Fig. 2.2):

- Mode I: the stress is normal to the crack plane (opening mode).
- Mode II: the stress is in the crack plane, perpendicular to the crack front (sliding mode).
- Mode III: the stress is in the crack plane, parallel to the crack front (shear mode).

The fracture mode depends on the stress field around the crack. Usually, a crack is not solicited in one mode only, but in a mixture of modes. From this analysis, the stress field (for

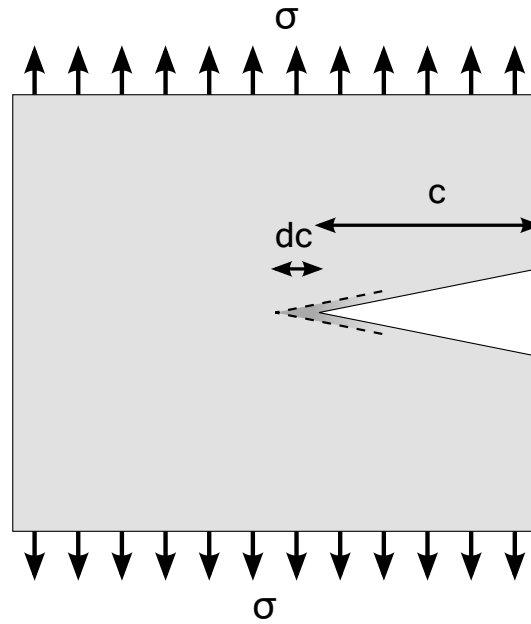


Figure 2.1: Crack propagation inside a sample. When the crack length (c) propagates a length of dc , elastic energy is released. On the other hand, energy is needed for creating the new crack surface. The balance of these energies determines whether the crack propagates when a stress σ is applied, see equation (2.3).

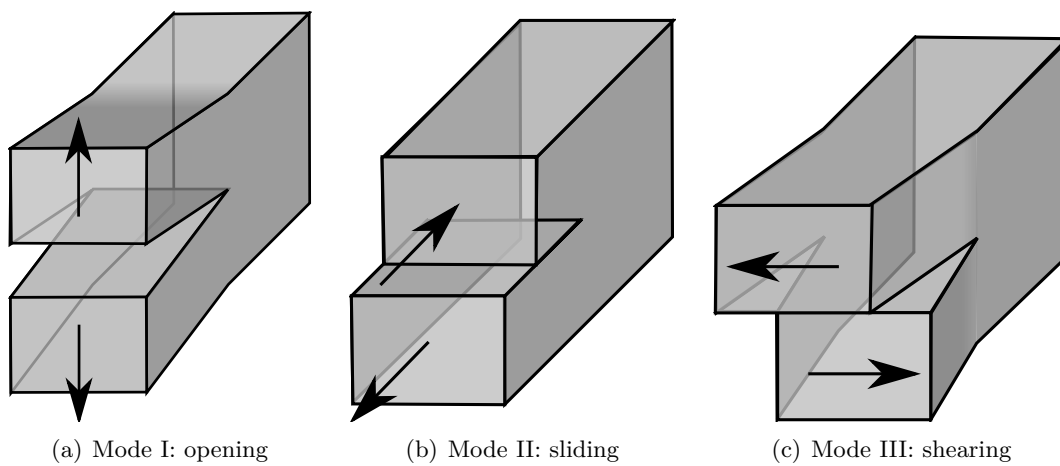


Figure 2.2: The three fundamental crack opening modes. Usually, the cracks are solicited in a combination of these modes.

mode I loading) can be described as:

$$\sigma_{rr} = \frac{K_I}{\sqrt{2\pi r}} \left(\frac{5}{4} \cos \frac{\theta}{2} - \frac{1}{4} \cos \frac{3\theta}{2} \right) \quad (2.4)$$

$$\sigma_{\theta\theta} = \frac{K_I}{\sqrt{2\pi r}} \left(\frac{3}{4} \cos \frac{\theta}{2} + \frac{1}{4} \cos \frac{3\theta}{2} \right) \quad (2.5)$$

$$\sigma_{r\theta} = \frac{K_I}{\sqrt{2\pi r}} \left(\frac{1}{4} \sin \frac{\theta}{2} + \frac{1}{4} \sin \frac{3\theta}{2} \right) \quad (2.6)$$

where r and θ are the coordinates in a polar system (Fig. 2.3). The stress near the crack tip can be rewritten as a product of three terms:

$$\sigma_{ij} = \frac{1}{\sqrt{2\pi r}} K_\alpha f_{ij}^\alpha(\theta) \quad (2.7)$$

where $\alpha = \{I, II, III\}$ is the crack opening mode. The factor K_α depends on the geometry of the crack and of the stress field, but not on the position near the crack front (as it is taken into account in the other terms). The value of K_α (called the stress intensity factor) can thus be written as:

$$K_\alpha = Y \sigma \sqrt{\pi c} \quad (2.8)$$

where Y is a factor depending on the problem that has to be solved. For instance, a single edge notched specimen (where the crack goes through the whole thickness of the specimen) has a value $Y \approx 1.12$ for small cracks. The crack propagates when the stress intensity factor (K_α) reaches a critical level K_c which is a material property. K_c is named the fracture toughness and can be linked to the surface energy used in Griffith's approach:

$$K_c = \sqrt{EG_c} \quad (2.9)$$

For a thin plate having a semi-elliptic crack at its surface and loaded in tension as shown in figure 2.4(a), the stress is not the same near the sample surface or at the bottom of the crack. This causes the crack to change its geometry during the crack propagation. The stress intensity factor for this problem has been solved by Raju and Newman using a finite element method in 1979¹⁰⁵, and this solution was then approximated to a closed-form equation⁹¹. This solution was then further improved, but the original solution gives results that are precise enough for this study:

$$K_I = (S_t + HS_b) \sqrt{\pi \frac{c}{Q}} F\left(\frac{c}{t}, \frac{c}{e}, \frac{e}{B}, \phi\right) \quad (2.10)$$

where S_t is the remote uniform stress, S_b is the remote outer-fibre bending moment, c is the depth of the crack, $2e$ is its width, t is the plate thickness, $2B$ is its width and ϕ is the angle

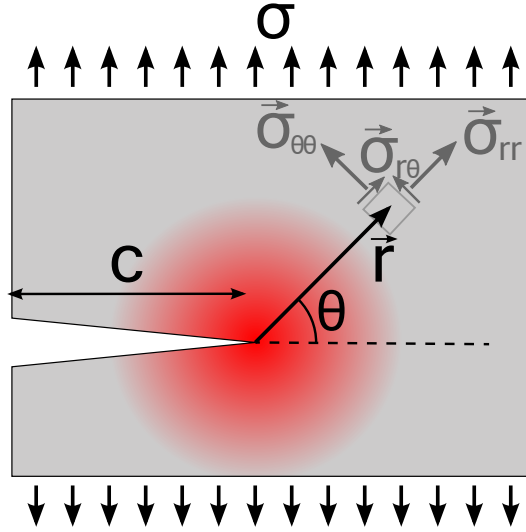


Figure 2.3: Simplified view of a crack of length c , subject to a stress σ far from its position. The coordinate system used for describing the stress in front of a crack is also shown.

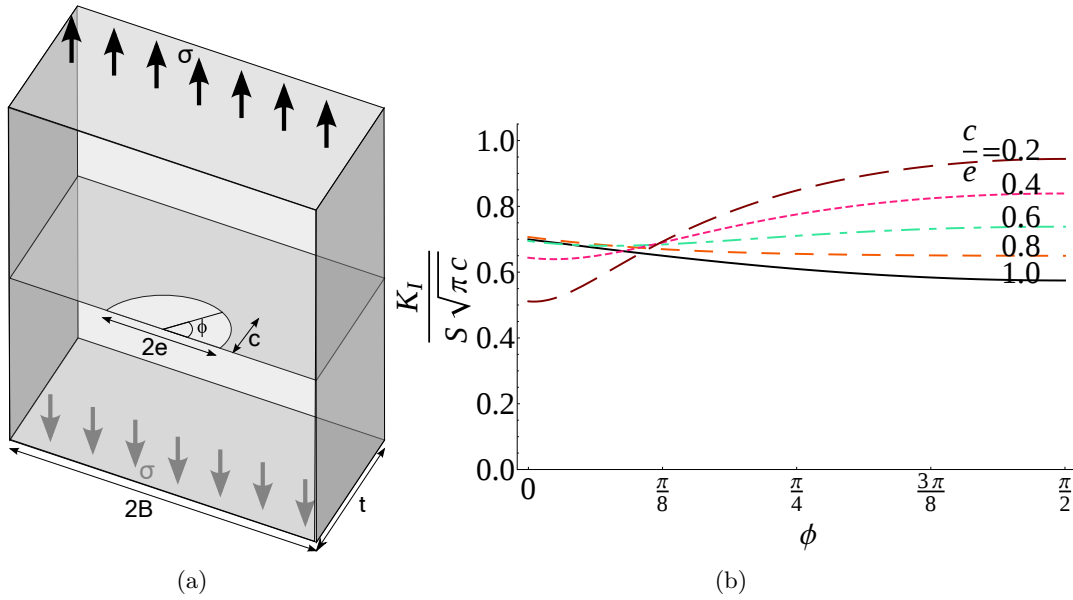


Figure 2.4: a) surface crack in a finite plate. The crack depth is c , its length is $2e$, the plate width is $2B$ and its thickness is t . The angle between the point observed and the surface is defined by ϕ . b) Stress intensity factor for a surface crack (depth $c = 20 \mu\text{m}$) in a $t = 200 \mu\text{m}$ plate in pure bending calculated with the equation (2.10) found by Newman et al⁹¹.

between the sample surface and the radial to the point where the stress intensity factor is calculated, as shown in figure 2.4(a). This equation is valid for $0 < \frac{c}{e} \leq 1$, $0 \leq \frac{c}{t} < 0.8$, $\frac{e}{B} < 0.5$ and $0 \leq \phi \leq \pi$. The functions Q , F and H are given by series of factor that can be found in Newman *et al*⁹¹.

The stress intensity factor calculated from these equations is plotted in figure 2.4(b). It appears that a half-penny crack in a plate under bending first propagates at the surface, until the a/c ratio reaches ≈ 0.6 . At that point, the stress intensity factor at the bottom of the crack and the one at the surface are equal, and the crack propagates in both directions. A very shallow but wide crack (like those found under a scratch, for instance), on the contrary, first grows deeper before getting wider. Figure 2.4(b) show the stress intensity factor of a crack depending on the position on the crack front, for several geometries.

2.2 Indentation mechanics

Indentation testing consists in progressively loading a hard tip on a sample and then removing the load, as shown in figure 2.5(a). There are two families of indenters: blunt indenters that produce essentially elastic contact patterns or sharp indenters that produce plastic contact patterns. Both indenters — if loaded enough — produce cracks, whose pattern depends on

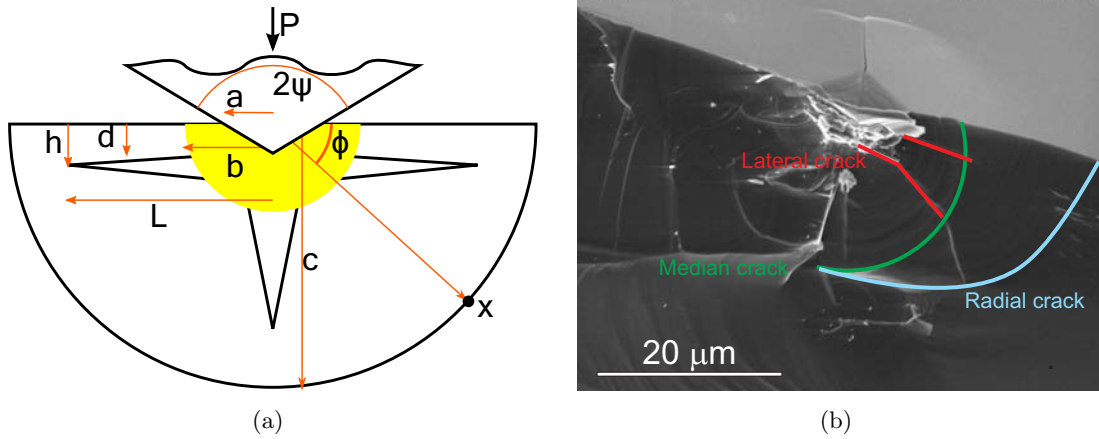


Figure 2.5: (a) an indentation and the cracks created. The force P is progressively loaded, then unloaded. The indenter penetrates to a depth d into the sample. The size of the imprint is represented by a and the size of the plastic deformation is b . The median cracks propagate down to a depth c . The lateral crack system is characterized by a depth h and a length L . (b) an SEM picture of the cracks under a Vickers indentation in silicon. The median, the radial and the lateral cracks have been underlined for clarity.

the geometry of the indenter, the maximal load and the indented material. The study of indentation fracture started in the 1970s with Lawn, Marshall, Evans *et al*^{26,27,38,78,79,83,84}. The blunt indenters produce so-called cone cracks starting from the edges of the imprint and propagating down into the sample in a conical shape. The sharp indenters, on the contrary, produce a larger family of cracks (Fig. 2.5(a)), some propagating during the loading part of the test (the median / radial cracks, on symmetry planes containing the load axis), others during the unloading part of the test (the lateral cracks, of a plate-shaped form near the sample surface⁸³), as shown in figure 2.5(b). The median / radial cracks can be separated in two different parts: the median orientation going deep into the sample and the radial orientation propagating near the sample surface. The median crack can be understood with the elastic stress field⁷⁸, but it does not provide a good explanation of the radial crack shape nor any explanation for the creation of the lateral cracks, that are entirely formed during the unloading, i.e. while the elastic stress field decreases. Only a plastic deformation can account for these crack families. Thus, taking into account a zone of plastic deformation under the indenter tip, Marshall *et al*⁸³ added stress intensity factors coming from the elastic deformation, from the plastic deformation and from a surface stress (e.g. coming from tempering the sample) to have a net stress intensity factor that can be used to calculate the crack depth and relate it to bending tests. Under a perfect elastic field, the stress intensity factor K_e is given by⁸³:

$$K_e = \chi_e \frac{P}{c^{3/2}} \quad (2.11)$$

where χ_e is a constant depending on the indenter and on the sample, P is the indentation load, and c is the median crack radius (assumed to have an ideal half-penny geometry). The plastic deformation around the indent has a similar effect on the crack, but this stress is still present after the indentation. The stress intensity factor from the plastic part of the deformation is:

$$K_r = \chi_r \frac{P^*}{c^{3/2}} \quad (2.12)$$

where χ_r is a constant depending on the indenter and the sample and P^* is the maximal load applied during the course of the indentation. In case a surface stress is present in the sample before the indentation test, it also has a surface stress intensity factor:

$$K_s = \sigma_s \sqrt{\pi \Omega c} \quad (2.13)$$

where σ_s is a surface stress acting uniformly on the crack area and Ω is a dimensionless crack geometry term. The resulting net stress intensity factor is then given by:

$$K = K_e + K_r + K_s = K_c \quad (2.14)$$

where K_c is the fracture toughness of the indented material. From this equation, it is possible to predict the size of the median crack during the indentation:

$$\chi_e \frac{P}{c^{3/2}} + \chi_r \frac{P}{c^{3/2}} + \sigma_s \sqrt{\pi \Omega c} = K_c \quad (P \uparrow) \quad (2.15)$$

$$\chi_e \frac{P}{c^{3/2}} + \chi_r \frac{P^*}{c^{3/2}} + \sigma_s \sqrt{\pi \Omega c} = K_c \quad (P \downarrow) \quad (2.16)$$

where $P \uparrow$ indicates that the equation is valid for the loading part of the indentation and $P \downarrow$ that the equation is valid for the unloading part of the test.

To account for different crack growth at the bottom of the crack and near the surface, as observed with an optical microscope during the indentation⁸³, the model needs to be refined so that the constants χ_e and χ_r depend on the position on the crack (at the bottom or at the sample surface) as determined with the angle ϕ between the position on the crack and the surface of the sample (Fig. 2.5(a)), and also depend of the indenter shape⁷⁸. The effect of the plastic zone can be modelled by an expending zone: first, an unstressed half-sphere of radius b is removed from the semi-infinite sample. Then, this half-sphere is plastically deformed by indentation over a contact a and a penetration d such that the strain associated with the indentation is accommodated by an expansion of the sphere radius (Fig. 2.5(a)). Finally, the deformed sphere is restored back to its original dimension by applying a hydrostatic pressure, reinserted in its original location and allowed to relax. After this treatment, χ_r is found to be⁷⁸:

$$\chi_r = \xi_r(\phi) \left(\frac{E}{H} \right)^{1-m} (\cot \Psi)^{2/3} \quad (2.17)$$

where $\xi_r(\phi)$ is a dimensionless term independent of the indenter and sample, H is the hardness of the sample, $m \approx 1/2$ has been found to be a reasonable approximation for a large number of materials⁷⁸ and Ψ is the indenter half-angle. For the elastic part of the stress field, it is found that⁷⁸:

$$\chi_e = \xi_e(\phi) \ln\left(\frac{2c}{b}\right) \quad (2.18)$$

where $\xi_e(\phi)$ is another global term and b is the radius of the plastic zone (Fig. 2.5(a)). From their analysis, Lawn *et al*⁷⁸ also found that during indentation, the median crack mostly propagated during the loading, and the radial part of the crack mainly grows during unloading. The definitive crack geometry, as it depends on the plastic deformation behaviour of the sample

in the term χ_r is material-dependant. The crack length evolution is shown in figure 2.6, for a maximal load of 10 N.

Chiang *et al*²⁶ took the same approach of an expanding cavity to model the plastic deformation around an indentation, but refined the mathematical treatment to find the stress field around the indent and, based on the material properties, to predict the extent of the cracks. They started by defining a relative indentation dimension β ²⁶:

$$\beta = \frac{b}{a} = \left(\frac{V}{\Delta V} \right)^{1/3} \quad (2.19)$$

where ΔV is the indentation volume and V is the plastic zone volume (Fig 2.5(a)). For monocrystalline silicon, Chiang *et al* calculated the value of β to be 2.65²⁶. For other materials, β varies between 2.3 for very brittle materials (soda-lime glass) to around 7 for a very ductile material (hot rolled brass)²⁶. With the spherical cavity solution, they found that:

$$\frac{p}{y} = \frac{2}{3} (1 + \ln(\beta)^3) \quad (2.20)$$

$$\frac{E}{y} = 3(1 - \nu)\beta^3 - 2(1 - 2\nu) \quad (2.21)$$

where p is the indentation pressure, y is the yield stress and ν is the Poisson's ratio. They started by calculating the elastic / plastic deformation for a spherical cavity of radius a under a pressure p , creating a spherical plastic zone of radius b . This provides a symmetric elastic / plastic field. A free surface is then created through the sphere centre and surface forces are

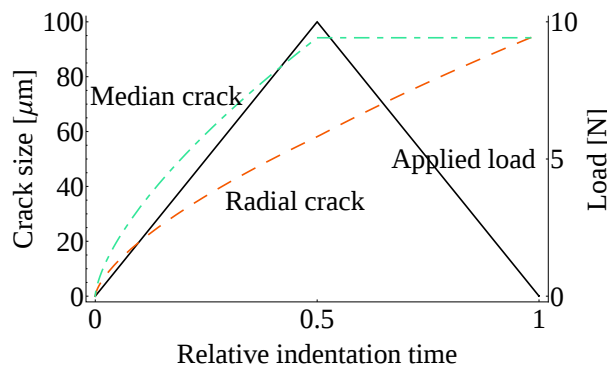


Figure 2.6: Evolution of the crack size during an indentation in silicon. The applied load increases during the first half of the indentation and then decreases. The median crack grows only during the loading, but the radial crack grows both during the loading and the unloading part of the indentation. From the data given by Lawn *et al*⁷⁸.

added to balance the stress from the cavity. The stress field during loading is finally given by²⁶:

$$\left. \begin{aligned} \frac{\sigma_r^{pl}}{p} &= \frac{3 \ln(r/a)}{1 + 3 \ln(\beta)} - 1 \\ \frac{\sigma_t^{pl}}{p} &= \frac{3(\ln(r/a) + 1/2)}{1 + 3 \ln(\beta)} - 1 \end{aligned} \right\} \beta > \frac{r}{a} > 1, \quad (2.22)$$

$$\left. \begin{aligned} \frac{\sigma_r^{el}}{p} &= \frac{-\beta^3}{(r/a)^3(1 + 3 \ln(\beta))} \\ \frac{\sigma_t^{el}}{p} &= \frac{\beta^3}{2(r/a)^3(1 + 3 \ln(\beta))} \end{aligned} \right\} \frac{r}{a} > \beta$$

where the superscript *pl* indicates the plastic region and *el* indicates the elastic region, and σ_r indicates the radial stress and σ_t indicates the tangential stress. After removal of the indenting load, the stresses become:

$$\left. \begin{aligned} \frac{\sigma_r^{r,pl}}{p} &= \frac{3 \ln(r/a)}{1 + 3 \ln(\beta)} - 1 + \frac{1}{(r/a)^3} \\ \frac{\sigma_t^{r,pl}}{p} &= \frac{3(\ln(r/a) + 1/2)}{1 + 3 \ln(\beta)} - 1 - \frac{1}{2(r/a)^3} \end{aligned} \right\} \beta > \frac{r}{a} > 1, \quad (2.23)$$

$$\left. \begin{aligned} \frac{\sigma_r^{r,el}}{p} &= \frac{1}{(r/a)^3} \left(1 - \frac{\beta^3}{1 + 3 \ln(\beta)} \right) \\ \frac{\sigma_t^{r,el}}{p} &= \frac{1}{2(r/a)^3} \left(\frac{\beta^3}{1 + 3 \ln(\beta)} - 1 \right) \end{aligned} \right\} \frac{r}{a} > \beta$$

where σ^r refers to the residual stress. The stresses σ^s created by the surface forces have the general form:

$$\frac{\sigma_{mm}^s}{p} = \int_{plastic} dA \frac{\sigma_t^j}{p} g_{mm} + \int_{elastic} dA \frac{\sigma_t^k}{p} g_{mm} \quad (2.24)$$

where $j = pl$, $k = el$ at peak load; $j = r, pl$, $k = r, el$ for the residual field; the subscript *mm* represent either *r, t* or ϕ and g_{mm} is a point force function²⁶. The final stress is obtained by superposing the equation (2.24) with (2.22) or (2.23).

The crack initiation is much harder to determine than the stable crack length. On a batch of indents made under the same conditions, it is possible that some tests have produced cracks but others not, or that the indents do not show any reproducible cracking pattern. It appears that the nucleation limits the crack creation, but once a crack is formed, it propagates in an unstable way until it is in equilibrium with the stress field and then continues growing in a stable way²⁷.

The residual stress field, as it is present long after the indentation has been performed, can in some environments lead to slow crack growth that diminishes the material toughness measured with post-indentation tests, as shown by Anstis *et al*⁴.

The lateral cracks are important for determining the wear rate of a sample subject to erosion or repeated indentations, as in the sawing process (Fig. 2.7). Indeed, as the median cracks go deep into the bulk of the sample but are not responsible of any material removal, lateral cracks — as they are close to the surface — can easily form chips leaving the sample that cause an important material loss, thus wear⁸⁴. Following the same approach as previously⁷⁸, Marshall, Lawn and Evans developed a model to determine the crack extension for a given indent⁸⁴. They assumed that the depth of the lateral cracks could be identified with the depth of the plastic zone³⁸: $h \approx b$ (Fig. 2.5(a)). The stress analysis from Chiang *et al* found a maximum tensile stress opening lateral cracks at a depth approximately half of that of the plastic deformation²⁶: $h \approx b/2$. Marshall *et al* found that the crack extension L was given by⁸⁴:

$$L = c^L \sqrt{1 - (P_0/P)^{1/4}} \quad (2.25)$$

where P_0 represents an apparent threshold:

$$P_0 = \frac{\zeta_0}{C^2} (\cot \Psi)^{-2/3} \frac{K_c^4 E}{H^3 H} \quad (2.26)$$

where ζ_0 is a dimensionless constant and c^L represents a limiting crack function:

$$c^L = \sqrt{\frac{\zeta_L}{C^{1/2}} (\cot \Psi)^{5/6} \frac{(E/H)^{3/4}}{K_c H^{1/4}} P^{5/8}} \quad (2.27)$$

and ζ_L is a dimensionless constant, independent of the material-indenter system, Ψ is the indenter angle and C is a compliance coefficient. In the case of high contact load, the equation (2.25) reduces to $L = c^L \propto P^{5/8}$. The volume of material removed when a lateral crack chips is given by:

$$V_l \propto L^2 h \quad (2.28)$$

Thus, the volume removed is proportional to the load applied at the power 7/4. Once again, this analysis does not take into account that a chip can be formed but still adheres to the specimen until a further indent removes it, which means that this second indent is less efficient in terms of material removal.

All these tests were made primarily on glass and ceramics, and with a maximal load of several newtons, so that cracks nucleate and are stable at the end of the test. In comparison, wire-sawing involves much lower forces and a crystalline material whose atomic planes influence

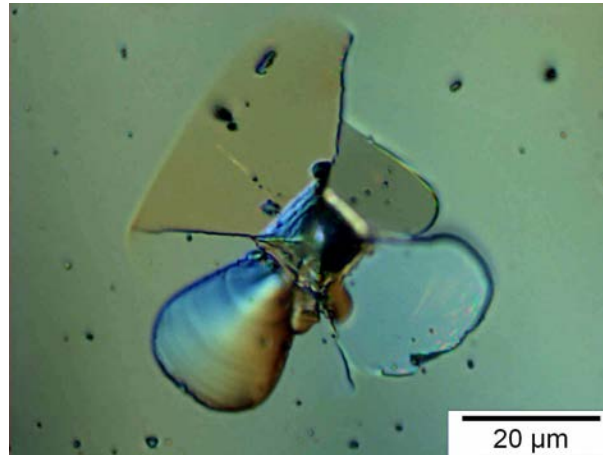


Figure 2.7: *Micrograph of a Vickers indent in silicon taken with an optical microscope. Radial cracks can be seen on the surface, as well as the trace of lateral cracks uplifting the sample surface. One lateral crack has chipped (lower left side of the indent) but the other only deformed the surface. Those about-to-chip cracks are the main source of wear due to indentation.*

the crack direction. Nonetheless, the same types of cracks are found when a silicon sample is indented at lower load, and the same formulae are applicable for lower-load indentation to predict the crack size. However, the crystallographic orientation of the sample can deflect the crack orientation, modifying the crack length.

The indenter shape is of paramount importance. But as the SiC particles are playing the role of indenter in sawing, characterising their shape is hard as it differs from particle to particle and depends on the orientation of the particle when it indents the silicon.

2.3 Plasticity of silicon

The theory of indentation implies that a region of the indented sample has to deform plastically. In the case of silicon, it can occur in several ways:

- by dislocation creation and movement at low temperature,
- by dislocation creation and movement at high temperature,
- by phase transformation.

2.3.1 Dislocations

At room temperature, silicon is considered brittle and can only sustain a small amount of plastic deformation by dislocation generation and movement (Fig. 2.8). Dislocation movement

is possible without diffusion of atoms, but only in a plane defined by the dislocation line direction ($\vec{\xi}$) and the Burgers vector ($\vec{b}$). In any other direction, the dislocation movement would require the diffusion of atoms, which is possible at high temperature but not at room temperature. This movement is called climbing. Dislocations are essentially one-dimensional defects and thus have no beginning or end. The dislocations always start at a free surface (surface of the sample, interface or grain boundary) and go on until they reach another free surface. Another possible configuration is to have loops, when the dislocation is closing on itself.

At room temperature, these dislocations are very slow and only produced under high stresses. On the contrary, at a higher temperature, the silicon undertakes a brittle-to-ductile transition and dislocations are much easier to nucleate and to move, making silicon a ductile material. This transition depends on many other factors than the temperature, such as the loading speed, the test sample geometry or the doping level⁵⁸. The study of dislocations in semiconductors has long been of interest. Indeed, dislocations not only allow plastic deformation, but may also be electrically active and can compromise the functioning of devices. In 1958, J. Hornstra⁶⁰ first deduced from geometrical considerations that many different types of dislocations were possible in the diamond lattice. This lattice, which is also the same for silicon, consists of two face-centred cubic (FCC) lattices fitted together with a translation vector of: $\left[\frac{1}{4} \frac{1}{4} \frac{1}{4}\right]$. There are three possible slip planes: the (001), the (110), and the (111), which is the most important slip plane. The shortest lattice vectors that can be allowed as Burgers vectors are $\frac{1}{2} \langle 110 \rangle$. The packing sequence of the closed packed {111} planes is ... AaBbCc... where A, B and C are the planes of one FCC lattice and the a, b and c planes of the second

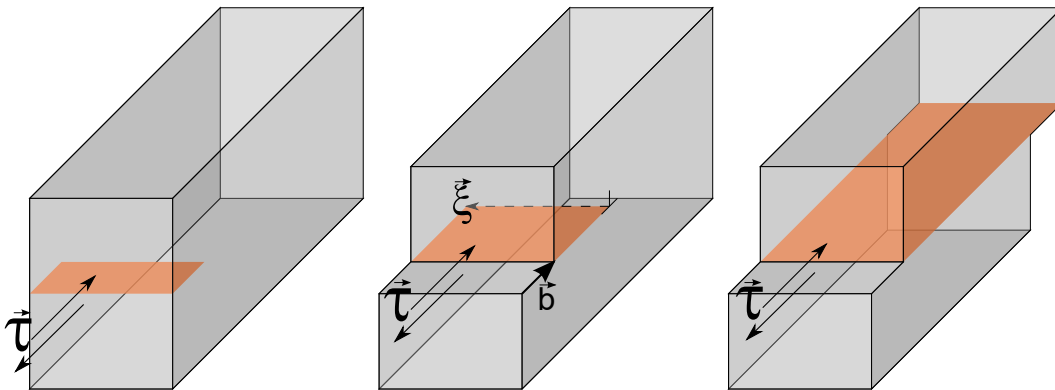


Figure 2.8: Simplified view of a dislocation gliding through a sample. The dislocation movement allows the sample to deform plastically. A dislocation can only glide on a plane (highlighted in the figure) defined by its line vector ($\vec{\xi}$) and the Burgers vector ($\vec{b}$).

FCC lattice. The distance between planes with the same letter (e.g. Aa) is smaller than the distance between planes of different letters (e.g. aB or bC). Dislocations can glide between these two different families of planes and are called “shuffle” when the core is laying between widely spaced planes and “glide” when the core is laying between closely spaced planes. From the geometrical considerations, Hornstra suggested that the basic dislocations possible in the diamond lattice were the screw dislocation (where the Burgers vector is parallel to the line vector), the 60° dislocation (the Burgers vector makes a 60° angle with the line vector) and the edge dislocation (the Burgers vector makes a 90° angle with the line vector). The dislocations are either stretching the inter-atomic bonds or ending atomic planes in dangling bonds. As having dangling — or stretched — bonds increases the internal energy of the crystal, it is possible that the dislocations split into two partial dislocations, putting less strain to the bonds. The dissociation of a dislocation depends not only of its type, but also on the plane (glide or shuffle) it is lying on.

Using TEM, it is possible to distinguish the Burgers vector of the dislocation. For example, Wessel and Alexander¹²² deformed a silicon sample at 420°C and observed samples with TEM. They found that the dislocations were dissociated, a 60° dislocation transforming into one 30° and one 90° partial gliding on the same plane and separated by a stacking fault. Two forces are competing between the partials: on the one hand, both partials create a stress field around them that acts towards a greater separation, but on the other hand, the stacking fault between the partials increases the internal energy of the crystal and the further apart the partials, the more energy is required, which tends to bring both partials together. Under a stress field, these partials do not have the same gliding speed and given the distance between them and the deformation they accommodated, Wessel and Alexander¹²² could determine which partial was the fastest. In order to minimize the internal energy, the core of the partial dislocation can again change, for instance by accepting doping atoms to avoid dangling bonds, or by reorganizing the atoms in the core^{65,80}. When the core is reorganised, the dislocation can no longer move, at least not without a new change of core configuration. In case this reorganisation involves doping elements, these atoms have to diffuse into the sample to follow the dislocation, which considerably slows down the glide.

Most of the studies on dislocation movement were made at high temperature where glide dislocations are created. Contrary to glide dislocations, shuffle dislocations are said not to be dissociable and to move much slower. But Rabier and Demenet^{100–104} found that under a high stress and a low temperature, the nucleated dislocations were in the shuffle set. They suggested that a transformation from one type of dislocation to the other was not possible¹⁰⁴ and that both types of dislocation were nucleated at a different range of temperature and stress. They found that the shuffle dislocation was primarily of direction $\langle 112 \rangle / 30^\circ$ and

$\langle 1\bar{3}2 \rangle$ / 41° from the Burgers vector (Fig. 2.9¹⁰⁰). Dislocations were also found near scratches made at room temperature¹⁰¹ and around indentations⁵⁷. In contrast to the dislocations in metals, silicon has deep Peierls valleys that constrain the dislocations to only a few well defined directions.

A dislocation increases the internal energy of the crystal. Thus, it is easier to nucleate a short dislocation than a longer one and dislocations are mostly created at stress-concentrating spots or near an interface. Usually, a dislocation is nucleated as a small loop that grows and extends as the crystal is deformed. The dislocation nucleation does not only occur at surfaces, but in the sample as well: dislocations can cross each other, leaving sessile dislocation segments that act as dislocation sources. In a Frank-Reed dislocation source, a dislocation is pinned at two positions (for instance by other dislocations, or inclusions, etc.) and a stress bends the segment between the pinned points until it makes a whole loop. The latter recombines into one regular loop and a dislocation segment between the two pinned points, as at the beginning (and thus in a configuration ready to form another new dislocation loop). In silicon, dislocations should be on shuffle planes, as it requires less energy to nucleate. But at high temperature, the dislocation movement is easier on the glide planes, as calculated by Duesbery and Joós³⁵. Furthermore, all the dislocations observed on samples deformed over the ductile–brittle transition are dissociated and thus in the glide plane. It appears that the nucleation in the glide plane is favoured at high temperature because nucleation is less difficult (so that dislocation both on the shuffle plane and on the glide plane can nucleate), but as dislocation

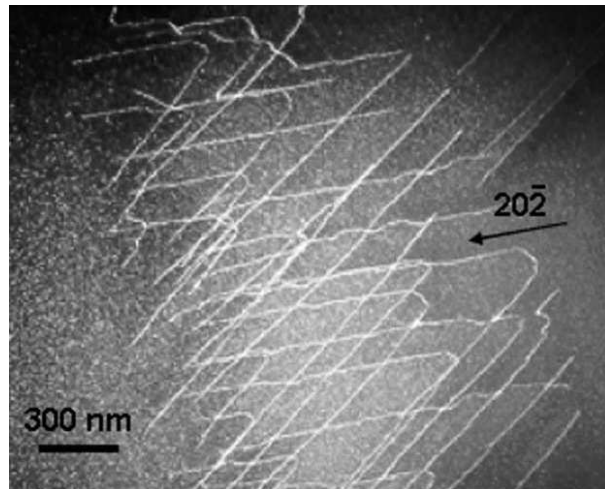


Figure 2.9: TEM micrograph of a silicon sample deformed at 150°C under a 5 GPa confining pressure. The dislocations are lying in a (111) plane. The micrograph was taken in weak-beam dark field with the diffraction vector $20\bar{2}$. After Rabier et al¹⁰⁰.

movement is favoured in the glide plane, these dislocations multiply.

2.3.2 Phase transformation

The study of silicon behaviour under high pressure began in the 1960s^{85,86}. Minomura and Drickamer⁸⁶ measured the electrical resistivity of several Zincblende lattice semiconductor (e.g. Si, Ge, GaAs, InP) subjected to an increasing pressure and observed a sudden drop of the silicon resistivity at a pressure around 195–200 kBar. They assimilated this drop with a phase transition to a denser metallic phase. This was confirmed by X-ray diffraction by Jamieson⁶¹. Since then, the study of high-pressure phase developed and more than seven different phases^{33,70,85} were found. During loading, the diamond lattice silicon (Si-I) transforms to a β -Tin (Si-II) phase around 12 GPa, then to Si-XI at ~ 13.2 GPa, to Si-V at ~ 16 GPa, then to Si-VI at ~ 37 GPa, to Si-VII at ~ 42 GPa and to Si-X at approximately 78 GPa^{70,85}. It was also found (as Minomura and Drickamer suspected) that a shear stress favours the phase transformation. Upon unloading, all the phase transformations at higher pressure than Si-II are reversible. But from Si-II, a slow decompression leads to Si-XII at about 10 GPa, which transforms reversibly to Si-III at approximately 2 GPa⁷⁰. Upon fast decompression, amorphous silicon (a-Si) is produced. Depending on the pressure release conditions, a mixture of Si-XII, Si-III and a-Si can also be obtained. Every phase transformation comes with a density change: the volume drop from Si-I to Si-II is 23.7 %. On unloading, the transition from Si-II to Si-XII results in a volume increase of 8 %⁹⁶.

All these tests were made on bulk samples subject to a hydrostatic stress, but the same phase transformations are found under silicon indents^{34,43,45,48,49,51,54,62,66,68,97,126–128}. Gupta and Ruoff⁵¹ used an indenter to measure the resistivity change of silicon during the test. They found that the phase transformation was different for a sample compressed in the $[111]$ direction than for a sample compressed in the $[100]$ direction and that the Si-II transformation was shear sensitive. As the resistivity of the sample dropped dramatically at the phase transformation point, they concluded that the phase transformation was to the metallic phase. This phase is much more ductile than Si-I and it could be seen on sharp indents that material was extruded out of the imprint, as shown in figure 2.10. Kailer *et al*⁶⁸ used micro-Raman spectroscopy to analyse the imprint of indentations with Vickers and Rockwell C indenters. They observed peaks related to the Si-III phase and other peaks that they related to the Si-XII phase. Then, they made faster tests and found only amorphous silicon. They concluded that Si-I was transformed to Si-II during the loading and further transformed into Si-III and Si-XII upon slow unloading, but into a-Si upon fast unloading. These phases were surrounded by a phase they called Si-IV where the stress was not high enough to cause a metallic phase transformation. They stated that the transformation to SI-IV was due to the shear stress.

The Si-IV phase is said to have a hexagonal structure. It was characterised by Kobliska *et al*⁷² in 1973. They produced bulk samples of Si-IV by annealing a sample of Si-III produced in a diamond anvil. Their characterisation was based on observations using Raman spectroscopy, X-ray spectroscopy, TEM observation and conductivity measurements. But their results are subject to caution, as this phase is hardly documented. Furthermore, the study of micro-crystalline silicon deposited by plasma or CVD with a Raman spectrometer shows that the Raman spectra assimilated to Si-IV is strangely similar to the one obtained with Si-I nano-crystals. Indeed, it was proved that the reduction of grain size allowed a relaxation in the phonon vibration constraints and thus the apparition of a new peak around 505–510 cm^{-1} ^{114,116}. Furthermore, it is also well known that annealing a sample of Si-III and Si-XII leads to a phase transformation to Si-I³³. Other occurrences of Si-IV phases were found after scratching or indenting silicon. In this case, it was argued that the presence of Si-IV came from a high pressure (but not high enough to lead to Si-II) together with a high shear stress. The zone where Si-IV was found, in the periphery of a zone where a “classical” phase transformation occurred, is a zone where a large amount of dislocations is present³³. This can explain the Raman spectra that were assimilated to the Si-IV phase, as twins and bands of dislocations can be present, also leading to a relaxation in the phonon vibration modes and a Raman spectrum assimilable to nano-crystalline silicon^{114,116}.

Ge *et al*⁴⁵ and Zarudi *et al*¹²⁷ have characterized the imprint of indents by transmission electron microscopy (TEM), as illustrated in figures 2.11 and 2.12. They found that Si-III and

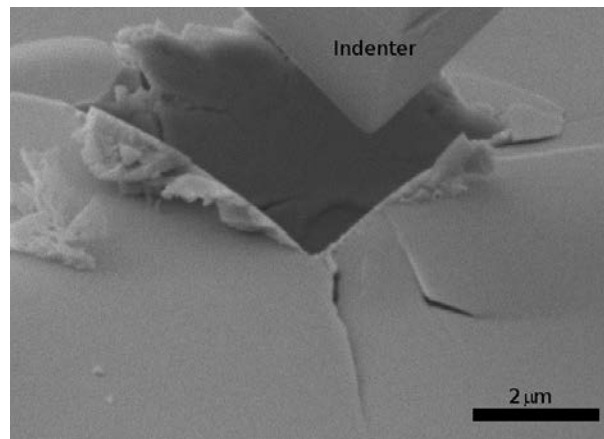


Figure 2.10: SEM micrograph of an indentation imprint from a cube-corner tip. As the indentation was made *in-situ*, the tip is visible over the imprint. Extruded silicon is visible on all sides of the indent, as well as radial cracks starting from each corner. The trace of a lateral crack forming a chip is also present on the right side of the imprint.

SI-XII coexist in the imprint, sometimes separated by an area of amorphous silicon, sometimes only by an interface. Previous TEM studies did not find traces of any metastable crystalline phase but this was believed to come from sample preparation⁴⁵.

Impacts of the indentation parameters (e.g. indentation speed, maximal load, shape of the indenter) were investigated by analysing the shape of the indentation curve and the microstructure produced, either by TEM or by Raman spectroscopy. Zarudi *et al* used a Berkovich and spherical indenters at several maximal loads, between 20 and 90 mN. They made a TEM analysis and finite element simulations of the pressure under the indenters to predict the extent of phase transformations. They concluded that a higher maximal load promoted a crystalline phase transformation and that the median crack has an important impact on the shape of the unloading curve, but could not relate this shape with the amount of phase transformation. Jang *et al*⁶² used pyramidal indenters with centreline-to-axis angle varying from 35.3° to 85.0°. They came to the same conclusions, but also found that a sharper indenter favoured crystalline Si-XII and Si-III phases because the transformed silicon volume increases with the sharpness of the indenter. In case of sharp indenters (e.g. cube corner), silicon can also be extruded out of the contact region, which has been taken as a sign of metallic phase transformation^{62,95}.

As for dislocations, a new phase has first to nucleate before growing. Bushby *et al* indented silicon, fused silica and InGaAs/InP with spherical indenters of different radii between 0.6 μm and 30 μm ²². They found that for large indents, the phase transition pressure was around 130 kbar, but for smaller indents (for an indenter radius $< 5 \mu\text{m}$), a higher pressure was needed for the material to yield. This is due, like the transition from Si-II to Si-III / Si-XII upon unloading, to a size effect: the likelihood of nucleating a new phase is higher when the volume of material that can undertake a phase transition is larger. Thus, when just a small volume of silicon (i.e. when the indenter radius is small) is stressed, a higher load can be applied before a phase transformation takes place.

Altogether, three mechanisms are at play during silicon indentation. On a large scale, cracks propagate both towards the bulk (median cracks) and parallel to the surface (lateral cracks) of the sample. Closer to the indentation, dislocations can be seen, but they do not account for much plastic deformation. Finally, near the centre of the indent, phase transformation (by decreasing the volume of silicon and rendering it ductile) allows plastic deformation. All three mechanisms are well visible on TEM micrographs taken by Zarudi *et al*¹²⁶, figure 2.13. Of all these mechanisms, the crack propagation is the most efficient in terms of material removal. But as the crack propagation is strongly influenced by the stress resulting from the plasticity near the centre of the indent (for example, the cracks in Fig. 2.13 start just under the transformed zone), dislocations and phase transformations should also not be forgotten.

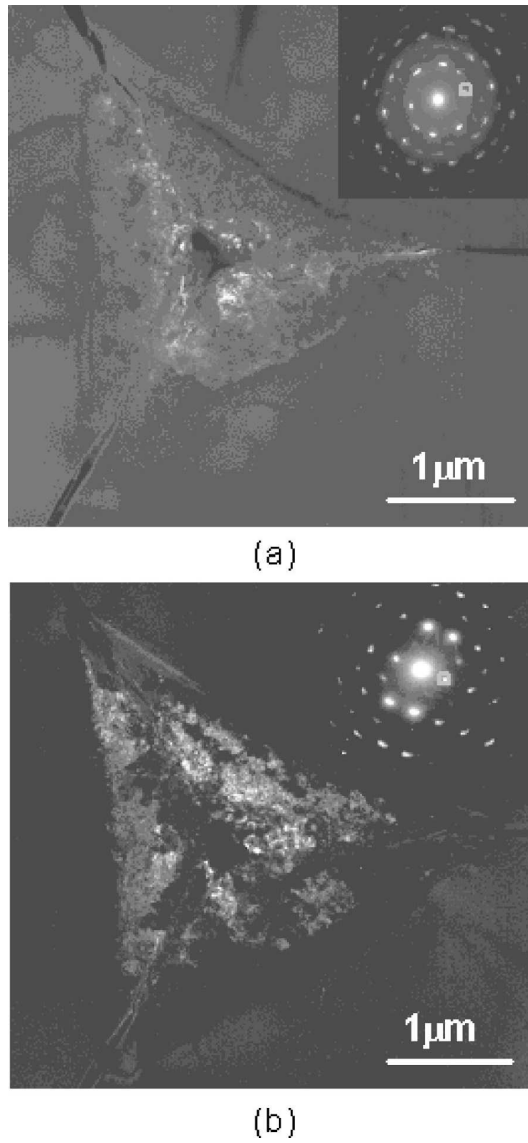


Figure 2.11: Dark-field TEM micrograph from the boxed reflections (200 of Si-III and 010 of Si-XII) and selected area electron diffraction patterns of (a) Si-III and (b) Si-XII in the nano-indentation on a (001) Si Wafer. After Ge et al⁴⁵.

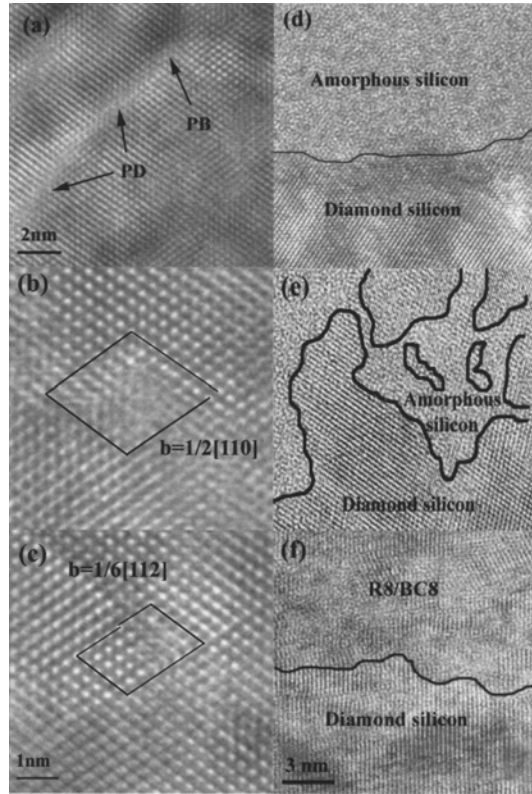


Figure 2.12: High resolution TEM micrograph (a) – (c) details of the plastic deformation in the pristine silicon near the transformation region: (a) plane bending (PB) and plane distortion (PD); (b) a perfect 60° dislocation; and (c) lattice shifting; (d) to (f): boundaries between the transformation zone and the pristine silicon: (d) taken at the bottom of the transformed zone; (e) taken on the edge of the transformed zone and (f) taken at the boundary of a deeper indent. After Zarudi et al¹²⁷.

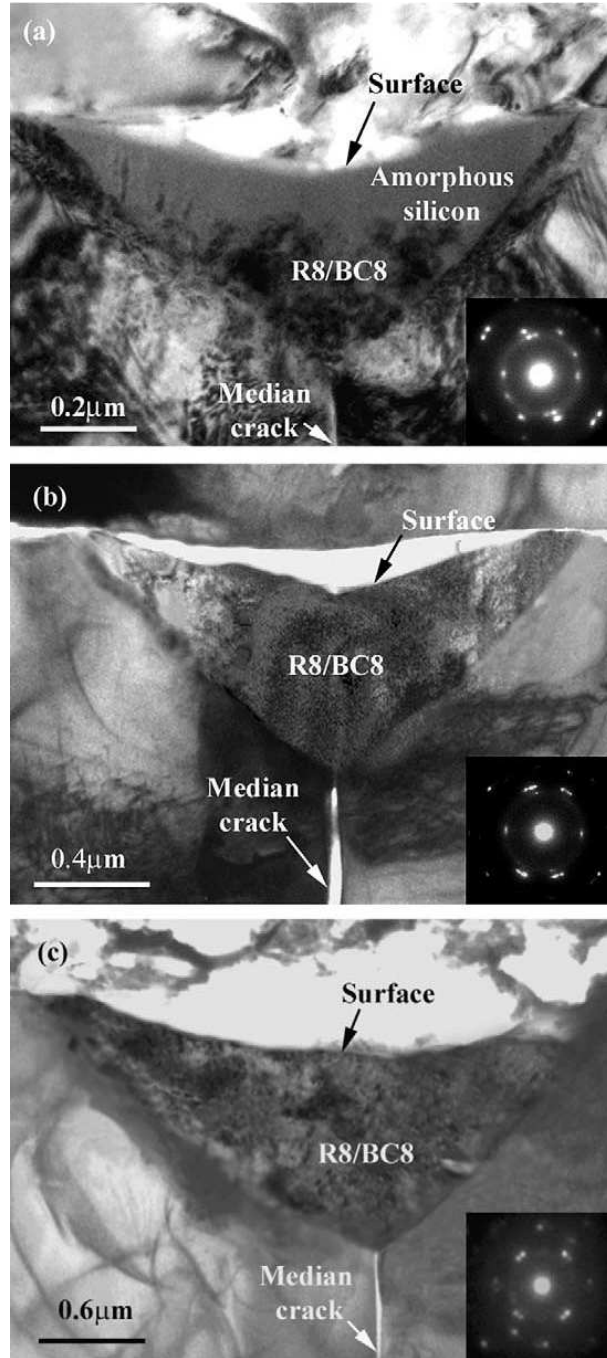


Figure 2.13: TEM micrograph of a silicon sample indented with a Berkovich indenter (the diffraction patterns of the transformation zones are inserted): (a) $P_{max} = 20$ mN, (b) $P_{max} = 50$ mN, (c) $P_{max} = 90$ mN. After Zarudi et al ¹²⁶.

2.4 Scratching

Scratching silicon is similar to indentation: a hard tip is pressed against the sample and dragged at the same time. Due to the lateral movement, the deformation speed is usually much faster than for an indentation. When scratching a silicon sample with a progressively increasing force, the same deformation mechanisms appear one after the other. First, a purely elastic deformation is caused by the tip, then a small groove plastically deformed can be seen, at a higher stress cracks appear on both sides of the groove until, at an important vertical force, chips appear. Similarly to the indentation, if the scratching speed is slow enough, a mixture of Si-III, Si-XII and a-Si can be observed, but at a high scratching speed, only amorphous silicon is present inside the groove and dislocation can also be seen under the scratch. Figure 2.14 shows a scratch at different loads and the different deformation stages.

Briscoe *et al* defined a scratching deformation speed as¹⁸:

$$\dot{\epsilon}_s = \frac{v}{d} \quad (2.29)$$

where v is the scratching speed and d is the depth of the indent. This was extended by Gassilloud *et al* to estimate the decompression rate⁴⁴:

$$\dot{\sigma}_s \approx \frac{2vP_m}{d} \quad (2.30)$$

where P_m is the mean contact pressure under the indenter:

$$P_m = \frac{P}{A} = q \left(\frac{4P}{\pi a_r^2} \right), \quad 1 \leq q \leq 2 \quad (2.31)$$

where P is the applied load, A is the projected contact surface, a_r the residual scratch width and q a parameter that considers the material response to scratching. They found out that at

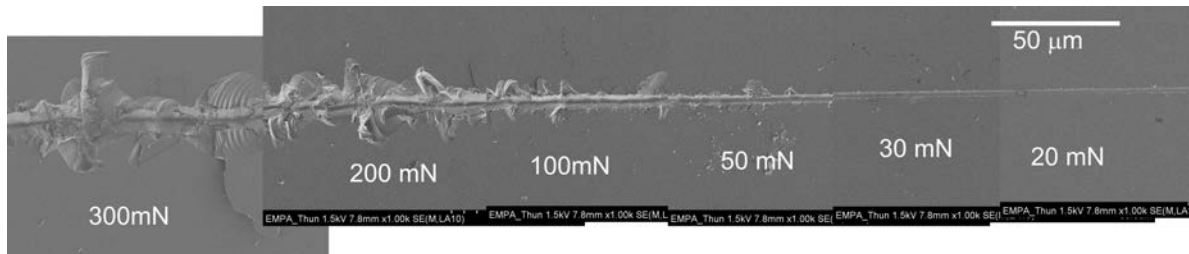


Figure 2.14: SEM micrograph of a scratch on silicon. Micrographs of several scratches at different normal forces have been joined, showing the different deformation mechanisms having a role in silicon.

a decompression rate slower than 10 GPa/s, a mixture of Si-XII and amorphous silicon was produced⁴⁴. At a decompression rate higher than this value, only amorphous silicon is created. Thus, for a scratch at constant speed but increasing load, the deformation first starts with amorphous silicon, then dislocations can be nucleated when the critical shear strain attains 4.2 GPa. At higher loads, the transformed silicon is a mixture of Si-XII and amorphous silicon⁴⁴.

2.5 Silicon anisotropy

Silicon — like any crystalline material — is anisotropic. The Young's modulus and the fracture toughness depend on the crystallographic direction (Fig. 2.15 shows the variation of elastic modulus with the crystallographic direction). O'Connor *et al*⁹² studied the thickness of plastic removal possible to achieve with a flycutter diamond tool (Fig. 2.16). It consists in a diamond tip rotating with a known radius of curvature and cutting into the sample. By knowing the length of the cut, it is possible to know its depth, and the depth at which a ductile-to-brittle transition appears. They cut (001) wafers along different directions, and observed that the most favourable cutting direction was along the [100] direction. In that direction, the depth of maximal plastic material removal was around 120 μm , compared to 40 μm on a harder [110] direction⁹². Transposed to the sawing, it seems that the best direction for sawing (or the one where it is harder to create defects) is the [100] direction, which is an unfavourable direction in terms of cleavage, according to Bhagavat *et al*⁸.

Bhagavat *et al*⁸ investigated the influence of the crystallographic anisotropy on the quality

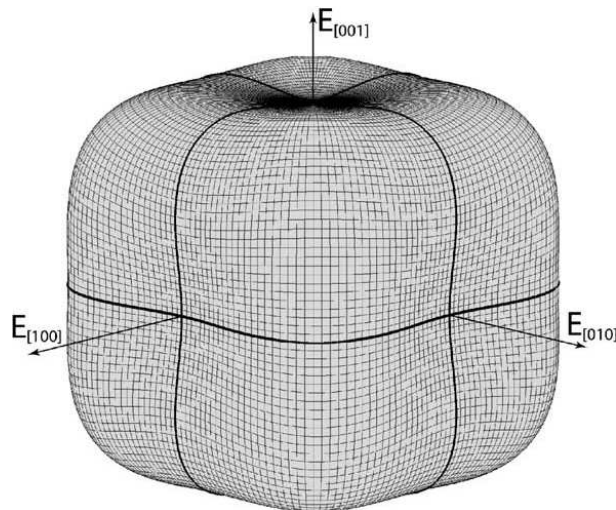


Figure 2.15: Elastic modulus anisotropy of silicon, after O'Connor *et al*⁹².

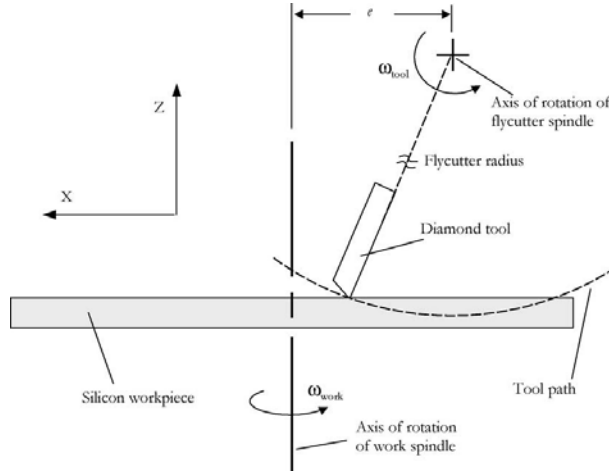


Figure 2.16: *Simplified view of the flycutter tool, after O'Connor et al⁹².*

of the wafers sawn. They stated that when keeping a crystallographic symmetry between both sides of the sawing groove, the silicon properties are the same on both sides of the wire, thus improving the sawing quality. For typical (100) crystals, this condition is always respected, but for (111) crystals, only six sawing directions (i.e. the feed rate direction, normal to the wire direction and parallel to the wafer surface) of the $\langle 1\bar{1}0 \rangle$ family respect this condition. On top of this, they took the effect of cleavage direction into account: when the abrasive particles induce cracks towards the wafer bulk in a favoured cleavage direction, these cracks are easier to propagate, making the wafers more fragile (the fracture toughness for the low index directions of silicon is given in table 2.1). According to this criterion, there are eight favoured cleavage directions for (100) crystals: $[01\bar{1}]$, $[0\bar{1}1]$, $[0\bar{1}\bar{1}]$, $[011]$ for the $\{111\}$ set of cleave planes and $[001]$, $[00\bar{1}]$, $[010]$, $[0\bar{1}0]$ for the $\{110\}$ cleavage planes⁸. To have stronger wafers, the wire axis has to be away from these directions. It is possible to respect these criterion only when sawing mono-crystalline silicon. Furthermore, this study is based only on geometrical considerations and is not backed by practical work.

Table 2.1: *Fracture toughness for different crystallographic orientations. After O'Connor et al⁹².*

Crystal plane	K_{IC} [MPa m ^{1/2}]
(100)	0.95
(110)	0.90
(111)	0.82

2.6 Chapter summary

The mechanical behaviour of silicon has been described. Silicon is mostly considered as a brittle material, although it can show some small-scale plasticity. When indented or scratched, the largest defects created are cracks. Two families of cracks exist: median / radial cracks are going deep towards the bulk and make the wafers fragile, whereas lateral cracks are staying parallel to the sample surface and are responsible for most of the material removal by creating chips. Closer to the indent, dislocations are found. When silicon is deformed at a low temperature, a large stress is needed to nucleate and move the dislocations, so that they cannot account for much deformation. The last deformation process described is the phase transformation. When a large pressure is applied, the diamond-lattice silicon transforms into a plastic Si-II (or α -Tin) lattice. This phase deforms plastically and is responsible of material extrusion when a sample is indented with a sharp indenter. On pressure release, Si-II transforms either into amorphous silicon (when the release is fast) or into a mixture of nanocrystalline Si-III, Si-XII and amorphous silicon (when the pressure release is slow). Each phase transformation implies volume change, and the last transformation can leave stress inside the silicon bulk.

In the next chapter, the equations used to describe the crack propagation during indentation are used to develop material removal models when silicon is worn. With the indentation fracture mechanics, it is possible to link the material removal process with the cracks created into the sample. Thus, by knowing the material removal conditions, the defects present in the sawn wafers can be estimated, which allows to guess the wafer mechanical strength.

Chapter 3

The sawing models

A wire-saw is a complex tool involving many input parameters, complex interactions of different natures, ranging from nanometres to a metre length scale, fast dynamic interactions as well as hour-long variations. The produced wafers are also not easy to characterise, as many different characteristics have to be taken into account for the solar cell production. Thus, it is not likely that a single model could capture every aspect of wire sawing, from the saw productivity to the wafer strength. Still, models proposed by other authors are helpful for understanding how the system works and getting hints about possible improvements.

As this work is focused on the defects created in the wafers and the fundamental material removal processes, only models related to the sawing process itself are presented. First, a micro-abrasion model is discussed. This model was developed to test the wear properties of hard coatings, but introduces useful concepts for slurry sawing. Then, the rolling-indenting model developed by Buijs and Korpel-van Houten is presented. It was first developed for describing the lapping of glass (and other brittle materials) and gives the crack depth and wear speed from the lapping parameters. Although this model is closer to wire-sawing than the micro-abrasion test, it cannot be readily used for describing the wafering. It is followed by a description of existing wire-sawing models. One was originally developed by Möller *et al* and focuses on the material removal rate. The other was developed by Wei *et al* to describe the wire vibrations. Finally, the ongoing research of other groups is presented.

3.1 The micro-abrasion test

In 1991, Kassman *et al*⁶⁹ developed a micro-abrasion test from a dimple grinder (Fig. 3.1(a)), consisting of a sample rotating around an axis normal to its surface and a hard counter-piece rolling at a fixed spot on the sample. One of the main advantages of this test is its ability to

characterise thin films because of the fixed shape of the wear scar. This test was then further developed by Hutchings *et al*^{1,108,115}. Instead of a dimple grinder, they used a hard ball rolling on the sample (Fig. 3.1(b)). This allowed better control of the experimental parameters and an easier analysis of the wear scar topography. They found that two wear regimes are possible, a “three-body abrasion”, also called rolling wear, where the particles are rolling on the surface and the region of the abrasive in contact with the sample is continuously changing, creating indentations, and a “two-body abrasion” or grooving wear^{1,115}, where the same region of the particle is always in contact with the sample and creates long groove on its surface. This depends on the wear conditions, in particular the abrasive particle concentration in the slurry and the normal load of the counter-body on the sample, but also on the respective hardness of the sample and of the counter-body. These two regimes showed different wear rates and a different dependence on the abrasive particle concentration¹¹⁵. They found that to have a three-body wear, the severity of the contact (S) has to be¹:

$$S = \frac{P}{AvH'} \leq \alpha \left(\frac{H_s}{H_b} \right)^\beta \quad (3.1)$$

where P is the applied load, A is the interaction area, v is the volume fraction of abrasive in the slurry, $\frac{1}{H'} = \frac{1}{H_b} + \frac{1}{H_s}$, H_b is the hardness of the ball and H_s is the hardness of the sample, α and β are empirical constants related to the abrasive size and the gap between the ball and the sample. Thus, a low load and a high abrasive concentration in the slurry favour a three-body wear, whereas a soft ball favours a two body wear.

But these tests are focused on the wear properties of metals and hard coatings and, despite an interesting view on the wear processes that can occur during silicon sawing and what the most important variables might be, they are quite different from wire-sawing. For one, the relative speed of the counter-body on the sample is slower (around 50 mm/s to avoid any hydrodynamic effect) and the geometry of the worn area is completely different (a crater in the case of the micro-abrasion test, and a long groove for the sawing). Nonetheless, a transition between rolling wear and grooving wear regimes is shown and is dependant — among other parameters — on the normal load on the sample and on the abrasive concentration.

3.2 The rolling-indenting model

In the beginning of the 1990s, M. Buijs and K. Korpel-van Houten worked on lapping of glass^{19,20}. They developed a model predicting the wear rate, the roughness and the crack depth from lapped samples in respect to the abrasive size, load, speed of the counter-piece and material properties (Young’s modulus, hardness and toughness of the sample)^{19,20}. This

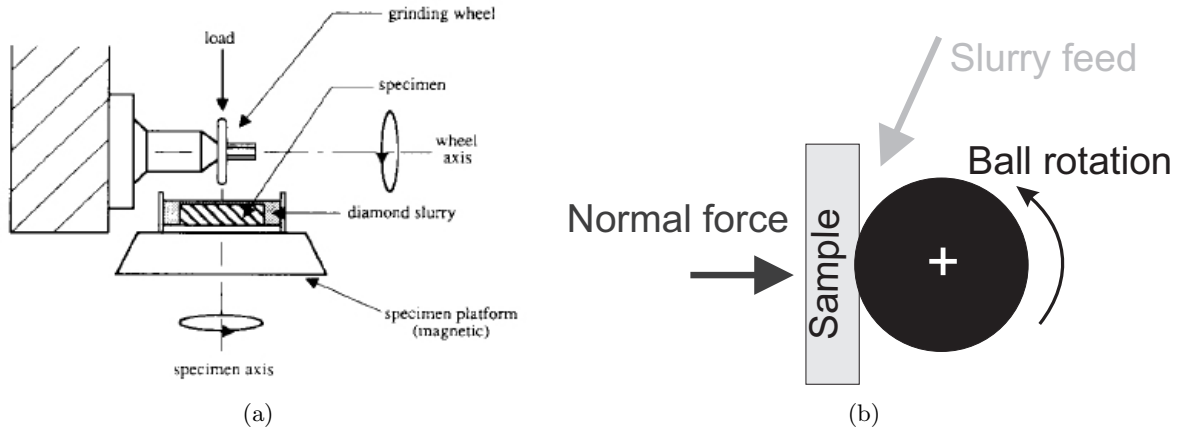


Figure 3.1: a) Abrasion test based on the dimple grinder originally used for TEM sample preparation. After Kassman et al⁶⁹. (b) Micro-abrasion test. A hard ball rolls on the sample and abrasive slurry is poured on the contact. The slurry composition, the normal load and the rotation speed can be set, wear is measured by the size of the crater.

experiment is illustrated in figure 3.2 and consists of a flat lapping plate turning and a sample holder on top of the plate, also turning. The samples in the holder are pushed on the lapping plate and slurry is poured on the plate which is taken into the contact between the sample and the plate.

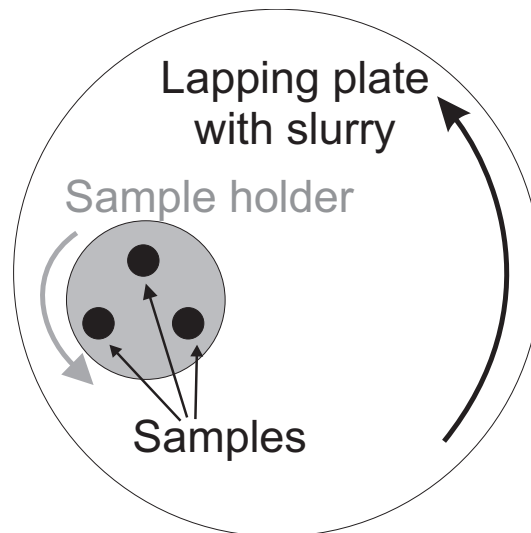


Figure 3.2: Diagram of the lapping test. Slurry is poured on the lapping plate and taken into the contact between the plate and the sample. The samples are pushed towards the plate.

As the abrasive particles are pressed between the sample and the plate, the mechanical properties of both bodies have to be taken into account. On the contrary, the particles are assumed to be rigid. They have found that the average peak-to-valley roughness and crack depth do not depend on the force applied, but only on the mechanical characteristics of the materials and on the abrasive size²⁰:

$$R_z = \alpha_1 \frac{E_w^{1/2}}{H_w} P_i^{1/2} \quad (3.2)$$

where R_z represents the peak to valley roughness, α_1 represents a constant depending on the particle shape ($\alpha_1 = 0.71(\cot \Psi)^{1/3}$ for a pyramidal indenter shape, where 2Ψ is the included angle), E_w and H_w represent respectively the Young's modulus and the hardness of the sample, and P_i is the normal load per load-bearing particle, which is not the average load per particle. Indeed, as the particles do not all have the same size and as the surface is rough, only the largest particles are in contact both with the sample and the lapping plate. By increasing the total load, the number of particles increases so that the load of each particle on the sample remains constant, exactly like when two rough surfaces are pressed against each other⁶⁴. From the indentation theory⁷⁸ (see section 2.2), they deduced the crack depth²⁰:

$$c = \alpha_2 \frac{E_w^{1/3}}{K_{Ic,w}^{2/3} H_w^{1/3}} P_i^{2/3} \quad (3.3)$$

where α_2 is a constant depending on the particle shape ($\alpha_2 = 0.1(\cot \Psi)^{4/9}$ for a pyramidal indenter) and $K_{Ic,w}$ is the fracture toughness of the sample. Finally, the material removal rate was found to be²⁰:

$$Z = \alpha_3 n \frac{P_i^{3/4}}{L_{m,c}} \frac{E_w^{5/4}}{K_{Ic,w} H_w^2} p v \quad (3.4)$$

where α_3 is a constant depending on the particle shape ($\alpha_3 = 0.01(\cot \Psi)^{7/6}$ for a pyramidal indenter), n is the number of indenting points on the circumference of the rolling particles, $L_{m,c}$ is the mean size of the load-bearing particles — which is not the mean size of the particle distribution — p is the applied pressure and v is the relative velocity of the sample on the lapping plate. From their experiments, it appears that the roughness — and the cracks depth — does not depend on the applied pressure (nor on the speed), but on the load per particle P_i . This is due to the fact that the applied pressure changes the number of particles in contact with the sample (thus the removal rate), but not the force applied by each particle on the sample. The same situation is encountered when two nominally flat rough surfaces are pressed

together⁶⁴. They finally found out that²⁰:

$$P_i = H_{eff} \left(1 - \frac{h}{L_{m,c}}\right)^2 L_{m,c}^2 \quad (3.5)$$

where h is the distance between the lapping plate and the sample and H_{eff} is the effective hardness defined by:

$$H_{eff} = \frac{\beta_w H_w}{[1 + (\beta_w H_w / \beta_{lp} H_{lp})^{1/2}]^2} = \frac{\beta_{lp} H_{lp}}{[1 + (\beta_{lp} H_{lp} / \beta_w H_w)^{1/2}]^2} \quad (3.6)$$

where β is a constant depending on the indenter shape ($\beta = 2 \tan(\psi)^2$ for a pyramidal indenter), the subscript w stands for the work-piece (the sample) and lp for the lapping plate. The ratio $\frac{b}{L_{m,c}}$ represents the angle of attack of the particle on the sample and depends, among other things, on the lubricant.

The crack depth was measured experimentally with a microscope, but also with bending tests and both methods correlated. This model shows that the roughness and the crack depth are correlated and do not depend on the applied pressure nor on the speed of the sample relative to the lapping plate. It puts the abrasive in the centre of focus in respect to the defects produced. When larger particles are used, the surface gets rougher and cracks get deeper. As the model assumes that only a few particles are in contact with the surface and that this number of particles is defined by the total load they have to sustain, the concentration of particles in the slurry does not come into play. The size of the particle in contact is given by the slope of the curve giving P_i as a function of L_m and is approximately twice the average diameter of the whole distribution.

This model neither takes into account the abrasive concentration in the slurry — contrary to the tests made with the micro-abrasion set-up — nor the particle size distribution. As for the micro-abrasion tests, the relative speed of the sample is much lower than the one of the wire during wafering. Another difference is that for both types of tests, the applied force of the sample on the counter-piece is known and the wear rate is measured, contrary to wire-sawing, where the sawing speed is set and the applied pressure has to adjust to it.

3.3 The wire-saw models

The wire-saw, in contrast to the other systems previously described, is characterised by a high wire speed, a long distance between the wire-guides and the sample that allows the wire to vibrate, and a long cutting area where slurry is only provided at the entrance of the wire into the block. One of the first groups that published work on the subject is the group of I. Kao *et*

*al*⁸¹. They started by developing a contact mechanics model, based on the indentation theory developed by Lawn, Marshall, Evans *et al*^{78,79,84} in the same fashion as the rolling-indenting model from Buijs and Korpel-van Houten^{19,20} for lapping described in section 3.2. But Kao *et al* focused on the interaction of a single abrasive particle and calculated the stress field around its indent, taking into account the shear stress due to the movement of the wire.

As it was stated earlier, the main difference between wire-sawing and lapping is that the wire speed is much faster and can give rise to hydrodynamic effects. In such a case, the lubricant film could form a cushion around the wire, supporting the vertical pressure, so that the abrasive particles are not in contact with the wire and the silicon block at the same time. It is possible to take a hydrodynamic approach, where for the first calculation, the abrasive particles do not play a role, only the slurry as a viscous liquid is taken into account. The main problem of such an approach is how the boundaries are set and how the semi-circular domain under the wire is transformed to facilitate the analysis. The pressure in the slurry can be calculated using Reynolds' equation (in 2 dimensions)⁷:

$$\frac{\partial}{\partial x} \left(\frac{h^3}{\eta} \frac{\partial p}{\partial x} \right) + \frac{\partial}{\partial y} \left(\frac{h^3}{\eta} \frac{\partial p}{\partial y} \right) - 6v \frac{\partial h}{\partial x} = 0 \quad (3.7)$$

where x is in the wire movement direction, h is the distance between the silicon and the wire, η is the slurry viscosity, p is the pressure, y is the direction transverse to the wire and v is the wire speed. Kao *et al* made a finite element analysis of the problem^{7,129}. They flattened the semi-circular domain around the wire using a mapping factor $f(y) = \cos(\frac{\pi}{2} \frac{y}{w})$ where w is the wire diameter and set a boundary condition so that the pressure is⁷:

$$p = 0 \quad \text{and} \quad \frac{\partial p}{\partial n_n} = 0 \quad (3.8)$$

where n_n is the outward normal to the boundary. They found a wire-silicon distance of around 400 μm . This distance is slightly smaller under the wire but in any case much larger than the particle size, which would imply that no direct contact between the wire, an abrasive particle and the silicon is possible. Möller *et al* made a similar calculus⁸⁸ but instead of converting the two dimensional flow around the wire into a flat flow, they assumed a one dimensional flow and added a correction factor taken as a “free parameter”. From this calculation, the film thickness was calculated to be about 40 μm . They concluded that only the coarsest particles could indent the silicon block, causing wear and creating cracks. The main drawback of these approaches is that their results were not confirmed by direct experimental observations. Furthermore, they are both incomplete: in the method used by Kao *et al*, the slurry cannot escape the semi-circular cavity (the term $\frac{\partial p}{\partial n_n} = 0$ prevents the slurry from flowing out of

the domain) and thus the slurry thickness mainly depends on the entry boundary condition. Möller *et al* used a “free parameter” to adjust the slurry layer to a plausible value. Finally, both analyses show very different results. Kao *et al* found that the slurry thickness is thicker near the entrance than near the exit (it decreases from 600 μm to less than 400 μm), and Möller *et al* found a constant layer thickness around 40 μm , apart from the very entrance and exit.

More recently, Wagner and Möller¹¹⁷ used a three dimensional model to estimate the distance between the silicon and the wire as well as contact forces between the silicon and the abrasive particles. They found that the wire-silicon distance was larger than the coarsest particles of the slurry. Also, Bierwisch *et al*¹⁴ used an explicit modelling of the PEG / SiC slurry in the aim of understanding the different contact regimes that can occur in sawing. They simulated the interactions between particles, PEG, the wire and the silicon. It turned out that in the non-contact regime (when the wire-silicon distance is larger than the particle size), only small contact pressures were possible. In contrast, relatively high loads are possible in the semi-contact regime (when the wire-silicon distance is smaller than the largest SiC particle size). Based on that, they stated that most of the material removal should happen in the semi-contact regime, but without being definitive about one type of contact or the other.

3.3.1 Wire vibration

As the wire is thin and only held by the wire-guides away from the silicon block (the distance between the wire-guides is almost one meter, but the silicon block is only 125 mm or 156 mm wide), it has room to vibrate. These vibrations induce a lower sawing quality and a higher kerf loss. Wei *et al*¹²⁰ have studied the vibration of such a wire with a purely theoretical treatment and also with finite element simulations. They found out that the wire was not running fast enough to have a critical vibration, but a cyclic excitation stress (provided by the indentation of abrasive grains on the wire) vibrates the wire. They described the movement of the wire by the Newtonian mechanics or Hamilton’s principle¹²⁰:

$$\rho(U_{TT} + 2VU_{XT} + V^2U_{XX}) - PU_{XX} = F \quad (3.9)$$

where U is the transverse (vertical) displacement of the wire in respect to its equilibrium position, V is the translating speed of the wire, P is the tension of the wire, F is the external excitation force applied on the wire per unit length, and ρ is the mass of wire per unit length, and the subscripts indicate the partial derivative (T for the time and X for the x direction, which is defined by the wire axis). The system also has the following boundary conditions

imposed by the wire-guides holding the wire at a fixed point.

$$U(0, T) = 0 \quad \text{and} \quad U(L, T) = 0 \quad (3.10)$$

Under cyclic excitation, the wire vibrates according to a vibration frequencies family. The slurry was also taken into account for damping the vibration. From this analysis, it was found that the vibrations could be decreased by increasing the tension, and that the speed of the wire had no significant effect. A more detailed study by finite element methods was made by Zhu *et al*¹²⁹ and they showed that a longer contact span (i.e. the width of the silicon block) induces less vibration. In the same study, they showed that a more important bow helps decreasing the vibrations, but could also cause the breakdown of a proper hydrodynamic machining environment. Finally, the viscosity of the slurry was not found to play a significant role in the vibrations. It is worth noting that all these findings are only theoretical and were not backed by experimental results.

3.3.2 Material removal models

Depending on the assumption made about the wire-silicon distance, the material removal rate depends on different sets of variables. For a direct wire-abrasive particles-silicon contact (the so-called semi-contact case), the situation is close to the rolling-indenting model developed for lapping described in section 3.2 and the equations derived for indentation cracking can be used (see section 2.2). According to Möller⁸⁸, the volume of material removed by a single grain is:

$$V_0 \approx F_N^{(4n+1)/2} \quad (3.11)$$

where F_N is the force applied by the grain and n is a factor that was determined experimentally to be equal to 0.85. The sawing rate can then be determined by:

$$v_s = \frac{mV_0}{A_s \Delta t} \quad (3.12)$$

where m is the number of indentation events, A_s is the global contact area (the surface of the groove) and Δt is the time interval during which the indentations occurred. Supposing that the grains are rolling and indenting the silicon once per revolution, and that the angular velocity is given by the slurry flow as $f = v/2L_0$ where v is the wire speed and L_0 is the wire-silicon distance, the sawing speed can then be described as⁸⁸:

$$v_s = v_{s0} v m F_N^{(4n+1)/2} \quad (3.13)$$

where v_{s0} is a pre-factor summarizing material and geometry parameters. The amount of particles indenting the sample (m) can be given from the total load of the wire on the sample, assuming that the total load is given by $F_{tot} = mF_N$, so that:

$$v_s \propto v F_{tot} F_N^{1.2} \quad (3.14)$$

indicating that for a semi-contact case, the sawing speed is proportional to the the wire velocity and wire load^{87,88}. In case of a non-contact case, there is no direct wire–abrasive particle–silicon contact so that the particles are flowing in the space between the wire and the silicon. For some reason, they can still indent the silicon — supposedly due to the hydrodynamic pressure and shear stress caused by the velocity difference between the wire and the silicon⁸⁷ — and the shear force acting on one particle is given by⁸⁷:

$$F_t = \tau \pi l_m^2 \quad (3.15)$$

where τ is the shear stress (given by $\tau = \mu \frac{dv}{dh}$, where μ is the slurry viscosity, $\frac{dv}{dh}$ is the slurry velocity gradient between the wire and the silicon) and l_m is the particles mean diameter. If one considers the iso-elastic regime (when the wire deforms elastically in response to the slurry pressure), the force acting on the particle is given by⁸⁷:

$$F_t = \pi l_m^2 \mu^{0.34} v^{0.34} F_{tot}^{0.21} E_{eff}^{0.44} / C_{IE} \quad (3.16)$$

where E_{eff} is the effective elastic modulus of the wire and silicon and C_{IE} is a geometric factor depending on the tool and workpiece surface⁸⁷. But this force is parallel to the slurry flow. Assuming an accidental deviation of the particle movement (for example because the surface is uneven), the normal force is then given by $F_N = \sin \phi F_t$ and the sawing rate depends on⁸⁷:

$$v_s \propto v^{1.1} \mu^{0.1} F_{tot}^{0.67} l_m^{2.4} \quad (3.17)$$

which shows a dependence on the wire velocity almost equal to the one for the semi-contact case, but a weaker dependence of the total force. Also, there is almost no dependence on the viscosity. With a similar approach, Bhagavat *et al*⁷ considered the energy transfer to the surface and found:

$$v_s \propto v^{0.68} \mu^{-0.32} F_{tot}^{0.42} l_m \quad (3.18)$$

Due to the different dependencies between the semi-contact and the non-contact model, it should be possible — assuming that the hypotheses founding the models are correct — to distinguish which model rules the wire sawing with a parametric study. Unfortunately, the

data available in the literature are too few and seem to indicate a mix of both models⁸⁷.

3.4 Research from other groups

There are several other groups working on the wafering, each with its own focal point. The group of H.J. Möller at the Bergakademie Freiberg concentrated on instrumenting the wire-saw, fitting it with measurement devices providing a more complete view of the sawing process. They installed a three dimensional force sensor between the silicon ingot and its holder. They also monitored the ingot temperature with an infra-red camera. From this information, they reached the conclusion¹⁰⁷ that the model they previously developed (see subsection 3.3.2) was accurately describing the impact of the sawing parameters on the macroscopic forces. With the same set-up, they studied the effect of using a smaller wire diameter and smaller abrasive on the force applied on the silicon. They arrived at the conclusion that better sawing conditions were achieved with a fine abrasive and a thin wire and that the wire diameter has to be adjusted to the abrasive size to have optimal results¹¹².

They also extended the previous model to a three dimensional model¹¹⁷. With finite element calculations, they simulated the course of abrasive grains inside the groove, for several slurry densities. They showed that it was possible that particles apply a force on the surface even when the wire-silicon distance was larger than the particle size.

Another research interest at the Bergakademie Freiberg is the modelling of wafer cracks in respect to the wafer strength and their surface treatment. Funke *et al* studied the different bending setups and the stress they apply on the tested wafers⁴⁰. As the wafers are thin and can sustain large deformations, finite element simulations were required to compute the bending stress^{40,41}. With this information, they related the fracture strength to the crack length of as-sawn and etched wafers. They could develop a length transformation function that relates the silicon etched thickness to a crack length decrease and a crack tip rounding and allows the modelling of the wafer strength change after etching⁴².

At the Fraunhofer-Center für Silizium-Photovoltaik in Halle, the research group working on wafering focused its research on the wafer mechanical stability and how to best test it¹¹¹. They studied the impact of edges on the wafer stability, but also the influence of different test set-ups on the results of wafer stability. Furthermore, they studied the impact of the crystallinity (mono- or multi-crystalline) on the wafer strength with ball-on-ring tests and the orientation of damages in respect to the sawing direction with 4-line bending tests and roughness measurements¹⁶.

The Fraunhofer Institute for solar energy systems (ISE) in Freiburg focused on the industrial improvement of wire-sawing, like the effect of decreasing the wire diameter and the

grit size on the wafers¹¹², the use of alternative substrates to replace silicon wafers⁹³ or the effect of etching, in addition to pursuing research towards a fundamental understanding of the wire-sawing process¹⁰⁶. They also studied the effect of cutting thin multicrystalline wafers on the wafer geometrical characteristics⁷⁵. Another subject they worked on is the comparison of diamond-plated wire sawing with slurry sawing, both in terms of wafer properties and in terms of costs⁷⁶. They concluded that both processes were comparable in terms of wafer quality, but the diamond-wire sawing was too expensive to be competitive with slurry sawing.

3.5 Chapter summary

In this chapter, several models describing wear rates have been described. Neither the micro-abrasion test where the existence of two different wear modes can occur, depending on the contact severity, nor the rolling-indenting model based on the indentation mechanics, describe accurately the wire-sawing situation in term of wear conditions but they provide meaningful insight in terms of wear mechanisms. Models specific to wire-sawing have also been introduced. One is focused on the wire vibrations and is based on theoretical models and the other is focused on material removal rate, depending strongly on the wire-silicon distance. Finally, the more recent research from other groups has been presented. But no existing model satisfactorily describes the defect size from the sawing parameters.

In the next chapter, the wafer characterisation methods are presented. Assumptions at the origin of the models presented above are checked, and the observed situation, in terms of defects present in the wafer, is compared with the defects presented in the previous chapter, so that a deeper insight into the wear mechanisms is gained.

Chapter 4

Wafer characterisation methods and typical results

As explained in Chapter 2, it is possible to find many different kinds of defects at and under the silicon wafer surface. Furthermore, not only are the defects present important, but also their localisation and orientation. In this chapter, the different characterisation methods used and sometimes developed in this study are described and illustrated with relevant results. It has to be kept in mind that the aim of this characterisation is to improve the sawing for the solar cell production, so that some wafer characteristics are more important than other.

After observing the wafer surface by SEM, the roughness measurement is presented. The roughness is found to be larger near the wire entry side of the wafer than near the wire exit. It can also be related to crack depth distribution and a method for measuring this is shown. The two bending set-ups used to measure the wafer strength are introduced and the stress they induce on the wafer is analysed by finite elements simulations. It was found that a breakage strength variation larger than 40 % was measured with a four-points bending set-up, so that a large maximal crack depth can be assumed. Thickness difference measurements are described. They reveal that the wafers are thinner near the wire entrance than near its exit. The surface condition at the top of the sawing groove is compared with the one at the wafer surface and reveals that the top of the groove is less rough than the wafers, but made of more sharp angles. Thus, the sawing conditions are different at the top of the groove than at the wafer surface. It is postulated that the coarsest abrasive grains are absent at the top of the groove, whereas they are active at the wafer surface, where they induce large cracks and roughness.

Finally, Raman and TEM measurements are used to characterise the silicon defects near the wafer surface: it was possible to see some dislocations right under the wafer surface and some regions where phase transformation occurred were also found. Furthermore, both

methods revealed that the wafers were highly stressed underneath the surface. It may be due to the observed meta-stable phases: each phase transformation induces volume change, that may not be accommodated by plastic deformation in the silicon bulk, leading to elastic strain in the wafer bulk.

4.1 Scanning electron microscopy

Scanning electron microscopy (SEM) is a powerful tool to analyse the wafer surface at a micrometer scale. Its main advantage over the optical microscope is its great depth of focus, resolution and the range of magnifications available. It allows the analysis of the surface topography of the wafers, but also the measurement of crack depth on wafer cross-sections or indented samples. It is very difficult to quantify the pictures obtained, because the samples can be prone to artefacts (modification of the surface during wafer handling, post-indentation crack growth, etc.) and the analysed area is usually quite small, which raises the question of the analysis representativity.

The wafer surface shows hills and valleys (Fig. 4.1). A striking feature is that the sawing direction (horizontal on the pictures) is not noticeable on the surface. Furthermore, there are only few indents or scratches on the surface and most of the topography seems to result from crack propagation.

The sides of the wafers are difficult to analyse with any other characterisation tool than an SEM, thanks to its deep field of focus. The side where the wire entered and the side where it exited the silicon brick are presented in figure 4.2. On both sides, chips can be seen. The chips on the exit edge are much sharper than on the entry edge. Likewise, the grinding grooves that are clearly seen at the exit side are only visible at the centre of the entrance side. This can be explained by the abrasive particle of the slurry that are projected on the brick side where the wire enters the silicon. These particles are eroding the silicon, thus smoothing the surface features.

Several microscopes were used during this work. Most of the pictures were taken with a Hitachi S-4800 fitted with a field emission gun, but other pictures were taken with a lower resolution tungsten cathode SEM from Zeiss or from Tescan.

4.2 Roughness

The topography observed by SEM can be quantified by profilometry. To do this, a profile of the sample is measured along a line (in the case of samples with a roughness around 1 μm like the wafers, the line measured has to be 5.6 mm long and the roughness is measured on 5 mm

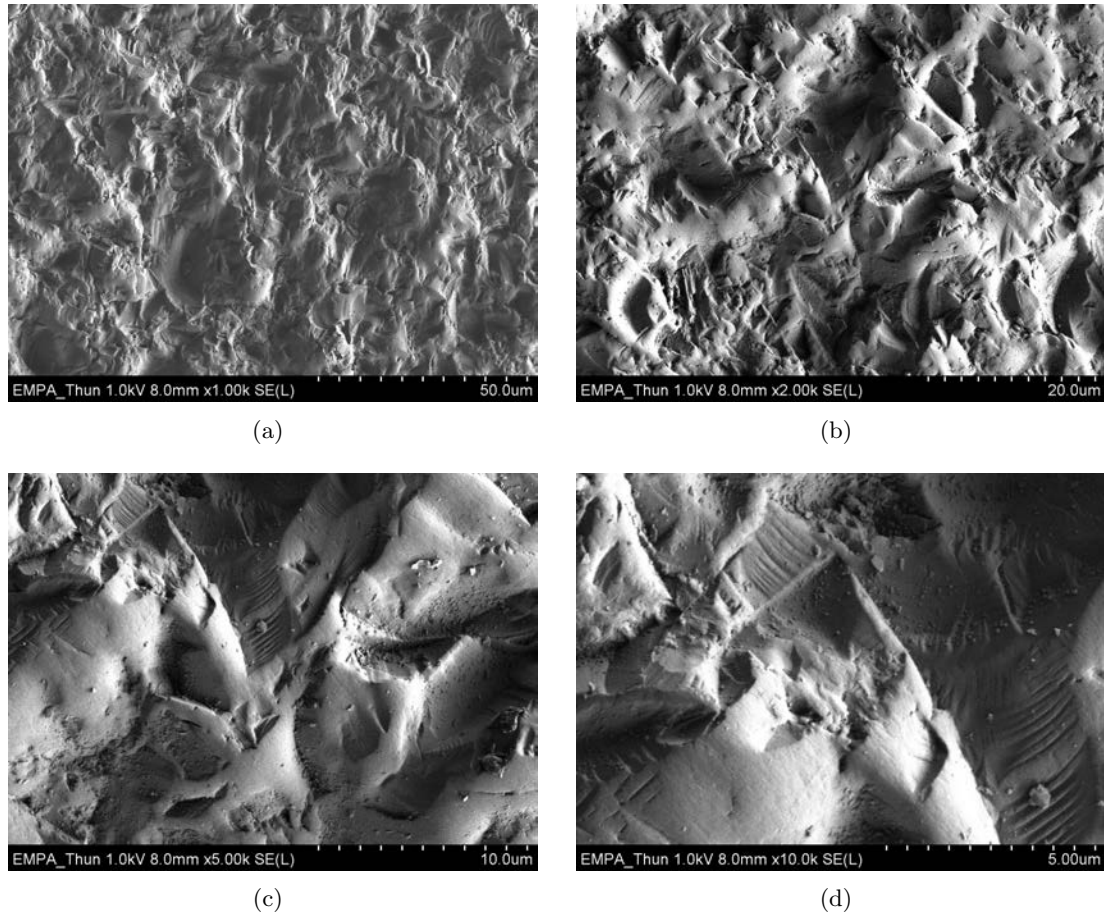


Figure 4.1: SEM picture of a sawn wafer surface: (a) a relatively low magnification, a succession of hills and valleys, can be seen, without a clear indication of the direction of the wire during sawing. This type of surface, with some round hills, but also some sharp edges shows few marks of indentations, and almost no scratches. At a higher magnification (b, c and d), the morphology of cracks having slowly progressed is clearer, but the whole surface is made both of cracks leaving a smooth surface and some leaving a wavy surface. Some short scratches can be seen on the surface, but they are very few. Due to the roughness, it is difficult to see cracks.

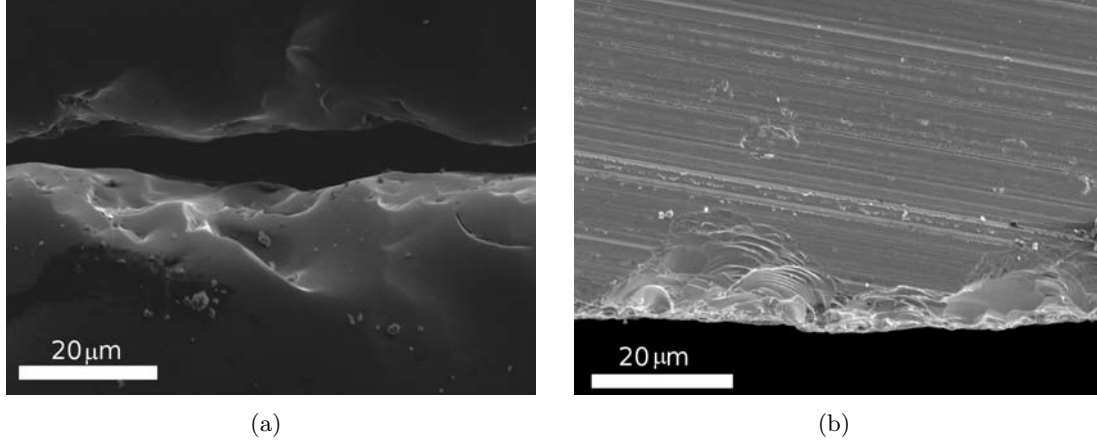


Figure 4.2: SEM pictures of the edges of a wafer: (a) entrance edge of the wire and (b) exit edge of the wafer. The bricks were ground prior to wafering. The grinding grooves can be clearly seen on the exit edge, but were eroded away on the entry edge. Likewise, the chips are much sharply seen on the exit edge, but have been smoothed on the entry edge.

at the centre of the measurement, according to the norm ISO 4287). After the measurement, the profile is levelled to remove the impact of an angle between the measurement plane and the surface. From this profile, a mean height is calculated and the average roughness (R_a) is given by the formula:

$$R_a = \frac{\sum_{i=1}^n |h_i - h_{mean}|}{n} \quad (4.1)$$

where h_i is the height of point i , h_{mean} is the mean height of the profile and n is the total number of points taken during the measurement (Fig. 4.3). For this calculation, a high-pass filter with a cut-off length of 0.8 mm is used to remove the long-distance height change (i.e. the waviness). The average roughness gives a value of the global roughness on the sample, but it is not enough to provide a clear understanding of the topography. The total roughness: $R_t = h_{max} - h_{min}$ where h_{max} is the highest point and h_{min} is the lowest point of the profile, gives an indication of the magnitude of height difference on the profile, and by comparing it to the average roughness, it can give an indication of whether the surface is mainly flat with just a few spikes or if the roughness is homogeneous⁶⁴. It is also important to note that the value of the roughness parameters depend on the measurement length and on the measurement resolution.

The roughness is a macroscopic measurement, but it is still local if the whole wafer surface is considered. As the sawing process is quite slow and because it should be stable through

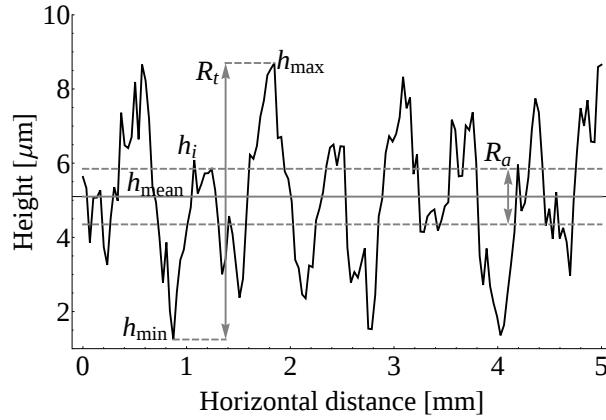


Figure 4.3: Schematic view of a profile and the different values that can be extracted from it: the height on point i (h_i), the mean surface height (h_{mean}), the average roughness (R_a), the highest point of the profile (h_{max}), the lowest point of the profile (h_{min}) and the maximal roughness (R_t).

time, the roughness at the start of a cut should be the same as the roughness at the end of the cut. This is without taking into account the wear of the slurry, and the possible effect of silicon debris. For a cut that has been sawn without problem, the roughness is indeed the same throughout the cut. In the other direction (i.e. between the entrance and the exit of the wire), the roughness evolves, as shown in figure 4.4. For a standard cut, the average roughness at the wire entrance is around $1\text{ }\mu\text{m}$ and progressively decreases to $0.45\text{ }\mu\text{m}$ during the first half of the wafer length. After this point, the roughness is stable until the exit.

To characterise the wafers, roughness has been measured on 5.6 mm long profiles oriented at 90° from the wire direction during the cut. For the wafers analysed at the beginning of this work, within the framework of an industrial project, the roughness was measured at 9 places: near each corner, near the middle of the edges and in the centre of the wafer (Fig. 4.5(a)). For the wafers analysed after that, the roughness measurement was more thorough: the profiles were situated 40 mm away from the glued edge of the wafers (Fig. 4.5(b)), one measurement was taken every 5 mm and five wafers were measured for each sawing condition.

4.3 Crack depth

Cracks are, as shown in section 2.1, responsible for the wafer breakage. Thus, it is important to know their size and the crack depth distribution inside a wafer. One method to measure them is to polish a cross-section of a sample with a small angle (around $3\text{--}5^\circ$) between the wafer surface and the polished face, so that the lateral dimension stays the same as the real

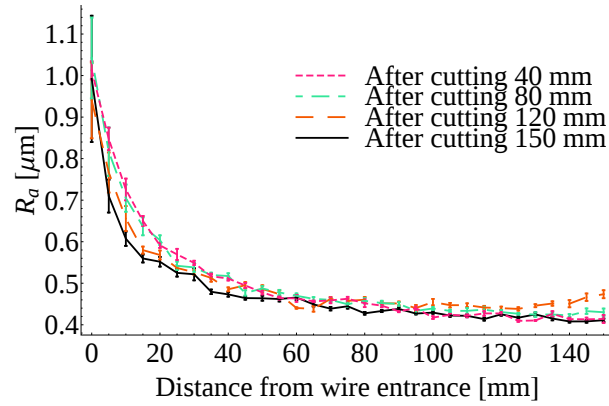


Figure 4.4: Evolution of the roughness on a wafer. The roughness is much larger near the entrance of the wire into the ingot than near the exit. In contrast, it stays the same between the beginning of the cut and its end (the black line represents the roughness at the end of the cut, the orange after cutting 120 mm, the turquoise after 80 mm, the fuchsia after 40 mm).

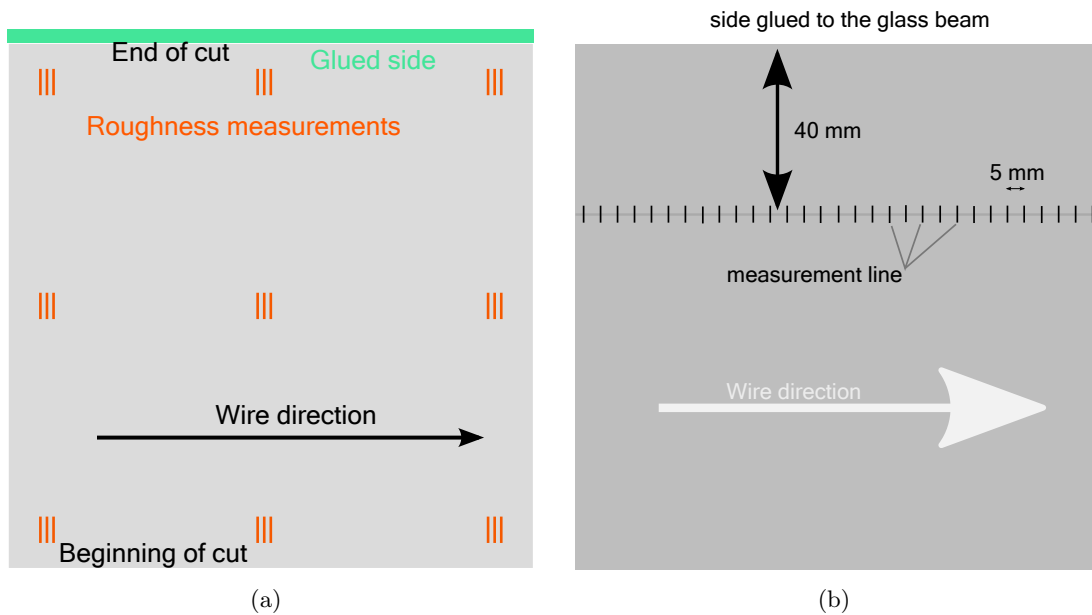


Figure 4.5: a) Roughness measurement positions for the first test campaign, where the roughness was measured at nine places. At each place, three measurements were made, and their results were then averaged. For each sawing condition, three wafers were measured. b) Measurement positions for the second campaign. For each sawing condition, five wafers were measured. The measurement length is 5.6 mm and the distance between measurements is 5 mm.

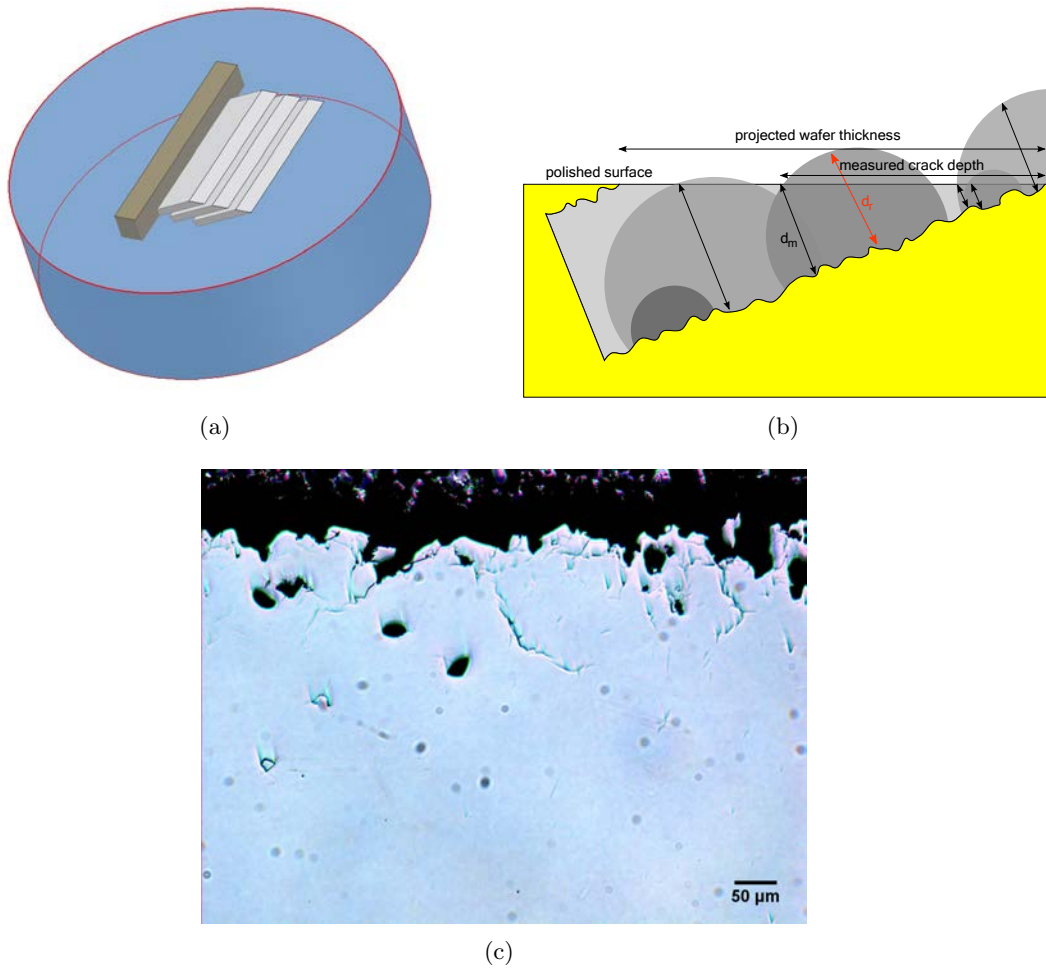


Figure 4.6: a) Three dimensional view of the sample used to measure the crack depth distribution. Silicon probes are embedded in resin at a small angle from the polished surface. b) Schematic cross-section of a sample used for determining the crack depth distribution. The sample is polished from the top before observation. Original wafer surface is seen at the bottom as well as on the right of the figure, near the polished surface. Cracks at different positions have been superposed to show different scenarios of crack measurement. It is possible that a deep crack is measured as shallow (as the one on the right of the sample). The measured depth (d_m) is smaller than the real depth (d_r) of the cracks. c) Micrograph used for measuring the (projected) crack depth. The scale is only valid on the horizontal axis as the projected crack depth is much larger than the real crack depth.

dimension on the wafer, but the depth into the wafer is magnified (Fig. 4.6). Using this method, the crack depth can be precisely measured with an optical microscope (as the crack depth is magnified). Thus, an important area can be measured (as taking micrographs with an optical microscope is fast and its field of view is large), giving a reliable crack depth distribution. To obtain a reliable statistic, a length of 3 mm was measured (giving 500–800 crack depths), but even though this statistic is good enough to give a crack depth distribution, it does not give the depth of the deepest crack in the wafer (the wafer is much larger than the sampled area). This distribution can be fitted with an exponential distribution formula (as presented in figure 4.7):

$$p(d) = Ae^{-\lambda d} \quad (4.2)$$

where $p(d)$ is the probability to have a crack at depth d , A is a pre-exponential factor that can be related to the crack density and λ is the characteristic crack depth. This parameter can be used to quantify the crack depth, allowing a comparison of the results.

As for the roughness, the crack depth of a given wafer is not the same everywhere: near the entry of the wire, the cracks are deeper than near the exit (Fig. 4.7). But the direction along which the cracks are measured is not playing a role: more cracks are measured perpendicularly to the wire direction than parallel to it, but the characteristic crack depth is the same.

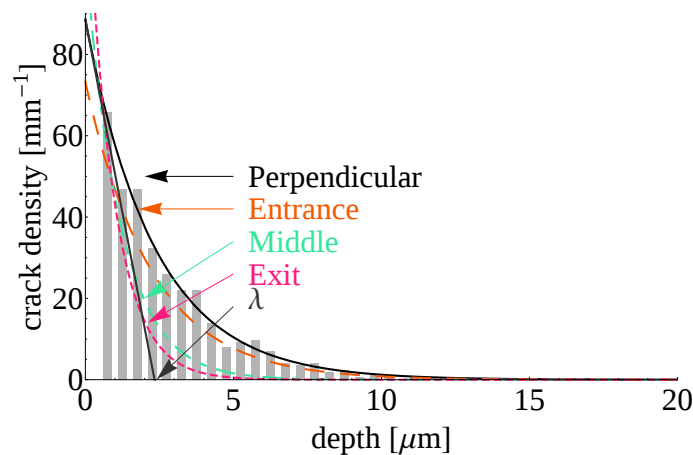


Figure 4.7: Crack depth distribution in a wafer. The bars show the measured depth and the curve is the fitted distribution. The characteristic crack depth is the decreasing rate of the distribution, which can be represented as the slope of the curve $p(x)$ at $x = 0$: $p'(0)$ in equ. (4.2).

4.4 Mechanical testing

In contrast to the crack depth distribution or the roughness, the breakage stress depends on the critical crack present in the wafer area under maximal stress. The geometry and size of this maximal stress area depends on the test used. Two families of tests exist: three or four lines bending tests that load the centre of the wafer as well as two of the edges, or bi-axial bending tests that only load the centre of the wafer (see Fig. 4.8). A third type of test exists: the twist test, where the wafer is twisted by its four edges¹¹¹. But as this test does not provide a constant stress along the edges, its interpretation is difficult and it was not used in this study. In the two other test families, one test is loading a smaller area than the other (e.g. the three lines test, where the maximal stress is under the central line versus the four lines test, where the maximal stress is in between the two central lines). The stress field of the bi-axial tests is more complicated than that of the lines tests, as the stress is important in two different directions at a given point and is not homogeneous inside the central ring (although this depends on the diameter of the inner ring and on the wafer thickness³⁹).

The wafer fracture happens when the stress intensity factor of one crack exceeds the fracture toughness of silicon. As it was shown in section 2.1, this depends not only on the applied stress, but also on the geometry of the crack and loading conditions. From the crack depth distributions, it was seen that there is not only one crack depth, but a distribution. Thus, the deepest crack depth (the crack that propagates and breaks the wafer during the bending test) varies from one wafer to another. In consequence, the measured breakage stress is described not only by one mean value, but by a distribution of breakage stress. This distribution is well described by the Weibull probability distribution given by¹²¹:

$$P(\sigma) = \frac{m}{\sigma_0^m} \sigma^{m-1} e^{-(\sigma/\sigma_0)^m} \quad (4.3)$$

where m represents the distribution width (named the Weibull modulus) and σ_0 is the characteristic stress, at which 63.2 % of the samples are broken. With a four-points bending tests, standard wafers are breaking at loads ranging from 100 to 200 MPa (see figure 4.9, it depends on the type of wafer — mono- or multi-crystalline and on the sawing quality). This breakage stress can in turn be related to a half-penny crack radius: figure 4.10 shows the critical (bending) stress in respect to the crack size calculated according to equation (2.10). It shows that if the stronger wafers presented in Fig. 4.9, breaking at a stress of 180 MPa, do not have cracks deeper than around 20 μm , the weakest wafers have (breaking at a stress of 120 MPa) cracks as deep as 40 μm . When the wafer is broken, it shatters in many pieces, so that it is very difficult to find the crack at the origin of the failure. Actually, it seems that the wafers break

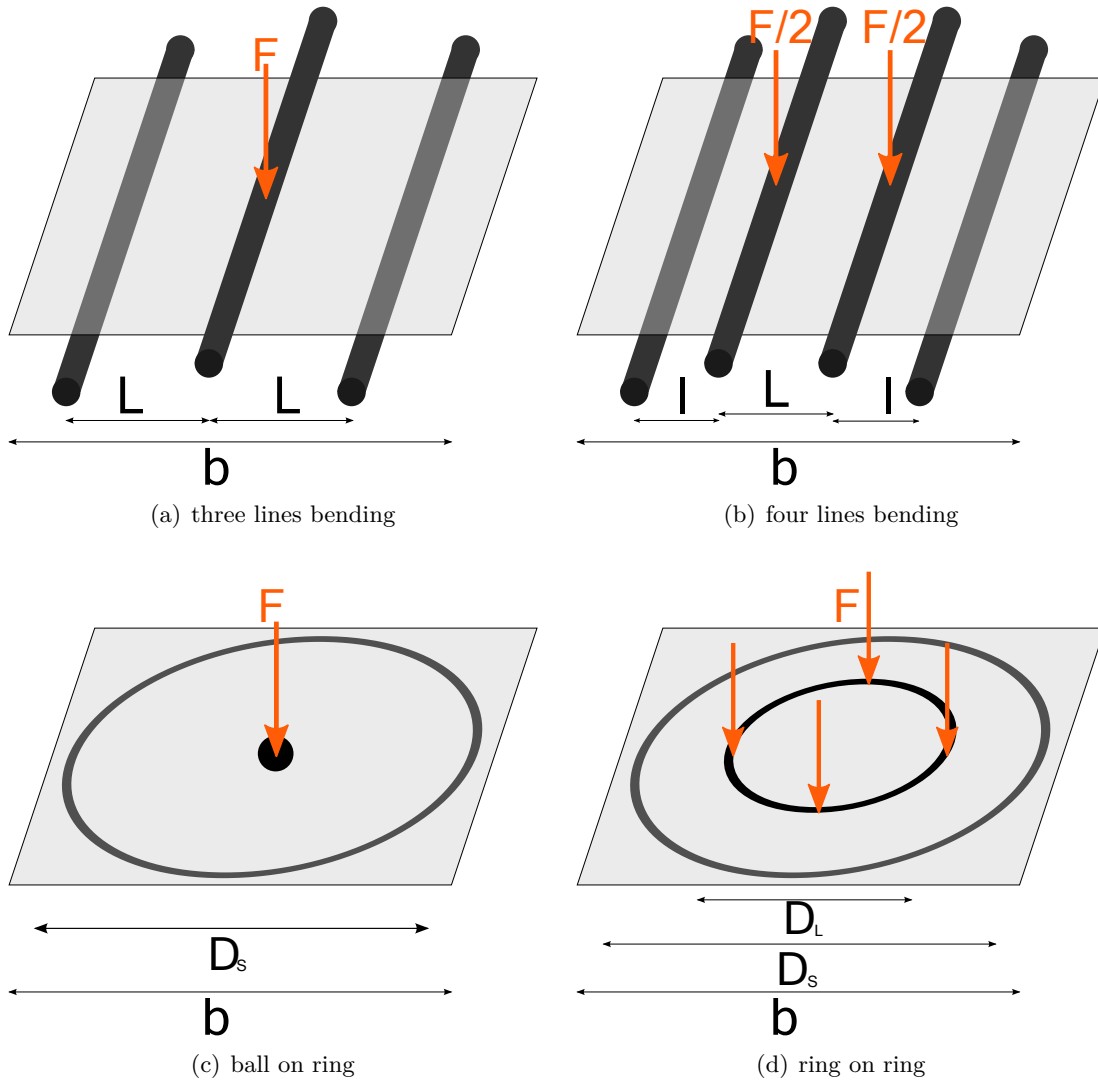


Figure 4.8: Wafer bending tests. The wafers are breaking in the highest stress area, under the middle beam for the three lines test or under the ball for the ball-on-ring test. For the four lines test, the stress is highest between the two centre beams and for the ring-on-ring test, the highest stress is under the centre ring.

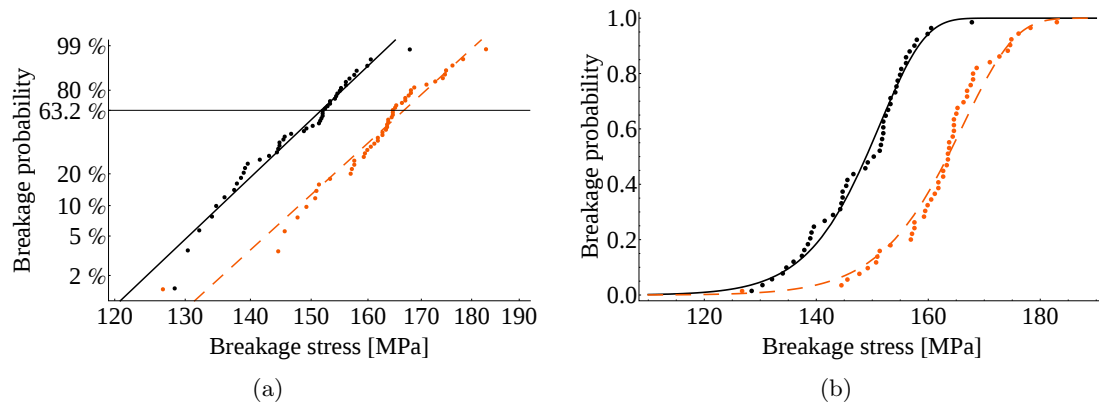


Figure 4.9: Weibull plots of a batch of wafers tested with a four-points bending test. Both plots come from the same data, and only the scales are different: (a) is the traditional Weibull plot with non-linear axes and (b) is its transformation into linear axes. The wafers were tested in the same direction as the wire during sawing (black curve) and perpendicular to it (orange curve).

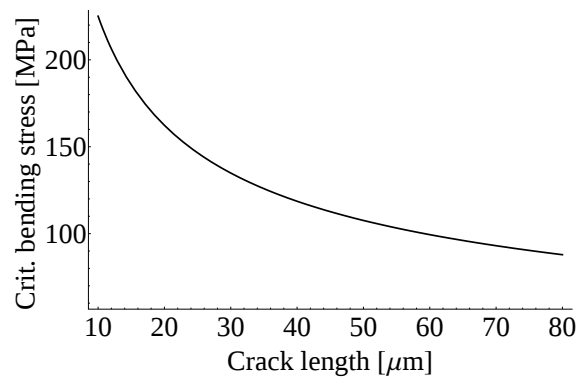


Figure 4.10: Breakage stress for a 200 μm thick wafer in pure bending. It is assumed that the crack is semi-circular. As this geometry of crack first propagates at the surface (Fig. 2.4(b)) the stress intensity factor was calculated at this position with equation (2.10) and with $K_{I,c}$ for $\{110\}$ planes.

in the same fashion as dry spaghetti⁵: the elastic energy stored in the bent sample is suddenly released, inducing a stronger bending of the remaining sample that leads to the propagation of other cracks, until the spaghetti is broken in many pieces. To observe the wafer breakage, a high-speed camera was used. A mirror was put under the wafer support to see the breakage from under the wafer (Fig. 4.11). Figure 4.12 shows the breakage of a wafer during a 4-lines bending test. It can be seen that the fracture starts at the edge (on the second frame), and that fracture lines propagate at 45° from the support lines and are spaced at roughly regular intervals, creating small rectangular pieces of silicon. The crack propagation in itself is very fast, as it requires less than one frame (0.05 ms) to break the wafer.

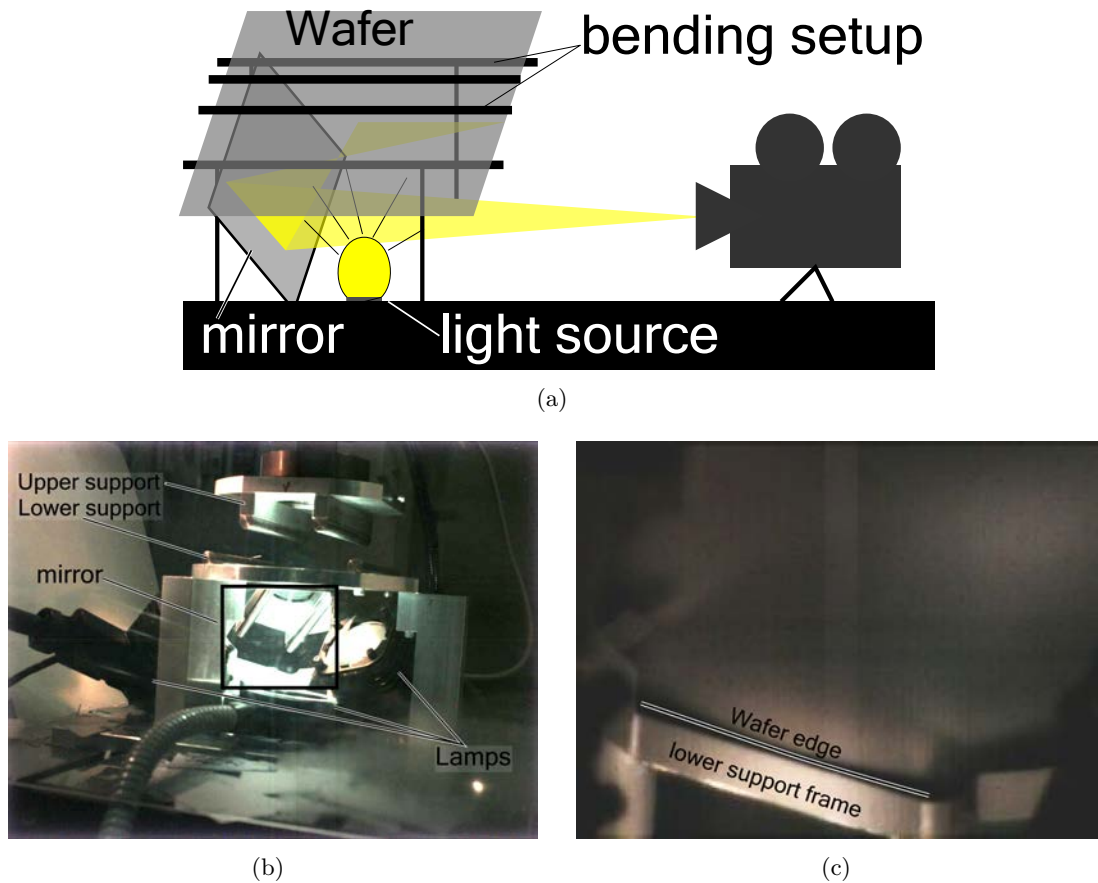


Figure 4.11: a) schematic view of the set-up: the camera is standing at the side, looking at a mirror reflecting the bottom of the wafer from an axis parallel to the bending lines. b) and c): pictures of the four lines bending test from the camera: b) the whole set-up without wafer and c) the area used for the high speed film. This image comes from the bottom of the wafer, reflected by the mirror visible in b). On the small image, the wafer edge and the support frame have been highlighted.

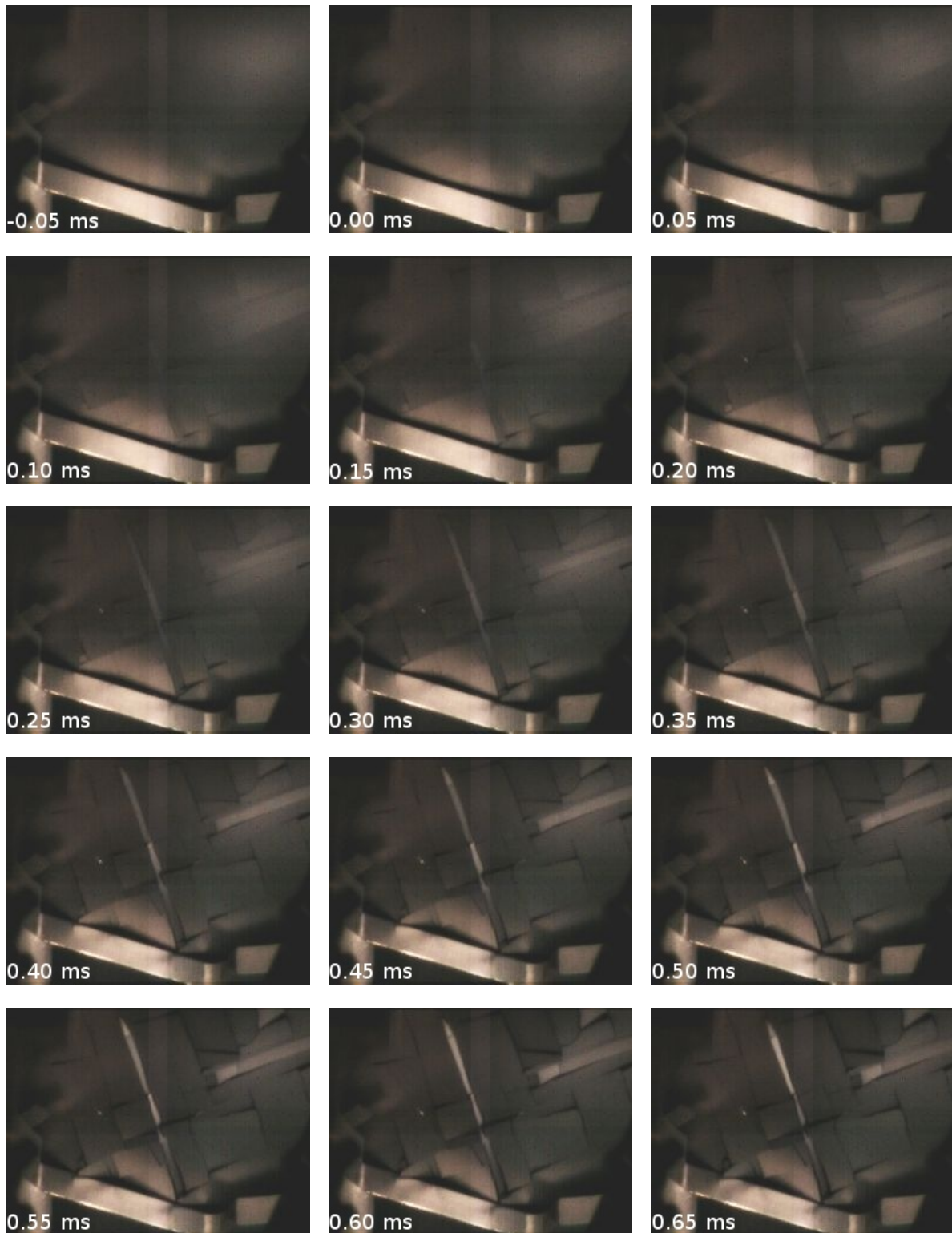


Figure 4.12: Sequence of pictures showing the breakage of a wafer during a 4-lines bending test. The frame rate is 20000 frames per second. The wafer breaks at the second frame (at 0 ms).

Nonetheless, it is possible to analyse the cross-section of the broken parts to measure the crack depth (Fig. 4.13(a)). As the wafer broke at the critical crack, measuring this depth on a batch of wafers does not give a representative value of the crack depth distribution as the one measured in section 4.3, but an idea of the deepest crack depth. It does not give the absolute crack depth either, as it would require finding the crack at the origin of the first failure and as it is pictured in figure 4.12, many cracks propagate after the first crack propagation, meaning that smaller cracks than the first one also propagate. This value of the maximal crack depth, contrary to the previous one (section 4.3), can be compared to the value given by the breakage test (with the help of the equations developed by Raju and Newman¹⁰⁵, equation (2.10)) to validate the measurement.

The four lines breakage test does not only load the surface of the wafers, but also the edges. Thus, it is possible that the breakage comes either from one or the other type of these locations (e.g. the wafer pictured in Fig. 4.12 first breaks at the edge). Again, this has to be put into perspective with the solar cell production, as the applied stress in production might not be the same as the one of the four lines test (e.g. a much larger force might be applied on the edges than on the wafer centre during the wafer manipulation). One note of caution,

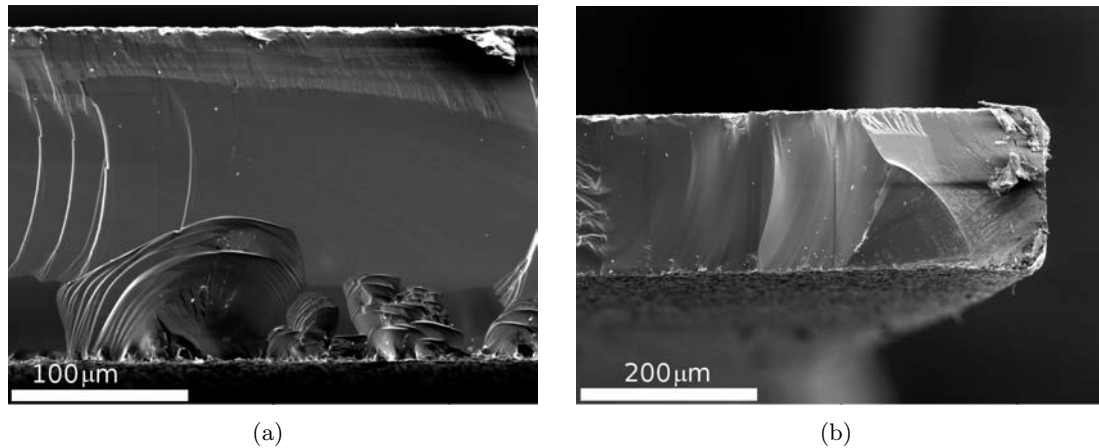


Figure 4.13: (a) SEM micrograph of a multi-crystalline wafer cross-section showing cracks. This cross-section was obtained from a bending test. The deepest crack on the picture is $82\text{ }\mu\text{m}$ deep and even if the crack is almost half the depth of the wafer, the breakage does not come from it, as it can be seen from the breakage front marks left and right of the crack. The half-penny shape of the crack is characteristic of all cracks found in a sawed wafer. Furthermore, as the dislocations in TEM lamellae (Fig. 4.25(a)), the crack origin cannot be related to a deep indent on the wafer surface. (b) SEM micrograph of a multi-crystalline wafer cross-section showing the wire entrance edge. The sample is the same as (a). No deep crack can be seen in this picture — which does not mean that there are no cracks at all on this edge.

though: these values were measured for bricks that were ground prior to being cut into wafers. The shaping process (bricketing or squaring) that comes before this grinding step induces deep cracks on what becomes the edge of the wafers. Without the grinding step, the wafers may be more brittle and the measured defect depth would have been the one of the edge defects, not the depth of the defects coming from the wafering.

It should be noted that the breakage stress does not depend notably on the wafer thickness, unless the cracks have a depth comparable to it¹⁰⁵. But the force and the bending needed to attain this stress depend on it. Thus, for a given maximal crack depth, a 100 μm thick wafer breaks at the same stress as a 200 μm thick wafer. But the force needed to attain this stress decreases with the thickness, contrary to the bending that increases when the wafer is thinner. This is also important to take into account for a transposition of the results to the subsequent process of thinner wafers, as they get stronger if the processes are deformation dependant or weaker if they are force dependant¹¹⁰.

In this work, two types of tests have been carried out: ring-on-ring tests and 4-lines bending tests. For the ring-on-ring tests, sheets of carbon paper were put between the rings and the samples to improve sliding. The rings had a diameter of 120 mm and 50 mm and the speed of one ring towards the other was 1 mm/min. When possible (depending on the amount of wafers available) 50 wafers were broken for each sawing condition. For the 4-lines tests, the lines were spaced at 100 mm and 50 mm intervals. The test speed was 30 mm/min. A faster speed was used for the 4-lines bending stress than for the ring-on-ring test because the bending at failure is more important for the 4-lines test. To avoid measuring the edge defects, both edges loaded during the test were were ground down to a 4000 grit. By doing so, around 500 μm of silicon were removed on each edge. A PTFE film was glued on the four lines to improve sliding. Approximately 35 wafers were broken for each sawing condition (depending on the amount of wafers available).

4.4.1 Computation of the breakage stress

The values measured during a breakage test are the displacement of one support relative to the other and the applied force. These values do not allow the comparison of wafer with a different thickness, nor the calculation of crack depth. Thus, the stress applied at the wafer surface has to be calculated. As the wafers are thin and wide, the analytic solutions are *a priori* not valid as they require the displacement to be lower than the sample thickness. Thus, finite element simulations of the tests have been made with Abaqus to determine the stress field and its amplitude for all the wafer thicknesses encountered during this study. The mesh consisted of 8-node linear brick (type C3D8) elements, with an area of $1 \times 1 \text{ mm}^2$ in the wafer plane and a height of one quarter of the total wafer thickness. The supports were set as solid

rigid elements. After making sure that the silicon anisotropy and the crystal orientation have a negligible influence on the results, the silicon was chosen as isotropic, its silicon Young's modulus was set to 163 GPa and the Poisson ratio to 0.28.

For the ring-on-ring test, the highest stress is found under the inner ring (Fig. 4.14(a)). In contrast, when the deformation is small, the highest stress is found to be homogeneous inside the inner ring. On the FE simulation, it is seen that the wafer centre is homogeneously deformed (Fig. 4.14(b)) and that the stress there is small. Furthermore, the stress under the inner ring is not constant, but presents peaks of higher stress. It is believed that these peaks are artefacts due to the mesh: when nodes are exactly under the contact point of the ring on the wafer, the stress is highest, and when the contact lies between the points, the stress is lower. Despite this inaccuracy, the FE model fits well with the experimental data in terms of force–displacement curve (Fig. 4.15(a)). This provides the confidence needed to use the simulations for extracting the breakage stress from the tests. As a comparison, a plot of the stress in respect to the position on a radial line starting from the centre of the rings is shown in figure 4.15(b) for a radius going through a maximum and through a minimum as pictured respectively by the grey and black lines in figure 4.14(a). The stress used as the breakage stress is the maximal principal stress found by the simulations.

In order to compute the breakage stress for all the broken wafers, simulations have been run for wafer thicknesses between 145 and 290 μm with an interval of 10 μm , except between 145 and 150 μm and between 200 and 210 μm where the thickness interval was 5 μm . The applied load varied between 0 and 50 to 150 N (depending on the wafer thickness) with 100 points between the minimal and maximal values. All these data were then fitted to a polynomial function of the thickness and the force giving the applied stress. This function has the form:

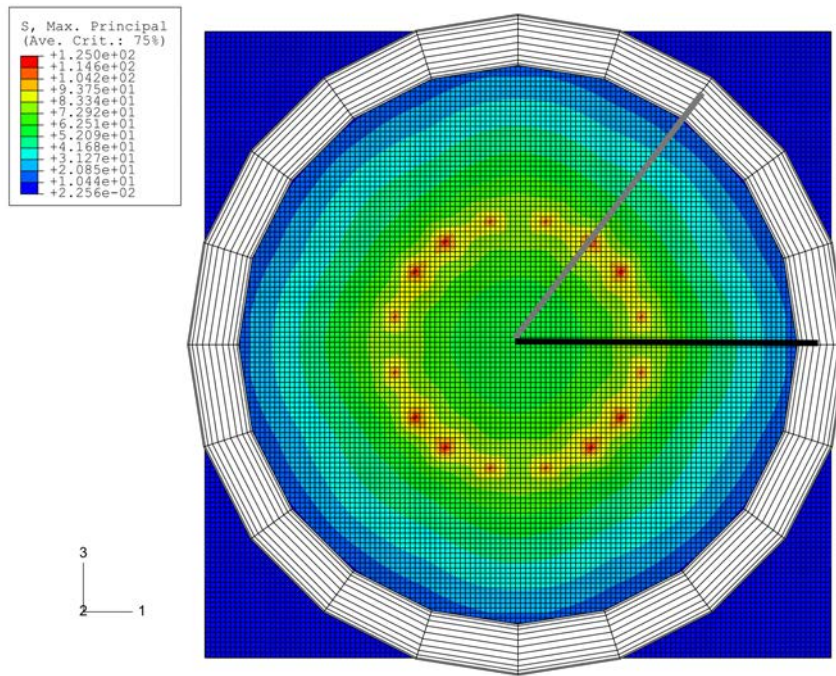
$$\sigma(t, F) = \delta_1 t + \delta_2 t^2 + \delta_3 F^{1/3} + \delta_4 t F^{1/3} + \delta_5 F^{1/2} + \delta_6 t F^{1/2} + \delta_7 F + \delta_8 t F + \delta_9 t^2 F \quad (4.4)$$

where t is the wafer thickness, F is the applied force and δ_i are constants to be fitted. The values of the constants are given in the Table 4.1.

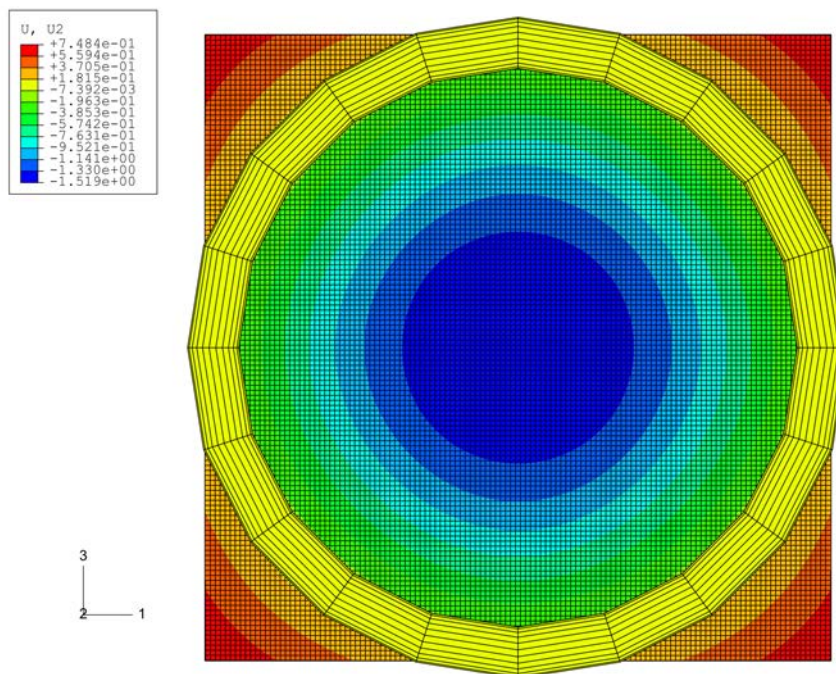
Because the wafers are not circular, the stress is not homogeneous under the inner ring (making abstraction of the local maxima): the stress on the diagonals is larger than the stress

Table 4.1: Constant values for equation (4.4). These constants were obtained by fitting the equation to results from finite element calculations.

δ_1	δ_2	δ_3	δ_4	δ_5	δ_6	δ_7	δ_8	δ_9
-36.07	295.8	-1.614	-150.0	24.74	40.3	1.509	-10.77	17.19



(a)



(b)

Figure 4.14: (a) Stress in a 200 μm thick wafer simulated by the finite element method. (b) Displacement of the wafer.

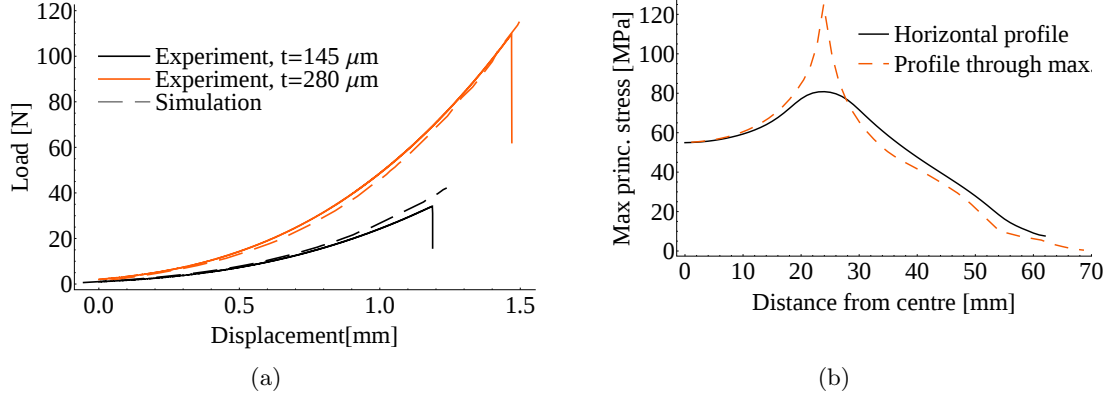


Figure 4.15: (a) Force-displacement plot of a 145 μm and a 280 μm thick wafer during a ring-on-ring test as measured experimentally and as calculated with the model. (b) Maximal stress on the lower wafer surface along a radius passing through a local maximum under the inner ring (grey line in Fig. 4.14(a)) and passing through a local minimum (black line in Fig. 4.14(a)) for a 200 μm thick wafer. The difference is assumed to come from the mesh too coarse to model the wafer-ring contact well.

on the radii parallel to the wafer sides, implying that the stress field does not have a circular symmetry and that some crack orientations are more stressed than others. Assuming that cracks are laying on (111) planes, the tension and shear on this plane can be calculated for the two locations (on a diagonal and on a radius parallel to the wafer side) for two wafer orientations: the [110] direction parallel to the wafer side and parallel to the diagonal. It turns out that on the diagonal, the maximal principal stress is oriented parallel to the ring radius so that cracks oriented perpendicularly to this direction are the first to propagate. In comparison, wafers with cracks parallel to their side seem stronger because the stress field is not oriented as detrimentally on the wafer diagonals. These wafers have cracks that are oriented perpendicularly to a principal stress where that stress is lower (i.e. on a radius parallel to the wafer side). For a 200 μm thick wafer, the wafers with cracks parallel to the diagonals are subject to a stress 1.25 times larger than cracks oriented parallel to the wafer sides.

In contrast, the four-lines bending test has a stress field essentially uniaxial, perpendicular to the support lines. This stress is almost homogeneous between the two inner lines (Fig. 4.16(a)) and the stress computed with the finite elements simulation is close to the stress calculated by the analytical formula (Fig. 4.16(b), for a 205 μm thick wafer). In consequence, the analytical formula has been used to compute the breakage stress from the experimental data.

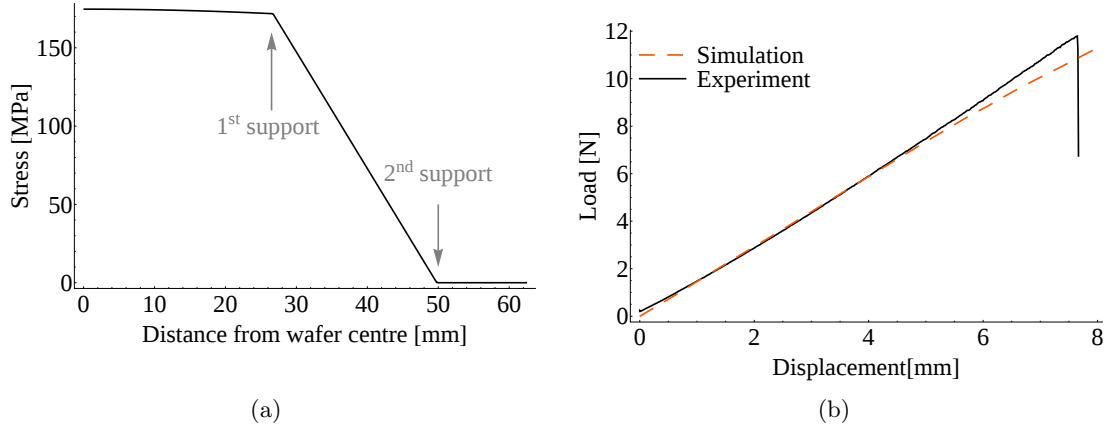


Figure 4.16: (a) Stress profile between the wafer centre and its edge during a 4-lines bending test. The area between the wafer centre and the first support can be taken as under homogeneous stress. (b) Load-displacement curve from experimental data and from the simulation. Both curves match closely enough to assume the analytical solution is valid.

4.5 Thickness differences

Wafer thickness difference can cause trouble during the downstream cell processes. The firing procedure of screen-printed cells depends strongly on the wafer thickness: if the wafer is thinner, it requires a shorter firing time than if it is thicker. Thus, it is important to have wafers with similar thicknesses, but also that the thickness variation in individual wafers is as small as possible. The definition of thickness is not evident, as the wafers are rough: when a total roughness greater than $5\text{ }\mu\text{m}$ can be measured on a 5 mm long profile, the precision of the thickness measurement cannot be better than that, i.e. at least a 3% measurement error can be expected. Also, the size of the measurement probe plays a role in the results: a punctual probe would give higher measurement variations than a larger probe.

Despite of the wafers being cut by parallel wires, each wafer shows thickness differences both in the wire direction and in the table direction. In the table direction, this can be caused by changes in the sawing parameters at the start or at the end of the cut, or by thermal effects (the silicon expands due to the heat produced by the sawing and the slurry viscosity changes with the temperature). The thermal effects are clearly visible when a cut is paused before its end, as shown in figure 4.17. One possible explanation is that during the time the saw is stopped, the silicon and the slurry cool down and when the saw is started again, the silicon is colder than prior to the interruption and the slurry more viscous. This makes a saw mark on every wafer at the position of the stop.

In the wire direction, the thickness difference can be caused by the wire vibrations (as

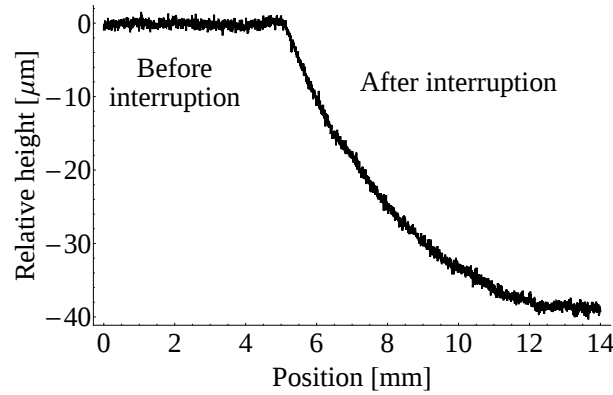


Figure 4.17: Wafer height profile across a saw-mark due to interrupting the cut. The region before the stop is on the left. The interruption was long enough to let the ingot cool down completely.

described by Zhu *et al*¹²⁹) or by a change of kerf loss between the entrance and the exit of the wire inside the silicon, for example due to a change in the particle size distribution between the entrance and the exit of the wire inside the silicon³.

The wafers are the thinnest at the wire entrance (Fig. 4.18). They quickly get thicker at first, but this rate decreases as the distance from the wire entry increases, until the last few 5–10 mm before the wire exit where the wafers get thinner again. This last decrease is due to the wire vibrations outside the silicon. It can be presumed that the vibrations have the same effect at the wire entrance, but the thickness change due to vibrations is hidden by the change caused by particle size change. As the geometry of the saw has an importance on the vibration, the effect of vibrations changes with the situation in the wire-saw (one or two bricks next to each other between the wire-guides, only one brick in the centre of the wire-guides, or on one side and also the position of the slurry nozzles, etc.) as the length of wire free to vibrate defines the amplitude of the vibrations.

There is also a thickness difference from one wafer to the other. One obvious reason for this would be that the wire-guide grooves are not regularly spaced, but this has only a marginal effect. Generally, a thick-thin sequence of wafers is observed. This can be caused by surface tension of the slurry, if the slurry film is not regularly poured on the wires. When this happens, thick-thin pairs of wafers can be found, where one wafer is thinner than the target thickness and the one next to it is thicker.

The wafer thickness was measured by a mechanical sensor. For each sawing condition, 10 wafers were measured. The thickness was measured each centimetre on two lines parallel to the wire direction, one after 1/3 of the cut and the other after 2/3 of the cut.

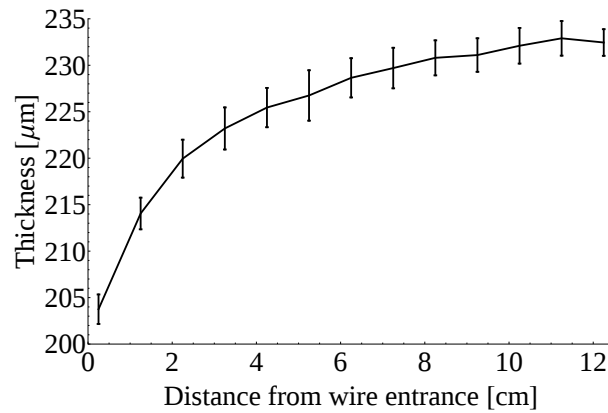


Figure 4.18: Wafer thickness for a wafer sawn with F600 grit. The wafers are thinner at the wire entrance, then get thicker until close to the wire exit, where the wafer gets thinner again. The error bars show the standard deviation of this measurement, made twice on ten wafers from the same cut.

4.6 Top of the sawing groove

The area where most of the silicon is worn is right over the wires, at the top of the sawing groove (the silicon blocks are lowered through the wire web during the sawing, thus, in the course of sawing, the silicon that has not been cut is over the wire, while the wafers are hanging below, Fig. 4.19). For this reason, what happens at the top of the groove is likely to have

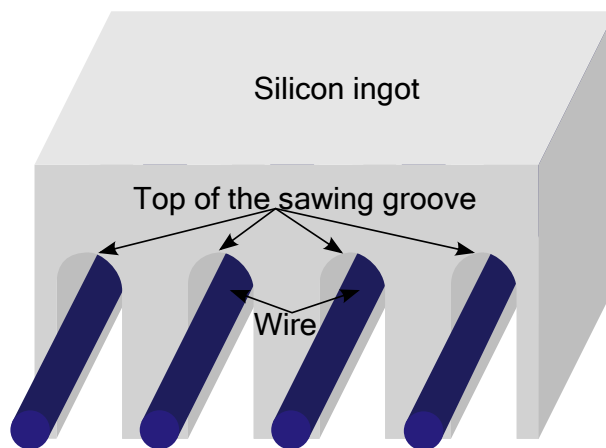


Figure 4.19: Schematic view of an ingot being sawn. The wires are making grooves inside the silicon, which separate the wafers at the end of the cut. As the ingot is pushed from the top, the silicon that is not sawn yet is over the wire web. The top of the sawing grooves is indicated.

an impact on the whole sawing process, and consequently on the cracks present in the wafers after the cut. By studying the surface morphology, insight into the sawing process can be gained, and by comparing it to the morphology of the wafer surface, a better understanding can be acquired. To study the top of the sawing groove, a cut has to be interrupted quickly to preserve the silicon topography created during the stable sawing. Artefacts might be created during the time when the wire is slowed down, but as the sawing speed is quite slow, they should not have too much impact on the surface. Figure 4.20(a) presents an SEM picture of the top of the groove. By comparing it to the wafer surfaces that were already cut when the cut was interrupted (Fig. 4.20(b)), it can be seen that the roughness on the groove has a lower length-scale and presents more facets than on the wafers.

From this analysis, it appears that the force per particle is smaller at the top of the groove than at the wafer surface. This is explained by a difference in particle size distribution between the two locations: at the top of the groove, the wire is exerting a large global pressure, the consequence of which is to eject the largest particles towards the groove sides (i.e. the wafer surface). There, the global pressure is small, as the silicon removal rate is low (the wire essentially moves parallel to the groove side), but a strong local force can occur when several particles are present at the same place. More information on this subject can be found in a previously published article¹².

The sawing groove roughness was measured in the same way as the wafer surface. But the samples had to be prepared prior to the measurement: first, the wafer parts that were already

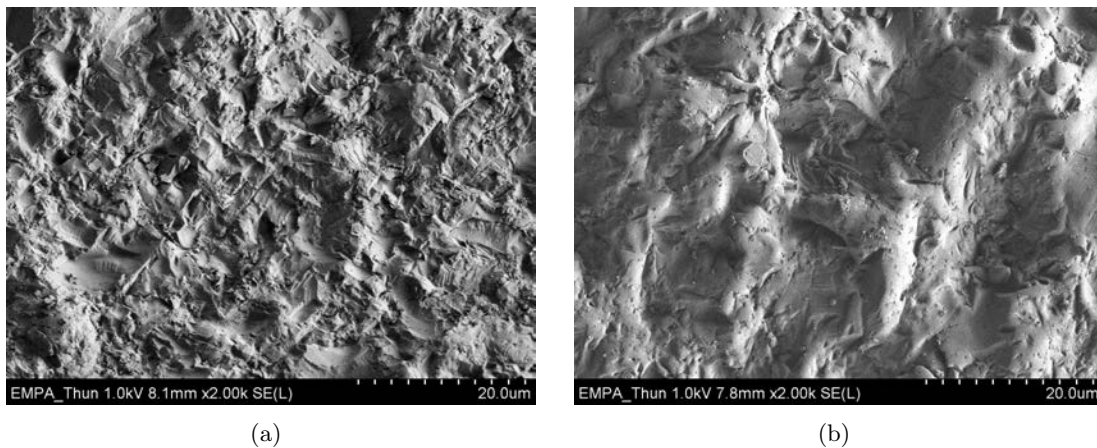


Figure 4.20: (a) SEM micrograph of the top of a sawing groove and (b) of the wafer that was already cut when the cut was interrupted. By comparing the two micrographs, it can be seen that the roughness on the wafer has a larger length-scale, and that the hills and valleys are rounder than on the groove. On both surfaces, the direction of the sawing cannot be clearly identified.

sawn were broken off. Then, the sample was cut into four pieces (approximately 30 mm long, the brick length being 125 mm). Each piece was measured 5 mm away from both sawn sides so that the eight measurement positions (that are equally spaced on the groove length) give a global overview of the roughness inside the groove. At each position, four measurements were made to have a representative value. As for the wafer surface, the measurement length was 5.6 mm.

4.7 Raman spectroscopy

Experiments on silicon indentation showed that phase transformations occurred under the tip (subsection 2.3.2). If the tip is sharp, the hydrostatic pressure under the tip increases quickly, so that only a small load is needed to create these phase transformations. It was seen on the SEM pictures (Fig. 4.1) that imprints of some indents were visible on the wafer surface and all the wear models presented in Chapter 2 imply that a particle of abrasive hits the silicon surface to remove material. Thus, some amount of amorphous silicon (or possibly small meta-stable silicon crystals) should be seen on the wafer surface. Raman spectroscopy is able to measure such phase transformation. The different silicon phases and the position of their major peaks are given in Table 4.2.

The wafer surface is mostly made of crystalline silicon. Nevertheless, a small amount of amorphous silicon can be seen on some regions, as it can be seen on figure 4.21.

Furthermore, some stress inside the crystalline silicon could be measured by analysing the peak shifting from its stress-free position. Indeed, a compressive stress shifts the peak towards a higher wavenumber and a tensile stress shifts the peak towards a lower wavenumber, both with a sensibility around 434–500 MPa/cm⁻¹ for a uniaxial stress^{29,30,119}. For a plane stress

Table 4.2: *Position of the Raman peaks of the different meta-stable phases of silicon. The reported values come from Ge et al⁴⁵.*

Phase	Space Group	Pressure region [GPa]	Peak position [cm ⁻¹]
Si-I	Fd3m (227)	0–12.5	520
nc Si-I	Fd3m (227)	0–12.5	505–510
Si-II	$I4_1/amd$ (141)	8.8–16	?
Si-III	$Ia\bar{3}$ (206)	2.1–0	166, 382, 433
Si-IV	$P6_3mc$ (186)	...	508
Si-XII	$R\bar{3}$ (148)	12–2	350, 394
Si-XI	$Imma$	13–18 (?)	?
a-Si	—	4–4.5	$\approx 470, \approx 150$

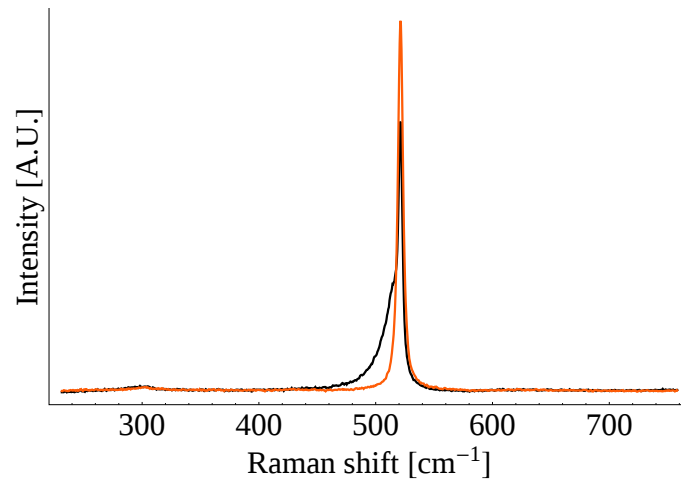


Figure 4.21: Raman spectra of a region with a larger than average amount of amorphous silicon (recognised by the broadening of the peak at lower wavenumber) and of a region without much amorphous silicon.

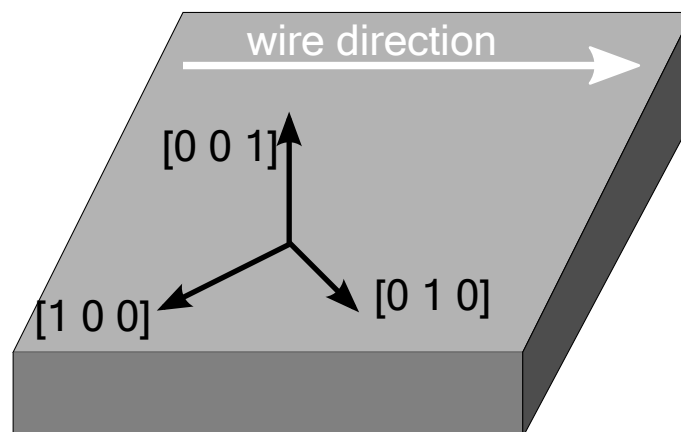


Figure 4.22: Crystallographic orientations on a wafer. The wafer surface was $\{001\}$ and the wire direction was $[110]$.

in the $\{001\}$ plane, the Raman shift is given by the equation²⁹:

$$\Delta\omega[\text{cm}^{-1}] = -4 \cdot 10^{-9} \left(\frac{\sigma_{11} + \sigma_{22}}{2} \right) [\text{Pa}] \quad (4.5)$$

where $\Delta\omega$ is the Raman shift, σ_{11} and σ_{22} are stress in the $[100]$ (defined as x_1) and $[010]$ (defined as x_2) directions (Fig. 4.22). The map of the stress at the wafer surface is shown in figure 4.23. It can be seen that some areas are strongly stressed, but most of the area is without much stress. The average stress at the surface is 100 MPa and the standard deviation is 220 MPa. So that if the surface stress can be taken as null on average, there are still large stress differences from one point to the other.

The spectrometer used in this work is a Dilor XY800 with a laser wavelength of 514 nm. An artefact that may occur with Raman spectroscopy is that the laser beam hitting the sample heats the silicon enough to cause a recrystallisation of the amorphous silicon into nano-crystals. Thus, filters are needed to lower the beam power and keep the silicon in its original state. This implies that to conserve an acceptable signal over noise ratio, the measuring time has to be increased. Hence, Raman spectra were taken with a laser beam power around 90 mW and a spectra was given by the sum of three 30 second long acquisitions. For maps, the laser power was 270 mW and the acquisition time was 2 seconds. For both types of measurement, the laser spot had a diameter of 1 μm .

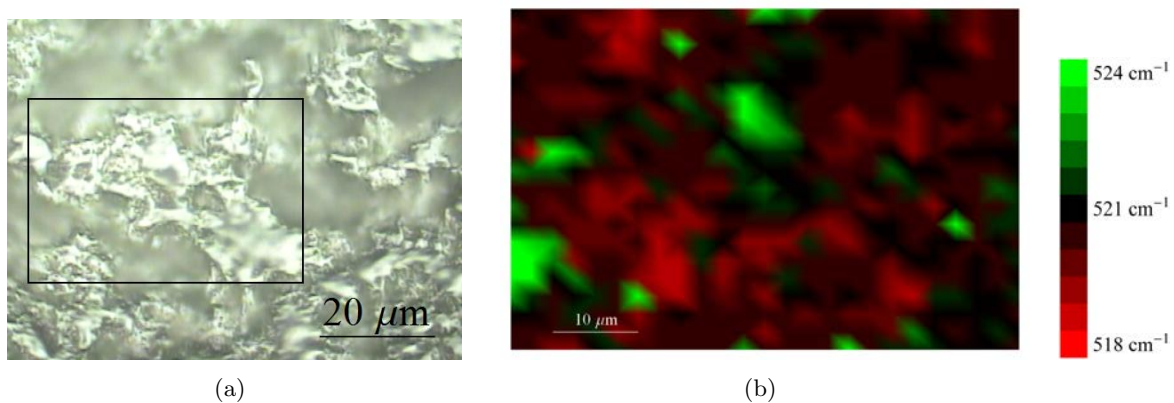


Figure 4.23: a) Optical micrograph of the analysed wafer. The area measured is shown by a rectangle. b) Raman map of the stress on a slurry sawn wafer. Green indicates tensile stress and red indicates compressive stress.

4.8 Transmission electron microscopy

Transmission electron microscope (TEM) lamellae of wafer cross-sections have been made by focused ion beam (FIB). The high resolution available with a TEM allows the observation of dislocations and small-scale phase transformation down to the sub-nanometre level. As it could be seen from the previous measurements, cracks are present under the surface (Fig. 4.24). It appears that dislocations are also present, but are constrained close to the wafer surface (Fig. 4.25(a)). It is interesting to note that these dislocations are found in small, densely packed arrays. They are only 1–2 μm deep. A closer look at these dislocation arrays shows that they are loops of dislocations (Fig. 4.25(b)). As expected, these dislocations greatly deform the crystal, but they cannot be accounted for a large deformation, as they are only confined to a small region below the surface. Furthermore, they cannot be related to a definite imprint on the surface.

The TEM measurements also show that the lamella is stressed. This is linked to the Raman measurements showing stress at the wafer surface. It can be explained by the presence of dislocations and by the small amount of amorphous silicon that was measured by Raman spectroscopy. The fact that no phase transformation is observed by TEM can be imputed to the small area observed. Indeed, Raman measurements have only measured amorphous silicon on some regions of the sample, and the TEM lamella is extremely small ($\approx 10\text{ }\mu\text{m}$ long) compared to the region observed by Raman spectroscopy.

From these TEM observations, the wear mechanism that leads to the wafers is hard to determine. On the one hand, the surface looks like it has been worn by indents, and cracks as well as some arrays of dislocations are observable, but on the other hand, proof of local high pressure that should come with indents (amorphous or meta-stable silicon phases, see section 2.3) is barely seen. Finally, the wafers have important elastic stress, but — apart from the dislocations near the surface — no plastic deformation. Cracks are created, but the process responsible for them is not clear.

4.9 Chapter summary

As the studied wafers are destined for solar cell production, it is important to know which characteristics are important, and which are secondary. From the characterisation methods described previously, it is seen that there are overall thickness differences between wafers from the same cut, and that these wafers have a varying thickness, a rough surface, and cracks below their surface making them fragile. The silicon under the surface is stressed and dislocations can be seen in arrays just below the surface, but almost no phase transformation

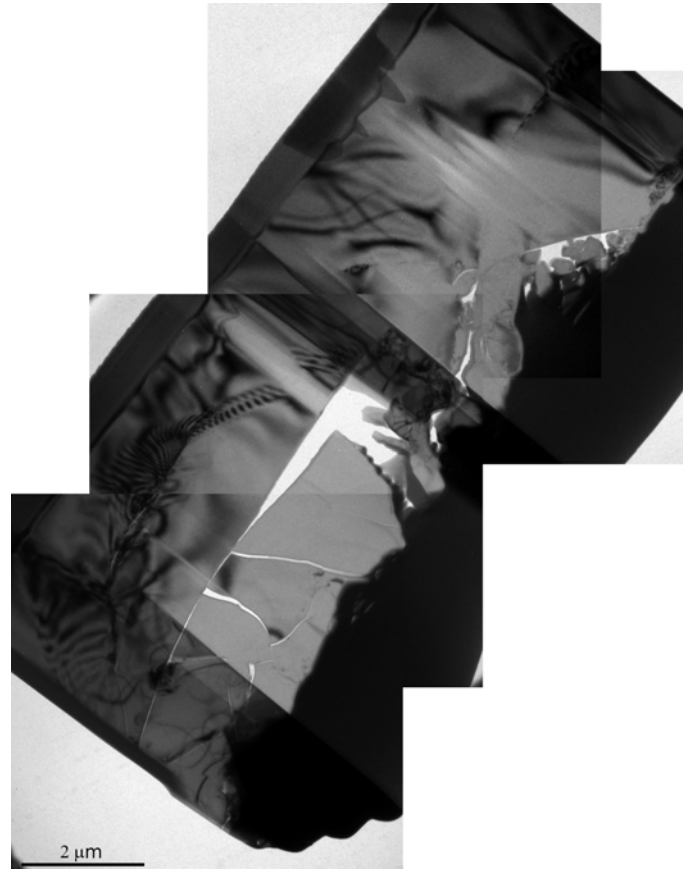
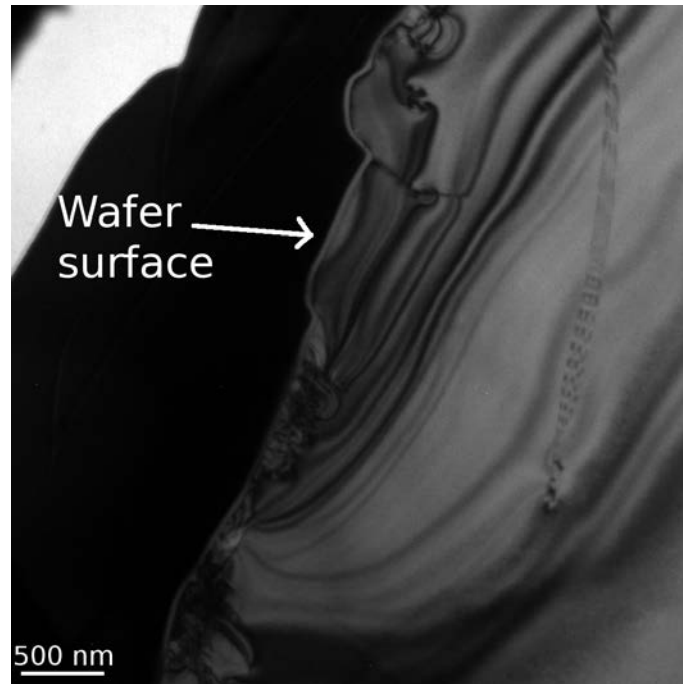


Figure 4.24: TEM images of the cross-section of a wafer. (a) A general view of the lamella: in black the platinum layer used to protect the sample surface, in grey the silicon with several parts broken near the surface and large elastic deformation under it. Beside that, the surface does not show traces of dislocations or phase transformation.

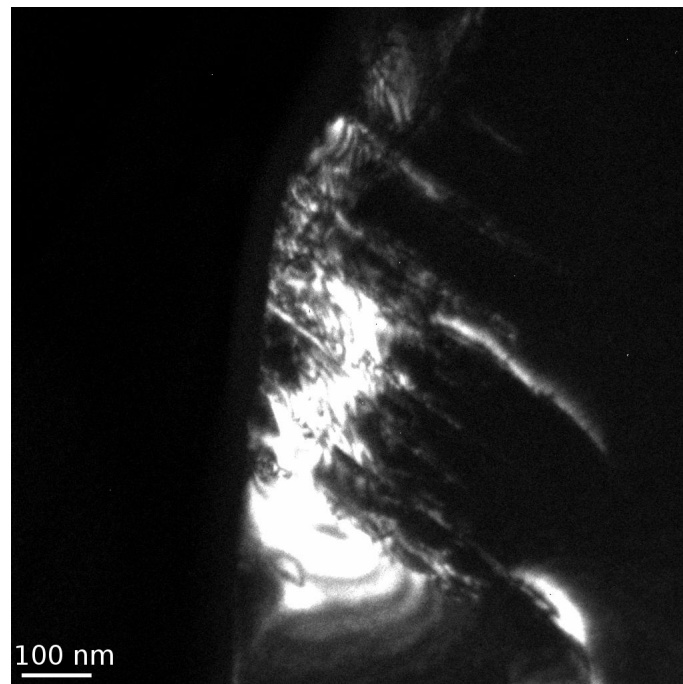
was observed.

The contact firing taking place in the screen printed cell production is very sensitive to the wafer thickness. Therefore, the overall thickness and — more importantly — the total thickness variation (TTV) are very important. If the wafer is too thin compared to the average wafer thickness, the wafer heats up faster and the contacts diffuse too deeply, thus shunting the cell. If the cell is too thick, the contacts will not diffuse deeply enough and the cell will have a too high series resistance. Both situations decrease the efficiency.

The average roughness as described in the section 4.2, on the contrary, is not important for cell production. In contrast, the saw marks, which can be represented as large height difference on the wafer surface on a millimetre scale, have an impact. They cannot be completely evened out during the saw-damage removal and texturisation etching step, and this large topography is



(a)



(b)

Figure 4.25: (b) Another wafer sample similar to Fig. 4.24, at higher magnification. The dark part is the platinum layer used to protect the sample surface during milling. Under it, the silicon is heavily deformed (elastically). The deepest defect that can be seen is a crack. Some array of dislocations can be observed close to the surface. They are only $1\text{--}2\text{ }\mu\text{m}$ deep and just on some small parts of the surface. A very thin layer of amorphous silicon can be seen at the interface between the silicon and the platinum, but seems to be an artefact coming from the protective layer deposition. (c) a dark-field image of an array of dislocations. The dislocations are mostly oriented in the same, well-defined direction and are densely packed.

harmful for the screen printing. It is likely that the masks used for printing the contacts cannot conform to the topography when the saw marks are too high, leading to finger interruptions or too large fingers.

It is obvious that the wafer strength is of prime importance for the breakage rate in the cell production. This is not really important for the processing of thick wafers, but increases in importance as the industry heads towards thinner wafers. The wafers gained much in strength by having their edges and corners ground¹¹⁸. This process removes the cracks introduced by the squaring / bricketing step before the wafering. As a comparison, the microelectronic industry grinds and rounds all corners of the wafers they use for the same reason, but this step is not made before the wafering but after it, so that they can cut the angles between the wafer surface and its edge as well to strengthen the wafers even more (by also removing the damage made by the wafering step at the entrance and exit of the ingot).

In the next chapter, the characterisation methods presented above are used to assess the quality of wafers sawn with different parameters. From these wafers, a model describing the crack depth from the sawing parameters is developed. This model is inspired from the models presented in the previous chapter and on the defects creation mechanisms presented in Chapter 2.

Chapter 5

Parametric study and modelling

The best way to understand the effect of the different sawing parameters on the wafer quality is to test them. By varying several parameters, their effects (and the interactions between these parameters) can be measured with the methods described in Chapter 4. Two sawing campaigns were carried out: a first one consisting of 19 cuts investigated the importance of the abrasive particle distribution, the slurry density, the wire tension and the feed rate on the wafer quality. The second campaign of 29 cuts was made to refine the analysis by changing the same parameters with less amplitude. The first campaign was completed in 2006 and the second in 2009. During these three years, the state of the art evolved dramatically: the wire and the wafers became thinner, the saw capacity increased and the abrasive size routinely used in the industry got finer. Consequently, the results from the two campaigns have to be compared with caution.

In this chapter, the effect of changing the wire tension, the feed rate, the abrasive size and the slurry density is measured. The variation range of each parameter is given in Table 5.1 for both test campaigns. From these results, a novel model determining the wafer strength is developed. This model allows the determination of the characteristic breakage stress and the Weibull modulus. It is found that each sawing parameter influences the effect of the others and that a low slurry density, a low wire tension and a low feed rate increase the wafer strength.

Table 5.1: *Parameters variation range of the two test campaigns.*

	First campaign	Second campaign
SiC median size [μm]	3–22.8	6.5–9.3
Slurry density [kg/l]	1.440–1.774	1.569–1.677
Feed rate [m/s]	173–727	378–450
Wire tension [MPa]	1086–1898	1377–1949

5.1 First test campaign

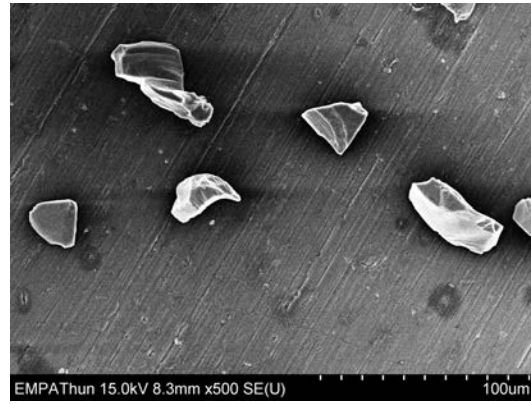
5.1.1 Sawing conditions

The first test campaign was carried out on a wire-saw that was originally designed for the microelectronics industry (an HCT E500ED-8 wire-saw). The wire diameter and the pitch were 160 and 445 μm respectively. The wire speed was 11.5 m/s. The slurry was made of HS20 (from Applied Materials) lubricant and silicon carbide from ESK. The slurry flow was fixed at 50 kg/min. As the slurry dispenser is 500 mm long, the flow is 0.1 kg/(min·mm). The silicon was mono-crystalline (100), pseudo-square $125 \times 125 \text{ mm}^2$ bricks around 20 mm long, giving approximately 40 wafers per cut. The [011] orientation on the wafers was parallel to the wire direction, so that wafers cleave in a direction parallel and perpendicular to the wire direction. It can be noted that this orientation is said to be not optimal⁸ (see section 2.5). The parameters that were changed are the grit size, the slurry density, the wire tension and the table speed, as described in Table 5.2. They were changed according to an equiradial plan, allowing to change as many parameters as possible in a limited number of cuts, but to still check cross-interactions of the tested parameters. It was planned to change the parameters as much as possible to better measure their influence. The SiC median size (d_{50}) corresponds to standard distribution F360 (22.8 μm), F400 (17.7 μm), F500 (12.8 μm), F800 (6.5 μm) and F1200 (3 μm). They were analysed by SEM to have a better idea of their shape. Figure 5.1 shows SEM pictures of particles from all grit sizes.

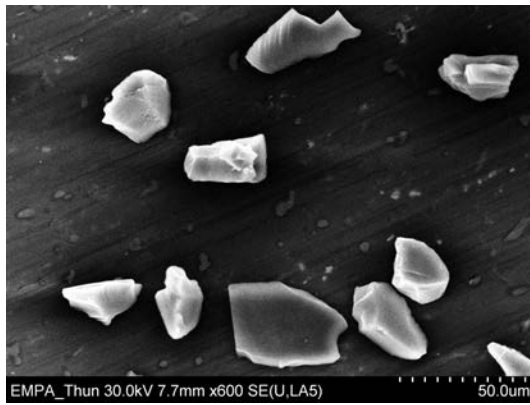
5.1.2 Results

One of the cuts planned in Table 5.2 failed in producing wafers: all the wafers sawn with the sawing parameters E broke before the end of the cut. In comparison, the cut F, that used the same parameters except the abrasive size, also produced many broken wafers. This is explained by too high a slurry density. As the slurry is poured on the wires in front of the brick, it is accelerated and hits the silicon with a speed comparable to the wire speed. It is possible, when the slurry is too dense, that this force is too large in respect to the wafer strength, inducing wafer breakage. In the case of the F800 slurry, the wafers are stronger and sustain this impact better, which explains why not all the wafers were broken.

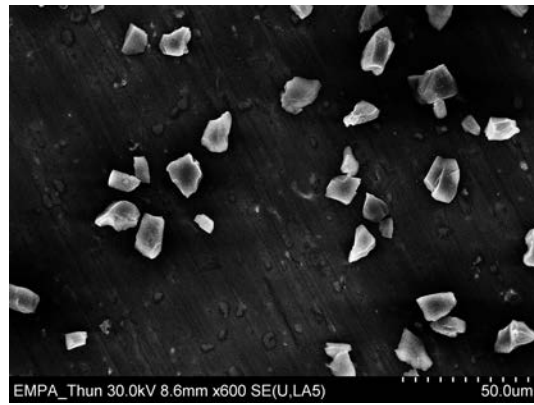
The wafer strength is shown in figure 5.2. The wafers were broken with a ring-on-ring set-up. Around 30 wafers were broken for each sawing condition. The wafers can be separated in three groups corresponding to the different grit sizes. The coarsest grit size (F360, $d_{50} = 22.8 \text{ }\mu\text{m}$) produces the most fragile wafers. It can also be noted that the wafers cut with the finest abrasive (F1200, $d_{50} = 3 \text{ }\mu\text{m}$) are not the strongest: some of these wafers are very strong but other are really weak. Thus, if the stress at which the first wafers break is taken



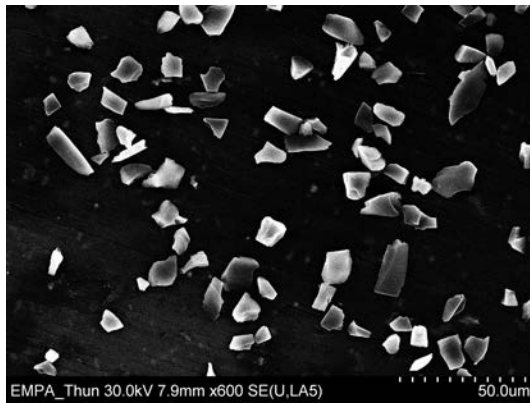
(a) F360



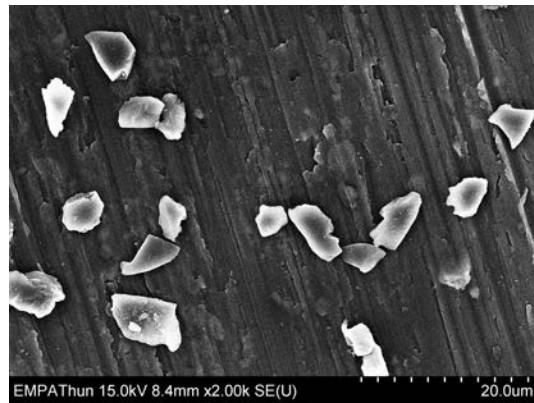
(b) F400



(c) F500



(d) F800



(e) F1200

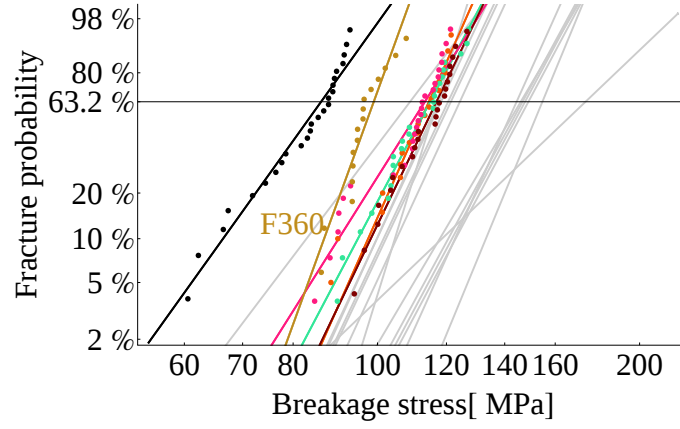
Figure 5.1: SEM micrographs of the SiC abrasives used for the sawing campaigns. The scale changes for the different abrasive sizes. The median abrasive sizes (d_{50}) are $22.8\ \mu\text{m}$ for F360, $17.7\ \mu\text{m}$ for F400, $12.8\ \mu\text{m}$ for F500, $6.5\ \mu\text{m}$ for F800 and $3\ \mu\text{m}$ for F1200.

Table 5.2: *First campaign sawing parameters. The cuts are given in their chronological order. The parameter sets were chosen by using a equiradial plan.*

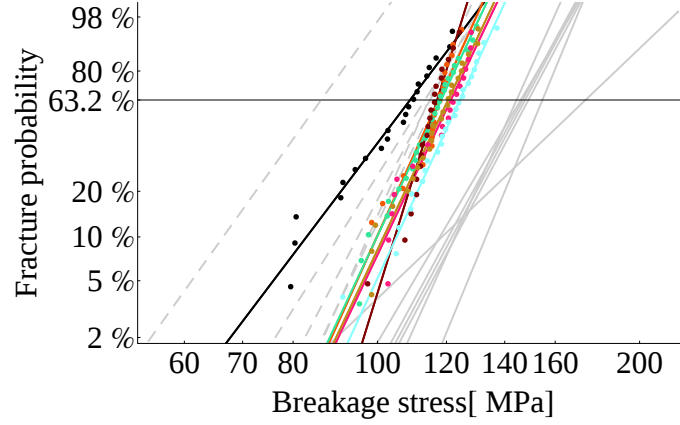
Name	d_{50} SiC [μm]	Slurry density [kg/l]	Wire tension [N]	Feed rate [$\mu\text{m}/\text{min}$]
M	12.8	1.727	21.84	450.00
T	12.8	1.727	27.96	173.29
A	12.8	1.624	30.00	450.00
R	12.8	1.624	23.88	726.71
U	12.8	1.624	36.12	173.29
K	12.8	1.506	38.17	450.00
Q	12.8	1.506	32.04	726.71
C	22.8	1.624	30.00	450.00
E	17.3	1.774	30.00	450.00
I	17.3	1.677	38.17	450.00
O	17.3	1.677	32.04	726.71
L	17.3	1.567	21.84	450.00
S	17.3	1.567	27.96	173.29
G	17.3	1.440	30.00	450.00
F	6.5	1.774	30.00	450.00
J	6.5	1.677	38.17	450.00
P	6.5	1.677	32.04	726.71
H	6.5	1.567	21.84	450.00
N	6.5	1.567	27.96	173.29
D	6.5	1.440	30.00	450.00
B	3.0	1.624	30.00	450.00

into account (and as solar cell production is looking for a very low breakage rate, this is the parameter that matters), the wafers cut with F800 are stronger than those cut with F1200. It can also be noticed that there is comparatively less difference between the wafers cut with F400 and F500 than between wafers cut with F500 and F800. However, apart from the wafers cut with F1200, it is clear that wafers cut with a smaller abrasive are stronger than wafers cut with a coarser abrasive.

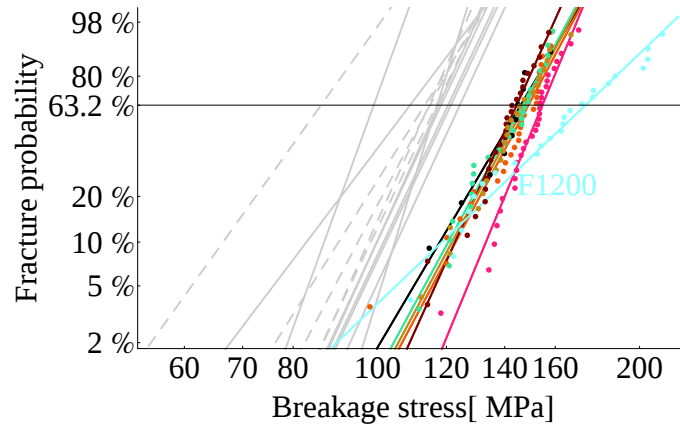
Roughness measurements show the same trend as the strength measurements: the wafers cut with coarse abrasive are rougher than the wafers cut with a fine abrasive. The large difference between wafers cut with F800 and F500 is again observable (Table 5.3). These results can be compared with the crack depth distribution. If the crack depth distribution of each wafer batch is plotted in ascending order and the wafer roughness is put on the same graph, it can be seen that both measurements correlate (Fig. 5.3). Thus, the roughness can be taken as a good indication of the cracks created in the wafers. This situation changes when the stress at rupture is compared with the previous results (Fig. 5.3): trends can be



(a) In colour: F400 and F360, In grey: F500, F400 and F360



(b) In colour: F500, In dashed grey: F800 and F1200, in solid grey: F400 and F360.



(c) In color: F800 and F1200, In dashed grey: F800 and F1200, in solid grey: F500

Figure 5.2: Weibull plots of the first campaign wafers (measured with a ring-on-ring set-up). Each grit size is presented in colour, the grey lines in the background are the other batches for comparison. For the F400 the strongest wafers are sawn with the parameters G and the weakest with the parameters I. For the F500, the strongest wafers are sawn with the parameters T and the weakest are sawn with the parameters M. For the F800 the strongest wafers are sawn with the parameters H and the weakest with the parameters F (see Table 5.2).

seen, for instance the wafers sawn with F800 are stronger than the wafers sawn with a coarser abrasive and are also less rough, but no clear correlation appear for wafers sawn with the same abrasive size. The roughness (or crack depth distribution) only gives a general idea of the wafer strength. It is not as precise as the bending test, because this type of measurement is based on a statistical description of the wafers, by just measuring a fraction of the total wafer and extracting an average roughness or a crack depth distribution valid for that area, which is taken as representative of the whole wafer. In contrast, the bending tests stress a much wider wafer area and are only sensitive to the largest crack present. This crack is by definition not possible to measure by optical microscopy or by looking at the surface roughness.

Despite that, the correlation between roughness and crack depth distribution is an indication that the sawing process can be described in the same fashion as the lapping of glass, and that the model developed by Buijs and Korpel-van Houten^{19,20} can give a hint about the most important parameters determining the wafer strength. Indeed, this model demonstrated that the particle size (and shape) was the most important parameter. This is also valid for

Table 5.3: *Roughness and breakage strength parameters of the wafers cut during the first campaign. The breakage strength parameters were obtained by ring-on-ring bending.*

	Grit size	R_a [μm]	R_t [μm]	R_{sk}	R_{ku}	σ_0 [MPa]	m	$\bar{R}^2$
M	12.8	1.12	17.0	2.37	-0.180	85.5	8.79	0.97
T	12.8	1.21	18.8	2.57	0.124	91.6	14.6	0.89
A	12.8	0.996	11.0	2.71	-0.458	92.4	14.1	0.98
R	12.8	0.908	11.2	2.34	-0.675	94.7	13.9	0.92
U	12.8	1.13	14.1	3.22	-0.366	91.4	21.4	0.92
K	12.8	0.833	9.48	2.31	-0.746	94.2	14.0	0.97
Q	12.8	0.794	9.11	2.16	-0.711	97.2	14.3	0.99
C	22.8	1.71	20.5	9.60	-0.337	76.9	18.6	0.90
I	17.3	1.43	20.2	3.52	-0.406	86.1	8.68	0.96
O	17.3	1.34	19.0	3.03	-0.345	89.4	14.9	0.97
L	17.3	1.26	14.5	3.32	-0.398	89.6	12.6	0.98
S	17.3	1.40	15.5	3.70	-0.252	88.2	10.6	0.91
G	17.3	1.09	12.8	2.69	-0.550	91.0	13.8	0.97
F	6.5	0.577	8.04	1.27	0.099	114	11.2	0.94
J	6.5	0.510	6.73	1.14	-0.012	117	12.1	0.94
P	6.5	0.448	5.72	1.32	0.053	115	11.8	0.97
H	6.5	0.438	5.32	0.933	-0.095	121	15.6	0.96
N	6.5	0.472	5.59	1.07	0.082	113	14.3	0.96
D	6.5	0.387	4.71	0.944	-0.384	115	12.1	0.98
B	3.0	0.310	3.41	1.11	0.358	136	6.03	0.97

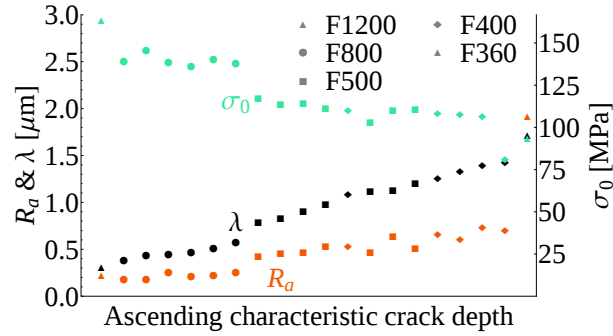


Figure 5.3: Average roughness (R_a) of all cuts in ascending order. For each cut, the Characteristic crack depth (λ) near the wire entrance and the characteristic stress (σ_0) are also plotted. It can be seen that the crack depth and the average roughness are correlated, but the correlation with the wafer strength is much poorer. Thus, the roughness and crack depth distribution only give a first impression of the wafer quality.

wire-sawing (Fig. 5.2). But the lapping model also pointed out that other parameters such as the abrasive concentration in the slurry or the total force of the lapping plate on the sample had no impact on the crack depth. This is not the case in the wire-sawing, as differences in breakage stress can be seen for all abrasives. In contrast, the rolling-indenting model predicts that the shape of the abrasive particles plays an important role in the damage depth. This parameter was not tested in this work, but a study from Québatte *et al.* showed that when the abrasive was less round, a slightly higher roughness could be seen, but only for the coarsest abrasives. They concluded that this change was insignificant⁹⁹.

By analysing the roughness measurements closer, it appears that the abrasive concentration also plays a role. Apart from the fact that too thick a slurry breaks wafers, the roughness of wafers sawn with a lower SiC volume fraction (i.e. with a lower density) is lowered in respect to wafers sawn with a higher volume fraction (Table 5.3, parameters D and F). This behaviour is also seen with the bending test: wafers sawn with a lower SiC volume fraction are stronger (Table 5.3). Wafers that have been sawn with a lower volume fraction difference but also different wire tension and feed rate show the same trend in wafer strength (i.e. a lower abrasive volume fraction gives stronger wafers, no matter what the other parameters are, Table 5.3). In contrast, the roughness measurement shows that depending on the wire tension and table speed, it is possible that wafers sawn with a higher SiC volume fraction have a lower roughness (Table 5.3). Finally, the other parameters that were changed also seem to have an influence, but the number of tested conditions is too small to identify it unequivocally.

Wafer thickness measurements showed that the abrasive size, as it was expected, plays a paramount role, as shown in figure 5.4. Furthermore, it also has an incidence on the thickness variation: the larger the abrasive size, the larger the thickness variation. Furthermore, it is seen that the other sawing parameters also influence the thickness, but they are less important than the grit size and it is not possible to sort them out with these measurements.

5.1.3 Conclusions from the first sawing campaign

With the wafers cut during this campaign, it can be concluded that the grit size had the largest impact on the wafers. When a thinner grit size is used, the wafers are stronger, less rough and have less thickness variation. Although, the wafers sawn with F1200 contradict this: the wafers are indeed less rough and have less TTV than the F800 wafers, but they are more fragile, and — more importantly — they show a larger breakage stress variation than the F800 wafers. An explanation could come from the small saw marks that can be found on the surface. They prove that the sawing was too fast for this abrasive, leading to the presence of a few large cracks. This phenomenon can be compared with the transition from a rolling wear to a grooving wear described in section 3.1.

The other parameter that was found to have an influence is the SiC volume fraction in the slurry. When a slurry with a lower volume fraction is used, the wafers are stronger and less rough. However, this observation was made by varying the abrasive volume fraction extensively and it is not sure that this effect is still seen with a smaller variation.

The other sawing parameters that were varied (namely the wire tension and the feed rate) might have an impact on the wafer quality. But their effect is too small to be distinguished

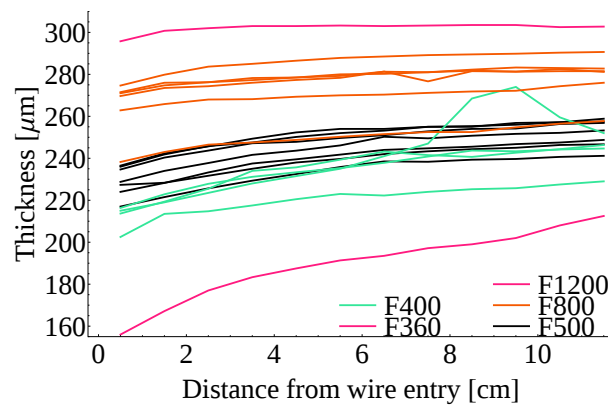


Figure 5.4: Thickness of the wafers sawn during the first campaign. Each abrasive size is plotted in a different colour. The thickness variation is larger for the largest abrasive size.

from random variations with the few cuts that were done.

By comparing these results with predictions from the rolling-indenting model presented in section 3.2, it appears that this model does not describe the sawing process in enough detail. As expected from the model, the grit size has an important impact on the wafer strength, and finer abrasives produce stronger wafers. But the model does not account for the slurry density effect, nor for the influence of the wire tension and feed rate. In consequence, the development of a novel model describing the wafer strength from the sawing parameters is needed. To do so, the second campaign was planned, with more parameter sets to have a more detailed view on the impact of each parameter.

5.2 Second sawing campaign

5.2.1 Sawing parameters

To better understand the influence of the different parameters, a second campaign was required. Its aim was to understand the effect of:

- the abrasive size distribution width on the thickness and thickness variation,
- the abrasive volume fraction on the breakage stress,
- the wire tension on the breakage stress and wafer thickness,
- the feed rate on the breakage stress and wafer thickness.

The experimental plan carried out is presented in Table 5.4. It is more thorough than the first experimental plan. Due to the important improvements that took place between the two plans, it was not possible to make this second plan completely comparable with the first campaign. In particular, the saw model changed dramatically. This second campaign was carried out on a modified HCT wire-saw dedicated for research and development tests. The position of the bricks during sawing is indicated in Table 5.4. The ingots were 50 mm long, giving around 120 wafers per cut. It was mono-crystalline (1 0 0) silicon, squared along $\langle 0 1 0 \rangle$ directions, thus the ingots were squared at a 45° angle from those used in the first campaign. Furthermore, as the maximal wire tension allowed by the saw was 30 N, the tested tensions had to be chosen accordingly. The wire diameter was 140 μm .

To obtain a larger abrasive size distribution, F600 ($d_{50} = 9.3 \mu\text{m}$) and F800 ($d_{50} = 6.5 \mu\text{m}$) abrasives have been mixed at a 50:50 ratio. To avoid throwing away slurry, the cuts made with F800 were done first, then half of the slurry was discarded and replaced with fresh PEG and F600 to cut the ingots with a wider abrasive size distribution. Then, the whole slurry was discarded and a new slurry with F600 only was prepared.

Table 5.4: *Experimental plan of the second campaign. The abrasive F800 has a median size of $6.5\text{ }\mu\text{m}$ and the F600 a median size of $9.3\text{ }\mu\text{m}$. The combination of both abrasives is evaluated to be around $8\text{ }\mu\text{m}$.*

Name	SiC median size [μm]	Slurry density [kg/l]	Wire tension [N]	Feed rate [$\mu\text{m}/\text{min}$]	Position
F800-A	6.5	1.677	30.0	450	Machine
F800-B	6.5	1.624	30.0	450	Machine
F800-C	6.5	1.569	30.0	450	Machine
F800-D	6.5	1.569	25.2	378	Machine
F800-E	6.5	1.569	30.0	378	Machine
F800-F	6.5	1.569	25.2	450	Machine
F800-G	6.5	1.569	21.2	450	Machine
F800-H	6.5	1.569	21.2	378	Machine
F800-I	6.5	1.624	30.0	378	Operator
F800-J	6.5	1.624	25.2	378	Machine
F800-K	6.5	1.624	25.2	450	Operator
F800-L	6.5	1.624	21.2	450	Machine
F800-M	6.5	1.624	21.2	378	Machine
Mix-A	~ 8	1.677	30.0	450	Machine
Mix-B	~ 8	1.624	30.0	450	Machine
Mix-C	~ 8	1.569	30.0	450	Machine
F600-A	9.3	1.577	30.0	450	Machine
F600-B	9.3	1.624	30.0	450	Machine
F600-C	9.3	1.569	30.0	450	Machine
F600-D	9.3	1.569	25.2	378	Operator
F600-E	9.3	1.569	30.0	378	Machine
F600-F	9.3	1.569	25.2	450	Operator
F600-G	9.3	1.569	21.2	450	Machine
F600-H	9.3	1.569	21.2	378	Machine
F600-I	9.3	1.624	30.0	378	Machine
F600-J	9.3	1.624	25.2	378	Operator
F600-K	9.3	1.624	25.2	450	Operator
F600-L	9.3	1.624	21.2	450	Machine
F600-M	9.3	1.624	21.2	378	Machine

5.2.2 Results

In contrast with the previous sawing campaign, these wafers were broken both with a ring-on-ring bending test and with a four-lines bending test. Fifty wafers were broken with the ring-on-ring test to compare results with the previous sawing campaign and thirty-three wafers were broken with the four-lines test. As the stress field is homogeneous on a larger area, the presented results mostly come from this test. The roughness was also measured in more detail, as measurements were made every 5 mm along the wire sawing direction (see section 4.2).

Difference between the two bending test set-ups

The main difference between the ring-on-ring and the four lines test set-up is that the ring-on-ring set-up does not test the wafer edges. But by polishing the wafer edges prior to the four lines test, it is possible to get rid of the influence of the edges and test only the cracks that are on the wafer surface. Thus, the influence of the material removal process only can be studied with the four lines test set-up as well as with the ring-on-ring set-up.

Another difference is that the maximum stress area is different: it lies between the two inner lines of the four lines bending test and it is confined near the inner ring for the ring-on-ring test (see subsection 4.4.1). The smaller area tested by the ring-on-ring set-up provides a lower chance to stress a larger crack and thus generally gives lower Weibull modulus and higher characteristic stress.

Furthermore, the stress is uniaxial in case of four lines bending and biaxial in case of ring-on-ring bending. The maximal stress of the 4-lines test is oriented at 45° from the breakage planes (see the wafer fracture in figure 4.12) so that the cracks are not solicited in pure mode I, but also in mode III (see figure 2.2), whereas the stress applied by the ring-on-ring test is (in some regions) in pure mode I and thus comparatively more harmful for the cracks. These differences in stress field may explain why the measured characteristic stress are lower for the ring-on-ring test despite the lower maximal stress area (Fig. 5.5).

In turn, the parameter influence measured with the four lines bending test cannot be directly extended to the results from the ring-on-ring test as the measured fracture stress is different from one set-up to the other.

Comparison with the first test campaign

The ring-on-ring tests done using these wafers can be compared with the results from the first campaign. Beside the sawing parameters, three things have been changed: the wire-saw, the wire diameter and the wafer crystallographic orientation. All these things may change the wafer strength, but it is not possible to know *a priori* how and how much. As the sawing

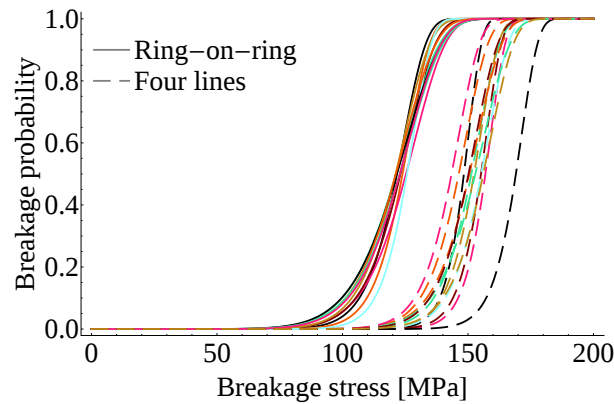


Figure 5.5: Wafer breakage probability measured by a four lines test and by a ring-on-ring test.

parameters used for the second campaign are within the boundaries formed by the sawing parameters tested in the first campaign, it is possible to compare all the series together and see whether one of these factors has a detrimental influence on the breakage strength. By comparing the stress-at-rupture of all the wafer series from both campaigns (Fig. 5.6), it is evident that the wafers cut during the second campaign are much weaker than the wafers from the first campaign.

Such a large difference can be explained by the crystallographic orientation. Although both series of wafers have a $\{100\}$ surface, their edges do not lie along the same direction: the wafers from the first campaign have their edges oriented along $\langle 011 \rangle$ directions whereas

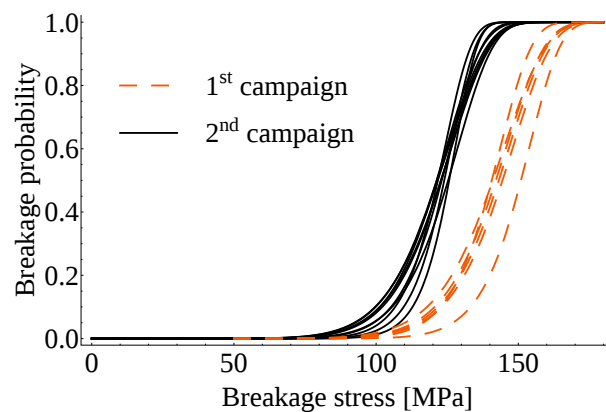


Figure 5.6: Wafer breakage stress comparison between the first and the second campaign. The wafers cut during the first campaign appear to be much stronger than the wafers cut during the second campaign.

the wafers from the second campaign have their edges along $\langle 010 \rangle$ directions (see figure 5.7). Assuming that the cracks are propagating on $\{111\}$ or $\{011\}$ (both type of planes have the same trace on the wafer surface, the fracture toughness of the $\{111\}$ planes is lower, but the stress is normal to the $\{011\}$ planes), the wafers from the first campaign (black axes in the figure 5.7) have roughly equal stress intensity factors at position (a) and (b): at position (a) the stress is more efficiently oriented, but is less intense than in position (b). For the wafers from the second campaign (orange axes in figure 5.7), the stress at position (b) is the most efficiently oriented and has the highest intensity, so that the stress intensity factor is highest at that point. Consequently, the stress intensity factor is higher at position (b) for the wafer from the second campaign than at position (a) or (b) for the wafers from the first campaign, which is why the wafers from the first campaign seem stronger than the wafers from the second campaign. This difference in crystallographic orientations accounts for a factor 1.25 in the breakage stress. When it is taken into account, both types of wafers show similar strengths.

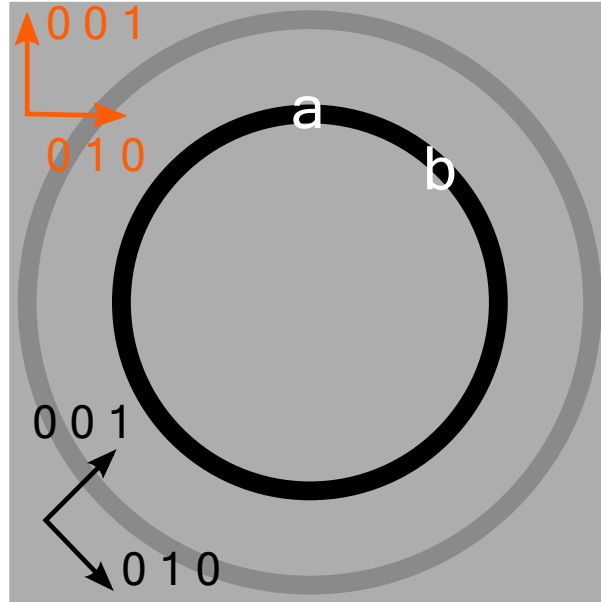


Figure 5.7: Wafer breakage positions for the ring-on-ring test. cracks propagate along $\langle 110 \rangle$ directions, which are parallel to the wafer edges for the wafer sawn during the first campaign (black axes on the figure) or parallel to the diagonals for the wafers sawn during the second campaign (orange axes on the figure).

Top of the sawing groove

Two cuts done with F800 were interrupted: one with a slurry density of 1.677 kg/l (cut F800-A in Table 5.4) and the other with a slurry density of 1.624 kg/l (cut F800-B). Figure 5.8 shows the wafer and groove roughness for both cuts. As the measurement is much harder to carry out in the groove, the error is larger.

The groove roughness is close to the wafer roughness. Nonetheless, the groove roughness varies less than the wafer roughness: it is slightly lower than the wafer roughness at the wire entrance and marginally higher than the wafer roughness at the wire exit. For the lower density slurry (F800-B), the roughness at the bottom of the groove decreases faster than for the higher density slurry (F800-A).

Effect of the abrasive particle size and size distribution width

Comparing the cut made with F600 and F800, it can be seen, as with the previous cuts, that the finer the abrasive, the stronger the wafers (Fig. 5.9). But it is worth noticing that the wafers cut with a mixture of F600 and F800 have almost the same strength as the wafers cut with F600. This suggests that only few large particles are needed to have a major impact on the wafer strength.

The effect of the density is not as straightforward as found in the first campaign. For both narrow distributions (F600 and F800), the wafers are most fragile at the intermediate density ($\rho = 1.624$ kg/l). This is seen in the characteristic stress (Table 5.5) and on the Weibull

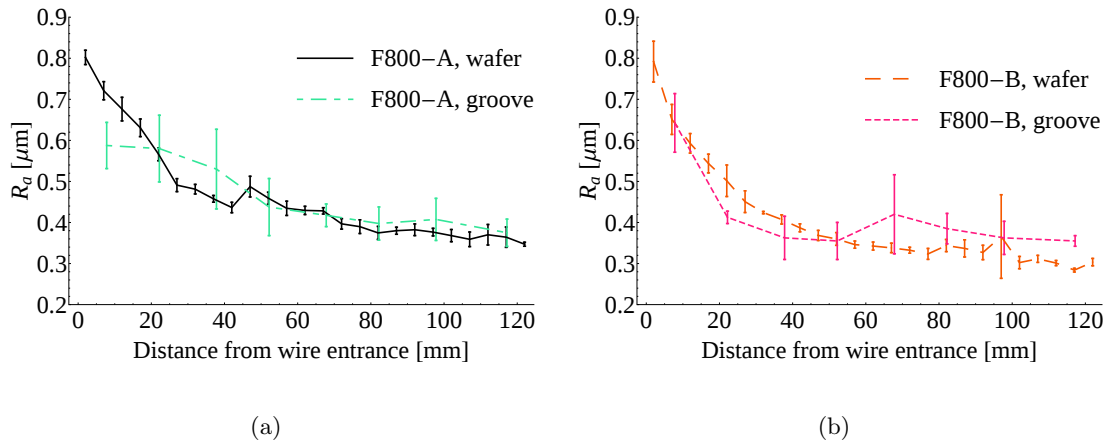


Figure 5.8: Roughness at the top of the groove and on the wafer for (a) the sawing parameters F800-A, and (b) the sawing parameters F800-B. It can be seen that the groove roughness is comparable to the wafer roughness for both sawing conditions.

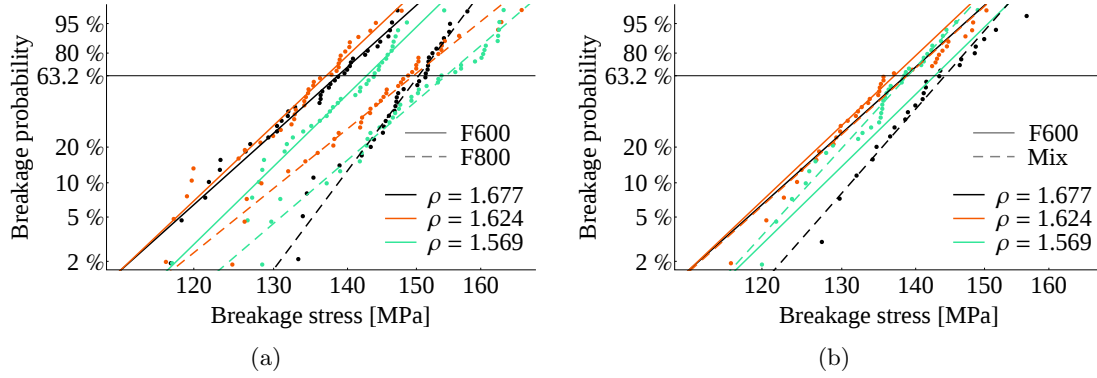


Figure 5.9: Weibull plots of wafers sawn with different slurry densities. (a) F600 and F800: the wafers cut with a thinner abrasive are stronger. (b) F600 and mixture F600 + F800. The wafers have almost the same strength, but depending on the slurry density, the wafers cut with F600 only are stronger or weaker than the wafers cut with the abrasive mixture.

plots (Fig. 5.9). The Weibull modulus shows that the two abrasives behave differently: for F600, it increases when the density decreases and for F800, it is highest for a high density, but increases between the medium and the low slurry density.

The wafers sawn with a mixture of F800 and F600 have a similar behaviour: the worst wafers are sawn with the intermediate density (1.624 kg/l) and as for the F800, the Weibull modulus is highest for the high density and increases between the intermediate density and the low slurry density. Nevertheless, the Weibull modulus of the high density slurry is not as high as for F800 and there is almost no increase of characteristic stress between the intermediate and the low slurry density.

The following mechanism can explain these wafer strength differences: at high SiC volume fraction, there are enough large particles to cut the Si ingot like it was F600 only and this situation can be thought of as a slurry made of F600 only, at a low density. For the two

Table 5.5: Values of the Weibull parameters for different slurry densities. The cuts correspond to the letters A, B and C for the three kind of abrasive size distribution from the parameters in table 5.4.

	$\rho = 1.677$ [kg/l]			$\rho = 1.624$ [kg/l]			$\rho = 1.569$ [kg/l]		
	σ_0	m	$\bar{R}^2$	σ_0	m	$\bar{R}^2$	σ_0	m	$\bar{R}^2$
F600	138.6	18.79	0.97	137.0	19.82	0.96	142.7	20.48	0.98
Mix	144.2	23.87	0.97	138.8	18.83	0.96	138.9	22.99	0.98
F800	150.3	28.02	0.97	149.5	16.90	0.96	154.5	17.98	0.97

lower slurry densities, there are not enough large particles present so smaller particles are also taking part in the sawing, and the lower the density, the larger the part of the distribution that is active. This explains why the characteristic stress is similar for the intermediate and the low slurry density. Nevertheless, between these two slurries, the concentration of particles diminishes and the Weibull modulus increases as for the slurries made of F600 (or F800) only. This is illustrated by comparing the fracture strength of the wafers sawn with F600 with wafers sawn with the abrasive mixture. The wafers cut with a low density slurry made of a mixture of F800 and F600 are weaker than wafers cut with the same slurry density but F600 only. At the intermediate slurry density, the wafers cut with the abrasive mix are comparable to the wafers cut with F600 only and at the high slurry density, the wafers cut with the abrasive mixture are stronger than the wafers cut with F600 only (Fig. 5.9).

The roughness measurement (Fig. 5.10) does not evolve much between the three cuts made with F600 and no conclusion can be drawn from this measurement. For F800, the wafers cut with the densest slurry present a larger roughness than the two other series, but this difference disappears at the wire entrance. Thus, the roughness does not give much indication about the wafer stability evolution with a change in slurry density. But comparing the effect of lowering the slurry density on the roughness of wafers sawn with different wire tensions and feed rate parameters, it is seen that the cuts made with a higher slurry density have a higher roughness. For all three cuts with the abrasive mixture, the roughness is comparable with that of the wafers cut with F600 only.

The wafer thickness measurements show that cutting with a wider abrasive size distribution does not induce a larger, or faster, change in wafer thickness (in the wire direction) compared to wafers sawn with F600 (Fig. 5.11(a)). From the wafer thickness, the wire diameter and the pitch, it is possible to deduce the space available for particles at the side of the grooves. This distance varies between 36 μm and 7 μm for the wafers sawn with F600 and between 40 μm and 6 μm for a mixture of F600 and F800, the largest space being at the wire entrance.

Adding F800 to F600 has quite a small impact on the wafer characteristics. The impact on wafer thickness and thickness variation is negligible, as is the effect on the average roughness (Fig. 5.10). Only the wafer strength shows differences (Fig. 5.9). It can be concluded that only a small fraction of the largest particles participate in the sawing, this fraction is so small that adding F800 up to a 50:50 ratio does not have much effect. If it is assumed that particles are ejected from the sawing area throughout the sawing groove — providing an explanation for the roughness and thickness variation — the rate at which it happens does not depend on the largest particles only, but on the total amount of particles (i.e. the slurry density or the SiC volume fraction). The thickness change for wafers sawn with a mixture of abrasive is comparable with that of F600. If the particle ejection rate depended only on the number

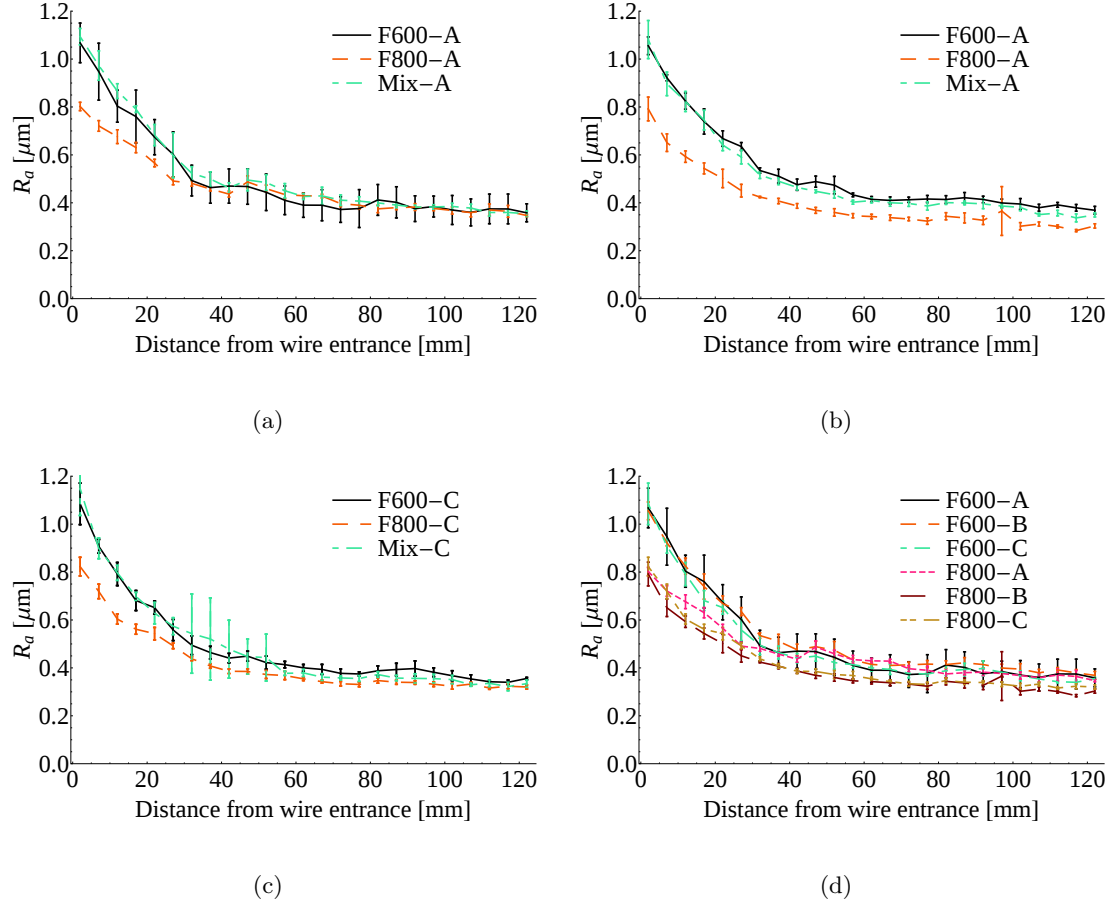


Figure 5.10: Roughness for different slurry densities: (a) high, (b) intermediate and (c) low. The sawing parameters are given in Table 5.4. The wafers sawn with a mixture of F600 and F800 abrasives have a comparable roughness to the wafers sawn with F600 only. (d) Shows the impact of different slurry densities on the wafers sawn with F600 or F800 only.

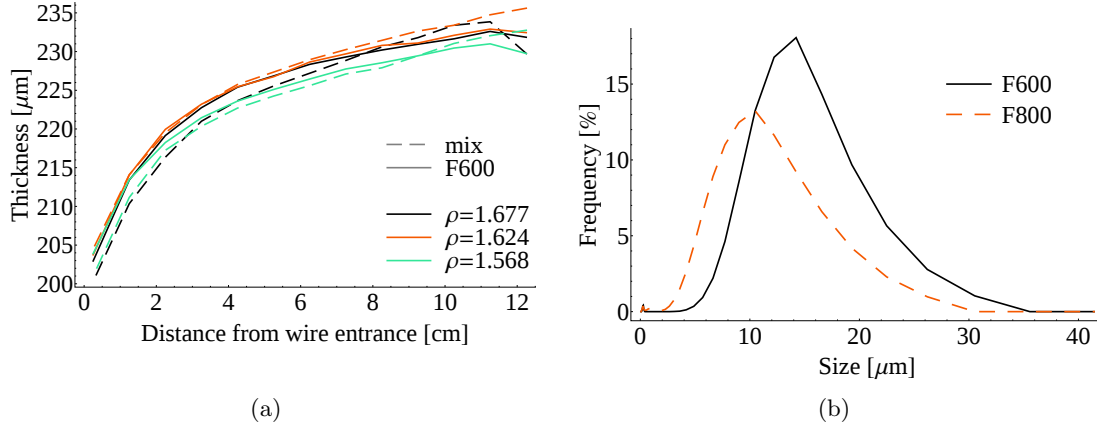


Figure 5.11: (a) Wafer thickness variation for the three slurry densities. The plain lines show the thickness for F600 and the dashed lines for the F600:F800 mixture. Despite that the thickness variation between the wire entrance and wire exit edges is around 30 μm , which is about half the width of the particle size distribution, the wafers sawn with a wider abrasive size distribution do not show larger thickness variation than wafers sawn with F600 only. (b) Particle size distribution of the F600 and F800 abrasive. The distribution has been measured by laser diffraction.

of the largest particles, the wafers sawn with the abrasive mix would show a faster thickness increase. Thus, it appears that the sawing quality depends more on the volume fraction of abrasive and on the size of the largest particles than on the particle size distribution width or the net amount of largest particles.

Effect of the wire tension and feed rate

Figure 5.12(a) presents the effect of wire tension and table feed rate on the characteristic bending stress for wafers sawn with F800. As previously stated, the wafers are stronger when sawn with a lower slurry density. But the importance of this effect depends both on the wire tension and on the feed rate. Furthermore, it can be seen that the lower the wire tension, the higher the characteristic stress, and that having a lower feed rate also strengthens the wafers. The Weibull modulus (Fig. 5.12(b)), in contrast, is not much influenced by the wire tension, but rather by the slurry density and by the feed rate. A high density and a low feed rate gives a higher modulus (i.e. a narrower breakage strength distribution).

The analysis of the wafers sawn with F600 shows different results (Fig. 5.13). Indeed, the parameters have less influence on the characteristic stress than for the F800. Furthermore, the wafers sawn with a wire tension of 25.2 N seem to have an anomalous behaviour. These wafers were sawn at the operator side of the wire-saw (Table 5.4) and that might have influenced the wafer strength — although it was not expected beforehand. These wafers will not be taken

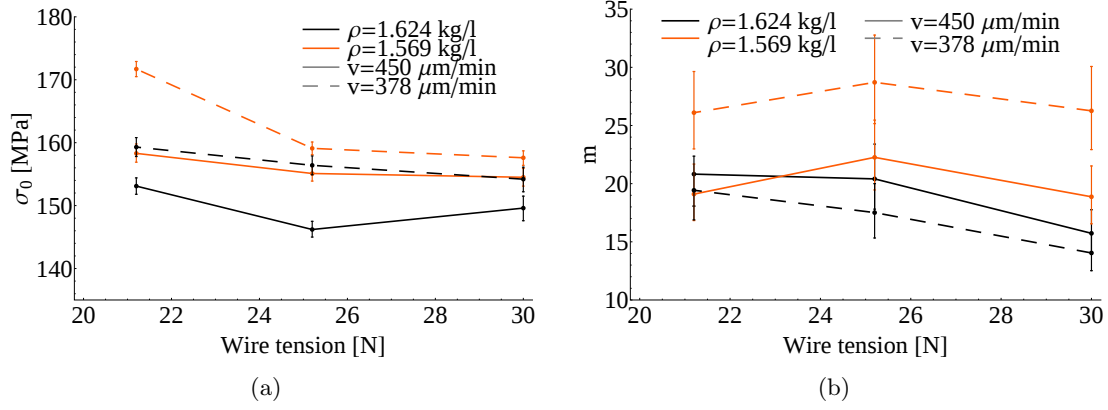


Figure 5.12: (a) Effect of the wire tension and feed rate on the characteristic stress, (b) on the Weibull modulus. The wafers have been cut with abrasive F800 only. The error bars are given for a 68% confidence interval.

into account for the following analysis.

With F600, the sawing parameters have a different influence: the lowest characteristic stress is found at a high feed rate and low slurry density. Also, at low slurry density but fast feed rate, the high wire tension has a higher characteristic stress than the low tension. Furthermore, the Weibull modulus is highest for a low feed rate and a medium slurry density, and the lowest Weibull modulus was found for a low feed rate and a low slurry density (these positions are inverted in the case of F800). Finally, it seems that the impact of the wire tension on the Weibull modulus is more important for the F600 than for the F800 abrasive.

From all these data (Table 5.6, Fig. 5.12 and 5.13), the relative impact of the sawing parameters can be extracted. Their influence can be explained with the help of different models and mechanisms that, when put together, give a global view of the sawing mechanism. Despite the large number of cuts done, the important amount of parameters having a sizeable impact (and their entanglement) prevents a thorough view of all the influences, but a model can be developed from the cuts made. As it was already seen, the parameters do not have the same effect with the different abrasives. This can be explained by the relative importance of the different crack creation mechanisms that are changing with the abrasive size.

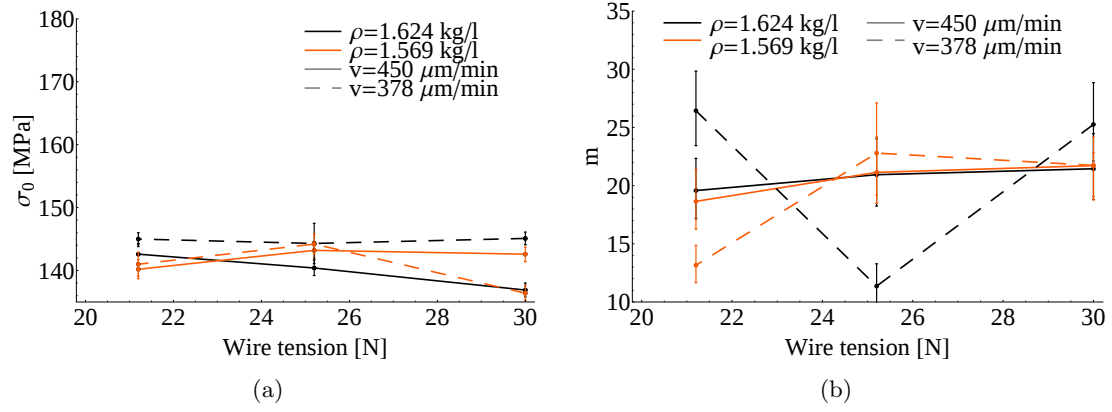


Figure 5.13: (a) Effect of the wire tension and feed rate on the characteristic stress, (b) on the Weibull modulus. The wafers have been cut with abrasive F600 only. The error bars are given for a 68% confidence interval.

Table 5.6: Weibull parameters from the second campaign. The parameters are given both for the four lines test and for the ring-on-ring bending test.

	4-lines test			ring-on-ring test		
	σ_0 [MPa]	CI	m	σ_0 [MPa]	CI	m
F800-A	150.2	{149.2; 151.1}	29.5	124.5	{123.3; 125.7}	16.0
F800-B	149.6	{148.0; 151.3}	15.7	125.7	{124.2; 127.2}	12.2
F800-C	154.5	{153.1; 155.9}	18.9	125.7	{124.1; 127.4}	11.2
F800-D	159.1	{158.1; 160.1}	28.7	128.8	{127.2; 130.6}	11.3
F800-E	157.6	{156.4; 158.7}	26.3	101.7	{100.6; 102.9}	12.9
F800-F	155.1	{153.9; 156.3}	22.3	126.4	{124.9; 127.9}	12.5
F800-G	158.3	{156.9; 159.8}	19.1	124.7	{123.2; 126.1}	12.8
F800-H	171.7	{170.5; 172.9}	26.1	127.7	{126.0; 129.4}	15.6
F800-I	154.2	{152.2; 156.1}	14.0	126.2	{124.5; 128.1}	10.5
F800-J	156.4	{154.9; 157.9}	17.5	125.6	{123.9; 127.3}	10.9
F800-K	146.2	{145.0; 147.5}	20.4	126.9	{125.2; 128.6}	11.0
F800-L	153.1	{151.8; 154.4}	20.8	101.2	{100.0; 102.4}	12.4
F800-M	159.3	{157.8; 160.8}	19.4	126.8	{125.3; 128.3}	12.6
Mix-A	144.6	{143.1; 146.2}	21.0	115.5	{114.1; 116.9}	12.1
Mix-B	138.9	{137.6; 140.3}	18.0	118.8	{117.6; 119.9}	15.4
Mix-C	138.9	{137.8; 139.9}	23.5	120.1	{119.0; 121.2}	16.2
F600-A	138.6	{137.4; 139.8}	20.0	116.3	{115.1; 117.6}	13.7
F600-B	136.9	{135.8; 138.0}	21.5	116.3	{114.7; 117.8}	11.1
F600-C	142.6	{141.4; 143.7}	21.7	118.6	{117.4; 119.8}	15.0
F600-D	144.2	{142.6; 145.8}	22.8	114.6	{113.1; 116.1}	11.1
F600-E	136.4	{135.3; 137.6}	21.7	90.1	{89.2; 91.0}	15.2
F600-F	143.2	{142.0; 144.4}	21.1	119.1	{117.9; 120.2}	15.2
F600-G	140.2	{138.7; 141.7}	18.7	118.9	{117.8; 120.0}	16.2
F600-H	141.0	{139.1; 142.9}	13.2	91.0	{89.9; 92.1}	12.5
F600-I	145.1	{144.1; 146.1}	25.3	116.9	{115.9; 117.9}	17.2
F600-J	144.3	{141.1; 147.5}	11.4	118.5	{117.2; 119.8}	13.4
F600-K	140.4	{139.2; 141.7}	20.9	119.3	{118.2; 120.4}	16.1
F600-L	142.6	{141.3; 143.8}	19.6	92.9	{91.8; 94.0}	12.8
F600-M	145.0	{144.1; 146.0}	26.4	116.6	{115.1; 118.1}	11.0

5.2.3 Development of a defect creation model

The two sawing campaigns show that both parameters determining the Weibull distribution are important to have an accurate description of the wafer breakage strength. Thus, a model has to take into account the characteristic stress (at which 63.2 % of the wafers have broken), but also the Weibull modulus (the width of the distribution) separately. The characteristic stress can be thought of as being determined by the typical maximal crack inside the wafer. In contrast, the Weibull modulus represents the variation of this maximal crack depth from wafer to wafer, or some sort of reproducibility of the sawing condition.

The wafer toughness is not the direct response to a change of the parameters controlled by the wire-saw. The sawing parameters have an effect on the material removal conditions, that in turn influence the force applied by the abrasive particles on the silicon, thus the size of the defects created. This indirect response implies that the sawing parameter effect is complex, but can be decomposed into several different effects.

The wire tension effect can be explained by looking at the interaction of the wire with the abrasive particles. In order to create a defect, an abrasive particle has to be pushed into the wafer surface. This can be due to a particle overtaking another when the available place is not large enough. A more likely situation occurs when the wire is held in place by two particles on one side of the groove and a third particle pushes its way on the other side of the wire (Fig. 5.14). If the particles are too large, the wire has to bend in order to accommodate the space required by these three particles. The force transmitted by the wire to the particle depends on its tension. The wire bending (that also determines the force applied on the particle) is more important when the particles are closer to each other. The distance between particles is proportional to the inverse of the SiC volume fraction ($1/V_{SiC}$)⁵³. Furthermore, the width of the groove depends (in a first approximation) also on the SiC volume fraction. Consequently, the angle between the wire and the groove (ϕ on Fig. 5.14) depends on $\tan(\phi) \propto \frac{V_{SiC}}{1/V_{SiC}} \propto V_{SiC}^2$, so that the indentation force: $P \propto V_{SiC}^2 T$. The crack depth depends on the indenter geometry and on the applied load to the power 2/3, as described in section 2.2: $c \propto P^{2/3} \propto (V_{SiC}^2 T)^{2/3}$. As the crack propagation depends on the inverse of the square root of its depth (equ. 2.8), it appears that the characteristic stress includes a term varying as:

$$\sigma_{0,T} = C_{1,T} + \alpha_1 \frac{1}{(V_{SiC}^2 T)^{1/3}} \quad (5.1)$$

where $C_{1,T}$ and α_1 are constants, V_{SiC} is the SiC volume fraction and T is the wire tension. From this equation, it appears that the higher the tension, the lower the fracture strength, as it is observed in figures 5.12(a) and 5.13(a).

It can be assumed that the particles at the top of the sawing groove are ejected to the

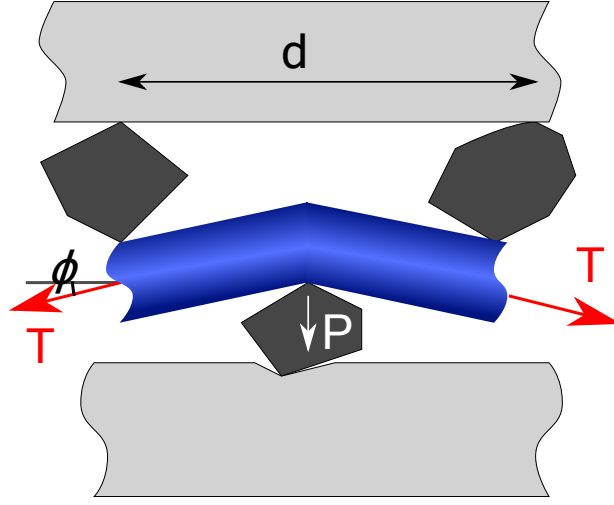


Figure 5.14: Influence of the wire tension on the load applied to an indenting particle (P). This force depends on the wire bending, thus on the tension and the distance between particles.

sides during their passage through the silicon ingot. With such an assumption, a higher feed rate increases the wire pressure on the silicon, ejecting more particles on the sides (Fig. 5.15). These particles are responsible for creating cracks. Thus lowering the feed rate diminishes the amount of particles ejected and so their interactions and the crack depth. Again, the abrasive volume fraction plays a key role, as for a given feed rate, a higher abrasive fraction ejects more particles, consequently increasing the chance to create deeper cracks. As it is seen in figure 5.13(a), the effect of the speed depends strongly on the SiC volume fraction (i.e. the slurry density) so that:

$$\sigma_{0,feed\ rate} = C_{1,feed\ rate} + \alpha_2 V_{SiC} f \quad (5.2)$$

where $C_{1,feed\ rate}$ and α_2 are constants and f is the feed rate. It appears that the lower the feed rate, the stronger the wafers — with one exception: the low slurry density with F600 particles and a high wire tension (Fig. 5.12(a) and 5.13(a)).

The effect of the abrasive volume fraction, as shown previously, is more complicated than what is taken into account by the two previous terms. Indeed, if there is a high concentration of particles, more of them are simultaneously in contact with both the wire and the silicon (or in contact with each other), so that the risk of having a violent impact of one particle in the silicon diminishes (this effect is opposite to the previously described implications of the SiC volume fraction), like the proposition from Wagner *et al*¹¹⁷. Consequently, a higher abrasive

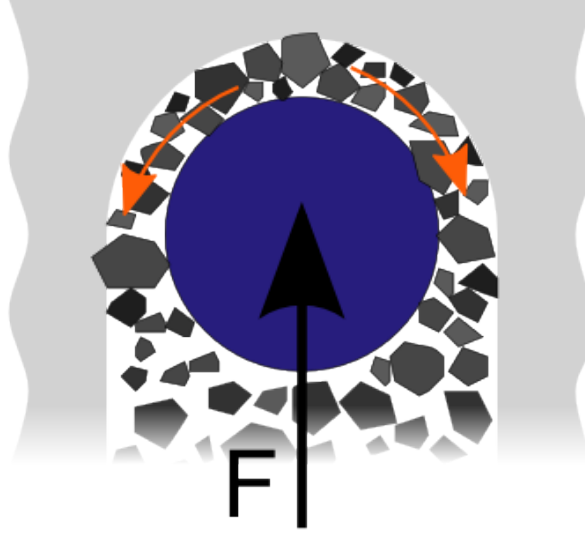


Figure 5.15: Particle ejection on the side of the groove caused by the wire pressure. When a higher pressure is applied, more particles are ejected, creating deeper cracks in the wafers.

volume fraction can increase the breakage stress:

$$\sigma_{0,V_{SiC}} = C_{1,V_{SiC}} + \alpha_3 V_{SiC} \quad (5.3)$$

Furthermore, the wire vibration has to be taken into account despite the fact that it occurs mainly outside the silicon brick. It has an influence not only on the wafer edges, but also a few millimetres inside the ingot: the wafer thickness decrease near the wire exit edge is explained by wire vibrations outside the ingot. The influence on the wafer strength can be expressed by:

$$\sigma_{0,vibrations} = C_{1,vibrations} + \alpha_4 T \quad (5.4)$$

A higher tension decreases the wire vibrations, consequently diminishing the damages created by the wire hitting the silicon and increasing the wafer strength. It has to be pointed out that this term has the opposite effect of the one taking the wire bending into account (equ. 5.1). Also, if the abrasive is coarse enough, the larger kerf loss at the wire entrance allows the wire to vibrate without causing more damage, thus diminishing the importance of this term.

Finally, the feed rate can have an effect that was not described in the previous equations. If the abrasive is coarse enough, the silicon has more time to get damaged by random strong interactions when the feed rate is lowered, making wafers weaker. Thus, a last term has to

come into play:

$$\sigma_{0,rate} = C_{1,rate} + \alpha_5 f \quad (5.5)$$

A global expression of the wafer strength can be found by subtracting the silicon fracture toughness from the defect creation terms described above:

$$\begin{aligned} \sigma_0 &= \sigma_0 - \sigma_{0,T} - \sigma_{0,feed\ rate} - \sigma_{0,V_{SiC}} - \sigma_{0,vibration} - \sigma_{0,rate} \\ &= C_1 - \frac{\alpha_1}{(V_{SiC}^2 T)^{1/3}} - \alpha_2 V_{SiC} f - \alpha_3 V_{SiC} - \alpha_4 T - \alpha_5 f \end{aligned} \quad (5.6)$$

where C_1 is a constant including the fracture toughness and all the constants from equ. (5.1) to (5.5) as it is not possible to isolate one effect from all the others.

The second parameter used to describe the Weibull distribution is its width, given by the Weibull modulus. It varies according to factors other than σ_0 . As for the characteristic stress, the abrasive volume fraction plays a paramount but complicated role: when the volume fraction is low, the particles are widely spaced from each other and few direct particle-particle interactions are expected. At a high abrasive volume fraction, direct particle-particle interactions occur often enough to be repeatable on a wafer scale. Both situations are able to provide a high Weibull modulus (i.e. a narrow breakage distribution). But between them, unrepeatable large interactions are found, making some wafers much more fragile than others, consequently diminishing the Weibull modulus. Thus, the influence of the abrasive volume fraction has the shape of a parabola, as it was observed in figure 5.9:

$$m_{V_{SiC}} = \beta_1 V_{SiC}^2 + \beta_2 V_{SiC} \quad (5.7)$$

The width of this parabola depends on the abrasive size (Fig. 5.12(b) and 5.13(b)): with F800, there is a minima somewhere at an intermediate density but for F600, the parabola is much wider and the minima is mostly outside of the abrasive volume fraction used.

The feed rate has an important impact on the Weibull modulus. The slower the cut, the more time the abrasive has to make similar defects on all wafers (but this also depends on the the SiC volume fraction to some extent):

$$m_{feed\ rate} = \beta_3 f + \beta_4 f V_{SiC} \quad (5.8)$$

For both abrasive sizes, the low density has a different behaviour than the medium density: for F800 at low density, slowing down the feed rate increases the Weibull modulus, whereas at medium density, slowing it down diminishes the Weibull modulus (Fig. 5.12(b) and 5.13(b)). For the F600 abrasive the opposite behaviour is observed. For both abrasive sizes, only one

cut was made with a high slurry density, so that no extrapolation is possible. Finally, a global expression for determining the Weibull modulus is given by adding the terms described above:

$$\begin{aligned} m &= m_{V_{SiC}} + m_{feed\ rate} + C_2 \\ &= \beta_1 V_{SiC}^2 + \beta_2 V_{SiC} + \beta_3 f + \beta_4 f V_{SiC} + C_2 \end{aligned} \quad (5.9)$$

For both equations 5.6 and 5.9, it is possible to fit the data from the breakage tests: the results are presented in figure 5.16 and the fitted parameters are given in Table 5.7. When comparing the parameters' influence on the characteristic stress (σ_0) for F800 and F600, it is clear that the sawing parameters have more effect on the smaller abrasive size. Also, for F800 they have the same influence for both SiC volume fractions studied (Fig. 5.16(a)). This is not the case for F600, as the wire tension plays a much smaller role than for F800, and the speed rate effect depends on the SiC volume fraction (Fig. 5.16(b)). Furthermore, there are parameters that have little effect: for F800, the term $\alpha_5 f$ can be omitted without noticeably changing the model. In contrast, this term plays an important role in modelling the effect of F600, for which the term $\alpha_6 T$ is not important. Finally, the last difference between the two abrasive sizes is the sign of $\alpha_1 \frac{1}{(V_{SiC}^2 T)^{1/3}}$ that is positive for F600 and negative for F800.

To fit the model, some cuts made with F600 were omitted (the F600-D, F600-J and F600-K: the cuts made with a wire tension of 25.2 N at the operator side of the saw as previously discussed) as it is much lower than the other points. As for the characteristic stress, the Weibull modulus model also shows differences between the two abrasive sizes. For the F800 (Fig. 5.16(c)), the second degree term of the SiC volume fraction has a clear influence, but not for the F600 (the parabola is much wider, Fig. 5.16(d)). Also, the feed rate influence is not

Table 5.7: Fitted parameters for equation (5.6) and (5.9).

	F600	F800
α_1	52.4	-530
α_2	4.07	0.00778
α_3	-1640	-1260
α_4	0.831	-5.71
α_5	-0.896	0.0774
C_1	-150	-725
β_1	230	10450
β_2	2204	-6642
β_3	-1.14	0.971
β_4	-5.17	4.18
C_2	-478	995

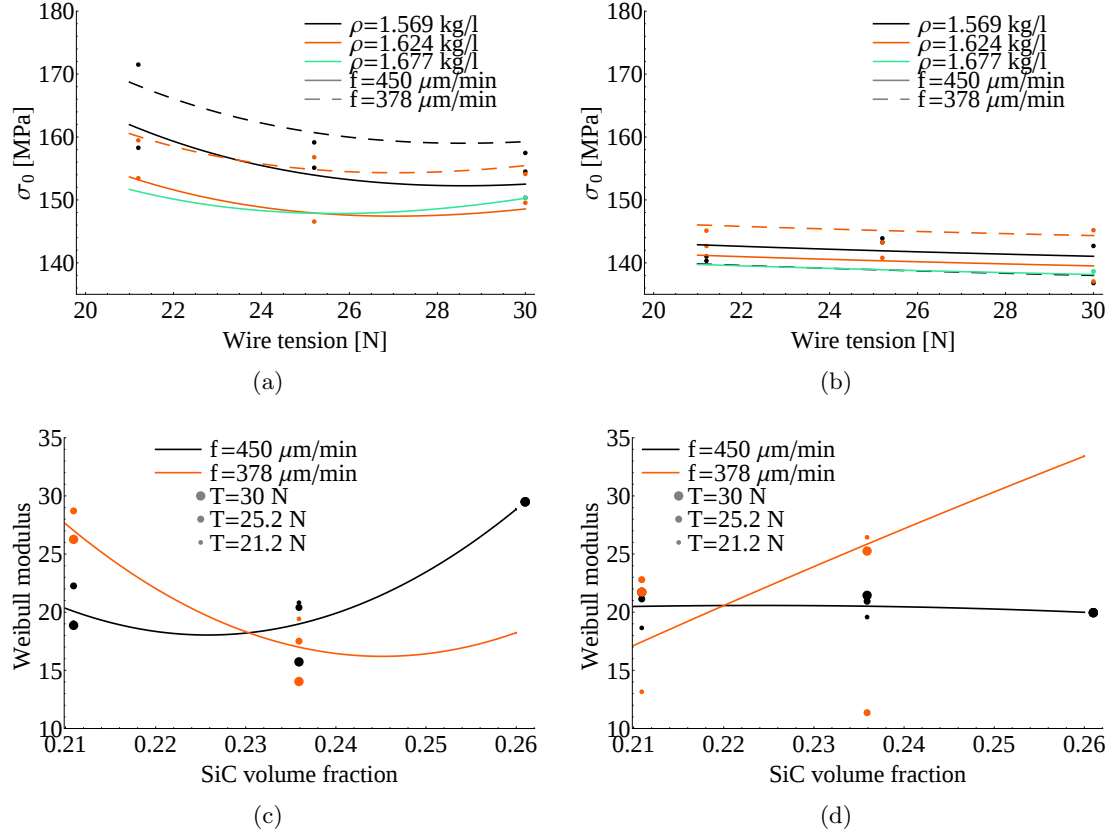


Figure 5.16: Characteristic stress model of the studied sawing conditions for (a) abrasive size F800, (b) for abrasive F600, (c) Weibull modulus for F800 and (d) for F600. The model fits the points well, apart from the cut with F600, at a volume fraction of 0.236, a wire tension of 25.2 N and a feed rate of 450 $\mu\text{m/min}$. Consequently, this point was not taken into account for fitting the model. Differences in the Weibull modulus can be seen when varying the tension, but as it seems that it depends on other parameters as well, the experimental plan was not detailed enough to include this effect in the developed model.

the same: for F800, increasing the feed rate moves the minima towards a lower SiC volume fraction, and for F600, it moves towards a higher fraction. Both abrasive sizes show that the tension indeed has an influence on the Weibull modulus. But this effect also depends on the other parameters, so that it is not possible to model it with the amount of available data.

The extension of the model to the cuts from the first experimental campaign is hard, as many parameters have changed. The silicon does not have the same crystallographic orientation, so that it has to be expected that for a given sawing condition, the defect depth is different (see section 2.5). Also, a different wire-saw was used, so it may be possible that the wafers are generally stronger (or weaker) than the wafers from the second campaign. Furthermore, the variation range of the parameters was larger for the first campaign, making it possible to exceed critical conditions that were not studied during the second campaign. As the wire diameter is different, all the parameters involving the wire tension cannot be directly translated. This should have no influence on the term $\sigma_{0,T} = \alpha_1 \frac{1}{(V_{SiC}^2 T)^{1/3}}$ but plays a role in the wire vibration ($\sigma_{0,vibrations} = \alpha_4 T$). Extrapolating the model to the higher tensions used during the first campaign shows that the term $\sigma_{0,T}$ does not have an influence and the only effect of the tension is determined by $\sigma_{0,vibrations}$. Consequently, a high tension of 38 N would give unrealistically strong wafers. In contrast, when using the wire tensile stress in the term $\sigma_{0,vibrations}$, the stress levels applied to the wire are in the same range as those in the second campaign and the model is more likely to be usable. Another change to accommodate the equation with the extended parameter range that was used concerns the sawing speed. Indeed, it was found that for F800, slower sawing increases the wafer strength. For the F600, the opposite was observed for some conditions. It is assumed that because the F600 is more efficient in sawing, a feed rate increase would not be detrimental for the sawing, but decreases the time available for the abrasive to create larger cracks. It can be expected that when sawing very slowly with F800, the same result should be observed (at much lower feed rate than for F600, because of the abrasive sawing efficiency) and that an optimal speed (that should depend on the slurry density) would be found between these two limits. To describe this effect, a new term depending on the feed rate and slurry volume fraction should be introduced to allow the existence of an optimal feed rate (e.g. $\alpha_6 f^2 V_{SiC}$). But given the few different feed rates studied, this term cannot be fitted with satisfaction. Thus, an improved model for determining the characteristic stress is given by:

$$\sigma_0 = C_1 - \frac{\alpha_1}{(V_{SiC}^2 T)^{1/3}} - \alpha_2 V_{SiC} f - \alpha_3 V_{SiC} - \alpha_4 T / s_{wire} - \alpha_5 f - \alpha_6 V_{SiC} f^2 \quad (5.10)$$

where s_{wire} is the wire section.

Furthermore, the test set-up used for the first campaign is the ring-on-ring test, so that

the test influence has to be taken into account. Fortunately, the parameters used to model the Weibull modulus are — with the exception of the term V_{SiC}^2 — also found in the characteristic stress model. Consequently, changing of the equations is not required and fitting the characteristic stress (equ. 5.10) to the data obtained with the ring-on-ring set-up provides a good enough fit to test the model with the sawing parameters used for the first campaign.

By introducing these modifications to the model and fitting the data from the second sawing campaign — without the speed limit term, but keeping its existence in mind when analysing the results — it is found that the predictions made by the model are close to what was found experimentally. The wafers sawn at 173 $\mu\text{m}/\text{min}$ are the most fragile (they were sawn 2.5 times slower than the wafers from the second campaign) and the wafers sawn with the lowest wire tension and a low slurry density are the strongest. However, the wafers sawn with an extremely low density are much weaker than predicted, but this can be explained by the density being far from those used in the second campaign.

The Weibull modulus modelling, in contrast, does not give as good a match as the characteristic stress. The wire tension, which seems to have a complex influence, was varied much more during the first campaign but is not taken into account by the model (that is derived from the results of the second campaign). The same argument is valid for the slurry density: it was seen that it has a paramount but complex influence and the variation range studied during the first campaign was much broader than for the second campaign. Thus, using the model fitted with the data from the second campaign to predict the Weibull modulus measured during the first campaign gives unrealistic values. Also, it is not possible to use the values obtained from the first campaign in conjunction with the results from the second campaign because the crystallographic orientation is different, and the number of sawing parameters is too small to use these results separately for fitting the model. Finally, it is not possible to compare the coarser abrasives, as F600 was only studied in the second sawing campaign.

5.2.4 Wafer thickness and thickness variation

The wafer thickness also depends on the sawing parameters. As a rule of thumb, the kerf loss is given by $d_{kerf\ loss} = d_{wire} + \kappa d_{50}$ where d_{wire} is the wire diameter, κ is an empirical constant around 3.5 and d_{50} is the median abrasive size¹¹². A more precise estimation of the wafer thickness requires the other sawing parameters to be taken into account. As expected from the breakage stress results, the influence of the sawing parameters is entwined and also depends on the abrasive size.

It can be thought that the slower the feed rate, the thinner the wafers, as the abrasive has more time to wear the wafers. Indeed, it is the case for F600, but it is the contrary for F800. The wire tension effect is more complex to decipher: a higher tension can lead to thicker or

thinner wafers, depending on the other parameters. As a trend, a lower tension gives thinner wafers. Although, this effect is much less important than the one of the feed rate or the slurry density. Taking all these effects into account, an equation describing the wafer thickness can be written:

$$t = \theta_1 T + \theta_2 f + \theta_3 T f + \theta_4 V_{SiC} + \theta_5 T V_{SiC} + \theta_6 f V_{SiC} + C_3 \quad (5.11)$$

where t is the average wafer thickness and θ_i and C_3 are empirically fitted constants. Figure 5.17 presents a plot of this function fitted to the data from the second sawing campaign. It can be seen that — as for the breakage stress — the sawing parameters have more impact with the fine abrasive than with the coarser one. The values of the constants θ_i are given in Table 5.8.

In contrast, the total thickness variation (TTV) does not change much when varying the sawing parameters. It stays in the range of 19–23 and 25–30 μm for F800 and F600 respectively. Consequently, it is important to notice that the abrasive density does not play an important role in determining the TTV. Nevertheless, as the TTV was not measured on each sawn wafer, it is possible that the sawing parameters have an influence on the number of wafers with an unexpectedly large TTV (the wafers that would not meet specifications in

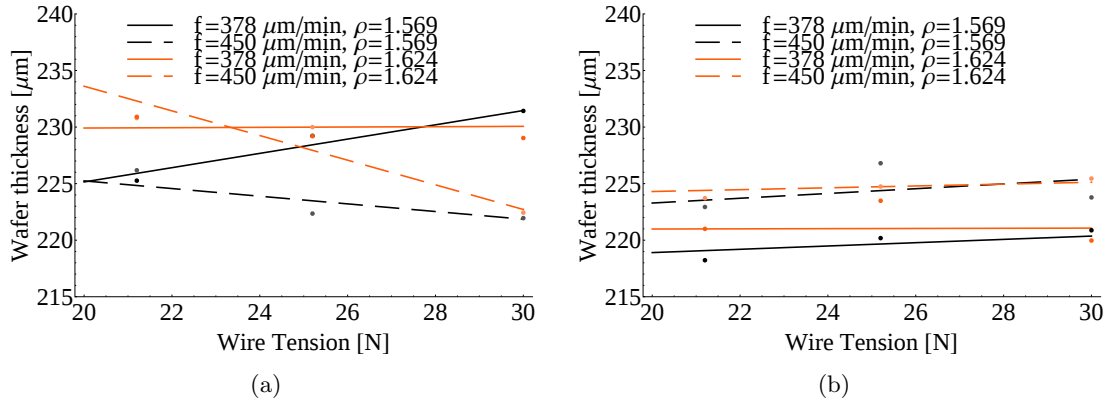


Figure 5.17: (a) Wafer thickness for the F800 abrasive, (b) for the F600. The thickness depends much more on the sawing parameters with F800, and the impact of the parameters changes with the abrasive size.

Table 5.8: Fitted parameters for the wafer thickness given by equation (5.11).

	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	C_3
F600	-0.789	-4.98	0.000901	493.9	0.208	0.851	96.1
F800	1.69	-29.0	-0.0135	143	-0.0843	11.8	80.3

an industrial environment), but it was not analysed.

The wafer thickness evolution shows that the space worn out by the particles decreases from the wire entry to its exit. This is explained by large particles leaving the region where sawing occurs. It is interesting to note that the rate at which the wafer thickness increases does not depend on the slurry density (i.e. on the volume fraction of abrasive), but the mean thickness does. Indeed, a lower slurry density provides thinner wafers, but the TTV is comparable to the wafers sawn with a higher slurry density.

5.2.5 Findings from the model and its limits

The novel wafer strength model developed in this work is important for getting a fundamental understanding of the sawing process and the defect creation mechanisms. More importantly, this model is based on interactions that have physical meanings. Despite this, the relative importance of each type of mechanism had to be empirically fitted. One important finding is that it is highly probable that there is an optimal feed rate, at which the wafers are the strongest. This rate should depend not only on the abrasive size but also on the slurry density: the wafers from the first campaign that were sawn with F800 were stronger when they were sawn at an intermediate speed than the ones sawn at a very low speed. A summary of the impact of each sawing parameter and their interactions is shown in figure 5.18.

It was shown that a lower wire tension is beneficial for the wafer strength. Unfortunately, the wafer thickness, and thickness differences from wafer to wafer degrade when using a lower tension. Indeed, a higher wire tension prevents the wire from moving laterally, consequently improving the wafer thickness and waviness (but these were not parameters that were investigated in this study).

When the slurry density is too high, the wafers are broken by the slurry impact at the wire entry. In contrast, when the slurry density is too low, there is not enough abrasive to cut silicon at the speed required by the feed rate and it leads to wire marks over the whole wafer surface. This limit should depend on the feed rate and also on the abrasive size (this effect was only observed on the smallest abrasive size, F1200, during the first sawing campaign).

Linking the findings from the model to the roughness and wafer thickness observations, allows deeper insight into the sawing model. As postulated by Möller⁸⁸, it seems plausible that only the largest particles create cracks inside the wafers. It was shown in this work that the size of these largest particles diminishes between the wire entrance and its exit. This translates to a roughness decrease and a thickness increase. But these two measurement types show a different trend near the wire exit: the roughness reaches a plateau approximately after the first half of the wafer length (Fig. 5.10(d)), whereas the thickness increases until the last few millimetres before the exit (Fig. 5.11(a)). Furthermore, the slurry density changes the

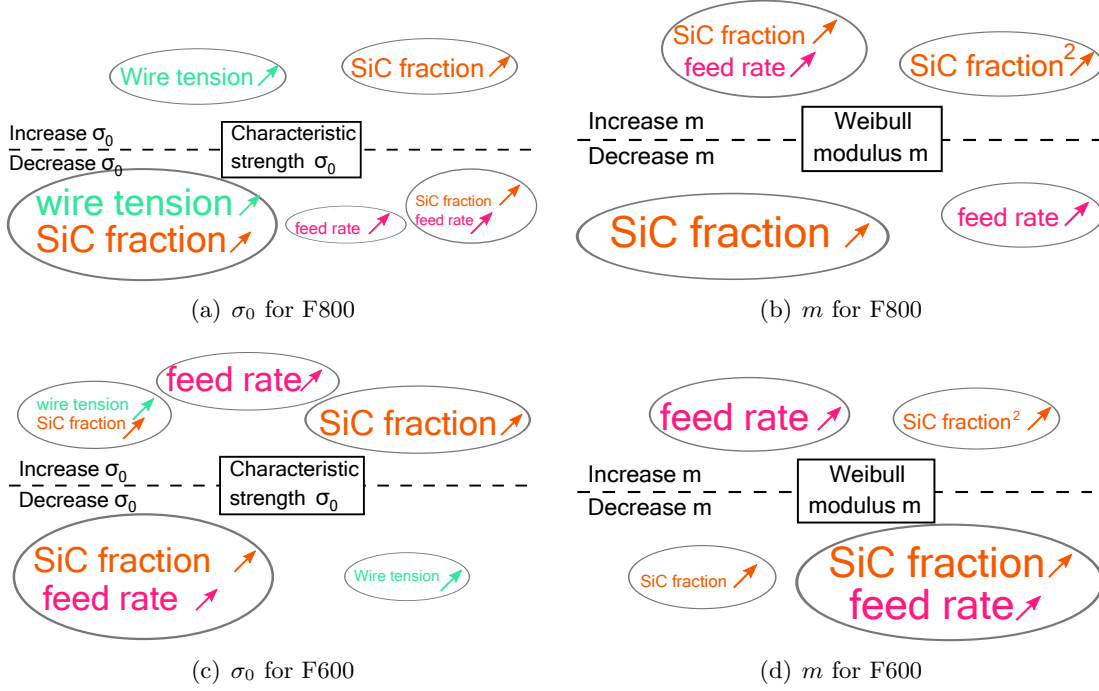


Figure 5.18: Summary of the sawing parameters interactions determined by the semi-analytical model: (a) the characteristic stress and (b) the Weibull modulus for F800, (c) the characteristic stress and (d) the Weibull modulus for F600. The size of the parameters represent their relative importance. The parameters are grouped in the same terms than in equation (5.9) and (5.10). As the effect of the parameters is entwined, changing one parameter can have a beneficial or detrimental effect depending on the other parameters, which is why some terms are found several times.

wafer thickness, but not the rate at which it varies between the wire entrance and exit — and this is even highlighted by the wafers sawn with a mixture of F600 and F800 abrasive. Their thickness and the thickness evolution is comparable to those of wafers sawn with F600 only, despite the fact that there are half the volume of coarse particles in the mixture.

The discrepancy between the roughness and thickness evolution can be explained by assuming not only a particle size distribution change between the wire entrance and its exit, but also a decrease in the particle volume fraction. The rolling-indenting model (section 3.2) predicts that the slurry density should not have any influence on the roughness, only that the particle size distribution does. In that aspect, the roughness evolution indicates a diminution of the particle size (which also leads to a thickness increase) during the first half of the wafer length. Then, the roughness stabilises, indicating that the particle size should remain constant. But if particles were escaping the sawing region near the wire entrance, there is no reason why they should not escape closer to the wire exit. As the space left for particles near

the wire exit is close to the diameter of the smallest particles, a lot of particles have a similar diameter (at least in the original particle size distribution) and a further decrease of the largest particle diameter requires that a large amount of particles escape. Thus, the effective largest particle diameter in the second half of the wafer length does not noticeably evolve, but the volume fraction diminishes. By lowering the particle volume fraction, the space between the particles increases, which gives the wire more freedom to bend between particles, applying less force on the particles. Consequently, the wafer can be thicker than it is nearer to the wire entrance, explaining the uninterrupted wafer thickness increase while the roughness stays constant.

The rate at which the larger particles leave the cutting zone is determined by the vertical pressure of the wire. This pressure depends on the feed rate and on the slurry density, but only to some extent. When the F600 is used, the abrasive is efficient enough to saw the silicon at the speed imposed by the different feed rates tested in this work without a large pressure change. The situation is different with the F800: feed rate change requires a larger pressure change (the same trend can be seen in the rolling-indenting model, equ. (3.4)). A higher pressure pushes more particles away from the cutting region. As already discovered by Rietzschel *et al*¹⁰⁷, when a thinner abrasive is used, the normal force decreases, so that when the larger particles have been ejected from the sawing region, the cutting efficiency increases and a stable condition is reached between the wire pressure and the abrasive cutting efficiency.

The wafer thickness variation can be separated into three effects: the first is due to the wire vibration. It has an influence only on the first few millimetres after the wire entrance and on the last few millimetres before its exit. The second effect is the maximal particle size decrease, having an effect until approximately the first half of the wafer length (until the roughness reaches a plateau). Finally, the third effect is a decrease in the local abrasive fraction volume, which is responsible of the wafer thickness change on the second half of the wafer length.

Finally, it is seen that sawing strong wafers is only partly compatible with a high productivity. The best sawing parameters involve a low slurry density, a low feed rate and a low wire tension. These parameters require more time to complete a cut and provides wafers with more thickness difference (from wafer to wafer). Ultimately, the most important parameter is the abrasive size: a smaller abrasive results in stronger wafers (for a similar particle shape).

5.3 Chapter summary

In this chapter, a novel model describing the wafer strength from the sawing parameters was developed. From the grit size, the slurry density, the wire tension and feed rate, the wafer

characteristic strength and their Weibull modulus is extracted. It was seen that using a finer abrasive results in stronger wafers. A lower slurry density also improves the wafer strength, but using too small an abrasive size (like F1200 in the first campaign) or too low a density gives weak wafers. A low wire tension and a slow feed rate also improve the wafer strength, although this effect is smaller than the one of the slurry formulation and also has some limits. Furthermore, the effect of the feed rate and wire tension are different for F800 than for F600.

In the next chapter, the effect of silicon debris in the slurry is analysed. The cuts described above were made using a small amount of silicon compared to what the wire-saws are designed to cut, so that the effect of silicon debris could be neglected. When cutting more important amounts of silicon, the debris can have a sizeable influence: saw marks appear near the wire exit edge of the wafers. This influence is quantified and a model describing this phenomenon is proposed. Finally, the effect of debris is put into perspective with what was presented in this chapter in order to get a better view of the sawing process.

Chapter 6

Effect of silicon debris on the wafer quality

One parameter that was not studied in the previous sawing campaigns is the influence of silicon debris. The amounts of silicon that were sawn were small compared to the loads the industrial wire-saw are designed to cut. Such machines need a large amount of slurry to work, so that the amount of debris produced previously was negligible. However, the effect of debris is important in industrial wafer production. The slurry is changed after each cut (or during the cut, depending on the producer) and has to be recycled. The recycling consists of centrifuging the slurry to separate in a first step the SiC abrasive from the lubricant containing debris and in a second step to separate the debris from the lubricant. Such a process recycles around 80–90 % of the abrasive and PEG², so that maximizing the amount of debris in the slurry before it is recycled lowers the costs (less slurry to recycle and less losses). But before optimising the recycling, a better understanding of the impact of silicon debris on sawing is necessary.

In this chapter, the effect of silicon debris in the slurry is studied and a model explaining its influence is presented. The measurements show that there is a threshold below which the debris have no influence. When the amount of debris exceeds this threshold, saw marks appear and if the saw marks are too important, the wafer strength decreases dramatically. It is shown that this decrease can be correlated with a roughness increase at the wire exit side of the wafers.

6.1 Sawing parameters

A Meyer Burger DS 264 wire-saw was used to cut multi-crystalline, $156 \times 156 \text{ mm}^2$ bricks. The loading length was 370 mm (approximately a half-load for this type of wire-saw). Four cuts were made without changing the 300 litres of slurry in the saw. The slurry was made of PEG and F600 SiC abrasive. The wire-saw measures the density of the slurry being poured on the wire web every 20 seconds and the value at the end of the cut was taken as the slurry density. The wire had a diameter of $140 \text{ }\mu\text{m}$, and the wire-guides pitch was $350 \text{ }\mu\text{m}$, leading to a wafer thickness of approximately $170 \text{ }\mu\text{m}$. After being cleaned, each wafer was characterised by a Henneke measurement system to measure its thickness, total thickness variation (TTV) and saw mark height. The saw mark height was measured as the largest height difference on a length of 5 mm.

Slurry samples were taken before the first cut and then after each cut. The particle size distribution was measured with a Beckman-Coulter LS13320 laser diffraction particle size analyser. From each sample, two particle size distribution measurements were made.

For each cut, five wafers located near the machine side of the brick were taken to measure the roughness. The measurements were done in a direction perpendicular to the wire direction. Their length was 5.6 mm as recommended by the norm ISO 4287. Measurements were done on three lines on each wafer: 25, 65 and 105 mm after the beginning of the cut. Along these lines, one measurement each 5 mm was made, as presented in figure 6.1.

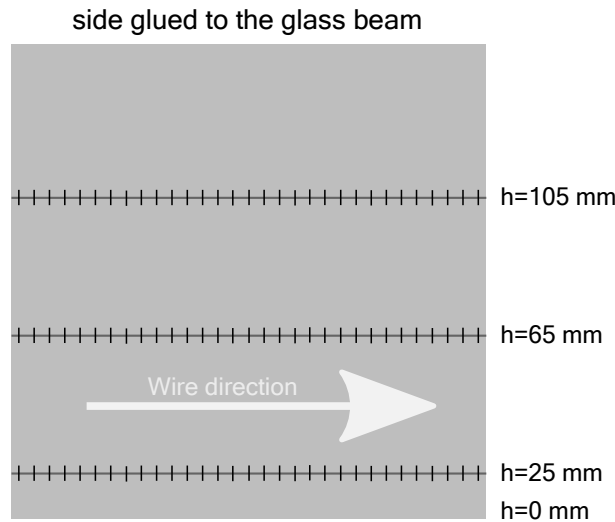


Figure 6.1: Schematic view of the roughness measurement positions on a wafer. The measurement lines are in black, their centre aligned on the grey lines at 25, 65 and 105 mm from the brick side where the cut started.

To evaluate the wafer strength, 50 wafers were taken from the machine side of the load, next to the wafers needed for roughness measurements. They were broken with a four-lines bending test whose supports were oriented parallel to the wire direction during sawing. The space between the two widely spaced lines and between the two central lines were 125 and 60 mm respectively.

Figure 6.2 presents the particle size distribution (PSD) measured after the first and the last cut. To model these particle size distributions, three distributions were used: a log-normal distribution for the smallest particles, and a normal and a log-normal distribution for the coarse particles. These three distributions fit the experimental measurements and allow the calculation of the relative volume of debris present in the slurry. Although this method permits a good description of the slurry particles, it is not possible to directly get the total amount of debris in the slurry using it, as the measured volumes are relative to the total amount of particles measured. But assuming that the coarse particles are only SiC and knowing the slurry density before the first cut allows the quantity of coarse particles present in the slurry to be known. In turn, this enables to calculate the total amount of debris from the particle size distribution measurements. Hence, the used slurry density can be calculated and compared with the density measurement made by the wire-saw (Fig. 6.3). The volume fraction of silicon debris after each cut is given in Table 6.1. At the end of the fourth cut, the silicon debris represents more that one fourth of the total particles volume.

It is also possible to calculate the theoretical debris volume from the sawing conditions. The volume of debris from one wire groove is given by: $V_{groove} = (d_{wire} + 3d_{SiC})l^2$ where d_{wire} is the wire diameter, d_{SiC} is the abrasive median diameter and l is the wafer size.

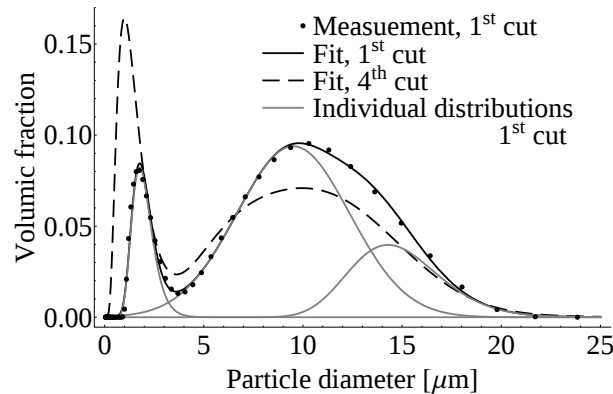


Figure 6.2: Particle size distribution of the slurry after the first cut (in black, the dots are the measured points and the line is the fit). The three distributions used to fit the measurement are plotted in grey. The dashed distribution is the particle size distribution after the fourth cut.

Table 6.1: Fraction of silicon debris to total particle amount after each cut, as measured from the particle size distribution (PSD), the slurry density and as calculated theoretically.

	After 1 st cut	After 2 nd cut	After 3 rd cut	After 4 th cut
From PSD	11 %	17 %	19 %	26 %
From density	4 %	11 %	17 %	24 %
Theory	7 %	12 %	17 %	22 %

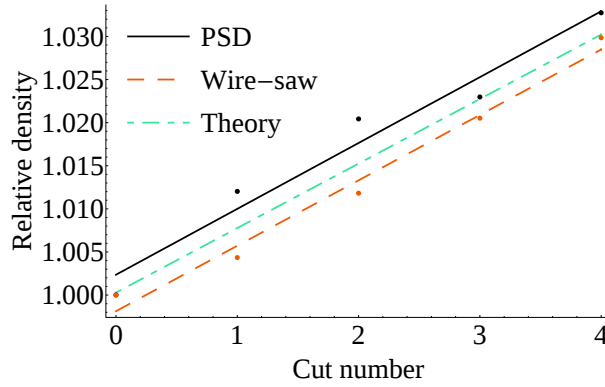


Figure 6.3: Slurry density after each cut. The black points represent the density measured by the wire-saw, the grey points are calculated from the particle size distribution and the original slurry density. The solid lines are the linear fits of the data and the dashed line is the theoretical density.

The amount of grooves that are sawn is: $n = \frac{L_{Si}}{p}$ where L_{Si} is the silicon brick length and p is the pitch. Thus, the volume of silicon debris is:

$$V_{debris} = nV_{groove} = \frac{L_{Si}l^2(d_{wire} + 3d_{SiC})}{p} \quad (6.1)$$

This volume is then used in conjunction with the volume of SiC and PEG first mixed to extract the theoretical fraction of debris after each cut. To calculate the density, the wear of the wire has to be taken into account. From the wafer thickness measurement, the wire diameter is assumed to decrease by 2 μm during the sawing. Though the amount of debris created by the wire wear is small, it has a noticeable impact on the density calculation because of the high steel density (7850 kg/m^3). By adding the steel and silicon debris to the original slurry mixture, the density can be calculated. This density is plotted together with the two other density measurements in figure 6.3. It can be seen in this plot that all three methods agree, despite the fact that the density coming from the particle size distribution is slightly higher (probably due to the sedimentation of coarse SiC particles, thus increasing the measured amount of debris). But it has to be kept in mind that the wire-saw density measurement

device may induce errors too. Finally, it appears that the silicon debris is small (in the range of 1–3 μm), and the SiC abrasive size does not decrease much during the sawing process (Fig. 6.2). Also, the theoretical amount of debris gives a good description of the measured density.

6.2 Wafer characterisation

The wafer characteristics (thickness, TTV and saw mark height) mean and standard deviation of each cut are given in Table 6.2. Figure 6.4 presents SEM pictures of the wafer saw marks visible on the wafers from the 4th cut. It is evident from this figure that large chips are present at the top of the saw marks, which indicates that deep cracks may be present under the surface.

Table 6.2: Wafer properties for each cut (mean values and their standard deviation s.d.). All the sawn wafers were measured.

	thickness [μm]	TTV [μm]	Saw mark height [μm]
1 st cut	170, s.d. = 4	15, s.d. = 10	7, s.d. = 6
2 nd cut	171, s.d. = 5	15, s.d. = 10	7, s.d. = 9
3 rd cut	172, s.d. = 6	17, s.d. = 9	16, s.d. = 11
4 th cut	174, s.d. = 8	27, s.d. = 20	22, s.d. = 11

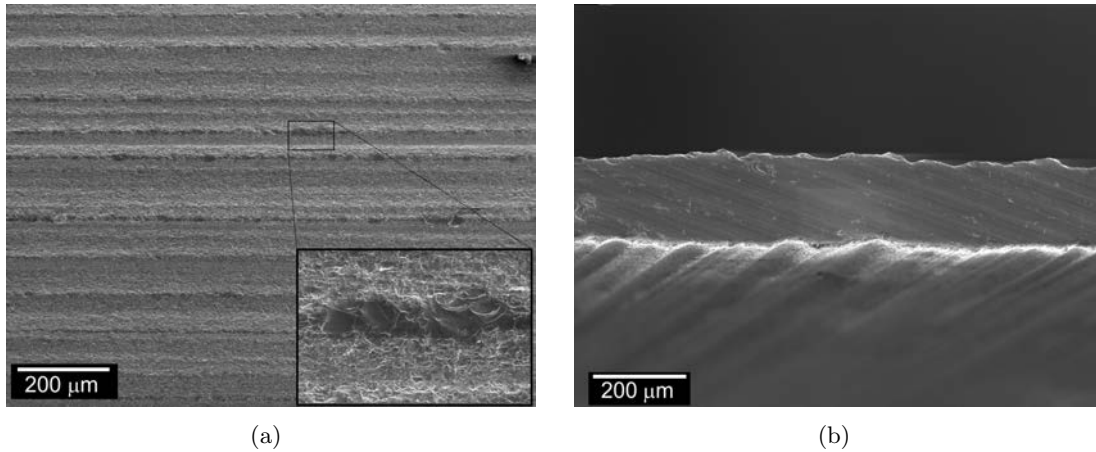


Figure 6.4: SEM picture of the saw marks: a) from the wafer surface and b) from the wire exit side. It can be seen that on the top of the saw marks, many places have been chipped off, contrary to the bottom of the saw marks. When the sample is looked at from the side, it is clear that there is no correlation between the saw marks on either side of the wafer.

The saw marks are characterised as the maximal height difference measured on a wafer, over a length of 5 mm. Figure 6.5 presents saw mark height for every wafer of each cut. It is seen that for the first two cuts, the saw marks do not increase and are constant throughout the load. For these cuts, no saw mark is present and this measure gives the waviness instead. But at the third cut, the first wafers (i.e. the ones on the operator side, where the wire is the most worn) have larger saw marks than the wafers on the machine side of the load (that have a saw mark height comparable with the previous cuts). On the fourth cut, all the wafers have much higher saw marks than for the first cut and wafers on the operator side have, similar to the third cut, larger saw marks than wafers on the machine side.

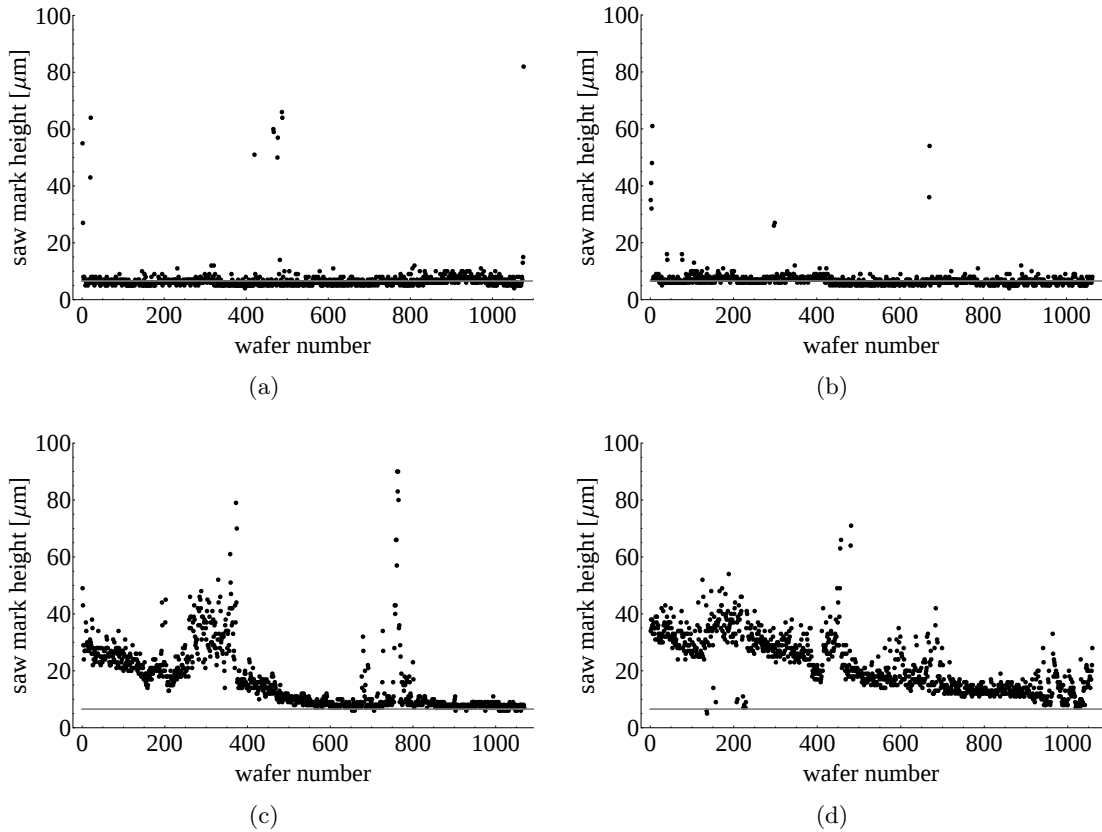


Figure 6.5: Saw mark height for a) the first cut (new slurry), b) second cut, c) third cut and d) fourth cut (highest debris amount). A grey line representing the median saw mark height of the first cut is plotted on each graph for comparison.

6.3 Roughness measurements

Figure 6.6 presents the wafer average roughness (R_a). When the slurry does not contain much debris, the roughness is highest at the wire entrance and decreases until around the middle of the wafer (Fig. 6.6(a)), after which it stays constant until the wire exit edge. The roughness does not evolve from the beginning to the end of the cut. In contrast, the wafers from the fourth cut (Fig. 6.6(d)) present the same decrease at the wire entrance side, but the roughness reaches a minimum and increases again towards the wire exit side. This last increase starts earlier at the end of the cut than at the beginning.

It is possible to measure the rate at which the roughness increases at the wire exit edge of the wafer between the position at 25 and at 105 mm (see the positions in Fig. 6.1). It is found that when cutting a silicon height of 80 mm (in the feed direction), the average roughness at the wire exit increases to 0.96 μm . Thus, if it is assumed that the saw marks start when the roughness at the wire exit increases to more than 0.41 μm (which is the minimum roughness when no saw mark is present), it follows that the saw marks appear after cutting a height of 408 mm (i.e. during the third cut, after having sawn 96 mm).

6.4 Fracture strength

From the measured breakage force and thickness, the fracture stress could be extracted and the breakage statistic calculated, as presented in Table 6.3. Figure 6.7 shows the Weibull plots of all four loads. It can be noticed that the first three loads have a comparable fracture strength, but the last cut has a much lower strength and a broad breakage stress distribution.

6.5 Discussion

From the results, the silicon debris effect can be separated in two phases: at a low concentration, the debris does not have a major impact on the wafer properties (TTV, roughness and

Table 6.3: *characteristic stress, Weibull modulus and adjusted coefficient of determination of the regression for the breakage tests.*

	σ_0 [MPa]	m	$\bar{R}^2$
1 st cut	146	17.4	0.958
2 nd cut	149	14.5	0.959
3 rd cut	143	15.5	0.987
4 th cut	89.5	7.26	0.969

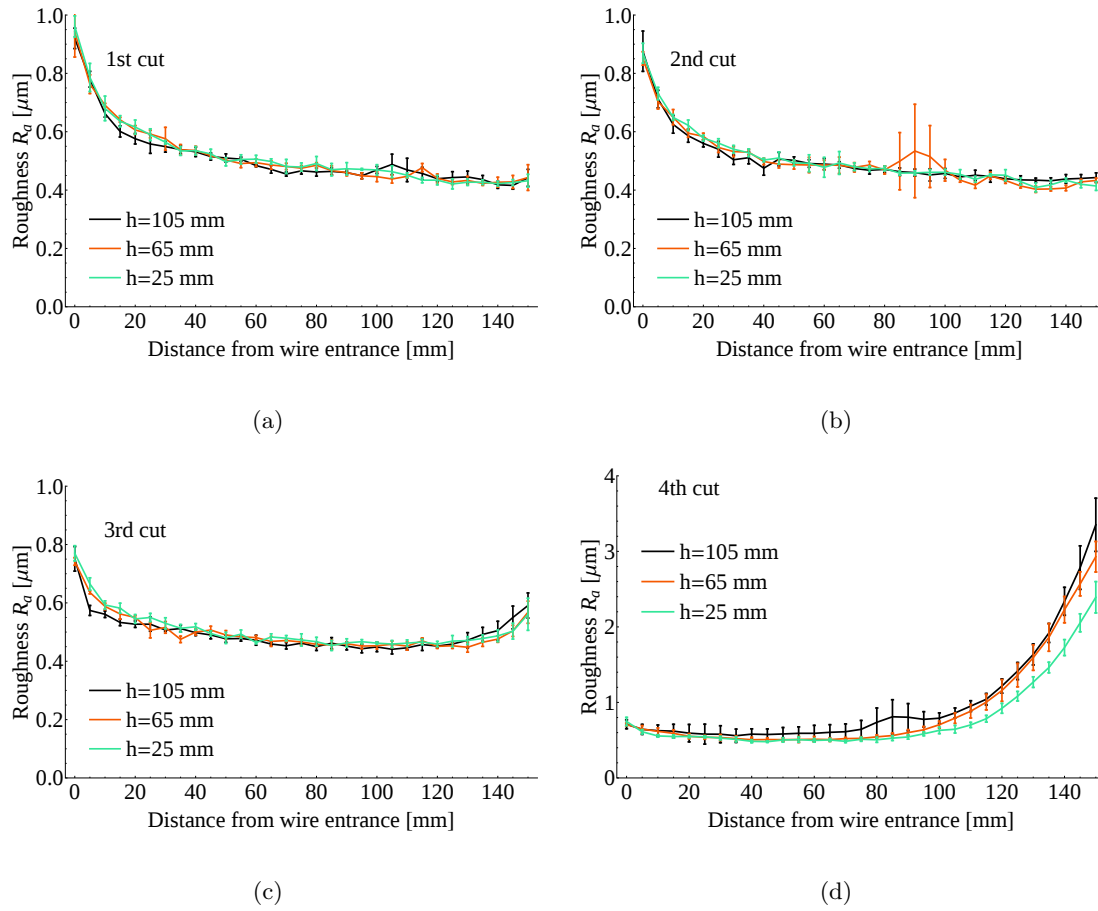


Figure 6.6: Wafer average roughness of a) the first cut, b) the second cut, c) the third cut) and d) the fourth cut. The yellow line is the roughness after 25 mm of sawing, and the orange and black are taken after more sawing (respectively 65 and 105 mm). The saw marks are visible from the third cut, but at that point, the roughness they induce is still lower than the roughness at the wire entrance. Note the different Y-axis scale of the fourth cut.

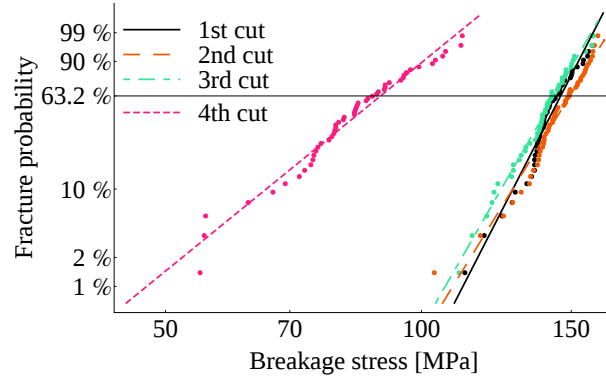


Figure 6.7: Weibull plots of the fracture stress from the four cuts. In black is the first load, in light grey the last one. The first three cuts have a comparable fracture strength, but the last cut (which has large saw marks) has a much lower fracture strength.

breakage strength). When the volume of debris has reached a critical level, saw marks appear, starting at the operator side of the brick, and progress towards the machine side. At the same time, the saw marks get longer and higher. The bending strength decrease is related to the roughness: as long as the average roughness at the wire exit edge is lower than the roughness at the entrance, the wafers do not show a significant strength reduction (see the third cut: small saw marks are present, the roughness increases at the exit edge but stays below the roughness at the entrance edge (Fig. 6.6(c)) and the wafers are as strong as the first two cuts, as shown in figure 6.7). Once the roughness at the exit side of the wafer is larger than at the entry side, the wafers become more fragile. It is worth noting that the roughness at the wire entrance does not depend on the amount of debris present in the slurry (Fig. 6.6).

It appears that the volume fraction of debris is of paramount importance to describe the apparition of saw marks. Assuming that the volume of debris is given by the kerf loss (equation 6.1), the critical volume fraction of debris is 15 % of the total particle volume. But, as the measurement of the wafers from the third cut shows, the transition is not sharp between a situation where no saw mark is present to one where every wafer has saw marks.

The apparition of saw marks is explained by the following mechanism: as the debris is much softer than the silicon carbide, it diminishes the cutting efficiency of the slurry by acting as “cushion” between the SiC particles and the silicon brick. Saw marks first appear at the exit edge of the brick because on the one hand, the abrasive particles are ejected from the sawing groove between the entry and the exit of the wire (see subsection 5.2.5), and on the other hand, the debris builds up at the wire exit. This makes the local debris fraction at the wire exit side of the groove much greater than the global debris fraction. Once a certain amount of debris is present in the slurry, the sawing cannot proceed as fast as required by the feed

rate (that is set in the sawing parameters). In turn, the wire bow increases and so does the pressure of the wire on the abrasive particles. When this pressure is large enough, the cutting mechanism changes to a more efficient mode. This makes the cutting speed go faster than the feed rate, diminishing the bow until the first (less efficient) sawing mechanism reappears. In such a sequence, the silicon is not cut at a constant speed but in fits and starts, giving rise to saw marks on the wafers. The point when the faster regime takes place depends on the wire pressure, so that the situation in one saw groove has an impact on the next grooves: when the silicon is sawn fast, it decreases the wire bow and, in consequence, lowers the pressure on the adjacent grooves (see figure 6.4: the saw marks are not regularly spaced and their position on one wafer side are not synchronised with the position on the other side). Because of the wire movement, this effect is more important on the groove after the place where the silicon is sawn faster (in the wire direction) than on the groove before. This explains why the saw marks appear first on the operator side, as small oscillations in the wire tension accumulate towards that end, until they are large enough to induce saw marks. Finally, the volume fraction of debris needed to create saw marks is low, because as the debris size is small, only a small volume fraction of debris is required for providing a large number of particles. Assuming that this model is valid, the volume fraction of SiC in the slurry should have an impact (if more particles can saw the silicon, it is possible that the slurry contains more debris before the saw marks appear), as well as the feed rate (if it is slower, the amount of debris has to be larger to slow the cutting enough).

6.6 Linking the impact of the wire-sawing parameters to the effects of silicon debris: a general picture of the sawing mechanisms

The silicon removal is made by SiC particles that are pressed by the wire into the silicon brick. These particles, by indenting, create cracks and roughness. This material removal occurs not only at the top of the sawing groove, but also on the groove sides. Different wear conditions are at work on these different positions, so that the wafer surface is not only the result of the conditions at the side of the groove, but also of everything that happened between the top of the groove and its side. One difference is that the surface at the top of the groove is made of facets and sharp edges, but the wafer surface has smoother edges. This is explained by the action of smaller particles on the side: as the effective sawing rate is lower at the side, the small particles — which have a low sawing efficiency — have time to make an impact on the surface topography, whereas their impact is invisible at the top of the groove (but this does

not mean that they are absent).

During the course of the wire through the groove, abrasive particles are being ejected under the wire. This produces an effective particle size diminution, and also a particle volume fraction diminution, as illustrated in figure 6.8. This particle size diminutions causes the roughness to decrease away from the wire entry side and the wafer thickness to increase, but after around the half of the wafer length, the particle size remains constant, and so does the roughness. However, the particle volume fraction keeps on decreasing, which is why the wafer thickness still increases, as the wire has more room to mend around the particles. The wire vibration outside the silicon are also causing a wafer thickness decrease, but this effect is only visible on the first and last few millimetres at the wafer edge. At the same time as the abrasive particle volume fraction decreases, silicon debris that were machined off the brick build up in the groove. This debris is lowering the slurry cutting efficiency. When too much debris is present in the slurry, the cutting efficiency drops too much to be able to cut silicon as fast as required by the saw feed-rate. When such a thing happens, the first area that is touched by the phenomena is near the wire exit (where the debris volume is highest and the amount of abrasive particles is the lowest). In such a case, the silicon is sawn in fits and stops: the wire is sawing slowly in the usual mode while the wire bow is increasing. The bow determines the wire pressure on the particles, so that when this pressure is too high, the sawing mechanism changes to a more efficient one (this is similar to what was observed by Adachi and Hutchings¹ for the micro-abrasion test: a 3-body to 2-body abrasion transition is observed when the applied pressure gets too large, see section 3.1) until the wire pressure decreases enough to turn back to the standard cutting mechanism. At the same time the mechanism does not change much at the groove side: the effective sawing speed is too low to create a mechanism change. Still, the sawing speed change produces thickness change, as it was also seen for sawing experiments without debris (Fig. 5.17). These thickness changes occur only where the change of sawing mechanism occurs: namely near the wire exit edge, producing saw-marks.

These saw-marks decrease the wafer strength, as it was expected from the saw-mark surface where large chips can be seen at their top. The same behaviour was seen on the cut made with F1200: small saw-marks were seen on the whole wafer length, not only near the wire exit edge. In this case, the saw-marks were presumably due to the small abrasive size (3 μm) that is too small to cut silicon at the speed required by the feed rate, no matter the amount of debris. These wafers are in turn more brittle than wafers cut with F800, and have a low Weibull modulus (i.e. a large breakage stress dispersion, Fig. 5.2(c)). These are the same characteristics as the wafers with large saw marks caused by silicon debris (Fig. 6.7).

A semi-analytical model predicting the wafer strength from the sawing parameters has

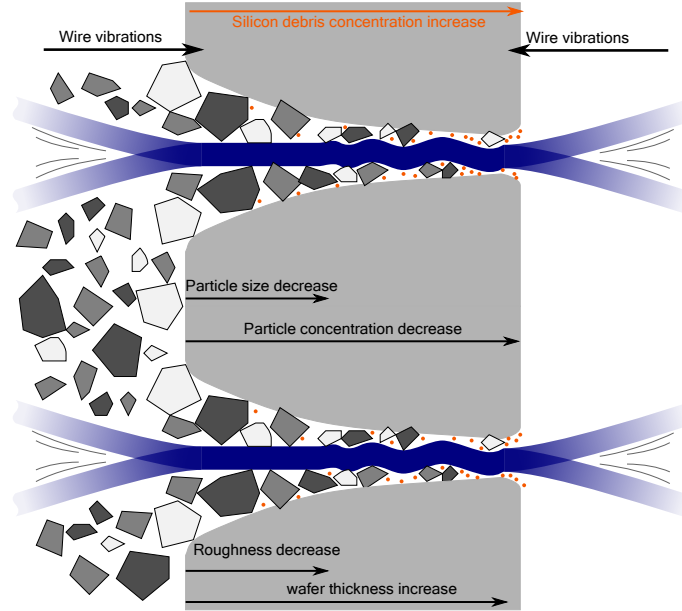


Figure 6.8: Schematic picture of the sawing mechanism. The wire vibration causes wafer thickness near to the wire entrance and exit edges. The particle size decreases induces a roughness decrease and a wafer thickness increases until around the first half of the wafer length and the abrasive volume fraction decreases cause a wafer thickness increase as the wire has more room to bend around the particles. At the same time, the volume fraction of debris increases towards the wire exit edge, which cause the sawing process to be less efficient, and can lead to the apparition of saw marks near that edge if the amount of debris is too important. The effect of particles on the wire entrance edge should also not be forgotten: as shown on figure 4.2(a), the particles projected on the silicon brick are polishing this edge, smoothing the trace of chips and of grinding lines that are still apparent on the wire exit edge of the wafers (Fig. 4.2(b)). For the sake of clarity, the effects described have been exaggerated.

been developed. It is based on meaningful interactions of the abrasive with the silicon and the wire. It was found that the abrasive volume fraction plays an important role in determining the wafer strength and is involved in most of the different mechanisms, acting in such a way that the parameters are entwined together, making it harder to decipher their respective roles. It was found that the sawing parameters influence increases when a thinner abrasive is used, and that fitting the model to wafers sawn with F600 gives different results than when it is fitted with wafers sawn with F800. Finally, it was found that the optimal parameters depend on the wafer properties required (e.g. if the most important factor is to have all the wafers with the same thickness, the sawing parameters are different than if the aim is to have a high mechanical strength).

In the next chapter, an emerging wafering process is presented: the diamond-plated wire-sawing. The wafers sawn with a diamond-plated wire are characterised and compared to

slurry-sawn wafers. The main difference is the presence of long grooves and of an important quantity of amorphous silicon, which is related to the fundamental scratching and indenting of silicon presented in chapter [2](#). Finally, the effect of the wafer surface on the subsequent solar cell production is analysed.

Chapter 7

Diamond plated wire-sawing

Recently, diamond-plated wire-sawing has become an alternative to the standard slurry sawing. It has several advantages such as a faster sawing rate, the use of a simple cooling fluid instead of an abrasive suspension, and the possibility to use the wire many times. But this technology is (in 2010) at the beginning of its deployment in the PV industry and improvements are needed to reach a competitive wafering cost. As diamond-wire sawing and slurry sawing are very different, a fundamental understanding of the diamond-wire sawing process is needed to reach its full potential. The differences in sawing methods start with how the silicon is removed by the wire, and in turn, most of the wafer properties, as they are defined for the slurry sawn wafers, have to be redefined.

The goal of this chapter is to give an overview of this new technology and to present some results obtained by diamond-wire wafer sawing. Hence, a first characterisation of diamond-plated wire sawn wafers is attempted. It is only a first study of the diamond-wire sawn wafer and some analysis are missing, the most obvious being bending tests. However, important differences with slurry-sawn wafers are pointed out and new investigation tools adapted for the diamond-wire sawn wafers are presented. A first model of the sawing process is proposed. It is found that the wafer surface is made of very long features created by the diamond particles scratching the silicon. On these scratches, important amounts of amorphous silicon are present, but crystalline silicon is visible where chips interrupt the scratches. The geometrical properties (roughness and TTV) are found to be comparable with those from slurry sawn wafers, or even better. Then, the wafers have been processed into solar cells and their efficiency is measured to be equal to the cells made from slurry sawn wafers. Finally, a second type of diamond-wire sawn wafers that has a faster etching rate is analysed and compared to the original diamond-wire sawn wafers.

7.1 Principle of diamond-plate sawing

A diamond-plated wire is essentially a thin steel wire (like the one used for slurry sawing, only slightly thinner) on which diamond particles have been attached. There are several ways to do this: mechanically embedding the diamonds into the wire, gluing them with a resin⁷⁴ (Fig. 7.1), or with a nickel-plated layer²³. With the diamond particles, the average wire diameter is larger than the slurry wire. However, as there is no particle in the cooling liquid, the kerf loss is hardly larger compared to slurry sawing. The diamond-plated wire is much more expensive than standard steel wire and much more difficult to produce. In consequence, the amount of wire on a spool is only 100–200 km²³, but the wire wears much slower than standard wire, so that it can be used for many cuts, before it needs to be changed. The cooling liquid is much easier to handle than standard slurry, as there are no abrasive particles in suspension. This also makes the recycling much easier: all particles have to be removed from the liquid, in contrast to standard slurry where the fine silicon debris has to be removed, but the coarser SiC particles have to be kept, and the recycled slurry has to have a precisely defined density.

Apart from a few modifications, a standard saw can be used with a diamond-plated wire²³. The most important modifications are made to accommodate the cooling fluid and to have a better control of the wire winding to sustain the multiple back-and-forth movements²³. In contrast to slurry sawing, diamond-plated sawing allows a faster cutting speed (2.5–3 times faster)⁷⁴. Furthermore, machine downtime is reduced as the wire can be used for many cuts before having to be changed.

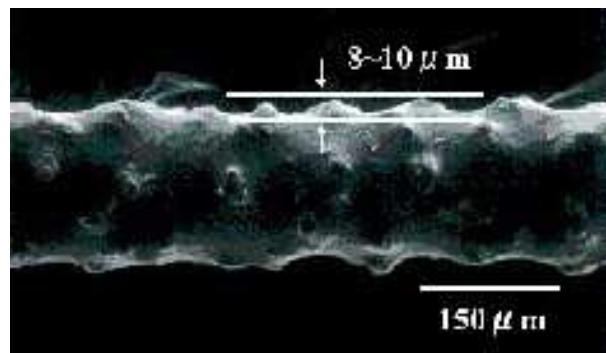


Figure 7.1: SEM picture of a new wire where the abrasive particles were bonded with a resin to the wire. After Kondo et al⁷⁴.

7.2 Wafer surface

7.2.1 Wafer topography

A photograph of a diamond-wire sawn wafer is shown in figure 7.2. Scratches can even be seen with the naked eye, and a succession of bright and dark areas extending over several millimetres width can be observed on the whole area. On a microscopic scale, the wafer surface produced with a diamond wire is fundamentally different than one obtained with SiC slurry (Fig. 7.3): the smooth grooves made by the diamond particles are clearly visible. Sometimes, these grooves are interrupted by rougher areas where the silicon chipped off.

These smooth grooves seem to have been plastically deformed (section 2.3), as it is the case

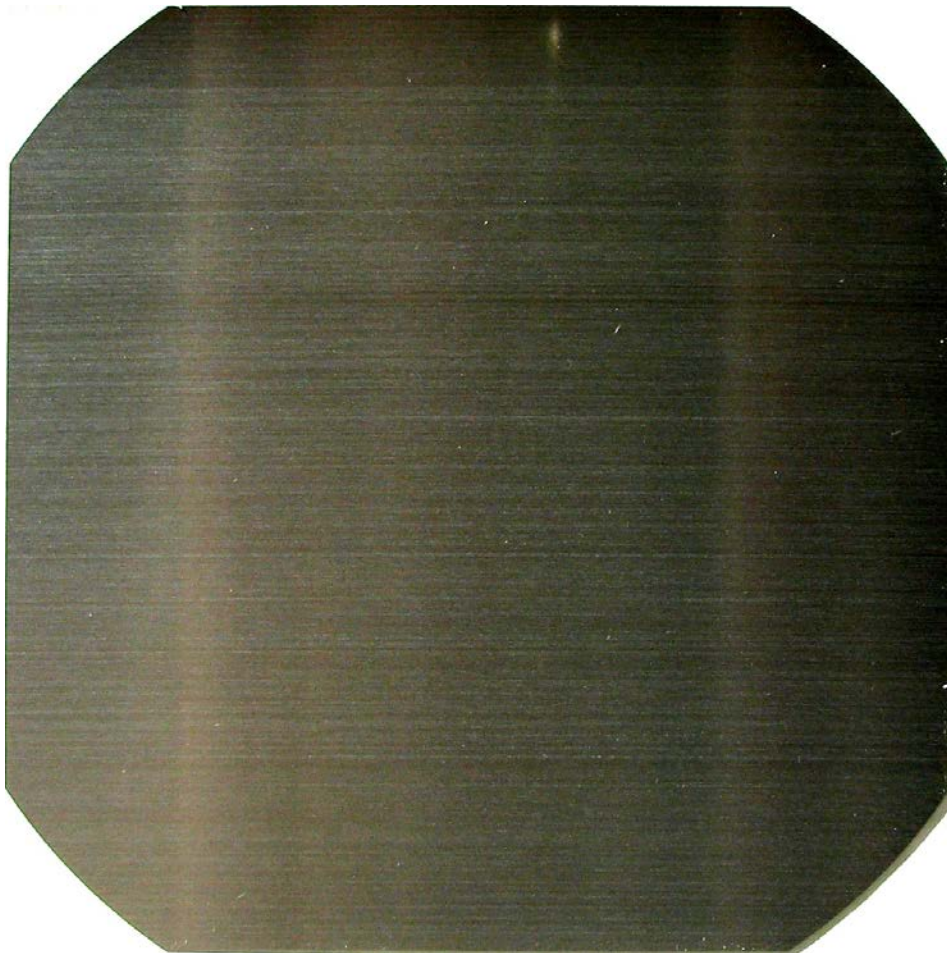


Figure 7.2: Photograph of a diamond-wire sawn wafer. Scratches along the whole wafer surface can be seen, as well as brighter and darker regions. The wafer size is $125 \times 125 \text{ mm}^2$.

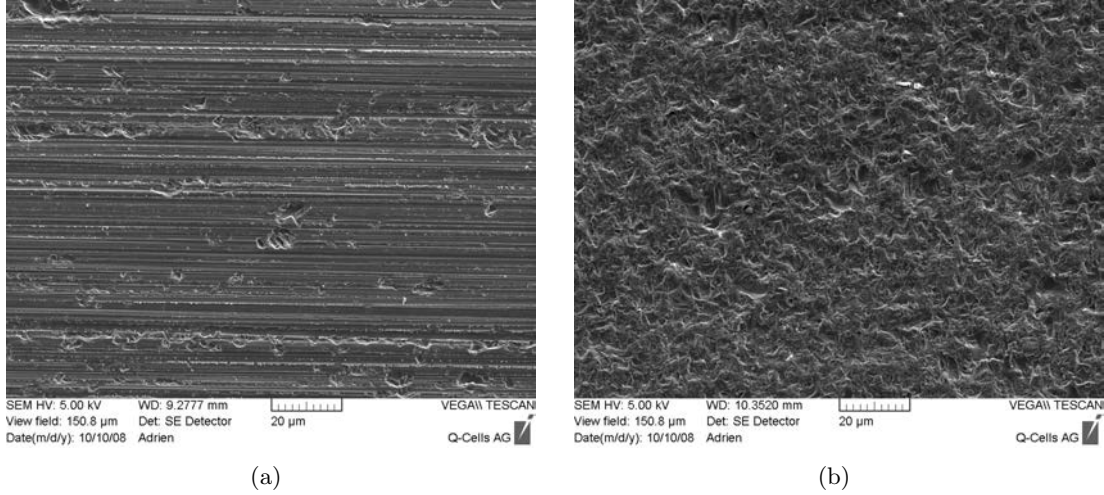


Figure 7.3: (a) SEM micrography of a diamond-wire sawn wafer surface. Long scratches can be seen, sometimes interrupted by chips. The scratches are in the direction of the wire during sawing. They are smooth, suggesting that plastic deformation occurred. (b) SEM micrography of a slurry sawn wafer surface. The surface is rough and the sawing direction is not noticeable.

when scratching silicon at low load⁴⁴. This would imply that a phase transformation occurred during the sawing, therefore that amorphous silicon or meta-stable phases are present at the wafer surface. Indeed, a Raman spectroscopy map of the surface confirmed the presence of amorphous silicon (Fig. 7.4). It is seen that the smooth grooves (Fig. 7.5(a)) are made mostly of amorphous silicon, with some small content of meta-stable Si-XII, Si-III and stable Si-I. In contrast, the chipped-off regions are made of Si-I only (Fig. 7.5(b)). To produce such a map, spectra were recorded for 2×20 seconds. The laser used had a wavelength of 514 nm and a power of 900 mW. Filters were used to reduce this power to 30 % in order to avoid recrystallisation of amorphous silicon by the laser. The space between measurement points was 2 μm . After the measurement, the spectra were flattened and smoothed. The peaks were then fitted with a combination of three distributions: a Cauchy distribution for the Si-I phase, and a normal and a Cauchy distribution for the amorphous phase. The amount of amorphous silicon was calculated as the ratio of the area under the two distributions describing the amorphous silicon to the total fitted area.

It is possible to quantify the fraction area of chips by optical microscopy in order to have a more representative measurement of the crystalline silicon surface fraction. To do so, micrographs were taken with differential interferometry contrast (Fig. 7.6). Only the blue component of the images were taken. The images were then filtered with a bandpass filter removing horizontal lines, the structures larger than 116 μm and smaller than 0.65 μm . Then,

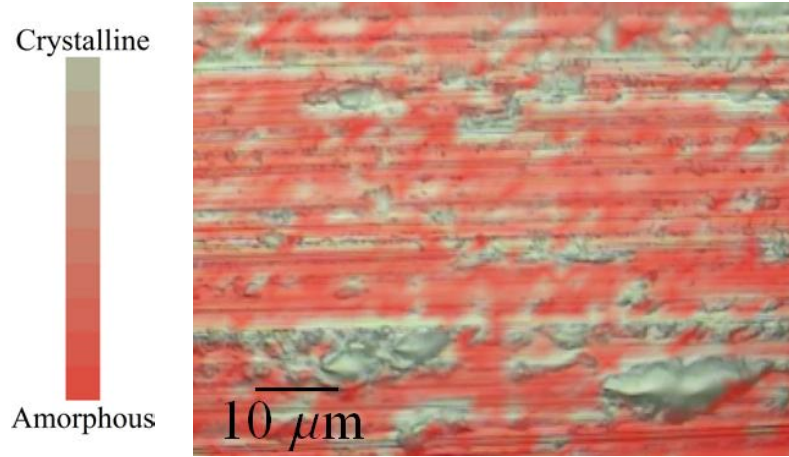


Figure 7.4: Map of the amount of amorphous silicon found on a wafer superposed to the corresponding optical microscopy micrograph of the region. The red intensity represents the amount of amorphous silicon. It can be seen that the smooth grooves are mostly amorphous and the chipped-off regions are purely crystalline.

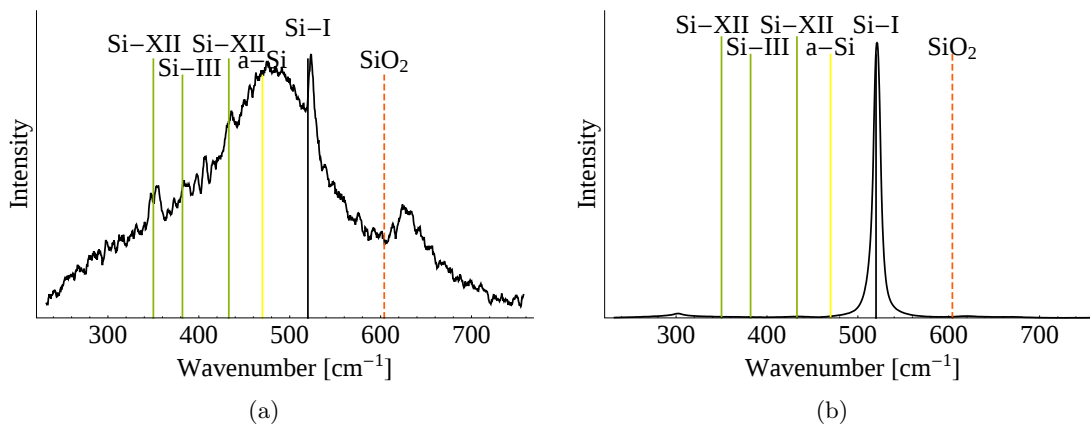


Figure 7.5: (a) Raman spectrum taken on a smooth groove of the surface of a diamond-wire sawn wafer. (b) Raman spectrum of a chipped-off region. The chipped-off region shows only diamond lattice Si-I, but the grooves region shows a mixture of Si-I and metastable Si-III, Si-XII and amorphous Si. The relative amount of amorphous and metastable silicon varies from point to point.

a Gaussian blur was applied with a radius of $0.26\text{ }\mu\text{m}$. On a wafer, 20 micrographs were analysed. It was found that the surface fraction of chips is 16.4 % with a standard deviation from picture-to-picture of 3.7 %. As a comparison, the surface fraction found with Raman spectrometry is 19.2 %, in reasonable agreement with the optical microscopy measurement. It can be seen in figure 7.6 that the smallest chips are not taken into account because of the filtering. But these chips are small and do not have much impact on the calculated crystalline surface fraction.

The amorphous layer does not have a constant thickness, even at a groove scale: as for nano-scratching, more amorphous silicon is found at the centre of the groove than at its side. A higher resolution map of a few grooves was made. For this, a $250\times$ objective was used and the laser intensity was reduced to 15 % of its original power. A recording time of 2×60 seconds per point was used and a step size of 300 nm was chosen. The amount of amorphous silicon is presented in figure 7.7(b). It is seen that on the groove edges, the amount of amorphous silicon is much lower than at the centre (where only amorphous silicon could be measured).

Thus, the wafer surface can be described as follows: on a scale of a few millimetres, small differences in the sawing process create lighter and darker areas (Fig. 7.2). On a micrometre scale, scratches are seen, interrupted by chips (Fig. 7.3(a)). The scratches are mainly covered with amorphous silicon, whereas the chips show crystalline silicon. The scratches are not homogeneous, though: a thicker amorphous silicon layer is present at their centre than near

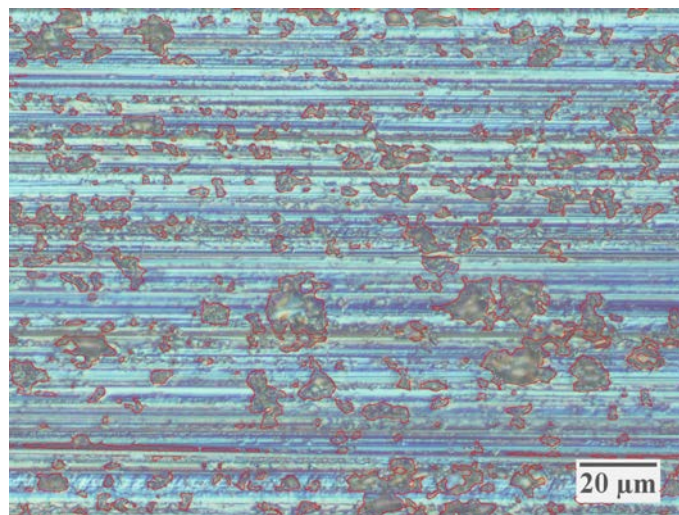


Figure 7.6: Optical micrograph of a diamond-wire sawn wafer surface. The picture is taken with differential interference contrast, so that there is a better contrast between the grooves and the chips. The chips as selected after filtering and thresholding the picture are circled in red.

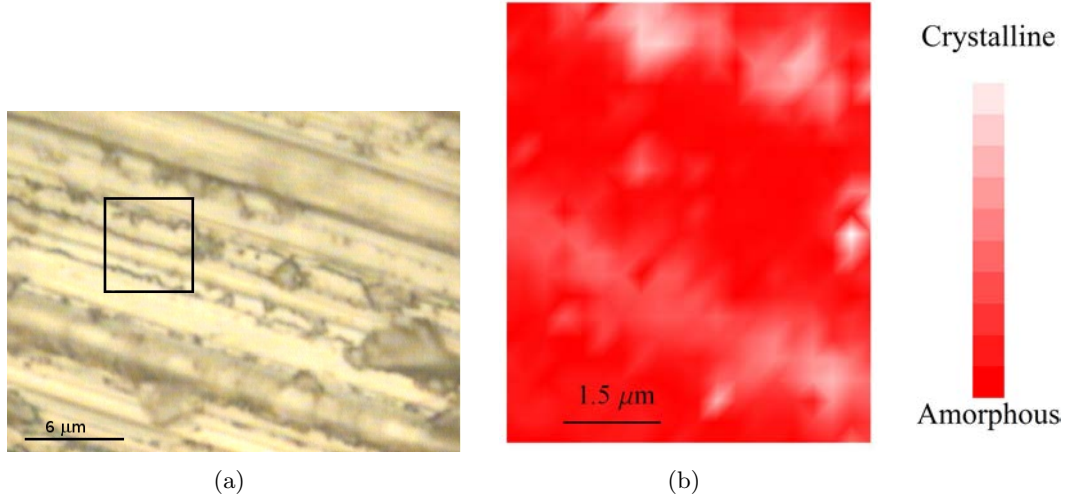


Figure 7.7: (a) Optical microscope image of the wafer surface. The area mapped with Raman spectroscopy is framed. (b) Raman map of the amorphous silicon thickness

their edges (Fig. 7.7(b)). Furthermore, there are small chips ($\ll 1 \mu\text{m}^2$) that are too small to be resolved by Raman spectroscopy or by optical microscopy on the scratch edges that seem to be crystalline, or only covered with a thin amorphous layer.

7.2.2 Internal stress

From the Raman measurements, it is also possible to extract the stress in the crystalline silicon (see section 4.7). For a plane stress, the Raman shift is given by the equation²⁹ (4.5). Figure 7.8 presents the stress state of the crystalline silicon under the wafer surface. It is important to note that this stress is not the one of the surface layer (which is amorphous, thus having a peak at another wavenumber that has a different sensibility to stress), but the stress of the crystalline silicon underneath. The measured median stress is -325 MPa (in compression) and the highest stress measured is larger than 1 GPa , both in tension and compression. The regions under high stress (either compressive or tensile) are near chips. The largest chips do not show larger stress than smaller chips. Indeed, it seems that small chips have the largest effect on the stress.

Assuming that the monocrystalline silicon ingot has no internal stress prior to cutting, the measured stress has to come from the sawing process. This can be explained by taking into account that the phase transformations induce volume change: the Si-II phase is 23.7 % more dense than Si-I and amorphous silicon has approximately the same density as Si-I. The Si-II phase is known to be ductile (see subsection 2.3.2), so that the Si-I to Si-II volume

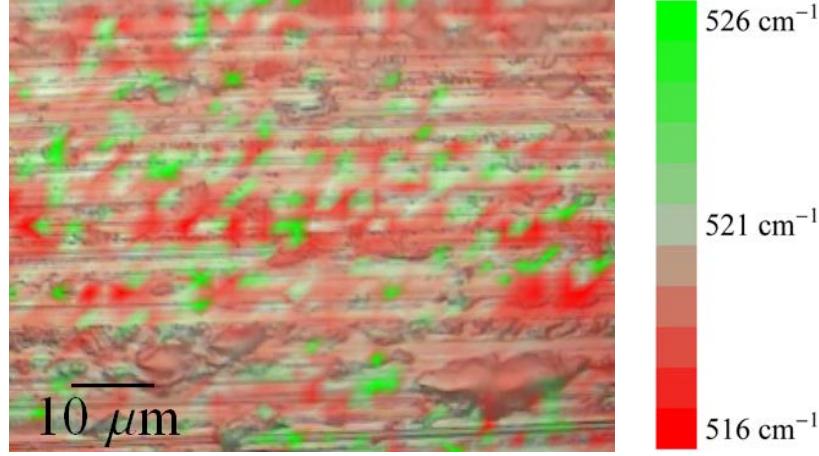


Figure 7.8: Stress on a diamond-wire sawn wafer surface. The red indicates compression and the green tension. The colour intensity indicates of the stress level.

change is accommodated by plasticity. But the following Si-II to a-Si transformation results in a lower density phase that is not known for its plasticity so that the stress created during this transformation is not relaxed. Thus, this stress is the one measured on the wafer surface. To transform Si-I into Si-II, the Si-I crystal lattice is dilated in the $[100]$ and $[010]$ directions and heavily compressed in the $[001]$ direction⁷⁰. The transformation from Si-II to amorphous silicon will likely require a reduction of the inter-atomic spacing, so that there is a compression in the original $[100]$ and $[010]$ directions of the Si-I crystal lattice, inducing a tensile stress in the amorphous layer (and a compressive stress in the underlying Si-I bulk). But as the amorphous Raman peak is wide and much less clearly delimited than the Si-I peak, it is not possible to evaluate precisely its position and to use it for stress measurements.

It is also possible to determine the stress with electron back-scattered diffraction (EBSD) by measuring distortions of the Kikuchi pattern. Such a method cannot be used on the wafer surface, because the amorphous layer is too thick and its surface too rough to obtain a clear pattern from the crystalline silicon underneath. Consequently, the wafers were cleaved and their cross-section analysed. As defects under the wafers surface were preventing the silicon from cleaving along a well-defined plane, the samples were then polished. Such a preparation method was chosen as it makes a surface adapted to EBSD measurements, but even if silicon is hard and great care was taken for preparing the surface, it may have been slightly deformed, so that artefacts may be observed. Furthermore, the stress in the observation direction x_3 (as determined in Fig. 7.9(a)) cannot be calculated by this method, so that the only stresses measurable are in a direction normal to the wafer surface (direction x_1 in figure 7.9(a)) and

parallel to the direction defined by the cleaving plane and the wafer surface (direction x_2 in figure 7.9(a)). A stress profile from the first 20 μm below the surface is shown in figure 7.9(b). It is seen that, on the contrary to what is expected, the stress σ_{11} along the x_1 axis is in the order of -100 to -300 MPa in the first 5 μm . Such a stress level cannot be explained by the action of a stressed amorphous layer on the wafer surface and may be an artefact. Nevertheless, the stress σ_{22} is in compression and with a value around -300 MPa at the surface. This stress then decreases exponentially as the distance from the surface increases and is negligible at a depth around 2 μm .

The presence of important σ_{11} stress under the wafer surface can come from dislocations. As is was seen in Chapter 2, silicon scratching not only induces phase transformation, but also dislocation creation. These dislocations are then trapped underneath the sample surface and induce stress in the silicon. As expected from the Raman measurement taken on the wafer surface, the stress field changes from one point to the other, some regions showing larger stress along the x_2 and others along the x_1 direction.

The same measurement can be carried out with Raman spectroscopy. However, the size of the laser beam prevents measuring the stress near the wafer edge. The Raman measurement probes a much deeper volume of silicon than the EBSD, so that the sample preparation does not create artefacts. But it is impossible to extract the complete stress field from such a

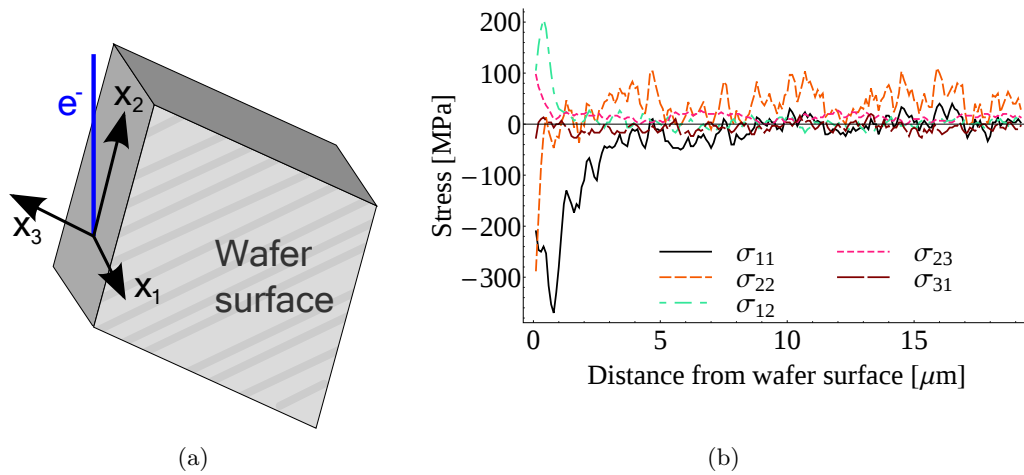


Figure 7.9: (a) Schematic view of the observed sample with the axes orientations. (b) Stress measured by EBSD depending on the position from the wafer surface. The stress σ_{33} is not plotted because it is impossible to measure it by EBSD. Some artefacts were not removed when the stress was calculated, as a linear variation of a stress component (e.g. σ_{23} is likely to be negligible on the whole measured area) and have to be taken into account when analysing the results.

sample, only an average stress value. For a stress field in the $0x_1x_2$ plane, the equation (4.5) prevails. On the other hand, for a stress in the $0x_2x_3$ plane, the Raman shift is given by the equation²⁹:

$$\Delta\omega[\text{cm}^{-1}] = -1.9 \cdot 10^{-9}\sigma_{22}[\text{Pa}] - 0.7 \cdot 10^{-9}\sigma_{33}[\text{Pa}] \approx -2.6 \cdot 10^{-9}\sigma_{22}[\text{Pa}] \quad (7.1)$$

if σ_{22} and σ_{33} are taken as equal (a reasonable assumption given that the scratches are bisecting the angle formed by x_2 and x_3). An example of such a measurement is shown in Figure 7.10. From this type of measurements, it is found that the highest compressive stress measured by Raman spectroscopy is larger than -700 MPa, with a mean stress at the wafer surface of -425 MPa (this stress is -357 MPa if the stress is assumed to be in the $0x_1x_2$ plane).

The difference with the values measured from the wafer surface are due to the fact that the wafer is heterogeneous, so that the stress varies from one place to the other, as observed from both the wafer surface (Fig. 7.8) and the wafer cross-section (Fig. 7.10(a)). Furthermore, some stress relaxation could have occurred and artefacts may have been introduced during the sample preparation.

The exponential stress decrease is compatible with the assumption that the stress is caused both by the amorphous silicon layer and by the dislocations. Indeed, the dislocations may stay close to the wafer surface, but the induced stress field extends on much larger distance,

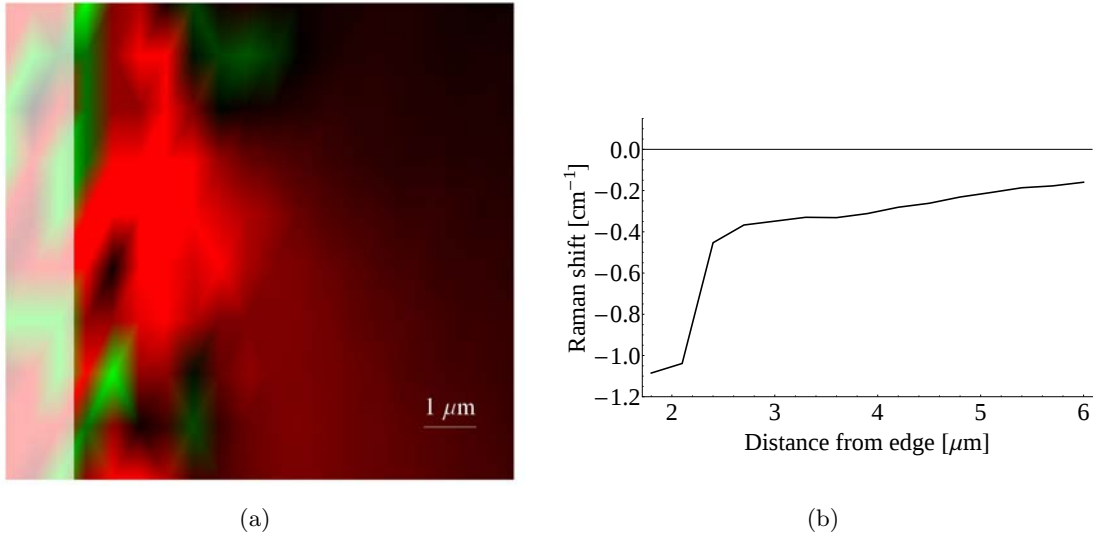


Figure 7.10: (a) Stress measured by Raman spectroscopy on the wafer section. The red colour indicates compressive stress and the green tensile stress. (b) Average Raman shift measured in respect to the distance from the wafer surface.

as the stress created by a surface layer goes deep under the sample surface. Nevertheless, the amorphous layer should be in traction, whereas the crystalline silicon is in compression. Such a stress difference between the amorphous layer and the crystalline silicon might be responsible for crack occurrence at the interface. This situation is observed on cross-sections of intentionally scratched samples, as shown in figure 7.11(a) and 7.11(b). The observation of an as-sawn wafer cross-section (Fig. 7.11(c) and 7.11(d)) reveals that some regions present delamination, although no generalised delamination of the amorphous layer is observed. Furthermore, only few sub-surface cracks are visible, whereas the scratched sample shows clear median and lateral cracks. The fact that few visible cracks are present under the diamond-wire sawn surface is not surprising: as the crystalline silicon is in compression, cracks are closed and the only visible feature giving a hint of their presence is the perturbed cross-section area near the wafer surface.

The stress in the amorphous layer cannot be sustained on a large scale: assuming that it comes from a volume change, the larger the area without chip to allow for a stress release, the larger the tensile stress. However, this stress reaches a limit level: either the tensile stress in the amorphous layer is too important and cracks appear in it, or the shear stress in the crystalline silicon gets high enough to allow the creation of dislocations leading to stress relaxation via plastic deformation.

Despite most of the crystalline silicon being in compressive stress, some regions are in tensile stress. This might be explained by the presence of cracks through the amorphous layer. In such a case, the stress in the bulk silicon is also released and it may be possible that some parts of the crystalline silicon end up being in tension whereas most of it is in compression. This situation is found at chips: they can be thought as being large cracks through the amorphous layer, releasing the stress where no amorphous layer is present, so that tensile stress can be present in the crystalline silicon under the interface between the chip and the amorphous layer.

Apart from the amorphous silicon, the long grooves on the surface indicate that the diamond particles had a long contact time with the silicon. Thus, diamonds might have been heated up enough by the scratching to induce a silicon oxide layer larger than the natural oxide on the wafer surface. EDX measurements were carried out to measure the oxide film thickness. A low accelerating voltage (3 kV) was used to increase the surface sensitivity, at the price of a lower detection rate. Spectra taken from a smooth groove and from a chipped-off region on a diamond-wire sawn wafer are shown in figure 7.12(a). The silicon peak (at 1.8 kV) is clearly seen, as well as the oxygen peak (at 0.5 kV) and the carbon peak (at 0.25 kV). The carbon peak comes from surface contamination and is strong even if the amount of carbon present is small. These spectra can be compared with measurements done on slurry sawn

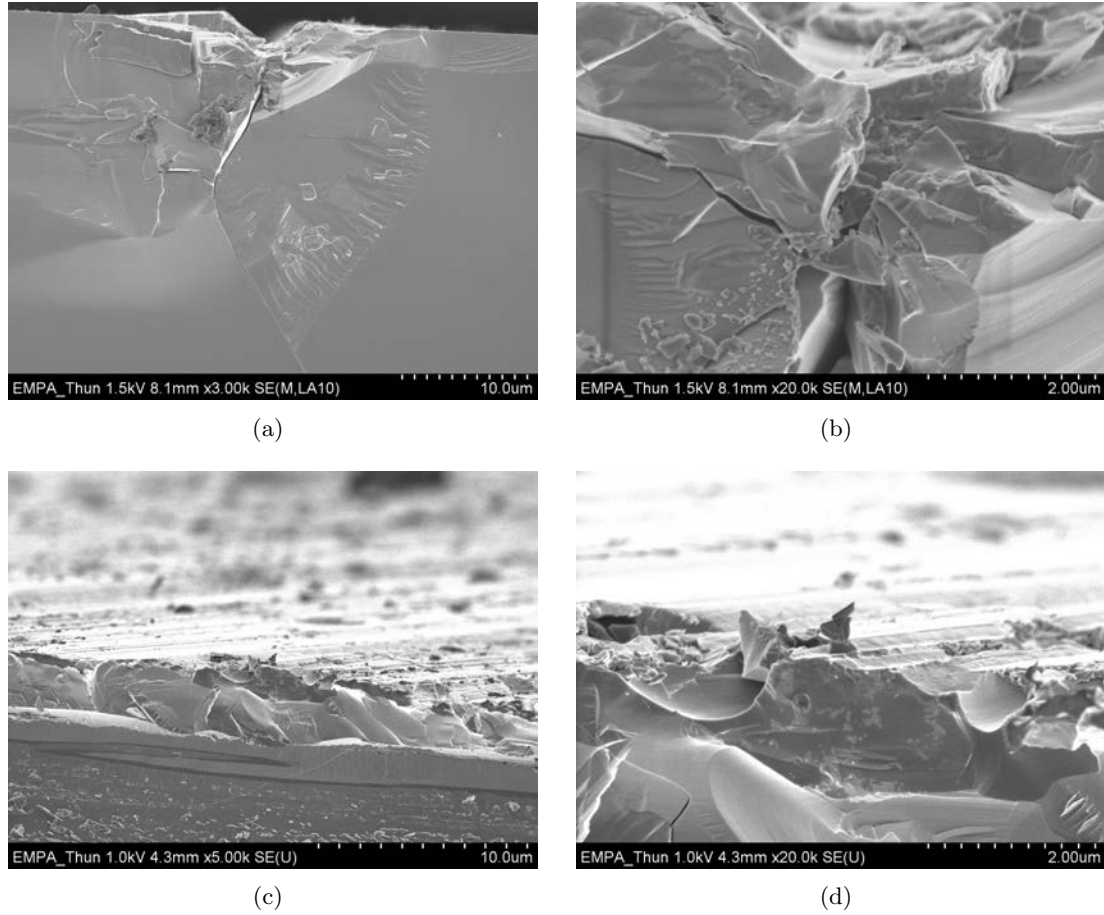


Figure 7.11: (a) Cross-section of a scratch on a (001) wafer. The normal force was 200 mN, the scratch speed was 0.16 mm/sec and the tip was a cone with an apex angle of 90° and a radius of $2\text{ }\mu\text{m}$. (b) Higher magnification of the scratch: cracks are present at the interface between the heavily deformed layer and the silicon bulk. This layer is around 300 nm thick. It is seen that the amorphous layer is separated from the bulk by cracks. Furthermore, median and lateral cracks are visible. (c) Diamond-wire sawn wafer cross-section. The wafer surface is on the top of the picture and the bulk on the bottom. Scratches are observed, with some chips. (d) Zoom on the cross-section edge. Some parts of the amorphous layer seem delaminated on both edges of the image, but only a few cracks are present under the surface.

wafers (Fig. 7.12(b)). The ratio of the oxygen peak to the silicon peak is comparable for both type of wafers, indicating that the oxide layer thicknesses are comparable, measuring around 1–2 nm.

7.2.3 Thickness and roughness

As the diamond abrasive is bound to the wire, the roughness of the wafer does not change much between the wire entrance and exit and is around 0.45 μm , i.e. slightly lower than the lowest roughness of slurry sawn wafers (Fig. 7.13(a)). Despite that, the roughness standard deviation is larger for the diamond-wire sawn wafers than for the slurry sawn wafers. But roughness cannot be easily compared between both wafer types, as the sawing mechanism is fundamentally different: the diamond-wire cuts the wafers in a two-body abrasion process whereas the slurry cutting is a three-body abrasion process (see section 3.1).

The wafer thickness shows the same tendency as the roughness (Fig. 7.13(b)). As the diamond particles are bound to the wire, there is no significant thickness difference between the wire entrance and exit. On the direction perpendicular to the wire, the thickness variation is larger than parallel to the wire. One possible explanation, among other things, is that the wire diameter changes or that the size of the diamond particles change. But such a variation has to appear over several kilometres of wire, which emphasize the importance of controlling tightly the wire quality to have a better wafer quality.

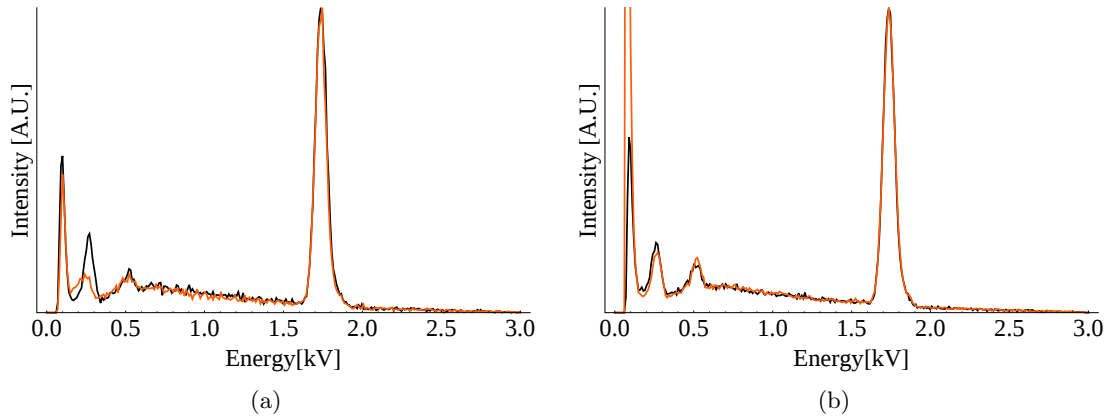


Figure 7.12: (a) EDX spectra of a diamond sawn wafer taken at a chipped-off region (in orange) and at a chipped-off region (in black). (b) Spectra of a slurry sawn wafer. Two spectra have been superposed, showing the variation in oxygen peak intensity, this the variation on the oxide layer thickness. For the diamond-wire sawn wafers, the oxygen peak is slightly larger on the groove than on the chipped-off region, but both spectra are comparable, in term of the amount of oxygen found, with the spectra taken on the slurry sawn wafer.

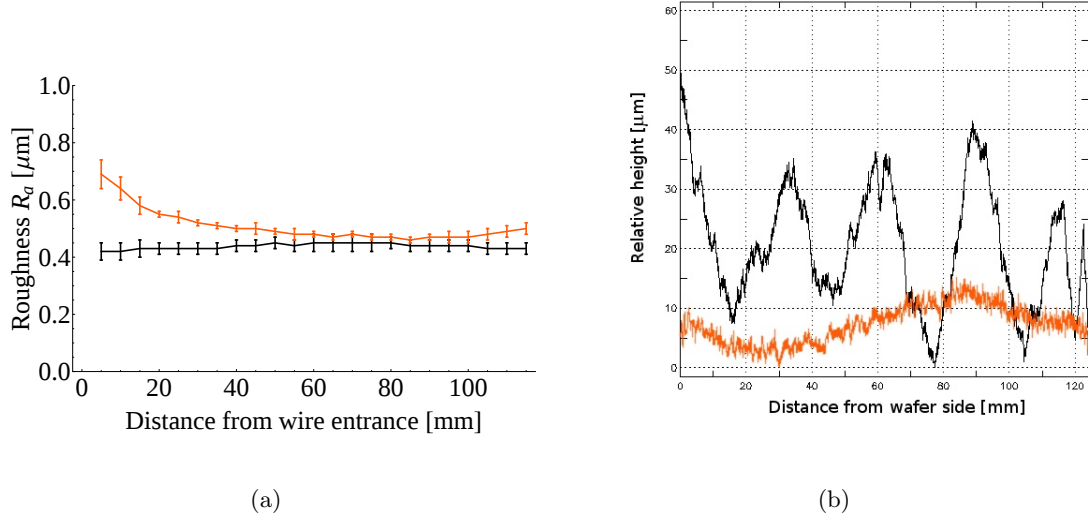


Figure 7.13: (a) Roughness evolution of a diamond-wire sawn wafer between the entrance and exit of the wire (in black). For comparison, the same measurement done on a slurry sawn wafer is shown in orange. In contrast with the slurry sawn wafers, the roughness of the diamond-wire sawn wafer is not evolving between the two edges of the wafer, but the standard deviation is larger. Five wafers were measured for both type of wafers. (b) Thickness variation of a diamond-wire sawn wafer: parallel to the wire in orange and perpendicular to it in black. The thickness variation is small parallel to the wire, but much larger than for the slurry sawn wafers perpendicular to it.

7.3 Solar cell processing

One of the first solar cell production steps is to etch the wafers to remove the sawing defects and to add a texture. On mono-crystalline wafers, this is done with an (anisotropic) alkaline etching which forms pyramids with $\{111\}$ faces on the surface. The texture defines the light-trapping properties of the cell, a good texture being required to have a good cell efficiency. The diamond-wire sawn wafers were etched and produced with the standard Q-Cells SE process to check the ability of these wafers to produce solar cells. After etching the diamond-wire sawn wafers together with reference slurry-sawn wafers, it turned out that the diamond-wire wafer thickness decreased only one third of what was expected. Slurry sawn wafers, in comparison, were etched the right amount (Fig. 7.14). The diamond-wire sawn wafers had too small a texture, reflecting light too much. A second run of the same etching process was required to etch the wafers enough and to obtain similar optical properties.

There are two possible explanations for the slower etch rate of diamond-wire sawn wafers. First, the lubricant used for sawing was not properly removed during the cleaning step prior to

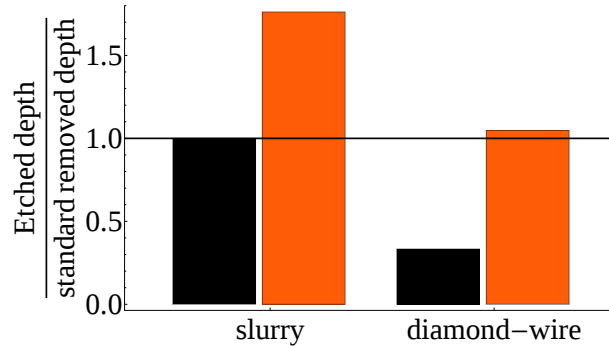


Figure 7.14: Relative etched thickness of diamond-wire and slurry sawn wafers. After the standard etching time (in black), the diamond-wire sawn wafers were etched only one third of what was expected. After a second etching run (in orange), the diamond-wire wafers were etched enough to have an efficient texture.

etching. This is possible, as the lubricant is different from the one used for slurry sawing and a small amount of molecules adsorbed at the surface can have a dramatic effect on etching rate. The other explanation comes from the presence of scratches and the amorphous silicon they are covered with. The impact of amorphous silicon on etching speed has been studied within the framework of micro-machining for MEMS applications, either aimed at using scratches as masks^{71,94,125} in KOH etching or aimed at using them as favoured etching sites⁴⁴ in HF etching or electrochemical etching. Park *et al* first demonstrated the masking potential of scratched silicon in 2004⁹⁴ by scratching a (1 0 0) wafer with a special AFM tip made of diamond. They first postulated that scratching induced the creation of an oxide layer acting as a mask, but later stated that the layer formed was only amorphous silicon⁷¹ after running a chemical and TEM analysis of the formed layer. Youn and Kang¹²⁵ observed the same phenomenon, but only stated that both mechanisms (thicker oxide or amorphous layer) were possible, without indicating which one was likelier to happen.

The difference between the diamond-wire sawn wafers and the structures studied for MEMS applications resides in the layer thickness involved: for the nano-scratching experiments, an amorphous layer of approximately 20 nm was employed as a mask whereas the amorphous layer found on the wafers is more than 100 nm thick. As the question of incorporating an important amount of oxygen in a 20 nm thick layer is relevant, the EDX measurements carried out on the wafer indicated that the amount of oxygen is insufficient to act as a mask (Fig. 7.12), *ergo* that the amorphous silicon prevents the crystalline silicon from being etched. In contrast, the chipped-off regions provides a crystalline surface that is quicker to etch and explains the structure found on partly etched wafers, Fig. 7.15(a).

When the diamond-wire sawn wafers were etched twice as long, the removed silicon thick-

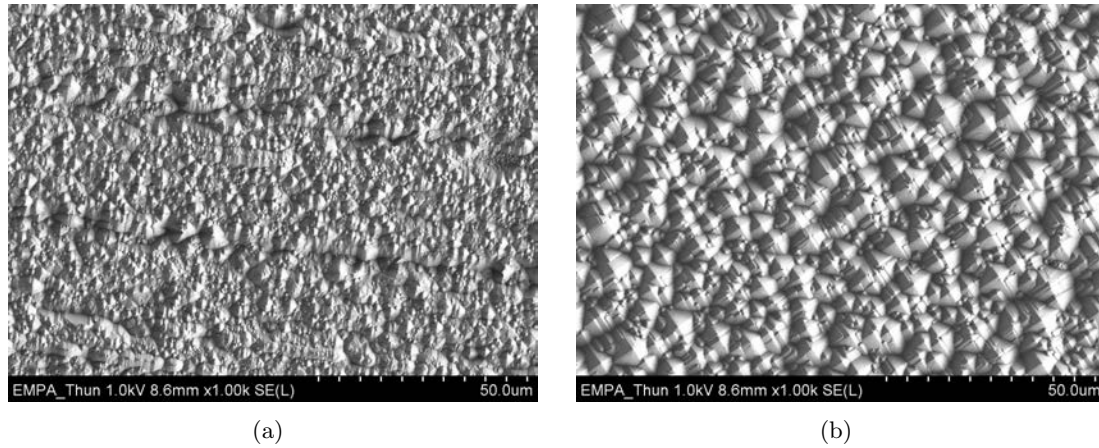


Figure 7.15: (a) SEM micrograph of a diamond-wire wafer after a standard etch (b) SEM micrograph of a slurry sawn wafer after a standard etch. The diamond-wire sawn wafers shows protruding parts of the surface that were not etched, where scratch traces are seen. On other parts of the surface, the pyramids are aligned with the scratch direction, in contrast to the surface of the slurry sawn wafer where nicely developed pyramids are found in a random arrangement.

ness was equivalent to the one of slurry sawn wafers etched a standard time (Fig. 7.14) and their light absorption was comparable to the slurry sawn wafers. They were processed into solar cells by Q-Cells SE on a standard production line and achieved an efficiency equivalent to the slurry sawn wafers (see Table 7.1). Thus, the diamond-wire sawing does not introduce deeper, potentially harmful defects than the slurry sawn wafers, which could impact the solar cell efficiency.

7.3.1 Comparison between wafers with different coolant

Other wafers, sawn with a diamond-plated wire and a different kind of coolant, have also been studied. The principal difference is the etching rate: these wafers are etched at a rate comparable with the slurry wafers, so that they do not need a specific etching procedure to

Table 7.1: Solar cell efficiency of mono-crystalline solar cells made from slurry sawn wafers (reference) and diamond-wire sawn wafers. All wafers are coming from the same ingot, so that the efficiency difference does not come from the material quality, but from the etching process.

	Reference slurry A	Diamond wire 2 etches	Reference slurry B	Diamond wire 1 etch
Efficiency	16.88 %	17.07 %	17.03 %	16.21 %

produce high-efficiency solar cells. This difference may come from molecules adsorbed on the first type of wafers surface, or from a difference in the amorphous silicon layer. As it was postulated that this layer was acting as a mask preventing the etching to proceed fast, the surface fraction of chips was measured by optical microscopy, as previously described for the first wafer type. This fraction was measured to be 12.9 %, so 4 % less than for the previous type of wafers. Thus, it appears that large chips are not responsible for a change of etching rate.

Another parameter that can change the masking efficiency of the amorphous layer is its thickness: if its mean thickness is smaller on the second type of wafers, or if there are more small regions where the crystalline silicon is apparent or close to the surface, the masking efficiency decreases. As the amorphous layer thickness varies significantly on a small scale, such a measurement is hard to achieve. However, it is possible to measure the effect of the amorphous layer on the crystalline silicon, i.e. the stress inside the crystalline silicon. Figure 7.16 shows a map of the stress in a wafer slowly etching (the map is actually the same as the one presented in figure 7.8 apart from that it is not superposed to the optical micrograph) and one of a wafer etching faster. It shows that the average stress is lower in the second type of wafers: the median stress is -206 MPa (compared to -325 MPa for the first type of wafers), indicating that the amorphous layer should be thinner for the faster-etching wafers.

Thus, the etching speed difference might come from the amorphous layer thickness that is

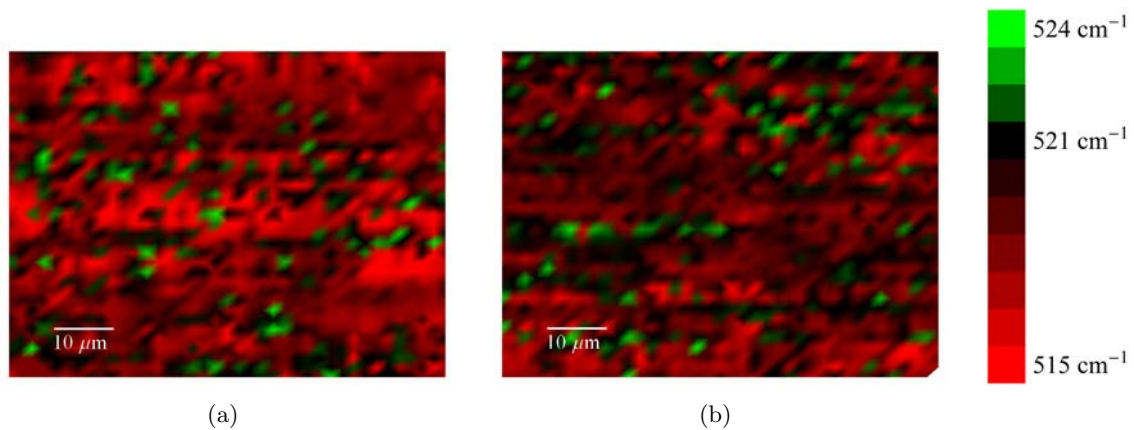


Figure 7.16: (a) Raman map of the stress in the first type of wafers. This map is equivalent to the one presented in Fig. 7.8, except that it is not superposed on the optical microscope picture. (b) Raman map of the stress in the second (faster etching) type of wafers. In both pictures, compressive stress is in red and tensile stress in green. The stress in the second type of wafer is globally lower than in the first type of wafers.

thinner on the wafers sawn with the second type of coolant, but this difference seems too small to explain such large etching rate differences. Another explanation is that some molecules of the first coolant were not properly cleaned off the wafer surface and acted as a mask during etching, although it was not possible to measure their presence.

Despite the faster etching rate of these wafers, the original direction of the wire is still recognisable on the etched wafers (Fig. 7.17). This has no influence on the reflectivity or on the cell efficiency, but it leaves the saw scratches visible on the completed cell.

7.4 Overall compatibility of the diamond-plated wire sawing with solar cell production and conclusions

As described earlier, the diamond-wire sawn wafers have a lower thickness variation in the wire direction than the slurry sawn wafers. Perpendicularly to it, the wafers studied have a larger thickness variation, but by improving the process it should be possible to reduce it. As the thickness variation causes problems when the wafers have to sustain a thermal process (such as firing the contacts) and as these effects are exacerbated when wafers become thinner, the diamond-wire sawing can offer a valuable alternative for producing thin wafers (if the thickness variation perpendicularly to the wire direction can be reduced). Furthermore, the saw productivity is increased by sawing faster and the downtime can be reduced by cutting several loads before changing the wire. This diminishes the cost of ownership of the wire-saws,

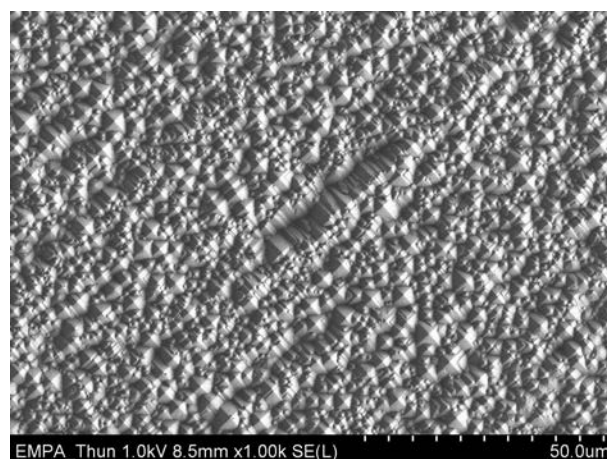


Figure 7.17: Surface of a diamond-wire sawn wafer after etching. The etching speed of this type of wafer is comparable with the one of slurry sawn wafers. Despite that, the original orientation of the grooves at the surface is still visible.

consequently reducing the wafer costs. In addition, the cooling agent is much easier to handle than the slurry as it contains no suspended particles. Its recycling is easier and it seems possible to recycle the silicon kerf⁸². Despite these advantages, the price of diamond-plated wire is still expensive and prevents this sawing method to be an alternative to standard slurry sawing. A cost estimation made in 2006 revealed that the wire cost had to be reduced by a factor of 3–5 to make this technology competitive⁷⁶. Since then, the wire price has decreased and diamond-wire cutting is closer to this goal. Furthermore, the costs might decrease rapidly when the wire producers increase their production as the technology is spreading across the industry.

Still, when the etched surface of a diamond-wire sawn wafer is analysed by SEM, the orientation of the scratches are identifiable (Fig. 7.15(a)): the top of the pyramids are preferentially positioned along the scratches. In contrast, the slurry sawn wafers present pyramids having random position (and size) (Fig. 7.15(b)).

In summary, some insight into the mechanisms of diamond-wire sawing has been highlighted. The wafer surface is made by repetitively scratching the silicon. This creates a thick layer of amorphous silicon, sometimes interrupted by chips when the local scratching load was too important. This process creates large stresses in the crystalline silicon underneath the amorphous layer. These stresses are mostly compressive, although some areas are under tension. One of the consequences is that the cracks under the surface are closed and thus difficult to see on a cross-section. However, an indication of their presence is found in the disruption of the cleavage plane.

The first batch of analysed wafers had a lower etching rate than slurry sawn wafers, whereas the second batch had an etching rate comparable with the slurry sawn wafers. Two explanations are plausible: some molecules of the lubricant used for sawing the first batch remained adsorbed on the surface after cleaning and slowed the etching down, or the amorphous layer is acting as a mask. The analysis of both wafer types was not conclusive, as only small differences of internal stress in the crystalline silicon were found, and no clear difference regarding the surface fraction of amorphous silicon on the wafer surface was measured. However, the literature is predicting that the amorphous layer has an impact on the etching rate, leading to the hypothesis that a change in the amorphous layer has an impact on the etching rate. The second batch of wafers were cut with a different coolant and have a lower amount of amorphous silicon on their surface, leaving room for both explanations.

Chapter 8

Conclusions

This thesis is focused on the interactions between the sawing parameters and the resulting wafer properties. The study is focused on four themes: the development of a semi-analytical model predicting the wafer strength from the sawing parameters, the refinement of the sawing process from the microscopic to the ingot scale, the effect of debris on the wafer properties, and a first description of diamond-wire sawing.

By testing several sawing parameter combinations, it was possible to deduce the effect of the most important parameters and to develop a novel semi-analytical model explaining the interactions between the parameters. It is found that the parameters are entwined and that the best parameter combination depends on the abrasive size distribution. As this study concentrates on the wafer mechanical stability, the best parameters were found to be (within the boundaries tested) a small abrasive size, a low abrasive volume fraction in the slurry, a low wire tension and a slow feed rate. These parameters are not optimal in a production environment, as a small abrasive is harder to recycle and more expensive, a low wire tension increases the wafer thickness differences and increases the wire jump probability, and a slow feed-rate requires a longer wire and induces a lower productivity.

Nevertheless, as the relative importance of the different parameters has been determined, it should be possible to circumvent the drawbacks of such a set of parameters. For instance, the development of a new slurry generation should ease the slurry recycling and lower the thickness differences. But such a change may have other consequences, e.g. on the wire vibrations.

In this thesis, a more detailed picture of the interactions between the wire, the abrasive particles, the silicon brick and the debris has also been developed. It is found that the situation at the top of the groove is different than on its sides. The material removal speed is much higher at the top, but the load on the particles is lower than on the sides because, as the wire is maintained on both sides by the silicon brick, the wire cannot be pushed away when the load

is too large. As the removal rate at the top of the groove is faster, its surface is made of more sharp edges than on the wafer surface. The pressure of the wire on the particles — that is required to wear the silicon — also pushes the particles from the top of the groove to the sides and the particles eventually leave the sawing region. As the wire is maintained laterally by the particles on one side of the groove, the place is limited on the other side. Consequently, if large particles are pushed on that side, they can indent the silicon with a large force, inducing large roughness and cracks that make the wafers fragile. At the same time, smaller particles also indent the surface with low force, smoothing the surface. This happens both at the top on the groove and on the sides, but this effect is erased on the top of the groove as the wear rate is large, whereas it is clearly visible on the wafer surface as the small particles had a long time to smooth the surface (as the feed rate is slow, the wire stays a long time near the same place, letting many small particles smooth the surface). The wafer thickness indicates that multiple particles have to be interacting in order to indent the wafer surface, as a simultaneous contact with the wire and the silicon would not be possible otherwise. To do this, either two large particles are overtaking each other (either on the same side of the wire, or with the wire between them) or — more likely — two particles are holding the wire on one side, and the wire is bent by the third particle indenting the silicon on the other side. This mechanism explains why a lower wire tension tends to produce stronger wafers. The amount of particles being pushed to the groove sides depends on the feed rate: the faster the feed rate, the higher the wire pressure on the particles at the groove top (the particles have to remove material faster). But the influence of an increased pressure on the removal rate depends on the particle size: the smaller the particles, the more important the pressure variation for a given feed rate change. Thus, increasing the feed rate while sawing with large particles will affect the amount of ejected particles less than for small particles.

The particles of debris that are created in the saw groove are taken away by the slurry. But before they are integrated into the slurry bulk, they travel in the groove down to the wire exit. Along the way, the amount of debris in the saw groove increases. As long as they are few, they have no noticeable effect on the wafer surface. But when their amount increases, they lower the abrasive cutting efficiency, resulting in saw marks. First, they appear near the wire exit and at the side of the silicon bricks where the wire is most worn. They increase in length with the amount of silicon sawn. The critical concentration of debris for the apparition of saw marks was measured to be 15 % of the particle volume. It is proposed that these particles of debris act as cushions between the SiC particles and the silicon. As they are much softer than the SiC, the load concentration at the particle tip is decreased and the particle efficiency diminishes. It results in a periodic change of sawing regime producing saw marks. When saw marks are small enough (i.e. when the average roughness at the wire exit is not larger than

at the wire entrance), the wafers are still as strong as wafers without saw marks. But larger saw marks render the wafers much more fragile.

The use of a diamond-plated wire to saw wafers was also investigated. In such a case, the abrasive particles are bound to the wire and produce long grooves on the wafer surface. These grooves are smooth, but interrupted by chips. The grooves are covered by a layer of amorphous silicon, whereas the chips show the bulk crystalline silicon. The amorphous silicon can be differentiated from crystalline silicon by Raman spectroscopy. This method also allows the measurement of the stress in the crystalline silicon. An important stress has been measured: the median stress was 325 MPa in compression. But this stress is not homogeneous, as compressive as well as tensile stress was measured. The highest stress measured was above 1 GPa (both in tension and in compression). In contrast with the slurry sawn wafers, the diamond-wire sawn wafers have a constant roughness and thickness from the wire entrance to its exit.

The presence of amorphous silicon and long grooves might be harmful to the texturisation. The high stress measured in the crystalline silicon right under the wafer surface may be harmful to the wafer strength. As the amorphous layer is removed during the texturisation step, this should not have any consequence on the solar cell mechanical stability, but it could cause an increase in breakage rate before this step (i.e. during the sawing, the ungluing, the cleaning, the characterisation and the packing).

Diamond-wire sawing presents an interesting alternative to the slurry sawing. As it is possible to saw faster and use the wire for several cuts, the saw downtime is reduced and the productivity is increased. Furthermore, diamond-wire sawing only requires a lubricant, without any free particle. This lubricant is easier to handle than the slurry and its recycling is straightforward, which also provides a cost reduction potential in comparison with slurry sawing. As the wafers have less TTV than the slurry wafers, the diamond-plated wire seems to be a good candidate to produce very thin wafers processable into high efficiency solar cells. Unfortunately, the diamond-plated wire is still too expensive to be considered as an advantageous alternative. Besides, and even though not realised within the frame of this study, it remains to be confirmed that diamond-wire sawn wafer can reach a wafer strength similar to the one of slurry-sawn wafers. This might be a critical factor for the success of this technology.

There are many topics left to be investigated. On a production level, the decrease of silicon needed per wafer (i.e. reducing the wafer thickness and the kerf loss) while maintaining competitive production costs remain a challenge. Moreover, the specifications of thin (i.e. $\sim 100\text{ }\mu\text{m}$) wafers for solar cells (e.g. the TTV and mechanical strength) have to be set and achieved. The use of thinner abrasive can solve some problems, but it is more expensive

and introduces recycling difficulties. Changing other parameters can help increase the wafer strength, but has a marginal impact on the TTV. Reducing the wire diameter makes the wire more sensitive to wear and easier to break. To prevent such an outcome, a lower wire tension has to be used, but this increases the risk of wire jumping from one groove to the next on the wire-guides as well as the thickness differences from one wafer to another. Finally, the development of a water-based slurry can reduce the slurry cost, improve the recycling efficiency and decrease the wire spacing differences.

On a fundamental level, the sub-surface defects creation mechanism in the wire-sawing process could be better understood, as well as how the surface structure is created. The reason why only a very small amount of amorphous silicon was found on the wafer surface is still not clearly understood, as is the quasi-absence of dislocation. If SiC particles are pressed into the silicon surface, they should induce a silicon phase transformation near the surface and nucleate dislocations. And if the particle load on the surface is too low to create a phase transformation, it should not be enough to create cracks. However, an explanation may be found in the way the surface is shaped: if light indentations are smoothing the wafer surface, they might be enough to remove the amorphous layer created by the larger, crack-inducing indentations. The interaction between SiC particles, the wire and the silicon brick is still not precisely known at the particle level. Finally, a better understanding of the sawing parameters role could help refining the model developed in this work: the impact of the sawing parameters on the Weibull modulus could not be precisely modelled. But this is not surprising: as it represents a kind of sawing process stability, any small detail can have an influence on it, in contrast to the characteristic stress that represents a general defect depth.

It was shown that using the right sawing parameters (primarily F800 abrasive), it is possible to increase the stress at rupture by more than 20 %. This allows sawing 19 μm thinner wafers that are breaking at the same force than reference wafers. Furthermore, as thinner wafers are able to sustain more bending, it is possible to saw even thinner wafers with the optimised parameters, while keeping a comparable yield in the cell production line (if it is assumed that the process leading to wafer failure do not only impose a certain force, but that the deformation and / or wafer weight also play a role). Also, with this set of parameters, the wire tension is reduced, so that a thinner wire diameter can be used without risking wire breakage, consequently diminishing the kerf loss and decreasing the amount of silicon needed per wafer. An approximate calculation shows that diminishing the wafer thickness to 140 μm , using a wire diameter of 100 μm and F800ⁱ would decrease the required amount of silicon per watt peak of 29 %ⁱⁱ which puts the required amount of silicon at 4.09 instead of 5.72 g/W_p.

ⁱindustrial wafers are about 180 μm thick, sawn with a wire of 120–140 μm and F600, but the possibility to saw wafers thinner than 100 μm has been demonstrated

ⁱⁱusing production yield values given by del Cañizo *et al*³¹: an ingot yield of 95 %, a wafer yield of 92 %, a

Hopefully, using some of the principle and results of this thesis, an further optimised sawing process can be developed. With such a process, it seems plausible that 100 μm thick wafers suitable for solar cell production can be industrially produced.

List of Symbols and Abbreviations

α	Empirical constant, page 42
α_i	Constant, page 44
β	Constant, page 45
β	Empirical constant, page 42
β	Relative indentation dimension, page 25
χ_e	Constant, page 23
χ_r	Constant, page 23
Δt	Time interval, page 48
ΔV	Indentation volume, page 25
δ_i	Constant, page 68
$\dot{\epsilon}$	Scratching deformation speed, page 37
$\dot{\sigma}_s$	Scratching decompression rate, page 37
η	Slurry viscosity, page 46
γ	Surface energy of the material, page 18
$\bar{l}_m$	Particle mean diameter, page 49
μ	Slurry viscosity, page 49
ν	Poisson's ratio, page 25
Ω	Dimensionless crack geometry term, page 23
ϕ	Angle between the sample surface and the point where the stress intensity factor is calculated, page 20
Ψ	Indenter half-angle, page 24
ρ	Mass of wire per unit unit, page 47
σ	Applied stress, page 18
σ	Fracture stress, page 61
σ_0	Characteristic stress, page 61
σ_s	Surface stress, page 23
τ	Shear stress, page 49

θ	Angle in a polar system, page 20
θ_i	Empirical constant, page 111
$\xi_r(\phi)$	Dimensionless term independent of the indenter and sample, page 24
ζ_0	Constant, page 27
ζ_L	Constant, page 27
A	Interaction Area, page 42
A	Projected contact surface, page 37
a	Contact width, page 25
a_r	Residual scratch width, page 37
A_s	Global contact area, page 48
b	Plastic zone radius, page 24
C	Compliance coefficient, page 27
c	Crack length, page 18
c	Depth of a crack, page 20
c	Indentation crack length, page 23
c_L	Limiting crack function, page 27
C_{IE}	Geometric factor, page 49
d	Depth of the indent, page 37
d_{50}	Abrasive median diameter, page 84
d_{SiC}	Abrasive median size, page 120
d_{wire}	Wire diameter, page 120
E	Young's modulus, page 18
e	Half-width of a crack, page 20
E_{el}	Elastic energy stored in a stressed sample, page 18
E_s	Amount of energy needed to increase the specimen surface, page 18
E_w	Young's modulus of the workpiece, page 44
E_{eff}	Effective elastic modulus, page 49
F	Applied force, page 68
F	External excitation force, page 47
f	Feed rate, page 104
$f(y)$	Mapping factor, page 46
F_N	Force applied by the grain, page 48
F_t	Force acting on the particle, page 49
G_c	Toughness of the material, page 18
H	Hardness, page 24
h	Distance between the lapping plate and the sample, page 45

h	Silicon–wire distance, page 46
H_b	Hardness of the ball, page 42
h_i	Height of point i, page 56
H_s	Hardness of the sample, page 42
H_w	Hardness of the workpiece, page 44
H_{eff}	Effective hardness, page 45
h_{mean}	Average profile height, page 56
K	Net stress intensity factor, page 24
K_c	Fracture toughness, page 20
K_e	Elastic part of the stress intensity factor in indentation, page 23
K_I	Critical stress intensity factor in mode I, page 20
K_r	Plastic part of the stress intensity factor in indentation, page 23
K_s	Surface stress part of the stress intensity factor in indentation, page 23
$K_{Ic,w}$	Fracture toughness of the workpiece, page 44
L	Lateral crack extension, page 27
l	Wafer size, page 120
L_0	Wire-silicon distance, page 48
$L_{m,c}$	Mean size of the load-bearing particles, page 44
m	Number of indentation events, page 48
m	Weibull modulus, page 61
n	Constant, page 48
n	Number of indenting points on the circumference of the rolling particles, page 44
n	Number of sawing grooves in the ingot, page 120
P	Applied indentation load, page 23
P	Tension of the wire, page 47
p	Applied pressure, page 44
p	Indentation pressure, page 25
p	Pitch, page 120
P^*	Maximum load attained during the indentation test, page 24
P_0	Apparent cracking threshold, page 27
P_i	Normal load of the load-bearing particles, page 44
P_m	Mean contact pressure, page 37
q	Material response to scratching, page 37
r	Radial distance in a polar system, page 20
R_a	Average roughness, page 56

R_z	Average peak-to-valley roughness, page 44
S	Severity of contact, page 42
S_b	Remote outer-fibre bending moment, page 20
S_t	Remote uniform stress, page 20
s_{wire}	Wire section, page 110
T	Wire tension, page 104
t	Average wafer thickness, page 111
t	Plate thickness, page 20
t	Wafer thickness, page 68
U	Transverse displacement, page 47
V	Plastic zone volume, page 25
V	Translating speed of the wire, page 47
v	Relative velocity of the sample on the lapping plate, page 44
v	Scratching speed, page 37
v	Volume fraction of abrasive in the slurry, page 42
v	Wire speed, page 46
V_0	Volume of material removed by a single grain, page 48
V_l	Material removed by lateral crack chipping, page 27
v_s	Sawing Rate, page 48
V_{debris}	Volume of debris in the slurry, page 120
V_{groove}	Debris volume produced by one groove, page 120
V_{SiC}	SiC volume fraction, page 104
w	Wire diameter, page 46
x	Coordinate in the wire movement direction, page 46
Y	Constant dependant on the crack system, page 20
y	Coordinate in the direction transverse to the wire, page 46
y	Yield stress, page 25
Z	Material removal rate, page 44
FCC	Face-centred-cubic lattice, page 29
LEFM	Linear elastic fracture mechanics, page 18
PEG	Poly(ethylene glycol), page 8
PV	Photovoltaic, page 1
SEM	Scanning Electron Microscopy, page 54
SiC	Silicon carbide, page 8
TEM	Transmission Electron Microscope, page 33
TTV	Total Thickness Variation, page 80

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List of Publications

Journal articles

- A. Bidiville, R. Kaft, I. Neulist, K. Wasmer, C. Ballif. The effect of debris on the silicon wafering for solar cells. article in preparation, 2010.
- A. Bidiville, K. Wasmer, J. Michler, P. M. Nasch, M. Van der Meer, C. Ballif. Mechanisms of wafer sawing and impact on wafer properties. *Progr. Photovolt: Res. Appl.*, 2010.
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