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0.35 μm 22μW Multiphase Programmable Clock Generator for Circular Memory SC FIR Filter For Wireless Sensor Applications

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***Abstract*-The paper presents the programmable multiphase clock generator for switched-capacitor finite impulse response (SC FIR) circular memory filters. The proposed programmable clock circuit enables easy division of such kind of filters into different orders smaller sections, which when connected in series, lead to increase in filter efficiency: reduction of chip area, power dissipation, and rising up of the speed. The proposed clock generator enables adjustment of the impulses width, that simplifies design process and leads to structure, which is more robust to process variation. The clock circuit realized in CMOS 0.35μm technology, dissipates 22 μW from 2 V power supply.**

1. INTRODUCTION

Wireless sensor network arguably represent one of the most important innovation in communication and computing that will bring huge benefits for the humanity in 21st century. Building low data-rate low-cost wireless transceivers is the key of that vision, to enable integration of computation, sensor and actuator nodes [1-3]. This so-called "ambient-intelligence" or "smart dust" have to process large aggregate amounts of data; however individual nodes participate in a small fraction of the overall data traffic. The nodes must be self-contained in terms of energy using a one-time battery charge or a scavenged energy from the environment.

To achieve very low energy usage radically new approaches at circuit and system level are required. In this work we are exploring possibility of using analog signal processing for baseband filtering applications. Instead of using standard digital processing (DSP) for implementation of digital filter functions we are proposing to use custom designed switch-C filters that dissipate an order of magnitude lower power. Such an implementation is possible since the wireless sensor networks do not require high performance. In particular, baseband filtering at only 20-30dB levels can be sufficient in some cases [4].

2. ANALOG SC FIR DISCRETE TIME FILTERS

Finite Impulse Response (FIR) filters offer many advantages in comparison to other kinds of filters [5-9], including absolute stability and linear phase response. These filters have also some disadvantages such as complexity, which results from the fact that a given frequency response requires higher order *N* compared to other active filters. FIR filters can be implemented in both digital and analog domains. This work uses switched C (SC) fully custom designed analog filters, where hardware is fitted to a desired frequency response, and in this case the power consumption is much lower than in the case of FIR filters realized digitally [5].

One of the disadvantages of SC filters is that signal samples are stored as voltages in the capacitors and are re-written between capacitors in the circuit. This causes errors affecting the attainable attenuation in the stopband, leading to lower filter performance compared to digital implementations where this type of error does not occur. However, for wireless sensor network applications where high selectivity is not required the levels of attainable attenuation levels in stopband are quite sufficient [4].

Another disadvantage of integrated SC FIR filters is their large chip area dependent on the frequency response. Values of the filter coefficients are directly proportional to the capacities of the capacitors. The greater the spread between the smallest and the largest coefficient values, the greater is the entire capacitance range leading to larger chip areas.

To minimize or even eliminate this disadvantage SC FIR filters must be divided into shorter section (with lower spread between coefficients) connected in series. In case of fixed frequency response filters of *N-th* order, values of the coefficients are fixed. Quite different situation is in case of programmable filters, where flexibility is required, both in filter order *N* and in values of filter coefficients.

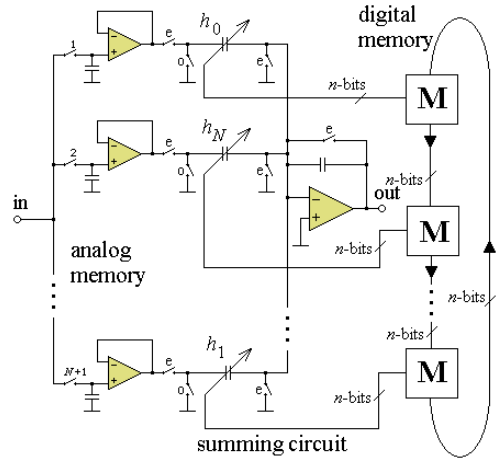

Fig. 1 General structure of programmable circular memory SC FIR filter with coefficients represented as *n*-bit words [9]

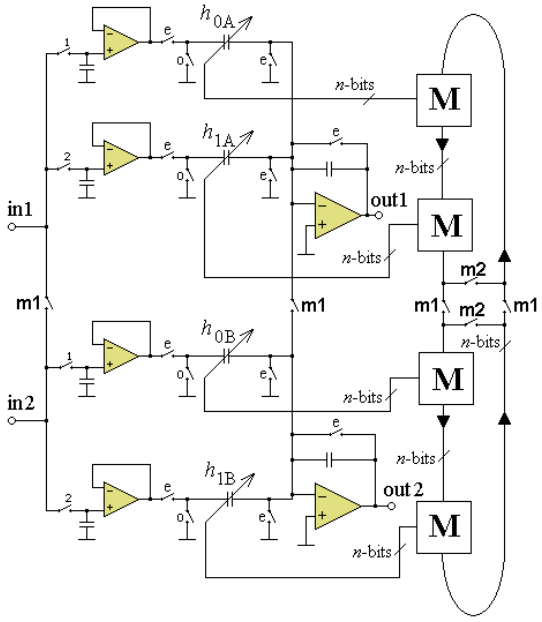

Fig. 2. Circular memory filter, which enables two modes: in two-sections mode switches m2 are closed, and in one-section mode switches m1 are closed. In two-sections mode an additional output op amp must be implemented, which can be switch off in one-section mode to save power.

There are different SC FIR filter architectures reported in literature [8, 9], but for programmability the recently proposed SC FIR circular memory filters [9] are the best. Circular memory filter structure is shown in Fig.1. This filter can be used in a one section mode, but can be easily divided into two sections as illustrated in Fig 2. The enabling key for the proper division is appropriate programmable clock generator. Prototype of such generator was realized in 0.35 μm CMOS technology and is presented in this paper. Reconfiguration of the filter structure is realized simply by reprogramming of the controlling clock generator and some additional switches m1 and m2 (Fig 2).

3. PROGRAMMABLE CLOCK GENERATOR FOR SC FIR FILTERS

Complexity of the clock generator is one of the most important parameters in design and optimization of the SC FIR filters [8]. Some of SC FIR filter architectures need simple clock generator but other ones need complicated multiphase system [8]. In SC FIR filters, which are fully programmable (filter order *N* and values of the filter coefficients) new clock circuit must be realized. This clock must enable division its structure into smallest subsystems.

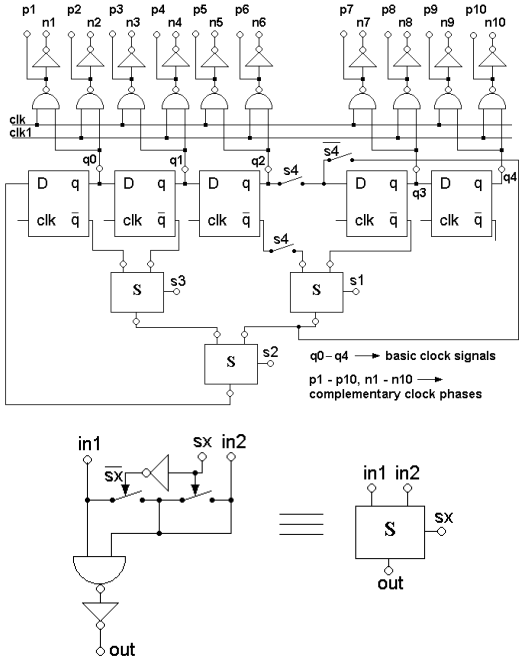

Fig. 3 Diagram of the programmable multiphase clock generator: (up) overall structure (bottom) structure of the special switch that enables feedback loop reconfiguration and division of the clock into subsystems

Diagram of the proposed clock circuit is presented in Fig. 3. The circuit is based on D-type flip-flops connected in the self-correcting counter. Division of the clock into subcircuits is realized by reconfiguration of the feedback loop of the circuit, in such a way to obtain independent loops for different parts of the D - flip flop chain. Configuration of the clock circuit is adjusted by the controlling signals s1–s4.

The layout of the clock circuit, realized in CMOS 0.35 μm technology is presented in Fig. 4. In Fig. 5 microphotograph of the clock circuit together with the SC FIR filter is shown. In Figs. 6 and 7 simulation results are presented for two cases: for not divided circuit (10-phase clock generator) and for the case, when circuit is divided into two independent sections (6 and 4-phases). In the second case each of the clock sections controls separated SC FIR filter section, as shown in Fig 2.

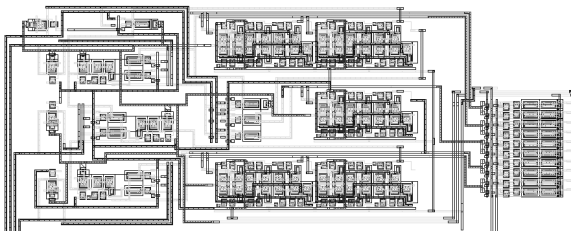

Fig. 4 Layout of the experimental clock circuit

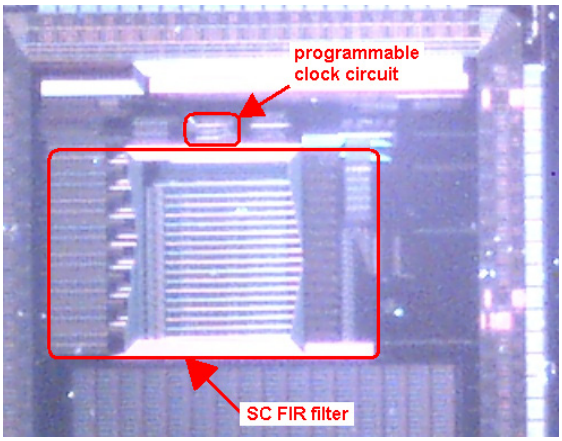

Fig. 5 Microphotograph of the experimental clock circuit and example SC FIR filter

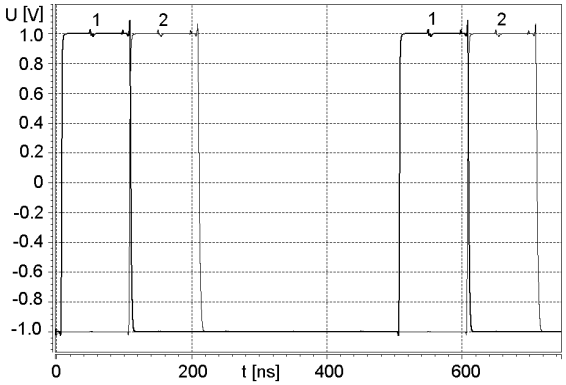

Fig. 6 Clock circuit in not divided mode: basic clock signals q1 and q2 in 5-impuls mode → 10 clock phases

One of the important problems in design of SC FIR filters was optimization of widths of the clock impulses. The general feature of all SC FIR filters is their sensitivity to the location of slopes crossing points of the adjoining clock phases. These time moments have to be adjusted very precisely to avoid such situations, when adjoining impulses overlap and in consequence all switches are simultaneously open. Such an overlapping causes short-circuit of the filter and leads to loss of charge stored in capacitors and to distortion of information stored in the filter. This effect is especially visible in the stopband of the frequency response. On the other hand, we have to avoid such situations when between adjoining clock impulses are "dead times" i.e., time instants, in which no relevant switches are closed, resulting in periodic opening of the operational amplifiers loops. This situations causes in some SC FIR filter structures saturation of the op amp's outputs, and thus, generation of undesirable peaks with relatively high amplitudes in the filter output signal [8].

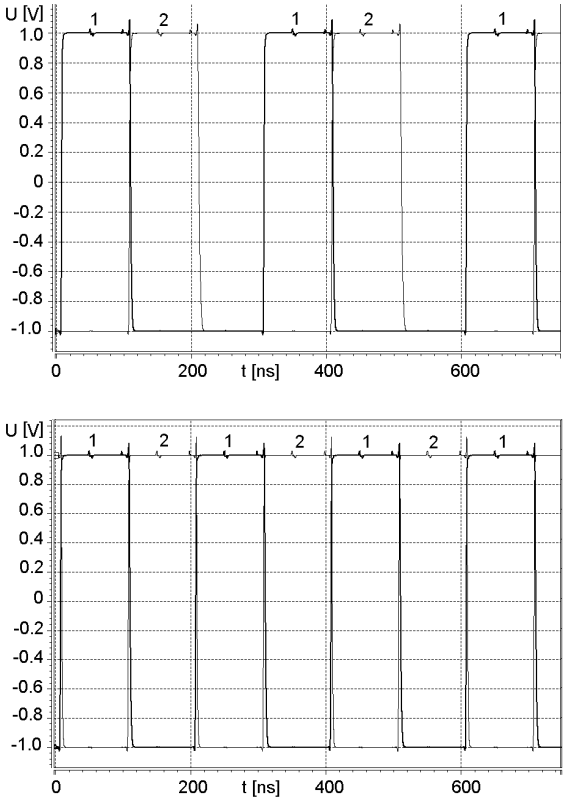

Fig. 7 Clock circuit in divided mode: (top) basic clock signals q1 and q2 in 3-impulse mode → 6 clock phases (bottom) basic clock signals q3 and q4 in 2-impulse mode → 4 clock phases

To make possible control of the crossing point of the adjoining clock impulses we propose a solution, where D – flip flops outputs *q* and *qn* do are not real clock phases but are the basis to create them. The real clock phases are obtained by cutting out them from these basic signals with an external controlling signals *clk* and *clk*1, using NAND gates, as shown in Fig. 3. Signals *clk*, *clk*1 form simple two-phase clock generator. One of the inputs of these NAND gates is driven by outputs *q* of the D-type flip-flops, but the second one is controlled by one of *clk* or *clk*1 signals. Because *clk* and *clk*1 are external signals, the width of their clock impulses can be adjusted and that constitutes the way for controlling of the mentioned crossing points. This greatly simplifies design process of the circuit and optimization of the layout, creating more robust structure for process variation. This enables also reduction of the area and power dissipation of the circuit, due to reduction of number of DFFs.

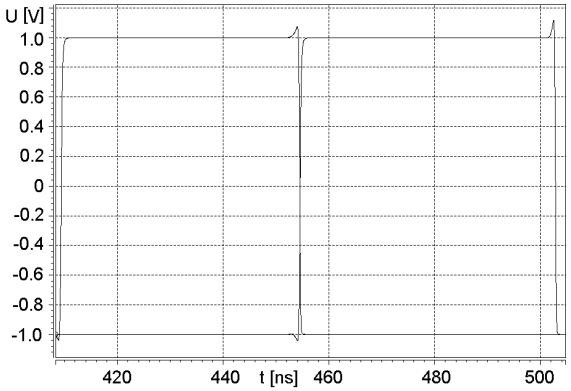

Fig. 8 Optimal crossing point of the adjoining clock phases

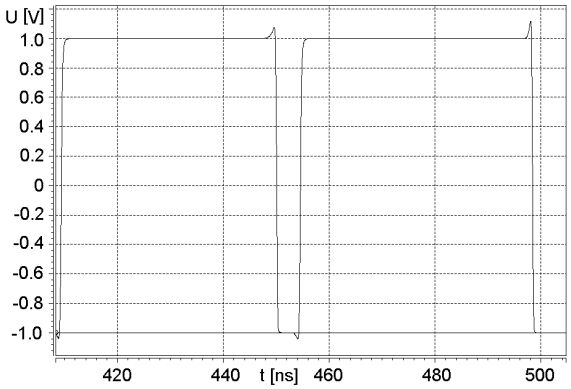

Fig. 9 Permissible but not optimal crossing point of slopes of adjoining clock phases

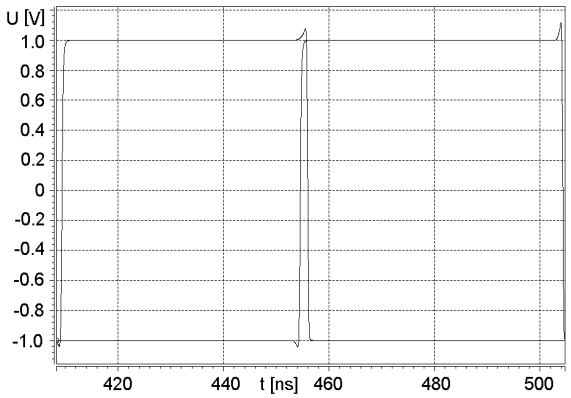

Fig. 10 Unacceptable crossing point slopes of adjoining clock phases

In Fig. 8 – 10 three cases for different *clk* and *clk*1 impulses widths are illustrated. The diagram in Fig. 8 shows the optimal crossing of the adjoining clock phases. In ideal placement the clock should be placed near the middle between the lowest and the highest voltage level. Fig. 9 shows a permissible but not optimal crossing point of slopes of the adjoining clock phases. In this case there exists a "dead time", in which the transistors controlled by both phases are in the off-stage. An unacceptable situation is presented in Fig. 10. In this case there is a non zero time, when transistors are in on-stage, thus the circuit is short-circuited, causing performance errors.

4. Conclusions

The new, programmable multiphase clock circuit for fully programmable SC FIR filters is presented in the paper. Reconfiguration of the feedback loop of this clock generator divides it into independent sections, that enables easy division of the SC FIR filter into different order smaller sections, which makes these filters more power and chip area efficient. One of the most important features in the proposed clock is that through adjustment of the clock impulses width, we have better control of the filter performance. This makes these filters more robust for process variations and greatly simplifies the layout design. Solution presented here is for maximum 10 clock phases, but can be easily extended for higher order filters. The clock circuit consumes 22 μW from 2 V supply voltage for the frequency equal to 100 MHz. For lower frequencies, VDD and power consumption can be reduced.

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