An Examination of the Effect of Feature Size Scaling on Effective Power Consumption in Analog to Digital Converters

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***Abstract* - Wireless Sensor Network (WSN) nodes require components with ultra-low power consumption, as they must operate without an external power supply. One technique for reducing consumption of a system is to scale it to a smaller technology; however, in recent technologies is not clear whether the decrease in dynamic power consumption outweighs the increase in static power consumption (due to leakage currents). Here this is considered by examining the power consumption of three implementations of an analog to digital converter (ADC). One in 350 nm, one in 180 nm, and one in 90 nm, were simulated and compared. The results show that the dynamic power consumption was reduced by a factor of four over the three technologies, but standby power consumption increased by an order of magnitude. The power consumption of the 180 nm implementation was always lower than the 350 nm implementation. However, assuming a WSN application with a duty cycle of 1%, the effective power consumption of the 90 nm ADC was higher than both the 180 nm and the 350 nm implementation. This highlights the dominance of leakage current in determining the effective power consumption in low-throughput nodes.**

I. Introduction

A wireless sensor network (WSN) is a network made of many small sensor nodes for measuring, monitoring, and managing data [1][2]. It may also contain one or more base stations, which centralize the data gathered by sensor nodes. WSNs are of increasing research interest because they offer the possibility in the development of a low cost, scalable and flexible network architecture. Potential applications are widespread; proposed applications range from data acquisition for industrial control to security to hospital patient-tracking systems [2].

WSNs create invisible interconnections with the physical world for managing data from multiple sensors with little constraint on their locations. In a typical WSN, sensors can communicate with a base station or directly between themselves in a peer-to-peer fashion. To accomplish this, a wireless sensor node typically consists of an RF front end, an analog to digital converter (ADC), an optional microprocessor to process the collected data, and a power supply block, as illustrated in Figure 1 [1].

For a WSN to be a truly wireless network, each node must be able to operate without an external power supply. As a result, an important goal for WSNs lies in being able to integrate many ultra low power nodes that require only a one-time battery charge or that scavenge energy from the environment. This is helped by the fact that sensor information generally needs to be conveyed at low data rates; this allows design optimization to instead focus on reducing power consumption. Ultra low power nodes have a duty cycle of about 1% and a low average throughput ranging from 1b/s to 10kb/s. However, for even the most successful devices the average power capacity is limited to 100 $\mu W/cm^2$, or equivalently 10mW of peak power, assuming a 1% duty cycle. This limits the transmission energy to below 2nJ/bit for 10kbps [1].

From this, it is clear that it is imperative to minimize the power consumption of every component. The designer has at his or her disposal various techniques to achieve this; among them is to scale the design to a smaller feature size. This is widely known to reduce dynamic power consumption, as smaller transistors require a lower power supply and have less parasitic capacitance, both of which are factors in dynamic power consumption.

Also key is appropriate selection of components. One of the largest power consumers in a WSN node is the ADC; thus considerable time should be spent ensuring that the power consumption of this component is minimized. Given this, certain architectures are more appropriate: for WSNs, the most popular ADC architecture is the Algorithmic ADC, a group that includes Successive Approximation (SAR) and Cyclic converters. These are popular for use in applications that require very low power consumption, particularly those that do not require a large number of bits of precision. A selection of recent publications on Algorithmic converters is shown in Table 1.

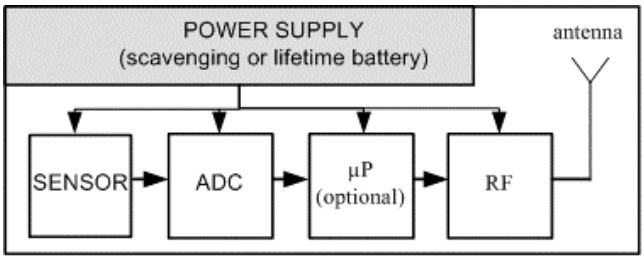

Fig. 1. Typical Architecture of One WSN Node

TABLE 1 – SURVEY OF RECENT SAR ADC DESIGNS

Ref.	Process	# of bits	fs kHz	Power µW	Supply Voltage (V)	Norm. Power µW	FOM	Mode
[3]	CMOS 0.18 µm	12	100	25	1	25	16.4	V
[4]	CMOS 0.13 µm	8	150	2.62	0.8	4.1	9.4	V
[5]	CMOS 0.25 µm	8	100	3.1	1	3.1	8.3	V
[6]	CMOS 2 µm	8	50	40	5	1.6	8.0	V
[7]	CMOS 0.18 µm	6	125	1	0.65	2.4	3.4	I
[8]	CMOS 3 µm	8	112.5	500	5	20	1.4	I
[9]	BiCMOS 0.8 µm	10	0.7	2.3	2	0.575	1.2	V
[10]	CMOS 0.6 µm	8	100	980	3	109	0.2	V
[11]*	CMOS 0.18 µm	8	250	0.37	0.55	1.9	33.7	I
This Work*	CMOS 0.35 µm	8	28	32.9	3.3	9.97	2.4	I
This Work*	CMOS 0.18 µm	8	28	15.77	1.8	8.76	1.5	I
This Work*	CMOS 90 nm	8	28	8.88	1	8.88	0.8	I

Power is active power only. Normalized Power is Power/(VDD^2); FOM is ($2^{(\#\ of\ Bits)}$*fs)/ (Norm. Power)
*Simulated results only.

In this table, Figure of Merit (FOM) accounts for the tradeoff between sampling frequency, bits of precision, and power consumption, allowing for more direct comparison between converters (a larger value is better). Also, Mode refers to current-mode (I) or voltage-mode (V) operation.

However, what is important to note when working with WSNs is that a power analysis that focuses only on dynamic power consumption is not sufficient to capture the full picture. The concern in WSNs is not necessarily peak consumption, but rather aggregate consumption over the lifespan of the node. This leads to the question at hand; while technology scaling is known to reduce dynamic power consumption, it is also known to increase static power consumption, due to an increase in leakage current. Given these contradictory trends it is not obvious whether scaling will always result in lower aggregate power consumption, and one may find that further scaling actually damages the overall consumption.

In a CMOS circuit, total power consumption in the active mode is the sum of dynamic power consumption (i.e. when the transistors are operational) and static consumption, dominated by leakage current, which is current that flows when the transistor is generally thought of as 'off' [12]. The dynamic power consumption has two major contributors, namely, the switching power (i.e. charge and discharge of load capacitances) and short circuit power due to rise and fall of input waveforms. The switching power tends to dominate overall dynamic power consumption. As the feature size is scaled from technology to technology, dynamic power consumption does decrease, but in order to satisfy performance requirements threshold voltage must be scaled as well. This, however, increases leakage currents due to a range of effects ([13], for example, provides an overview). When operating in very small feature sizes (on the order of 90 nm) the selection of a threshold voltage value becomes a very important concern as it has a direct impact on leakage current. A tradeoff thus exists between performance and power consumption requirements.

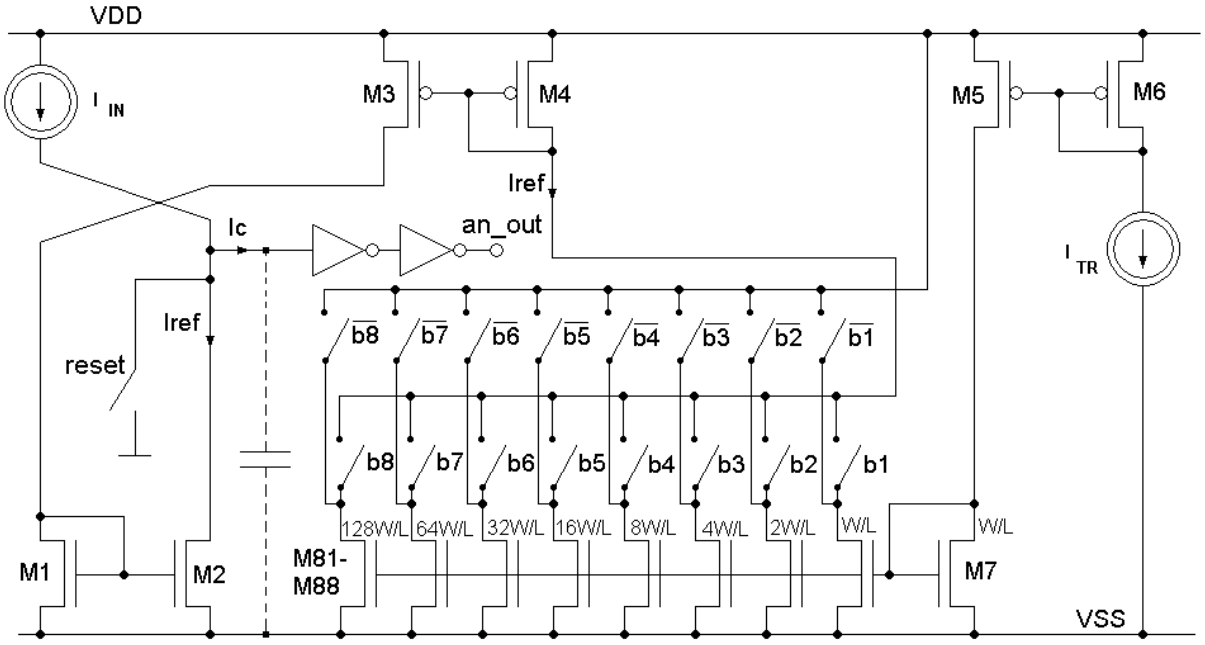

Fig. 2. Schematic of Analog Component of SAR ADC Used in Power Analysis [11]

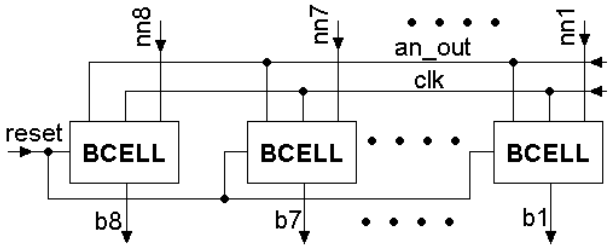

Fig. 3. Digital Component of SAR ADC Used in Power Analysis [11]

In this paper we consider the power consumption of an analog to digital converter (ADC), specifically the ADC featured in [11], which is shown in Figures 2, 3, and 4. The circuit is a current mode Successive Approximation (SAR) type converter, which is of increasing popularity in WSN applications due to its low power consumption [14]. SAR converters use a binary search algorithm [15]: they generate an internal reference signal (in this implementation the current I_{REF}) and compare it against the input signal (in this implementation the input current I_{IN}). The reference signal is first set to half of the maximum value. If the input signal is larger than this, the MSB of the digital output (in this implementation the digital values $b_{1\text{-}8}$) is set and the reference value is set to three-quarters of the total. If, however, the input value is less than the reference value, then the MSB is cleared and the reference value is set to one quarter of the total.

The basic operation is as follows (refer to Figure 2): The ADC takes as an external input a DC current I_{TR}, which is the base current used for the DAC. The DAC is an eight-output current mirror with each output transistor having twice the (W/L) ratio of the previous output. The output of the DAC is controlled by a set of eight digital signals, $b_{1\text{-}8}$. Those signals whose respective b_X signal is high are summed to create the reference current I_{REF}. I_{REF} is mirrored through *M1-M4*, where it meets the input signal I_{IN}. The node (with the two inverters) acts as a current comparator; the difference between the two signals create a resultant signal I_C:

$$I_C = I_{REF} - I_{IN} \tag{1}$$

I_C charges or discharges the input capacitance of the inverter (based on whether it is positive or negative, respectively). This will cause the inverter chain to switch allowing a digital output *an_out*. *an_out* is the digital feedback from the comparator used to set or clear the signals $b_{1\text{-}8}$ (as in Figure 4). In active operation, the *reset* signal is first set high to clear all values. Then b_8 is set high, and an_out is loaded into the D-FF for b_8. The same pattern is repeated for each value b_X; after b_1 is complete the final result is available. For this reason it takes 9 clock cycles for a full conversion cycle to complete.

This paper covers an analysis of the simulated power consumption of this ADC, and discusses the implications of these findings on scalability of devices for WSNs. These results are simulated only; layout, extraction, and manufacture were all considered to be beyond the scope of this paper.

The remainder of the paper is organized as follows. Section 2 outlines the methodology of our analysis. Section 3 shows the results of power consumption simulations of the selected ADC implemented in three technologies (350 nm, 180 nm, and 90 nm). Section 4 outlines the implication of the results on WSN applications, and Section 5 offers a broader perspective on the results of this analysis, and discusses limitations and further work.

II. METHODOLOGY

1.1. Analysis Methodology

The same architecture is implemented in three separate technologies: 350 nm, 180 nm, and 90 nm with "typical" process parameters. These are simulated and analyzed for their power consumption, as broken down into the following categories:

- Analog versus digital section
- Standby versus active operation

The analog section is defined as the input current mirror, D/A converter, and current comparator, as shown in Figure 2. The digital section is defined as the "bcell" structure (shown in Figure 4), replicated 8 times (one for each bit), as shown in Figure 3. While the converter also calls for a clock generation circuit and a current-mode sample and hold unit, these are not used in the power analysis. The architecture is kept as similar as possible to ensure that the values are comparable. In addition, values for measurement such as speed range and naming conventions are the same as the original publication. Standby power consumption is considered to be the power consumption when I_{TR} (the input current for generating the reference current) is zero and the clock is off. Since all other digital circuits are based on the clock, there will be no switching activity in the digital section. As a note, simulation does not proceed properly if I_{TR} is set to exactly zero, so I_{TR} was instead set to 1 pA, more than three orders of magnitude smaller than the 'active operation' value of I_{TR}. Active operation is considered to be an active clock and an I_{TR} of 8nA.

The aspect ratio of the transistors is maintained closely as well. As lengths are scaled in each technology, the width of the transistors is scaled accordingly to maintain approximately equal geometry.

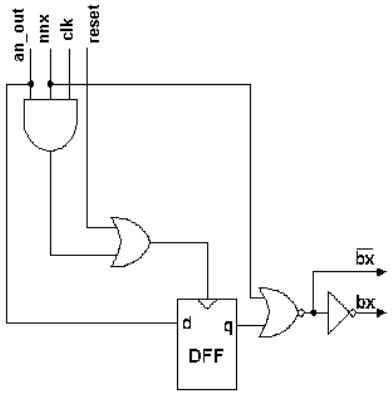

Fig. 4. Simplified Schematic of One Bcell as Defined in [11]

1.2. ADC Structure

The analog component of every SAR converter consists of (among other possible components) a DAC and a comparator (the SAR uses a binary-search algorithm, comparing the input to a value generated by the DAC, to converge to a digital value). The architecture of these components has a strong effect on the functionality of the overall circuit. In this section, the structure of these two components and its impact on the analysis methodology is discussed.

2.2.1 DAC

The DAC in this circuit consists of a current mirror with increasingly large widths on the output transistor. The input to this mirror is denoted as I_{TR}; the same value of 8nA was used for all three technologies. I_{TR} is the reference current; it (like in all algorithmic ADCs) directly affects the input range. Because the comparison current is limited to integer multiples of I_{TR}, the input range of the ADC is limited to:

$$I_{TR} < I_{IN} < 255 * I_{TR}. \quad (2)$$

As a result, while it is possible to operate the 90 nm ADC at a lower I_{TR}, a given application may require this input reference. Since the goal of this project is a comparison of ADCs in the same (theoretical) application, the value of I_{TR} was held constant in each trial at 8nA. This also avoids difficult questions regarding minimum current. Simulation results can easily show operation at extremely low currents, but this may not be realistic in an actual implementation. Simulators are notoriously poor at simulating the effects of noise, which would be the dominant effect limiting the minimum current. Using the same I_{TR} thus avoids potential inaccuracies due to overstated current scaling.

2.2.2 Comparator

The current comparator uses mirrors (*M1-4* in Figure 2) to make two currents (the output of the DAC and the value to be converted, I_{REF} and I_{IN} in Figure 2 respectively) meet at the input of an inverter. The currents either charge or discharge the gate capacitance of this inverter depending on their relative magnitudes, eventually causing the inverter to switch (the gate capacitance is shown in Figure 2, as two capacitors with dotted lines to show that they are not placed capacitors).

While this is effective, because this is only run at the simulation level the capacitance is not effectively modeled and the comparator does not work. To correct this a small capacitor was placed from the node to ground to model the gate capacitance. As this value is needed only for simulations, and not to genuinely model the capacitance at the node, it was kept constant at a value of 0.5 fF in all three cases.

The values used in simulation are together in Table 2.

III. RESULTS

The results are contained in Table 3. Active Consumption is the ADC's power consumption when the ADC is active (leakage, dynamic, and switching power combined). Standby power consumption is the ADC's power consumption when the input currents (I_{TR} and I_{IN}) are zero and the clock is off (leakage only).

TABLE 2 – VALUES USED IN SIMULATION

Property	90 nm	180 nm	350 nm
Supply Voltage	1 V	1.8V	3.3V
Length/Width (Standard)	100 nm/ 200 nm	180 nm/ 400 nm	350 nm/ 800 nm
I_{TR} (Active)	8 nA		
I_{TR} (Standby)	1 pA		
Clock Period	5us		
I_{IN} (Active)	1nA		
I_{IN} (Standby)	1 pA		
Comparator Input Capacitance	0.5fF		

TABLE 3 – POWER CONSUMPTION SIMULATIONS FOR AN SAR ADC IN THREE TECHNOLOGIES

Property	Power (nW)		
	90 nm	180 nm	350 nm
Digital (Active)	840	4464	14421
Digital (Standby)	59.0	2.00	1.01
Analog (Active)	8041	11304	18480
Analog (Standby)	1684	77.40	49.50
Total Active	8881	15768	32901
Total Standby	1743	79.00	50.52

It should be noted that the power numbers shown here do not match the values given in [11]. This is because this analysis was performed using 'standard' supply voltage values, instead of the minimum possible. This was done to more accurately represent a real application, where several circuits are combined together and the designer chooses not to include voltage regulators for individual blocks.

IV. DISCUSSION

It is unsurprising to see that active power consumption scales with technology. However, in many applications active operation is only a fraction of the total operating time. The suggestion in [1] is to assume that, for a node in a wireless sensor network, active operation consists of 1% of the total operating time, with standby operation consisting of the other 99%. Thus to get a complete picture of energy consumption, one must weight active and standby power consumption accordingly:

$$P_{TOTAL} = 0.01 * P_{ACTIVE} + 0.99 * P_{STANDBY} \quad (3)$$

Using this formula, the total power consumption for each technology is calculated as in Table 4.

In scaling from 350 nm to 90 nm, the active power consumption was reduced by a factor of almost four. However, at the same time the standby consumption increased by a full order of magnitude. Effectively, for the selected application the power consumption of the ADC in 90 nm is higher than the consumption in 180 nm!

TABLE 4 – POWER CONSUMPTION SIMULATIONS FOR AN SAR ADC IN THREE TECHNOLOGIES

Property	Power (nW)		
	90 nm	180 nm	350 nm
Active (Weighted)	88.8	157.7	329.0
Standby (Weighted)	1726	78.23	50.01
Total Effective Consumption	1815	235.9	379.0

Clearly this analysis is dependent on the assumed duty cycle, or percentage of time the ADC is in active operation. This is illustrated in Figure 5, where the total power consumption of each implementation is plotted against duty cycle (here defined as the percent of time the ADC is active). While the power consumption of the 180 nm implementation is always lower than the 350 nm implementation, the advantage of the 180 nm over the 90 nm technology is realizable only for applications which have less than a 21% duty cycle.

Also plotted is a line labeled "Max Consumption". This line is based on the 2nJ/bit value suggested in [1], using the bit rate used in these power simulations and assuming the ADC accounts for 10% of the total power in the node. This illustrates that, for a suitably low bit rate, even a 350 nm implementation can meet the power requirements.

V. LIMITATIONS OF STUDY

It is not necessarily a valid conclusion to stretch these results into a dismissal of further scaling. These results present a difficulty that must be overcome, but one that can be overcome with future design effort. For example, increases in comparator mismatch and its effects on ADC accuracy are another major concern for feature scaling, but recent work (such as [16]) offer (partial) solutions to this problem.

In particular, consider that this analysis uses identical schematics for each circuit. This requires that, even if a design technique makes sense in a given technology, it could not be used in the name of uniformity. For example, if anti-leakage design techniques are used in 90 nm (such as high-V_T transistors), leakage can be minimized so that it is the unqualified minimum consumer of power. Likewise, attaching an 'enable' signal to the power supply so V_{DD} is reduced to zero when on standby mode would also dramatically reduce standby power consumption. However, this analysis does serve to emphasize the growing importance of leakage cancellation or compensation, rather than being additional features for consideration if time allows.

It should also be noted that these results are based on schematic simulation only; full layout and extraction was considered to be beyond the scope of the project.

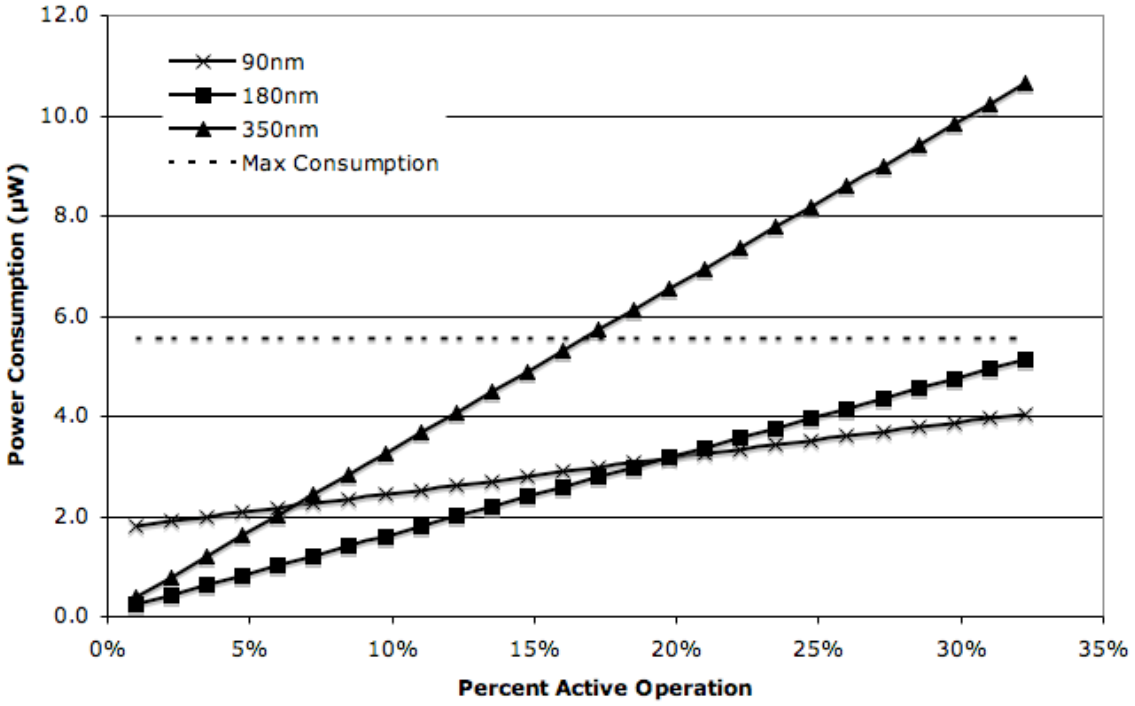

Fig. 5 – ADC Power Consumption vs. Duty Cycle

VI. Conclusion

The power consumption of three implementations of an ADC, one in 350 nm, one in 180 nm, and one in 90 nm were simulated and compared. The results showed that the dynamic power consumption was reduced by a factor of four, but standby power consumption increased by a full order of magnitude. Assuming a Wireless Sensor Network application with a duty cycle of 1%, this leads to an effective power consumption of 1.8 uW for the 90 nm implementation, 0.23 uW for the 180 nm implementation, and 0.3 uW for the 350 nm implementation. This underlines the increasing dominance of leakage current over the power consumption in low-throughput nodes.

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