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MICRO POWER 14-BIT A/D CONVERTER: 45 µW AT ±1.25V AND 16 KSAMPLES/S

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Abstract: Micro power converters are required for power sensitive, battery-operated devices. Keeping this goal in mind IMT first developed a RSD cyclic converter featuring 13 bits of dynamic range and 60 dB of SNR. The relative precision behavior is due to technology limitations (capacitor mismatch, finite DC gain of OTA). However, digital correction is possible and this paper presents the implementation in a low voltage 1 µm CMOS technology of a new linear ADC. The targeted performances were 14 bits and 45 µW @ 16 kHz & ±1.25 V power supply for a die size of 1.17 mm^2. "Layout level" simulations however showed that to reach the 14 bits, a power supply of ±1.5 V is required and results in a 65 µW power consumption.

1 Introduction

Progress in low power micro-electronics technologies and digital signal processing has opened the way to numerous digital portable applications. Targeted low power A/D converters are thus required to improve the overall power consumption and consequently the battery life.

In previous work, a Redundant Signed Digit (RSD) algorithmic converter was developed at IMT [Heub96]. It features 13 bits dynamic range, 60 dB SNR and its power consumption at ±1.25 V and 16 kHz is less then 50 µW. The limited SNR is well suited for audio application where masking effects take place. It is however a drawback for applications such as instrumentation.

The 'relative precision' (error proportional to input signal) results from imprecise doubling operations and finite DC gain. Consequently each bit b_i computed by the RSD converter has a $(2+e)^{-i}$ weight, while in an ideal case this weight would have been 2^{-i}. A simple base translation can thus be performed to obtain the correct word and achieve a linear characteristic over the whole input range.

This paper focuses on the implementation of the above base translation in a low voltage 1 µm CMOS technology. Section 2 describes the relative precision RSD converter as developed by A. Heubi [Heub96] while the correction algorithm is explained in section 3. It's implementation and the resulting chip are presented in section 4. Section 5 gives the test measurements while devices with a higher dynamic range or faster sampling frequency are considered in section 6. Finally, section 7 concludes the discussion.

2 Relative precision converter [Heub96]

In conventional binary representation, a single word matches a numerical value. In [Gine88], a Redundant Signed Digit (RSD) code is proposed. Because of the redundancy, many words can represent a same value. For example, [0 1 0 0 0 1], [1 -1 0 0 0 1] or [0 1 0 0 1 -1] all represent the value 0.265625.

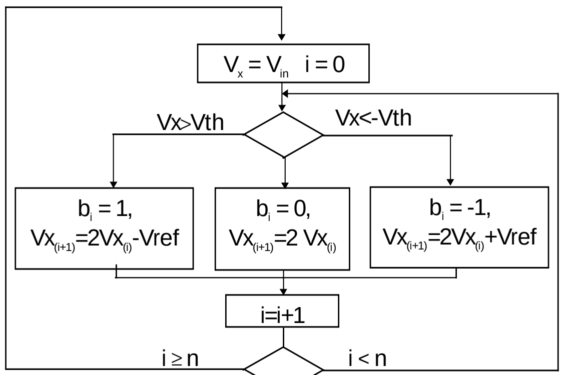

Figure 1.1 : Cyclic RSD conversion algorithm

The advantage of the RSD conversion is that the very accurate comparison (inaccuracy smaller then a half LSB) that is normally performed in cyclic converter is replaced by two comparisons as shown in figure 1.1 [Gine92]. Hence, the design constraints on the comparators are drastically simplified and inaccuracies of up to half Vref are tolerated, regardless of the number of bits.

Alexandre Heubi proposed a very efficient switched capacitor implementation of the above algorithm. The input signal is sampled at the beginning of the conversion cycle and thus no sample & hold is required. The large tolerance comparators are realized by simple strobed cross-coupled inverters. The RSD output is converted into a two's complement representation. The proposed schematic requires one active element only and 3 identical capacitors. Its advantages are :

- active element offset gives only a digital offset (which can be easily compensated if needed)

- switch charge injection has the same effect as above

- active element saturation causes digital saturation (no distortion for low level input signals)

Alexandre Heubi converter is covered by patent #9510174 and was implemented in the ALP2 LV double metal, double poly, 2 µm CMOS technology from EM Microelectronic Marin SA in Switzerland. [Heu96] details chip implementation and measured performances. Power consumption and Total Harmonic Distortion (THD) are particularly relevant: the measured power consumption at ± 1.2 V power supply and 16 kHz sampling frequency was 48 µW while the THD as well as THD + noise, for a 1 kHz sine wave, are given in figure 2.1. The latter shows a saturation at about 60 dB for large input levels and a linear behavior for low input levels. It can be concluded that A. Heubi's converter posses a dynamic of 78 dB (13 bits) and a limited SNR of 60 dB. The converter thus features a relative precision characteristic. Informal listening tests resulted in excellent perceived quality.

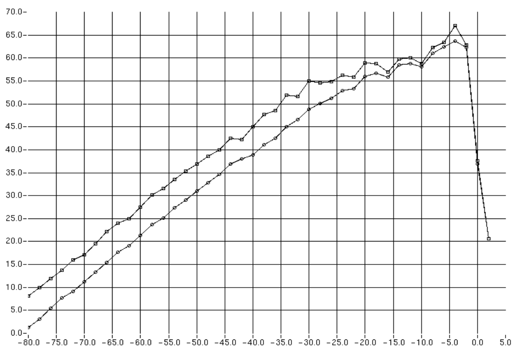

Figure 2.1 : THD and THD+noise versus input signal level

3 14-bit linear RSD Converter [Gris96]

As mentioned in the previous section A. Heubi's converter presents a relative precision behavior. Because of technology sensitivity, the « real » (or implemented) algorithm can be expressed as in figure 3.1

Three error sources can be defined : offset (ϕ), add/sub of Vref (β) and doubling (ε). Let's assume a zero offset, the digital output magnitude should thus be computed according to equation 3.1 :

$$DIG\_out = (1+\beta)\cdot\sum_{i=0}^{n-1} b_i\,(2+\varepsilon)^{-i} \qquad 3.1$$

Because of the non ideal doubling factor, each bit computed by the implemented RSD algorithm has a weight of $(2+\varepsilon)^{-i}$ [Gine88]. In the ideal case, this weight would be 2^{-i}. A « base translation » has thus occurred. The add/sub Vref error results in a $(1+\beta)$ scaling of the bits.

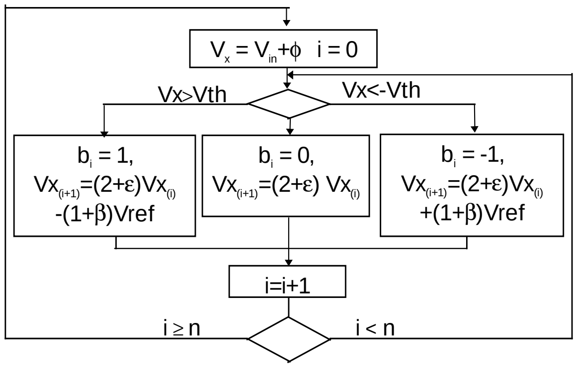

Figure 3.1 : Implemented cyclic RSD algorithm

Since ε is fairly small (<0.4 %), $(2+\varepsilon)^{-i}$ can be expressed by the two first terms of its Taylor development as in equation 3.2.

$$(2+\varepsilon)^{-i} = 2^{-i} + \frac{i\cdot\varepsilon}{2^{i+1}} \qquad 3.2$$

Doubling and add/sub errors are taken into account by the correction algorithm of figure 3.2 where b_i are the bits computed by the RDS converter. In fact, the algorithm realize equation 3.2. Register #1 is initialized (at each conversion beginning) at $1+\beta$ and register #2 at $\varepsilon/2$. If necessary, register #3 can be initialized at the proper value to ensure offset compensation. The algorithm directly performs the RSD to two's complement transformation.

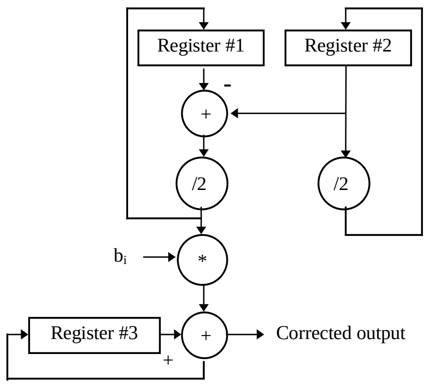

Figure 3.2 : Correction algorithm

Using β and ε values of 0.4 % (maximum mismatch for ALP1 or ALP2), simulation showed that a 17 bit decimal datapath is necessary and results in an average absolute error of 0.4 LSB. The maximum error is 1 LSB with a probability of 0.05 %.

Provided ε, β and ϕ values are available, the above algorithm is successful in linearizing the RSD converter.

4 Implementation of the linear converter

The converter has been designed in ALP1, the low voltage 1µm 2 poly 2 metal CMOS technology from

EM Microelectronic Marin SA. The general design principles employed in the relative precision chip have been reused. It was also decided that calibration would be performed at each power on. The values of ε, β and φ are thus measured and store locally.

4.1 Analog design :

The analog part of the linear RSD converter is very similar to that of the relative precision one. In addition to a technology redesign (from ALP2 to ALP1), three supplementary switches and a slightly modified switching control was required (to properly measure ε, β and φ [Lee93]).

The targeted performances were 14 bits at ± 1,25 V and 16 kHz and analog design was done accordingly. However, a final 'post layout' simulation showed that at this supply voltage a dynamic of only 13 bits is obtained. This is due to the OTA internal noise which is a little higher then in the first 'transistor level' simulation. At ± 1.5V, according to the post layout simulation, the dynamic reaches 14 bits and the power consumption is 51 μW.

4.2 Digital design

The digital design includes 3 main modules:

- correction algorithm and the initialization registers
- digital and analog control
- output interface

Regarding the correction, a VHDL code was written, simulated and synthesized within COMPASS. To optimize the area and power consumption, each register's size was minimized and subsequent sign extension used whenever possible.

The control module generates the control signals for the analog switches (to allow proper measurement of ε, β and φ and conversion) as well as those used by the correction algorithm (to store/load ε, β and φ, clock the registers, etc.).

The output block allows the users to chose between a serial LSB first or MSB first output. Furthermore to be compatible with commercial DSP processors the number of output bits can be set to 8, 12, 14 or 16. It must be stressed out that when 16 bits are output, the converter actually furnishes 14 true bits and two noisy ones (LSB and LSB-1).

Level shifters between analog and digital part made it possible to supply the digital part with half the voltage. The simulated power consumption of the digital part is thus of 8.5 μW at 1.25 V.

4.3 Final layout :

The final chip layout is given in figure 5.8. The die size is 1.03 by 1.14 mm (1.29 by 1.45 with pads). The simulated total power consumption at 16 kHz and ± 1.25 V is 45 μW for a reduced dynamic of 13 bits. For a 14 bits dynamic, a supply voltage of ± 1.5 V should be used resulting in a power consumption of 64 μW.

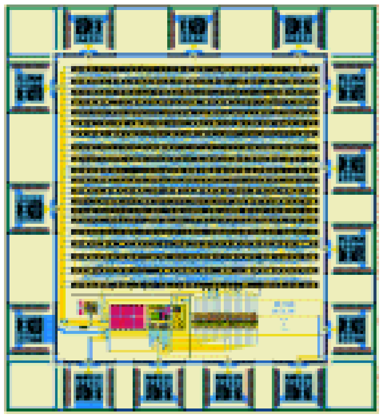

Figure 4.1 : Layout of linear RSD converter

5 Test measurements

The measurements were performed 'in house' using non professional equipment. Problem such as environmental noise circumscribe the results.

Power consumption values are given in the table below and are in agreement with the predictions.

Sampling frequency	Power Cons. [μW] at ± 1.25 V	Power Cons. [μW] at ± 1.5 V
8.9 kHz	26.1	36.75
17.8 kHz	47.5	65.4

Table 5.1: Measured power consumption

A second set of tests showed that the internal reset of the converter capacitors (performed at the beginning of each conversion cycle) is a little short to allow full discharge at 16 kHz. As a result all the following measurements will be performed at a lower sampling frequency. This reset problem will be easily corrected in a future redesign by modifying the control signals and will imply no power consumption or die area increase.

The noise floor is given in figure 5.1 for supply voltage of ± 1V to ± 1.53 V.

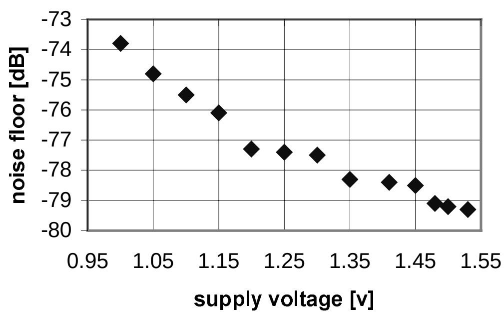

Figure 5.1: Noise floor measurement

The noise floor value at ± 1.25 V shows a dynamic of 12.9 bits. At ± 1.5 V, only 13.2 dB are reached.

These values are slightly lower then the prediction of section 4.3 (based on post-layout simulations). It is difficult to determine whether the measurements are accurate (i.e. exact measurement of the converter noise floor), or whether they are tarnished by environmental noise. Perturbation such as probes, supply cables, power network etc. strongly influence the measured value. Although means to limit the perturbations effects were used, one cannot guaranty that they have been completely removed. It must also be stressed that layout simulation do not take into account bulk effects. The perturbations due to the switching of digital circuit over the analog part is thus not considered. This could also explain the difference between the measured and simulated noise level.

The transfer function of the converter was measured under far from ideal conditions. Indeed, the Farraday cage could not be used and as a result environmental perturbations limited the noise floor to about 12 bits. The Differential Non Linearity (DNL) is plotted in figure 5.2 where the values are given in LSB's. Because of the environmental noise, DNL of up to 3 (2 bits) can be considered as within the measurement error. However, one sees that for high input levels the DNL value can get as high, in magnitude, as 4 (or 3 bits). This means that a prefect linearity of 12-bit is not reached. This is probably due to an imprecise measurement of the β values during the calibration phase. The higher the input level, the sooner an addition/subtraction must take place. A correction error occurring during this operation is then multiplied in all the successive iterations. Means to improve the β value should thus be investigated to improve the overall linearity behavior.

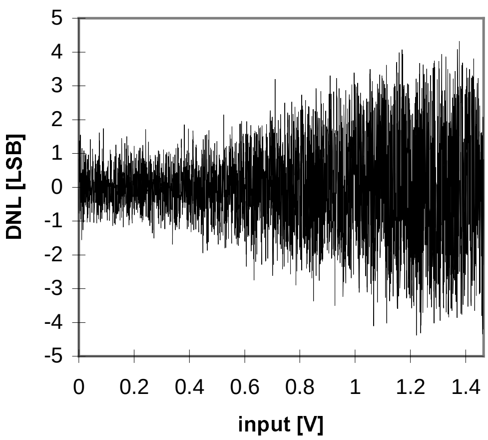

Figure 5.2: DNL characteristic

6 Other devices

Various devices, using the RDS principle and other enhancement have been developed at IMT.

A 8-bit 128 kHz aimed at video processing has been implemented in a 1 µm technology. Its die area is 0.05mm^2 and features a power consumption of 50 µW at ±1.5V. Cascading 400 of the above converters would result in a 8-bit 50 MHz device burning 60 mW for a total area of about 18 mm^2. Compared to one of the best currently available converter [Kuma96], this represent a 5X gain in power consumption for a 2.5X loss in density.

A 16-bit converter featuring 120µW at ±1.25 V and 50 kHz is currently in fabrication. Its die size in a 1µm technology is 0.5mm^2.

7 Conclusions

A micro power 13-bit 'relative precision' RSD cyclic ADC, featuring a limited SNR, was previously developed at IMT. For non-audio applications, the maximum 60 dB SNR is not sufficient and the non linearity and offset have to be corrected.

Since the non linearity mainly results from a doubling error and imprecise reference voltage subtraction/addition, a simple 'base translation' combined with a scaling can be performed. The offset is then digitally subtracted to obtain the corrected digital word.

The implementation of a self calibrating, 14-bit linear converter in a low voltage 1 µm technology has been performed. Power consumption predictions, based on post layout simulations, have been confirmed by chip measurements. The dynamic range could not be satisfactorily tested because of environmental noise. However, it was possible to bring to light that the calibration phase must be improved in order to ensure linearity over 14 bits.

In spite of a few youthful indiscretions that could be easily corrected, the presented ADC is a contribution to the development of ultra low power devices to be used in battery operated and portable applications

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